Physical Design Project Report

Candidate Name: Karthik Pamula
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Project: RTL to GDSII Implementation of a 32-bit RISC Core (28nm)

Tools Used:

Design Compiler (Synthesis), IC Compiler II (Floorplan to Routing), PrimeTime (Static Timing Analysis), StarRC (Parasitic Extraction)

Project Flow:

This project involved the complete backend implementation of a 32-bit RISC processor using Synopsys tools on a 28nm technology node. The process included logic synthesis, floorplanning, placement, clock tree synthesis (CTS), routing, and signoff (timing and physical). Special emphasis was placed on timing closure, power integrity (IR drop and EM analysis), and physical verification (DRC/LVS).

Key Stages and Tasks Performed:

Stage	Task
Synthesis	Generated gate-level netlist using Design Compiler
Floorplanning	Defined die/core area, macro placement, and power planning
Placement	Standard cell placement and optimization
CTS	Built balanced clock tree and resolved skew/insertion delay
Routing	Performed global and detail routing with congestion optimization
Timing Analysis	Fixed setup/hold violations using PrimeTime
Signoff	Parasitic extraction (StarRC), IR drop & EM analysis, DRC/LVS cleanup

Project Highlights:

- Achieved 0 timing violations (setup/hold) at signoff. - Fixed all DRC and LVS violations for clean GDSII output. - Performed IR drop and EM analysis on power grid. - Gained hands-on experience on 28nm node constraints and low-power UPF-based design.

Conclusion:

This project provided deep exposure to the full RTL to GDSII physical design flow and enabled strong hands-on understanding of industrial signoff checks and tool usage, preparing me to contribute to live backend design teams effectively.