ECE335 Communication Theory I (3-1-0-4):

Lecture 11:

Analog Communication Techniques:

Phase Locked Loop (PLL)

Feb. 22, 2025

INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY
HYDERABAD

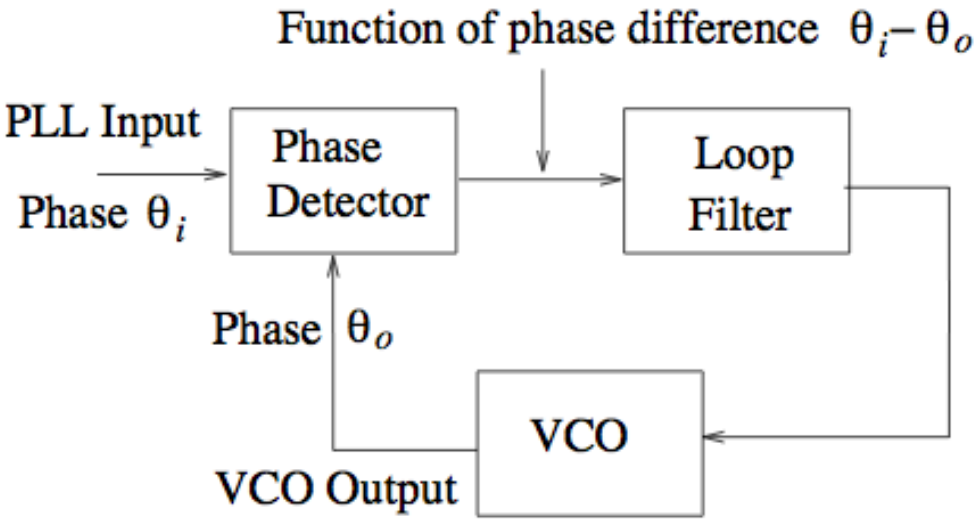
References

- Chap. 3 (Madhow)

PLL intro

- Legacy applications in analog communication and analog front-end of digital communication
  - FM demodulation
  - Carrier synchronization
- Key application in communication today: LO frequency synthesis
- Canonical structure for using feedback for continuous tracking

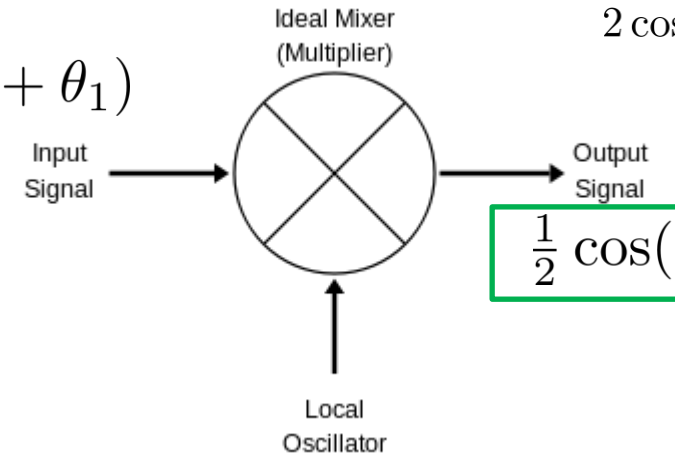
High-level view of PLL



- Aim is to lock on the phase of the PLL input
- Phase detector compares input phase with locally generated phase at the VCO output
- Phase detector output is smoothed through loop filter and fed back to VCO input
  - If VCO output is ahead of the input phase, then retard the VCO phase
  - If VCO output is behind of the output phase, then advance VCO phase

Mixer as Phase Detector

Mixers can extract phase differences



$\cos(2\pi f_c t + \theta_1)$

$\cos(2\pi f_c t + \theta_2)$

$2\cos A \cos B = \cos(A - B) + \cos(A + B)$

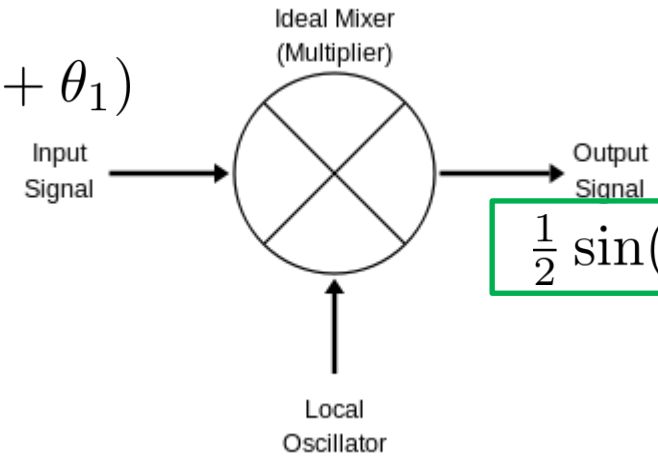
$\frac{1}{2}\cos(\theta_1 - \theta_2) + \frac{1}{2}\cos(4\pi f_c t + \theta_1 + \theta_2)$

Phase lock condition: The term $\cos(\theta_1 - \theta_2) = 0$, i.e., $\theta_1 - \theta_2 = \pi/2$

For a natural phase lock condition of $\theta_1 - \theta_0 = 0$, change one of the sinusoids to sine wave.

Mixers can extract phase differences

$$-2\cos A \sin B = \sin(A-B) - \sin(A+B)$$



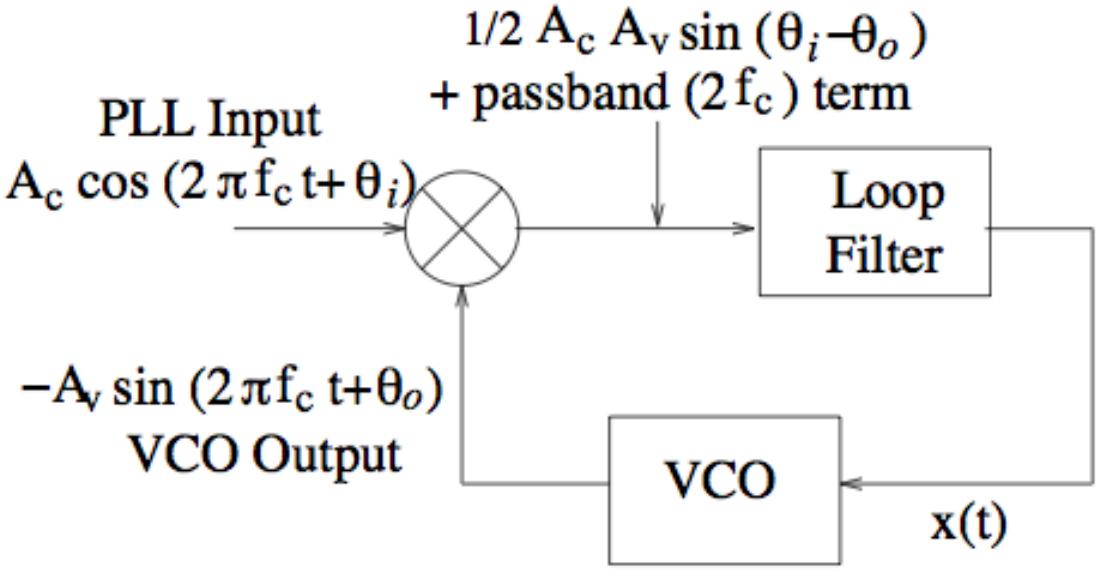
$\cos(2\pi f_c t + \theta_1)$

$\frac{1}{2}\sin(\theta_1 - \theta_2) - \frac{1}{2}\sin(4\pi f_c t + \theta_1 + \theta_2)$

$-\sin(2\pi f_c t + \theta_2)$

Phase lock condition: The term $\sin(\theta_1 - \theta_2) = 0$, i.e., $\theta_1 - \theta_2 = 0$

Mixer-based phase detector



- With this convention, the mixer output is given by

$$- A_c A_v \cos(2\pi f_c t + \theta_i(t)) \sin(2\pi f_c t + \theta_o(t))$$

$$= \frac{A_c A_v}{2} \sin(\theta_i(t) - \theta_o(t)) - \frac{A_c A_v}{2} \sin(4\pi f_c t + \theta_i(t) + \theta_o(t))$$

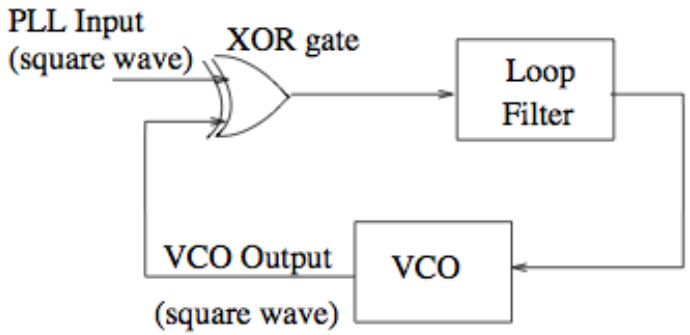
Phase difference term driving feedback loop

Double frequency term (filtered out)

Mixed signal phase detection

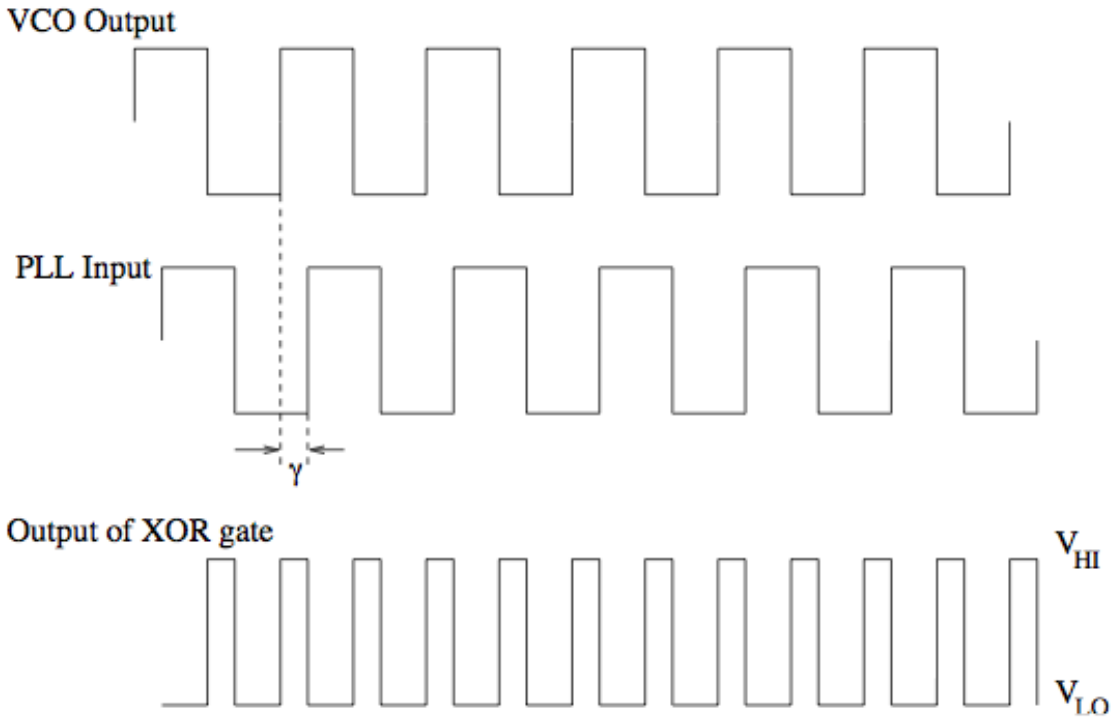
- Modern PLL implementation often make heavy use of digital logic
- For frequency synthesis application, VCO output is often a square wave (filtered later to extract sinusoid as a harmonic)
- Phase detector can also be implemented using digital logic, example, XOR gate

XOR-based phase detector



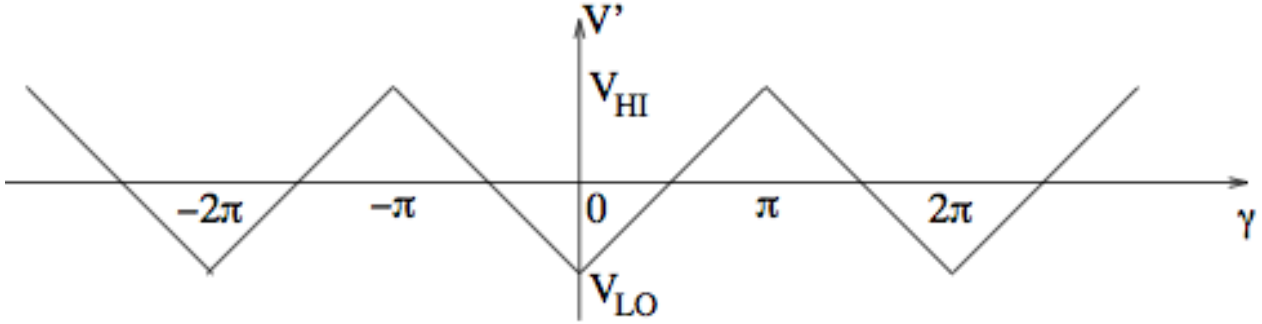
Exclusive-OR gate

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0



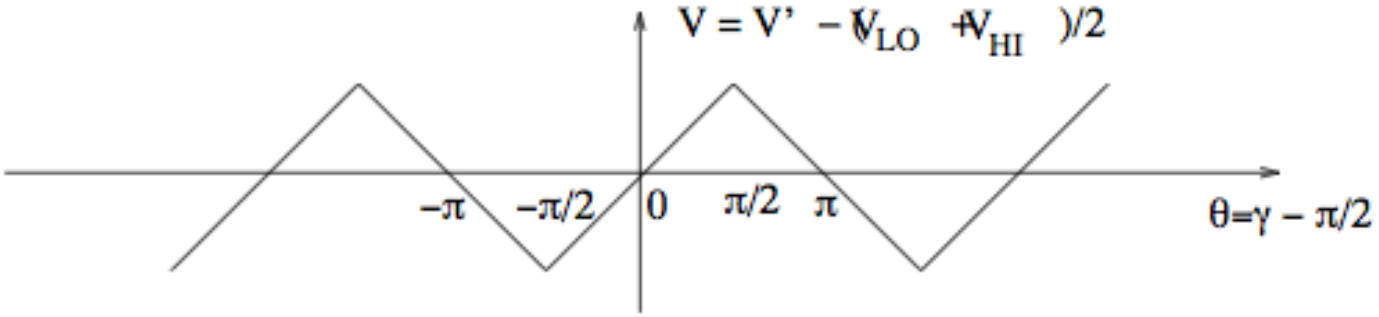
Average of XOR output is related to phase difference

XOR-based phase detector output



(a) DC value of output of XOR gate.

- Translate along both axes to get a more natural curve, i.e., phase detector output is zero for zero phase difference
- Response symmetric around origin



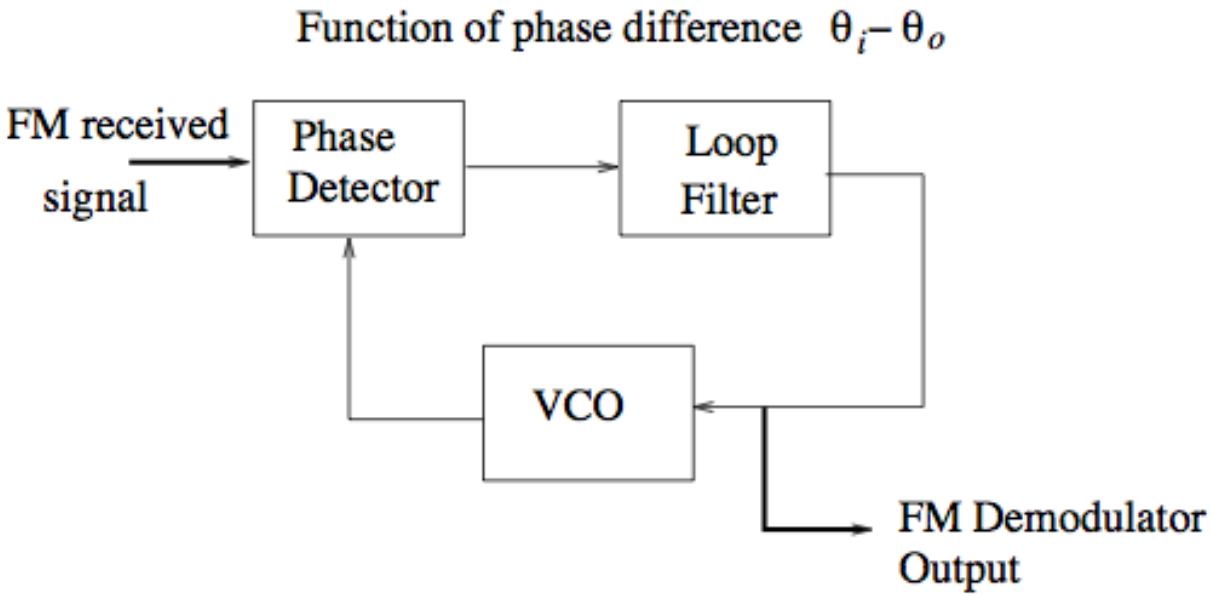
(b) XOR phase detector output after axes translation.

Today's Class

PLL Applications:

FM Demodulation and Frequency Synthesis

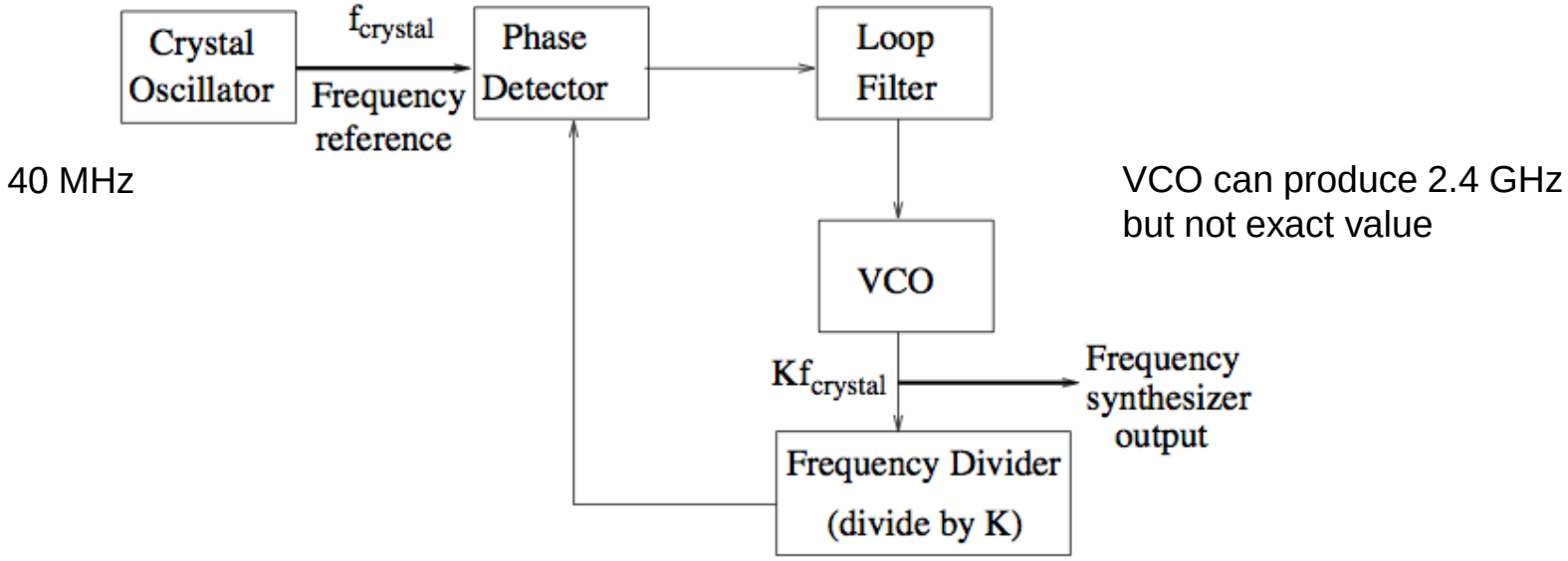
PLL for FM demodulation



- Show that if the PLL is tracking and PLL input is FM signal, then the input to VCO is a scaled version of the message.

PLL for frequency synthesis

- Typical application in communication transceivers
- Synthesize LO (e.g. at 2.4 GHz) from a lower reference frequency source (such as crystal oscillator)



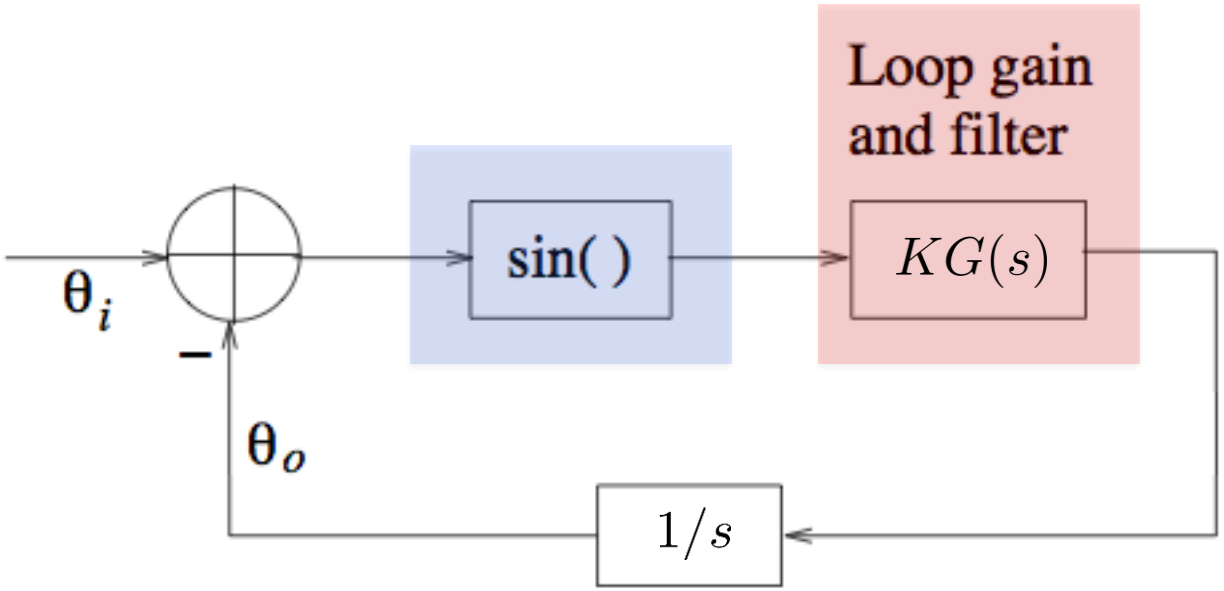
- VCO quiescent frequency is around the desired frequency. Precise lock to multiple of crystal frequency is enabled by the PLL.
- Divide frequency of VCO (e.g., by skipping clock cycles in a digital implementation).
- Compare with crystal phase/freq to drive VCO

Mathematical Model for PLL

For mixer-based phase detector

Output of mixer as phase detector

$$= \frac{A_c A_v}{2} \sin(\theta_i(t) - \theta_o(t)) - \frac{A_c A_v}{2} \sin(4\,\pi f_c t + \theta_i(t) + \theta_o(t))$$



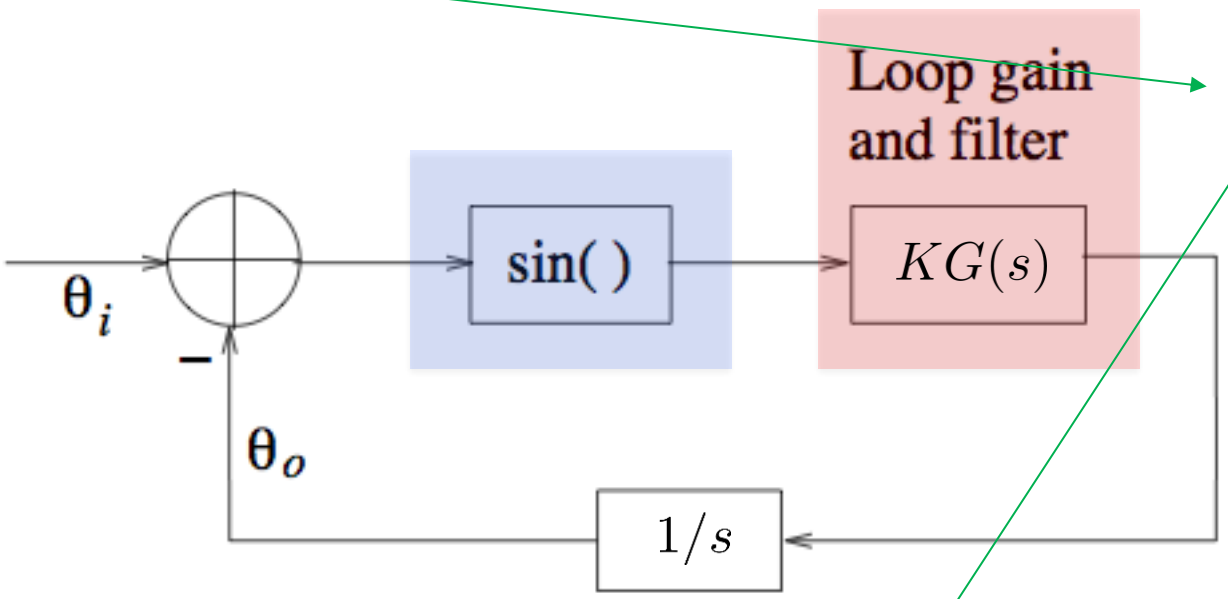
VCO functionality
(normalized)

$$\theta_o(t) = K_v \int_0^t x(\tau) d\tau$$

For mixer-based phase detector

Output of mixer as phase detector

$$= \frac{A_c A_v}{2} \sin(\theta_i(t) - \theta_o(t)) - \frac{A_c A_v}{2} \sin(4\,\pi f_c t + \theta_i(t) + \theta_o(t))$$

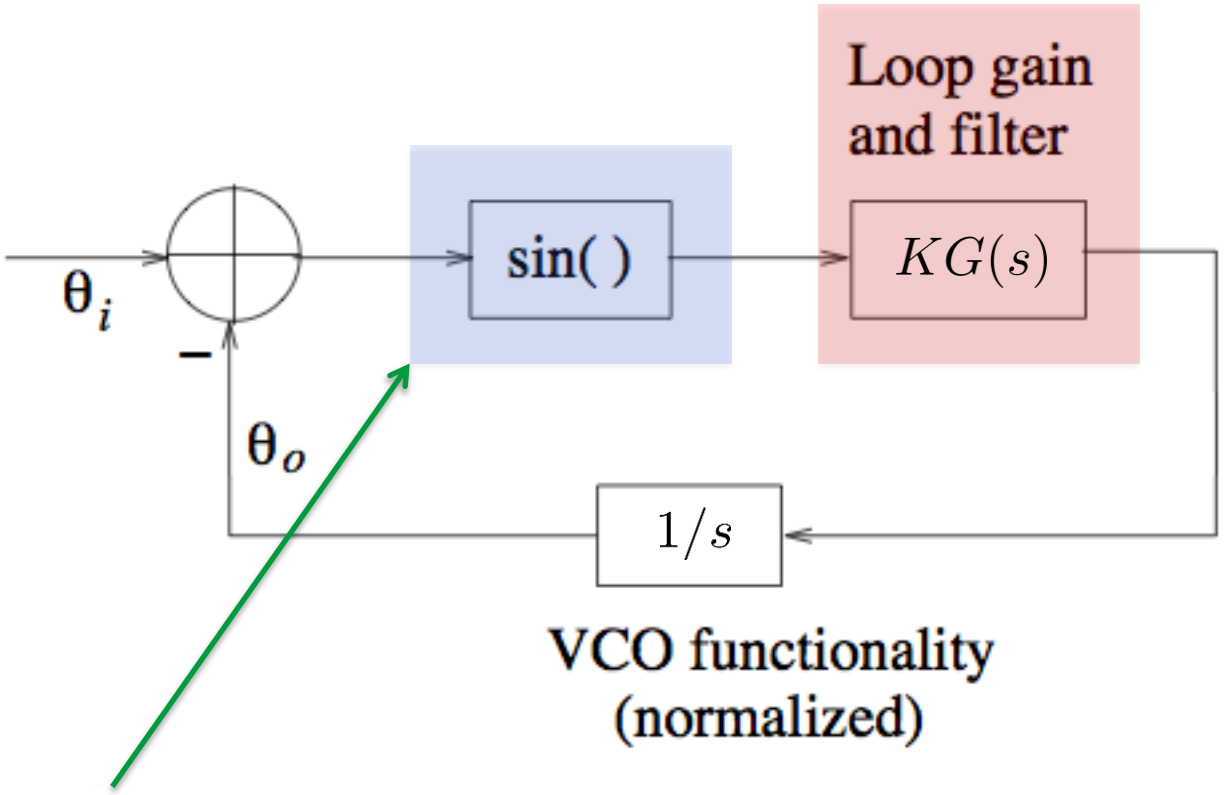


$$K = \tfrac{1}{2} A_c A_v K_v$$

VCO functionality
(normalized)

$$\theta_o(t) = K_v \int_0^t x(\tau) d\tau$$

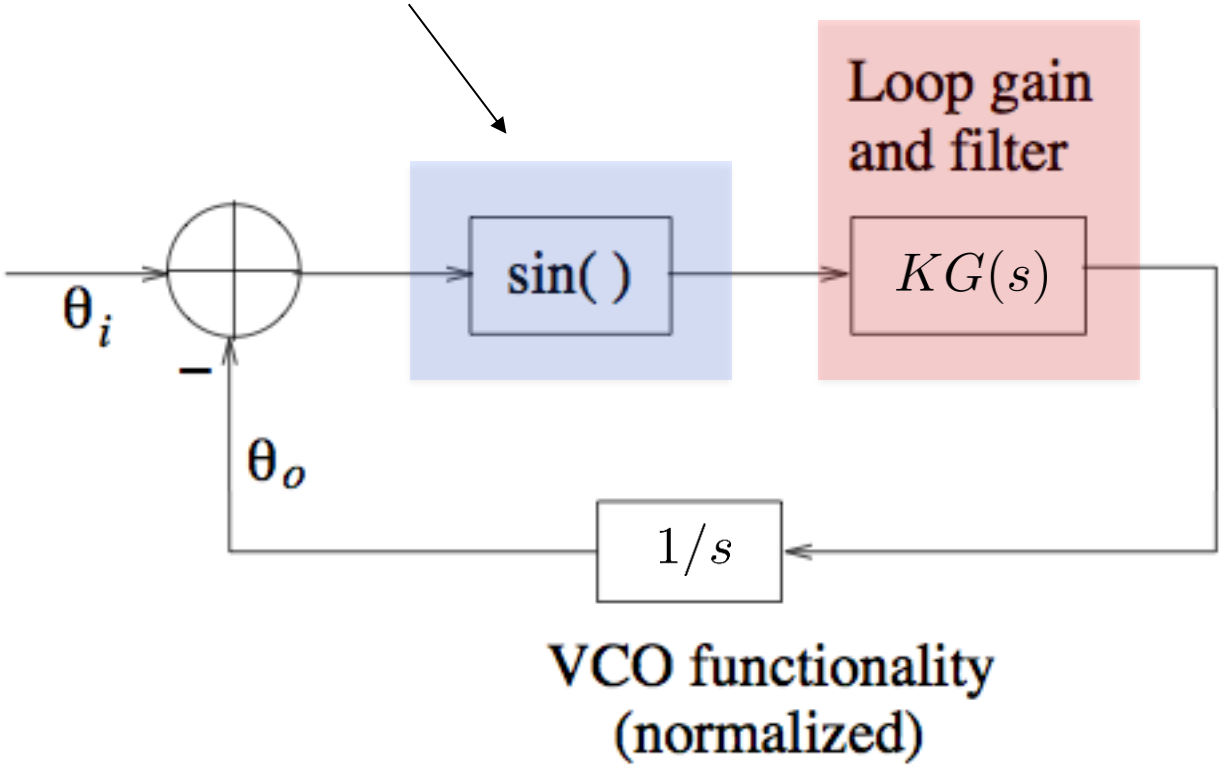
For mixer-based phase detector



Replace sine by triangular wave for XOR-based phase detector

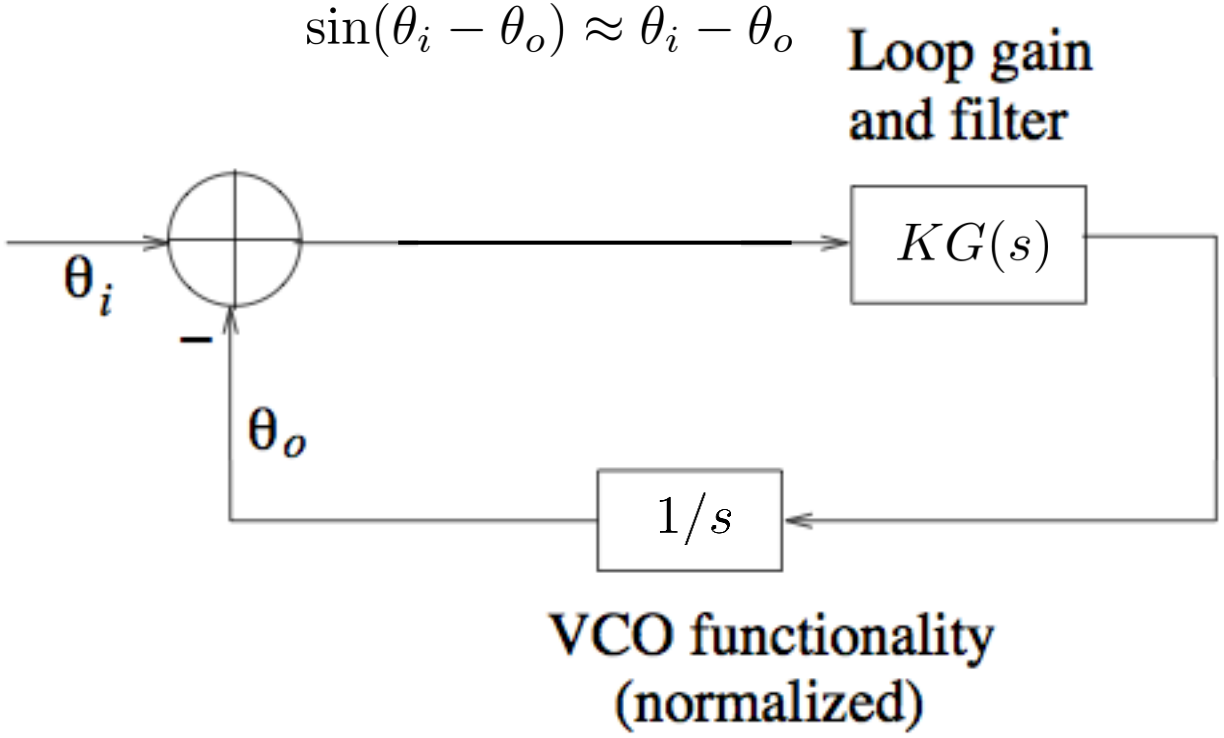
For mixer-based phase detector

This is difficult to analyze as system is non-linear



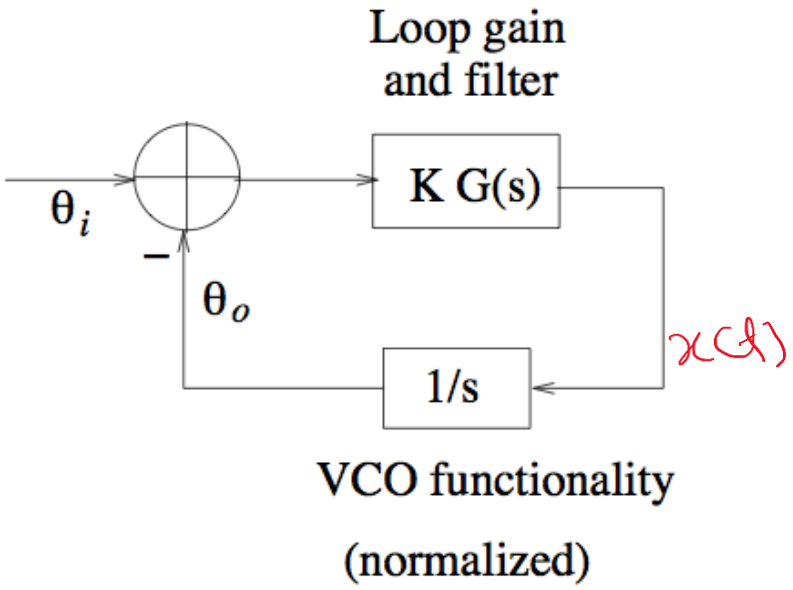
Linearized Model

$$\sin(\theta_i - \theta_o) \approx \theta_i - \theta_o$$



- Can analyze using Laplace transform.
- Linearized approximation applies even better to triangular response corresponding to XOR-based detector since response is exactly linear for small phase error.

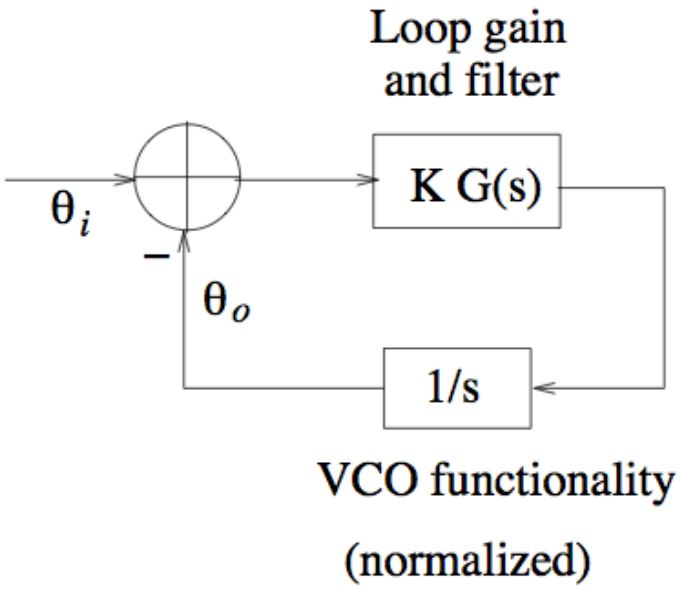
Linearized analysis



- Show that the transfer function between input and error

$$H_e(s) = \frac{\Theta_i(s) - \Theta_o(s)}{\Theta_i(s)} = \frac{s}{s + KG(s)}$$

First order PLL



$$H(s) = \frac{KG(s)}{s+KG(s)} \qquad H_e(s) = \frac{s}{s+KG(s)}$$

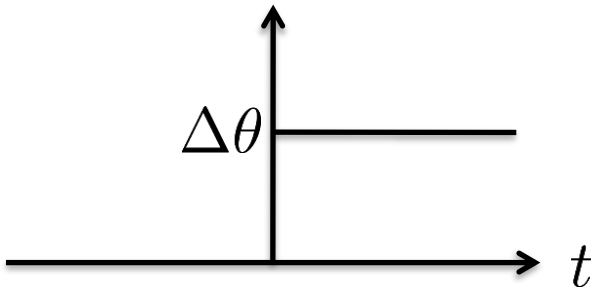
$$\downarrow \quad G(s) = 1$$

$$H(s) = \frac{K}{s+K} \qquad H_e(s) = \frac{s}{s+K}$$

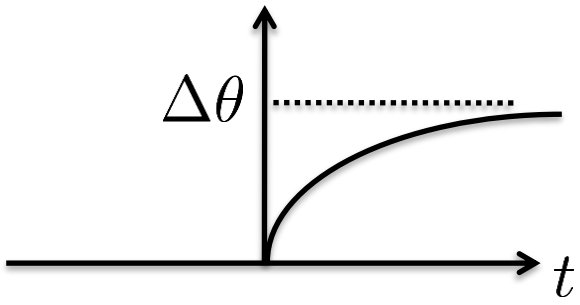
Single pole at $s = -K$
Stable when loop gain $K > 0$

1st order PLL: phase step response

$$\theta_i(t) = \Delta\theta I_{[0,\infty)}(t)$$



$$\theta_o(t) = \Delta\theta(1 - e^{-Kt})I_{[0,\infty)}(t)$$

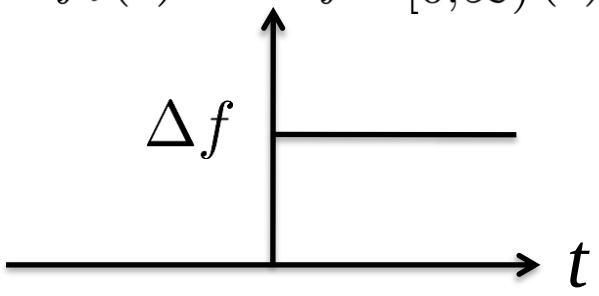


- Assume PLL is tracking well. If the input phase suddenly jumps, then would PLL be able to track down this change? To answer this, we need to answer following question
  - Find $\theta_o(t)$ in terms of $\theta_i(t)$.
  - Also find steady state error.

$$\lim_{t\to\infty} \theta_e(t) = 0$$

1st order PLL: freq step response

$$f_i(t) = \Delta f \; I_{[0,\infty)}(t)$$



- Assume PLL is tracking well. If the input frequency suddenly jumps, then would PLL be able to track down this change? To answer this, we need to answer following question
  - Find $f_o(t)$ and $\theta_o(t)$ in terms of $f_i(t)$ and $\theta_i(t)$.
  - Also find steady state error.

Second order PLL

- Can we track frequency step using a more complex loop filter?
- What if we feed both the phase error and the integral of the phase error (Proportional + Integral Feedback)

$$G(s) = 1 + \frac{a}{s} \quad a > 0$$

- For the above $G(s)$, the frequency responses $H(s)$ and $H_e(s)$become

$$H(s) = \frac{KG(s)}{s + KG(s)} = \frac{K(s+a)/s}{s + (s+a)/s}$$

$$= \frac{K(s+a)}{s^2 + Ks + Ka}$$

$$H_e(s) = \frac{s}{s + KG(s)}$$

$$= \frac{s^2}{s^2 + Ks + Ka}$$

- Poles at $s = \frac{-K \pm \sqrt{K^2 - 4Ka}}{2}$
- Stable for $K > 0$
- Oscillations in response if poles have an imaginary components.
  Happens if $K^2 - 4Ka < 0$ or $K < 4a$

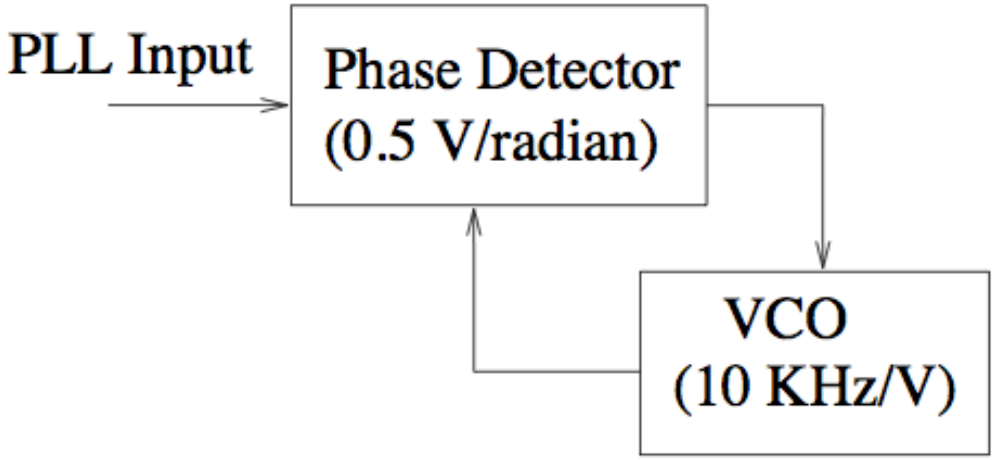
2nd order PLL: freq step response

- Similar to first order PLL, we can find expressions for phase and frequency!
- However we are more interested if the phase error goes to zero in this case (Show!).

Choosing PLL order

- First order PLL can track step in phase
- Second order PLL can track step in frequency (i.e., linear ramp in phase)
- Third order PLL can track step in frequency derivative (i.e., linear ramp in frequency)
- Typical design choice is 2nd and 3rd order PLL.

Example



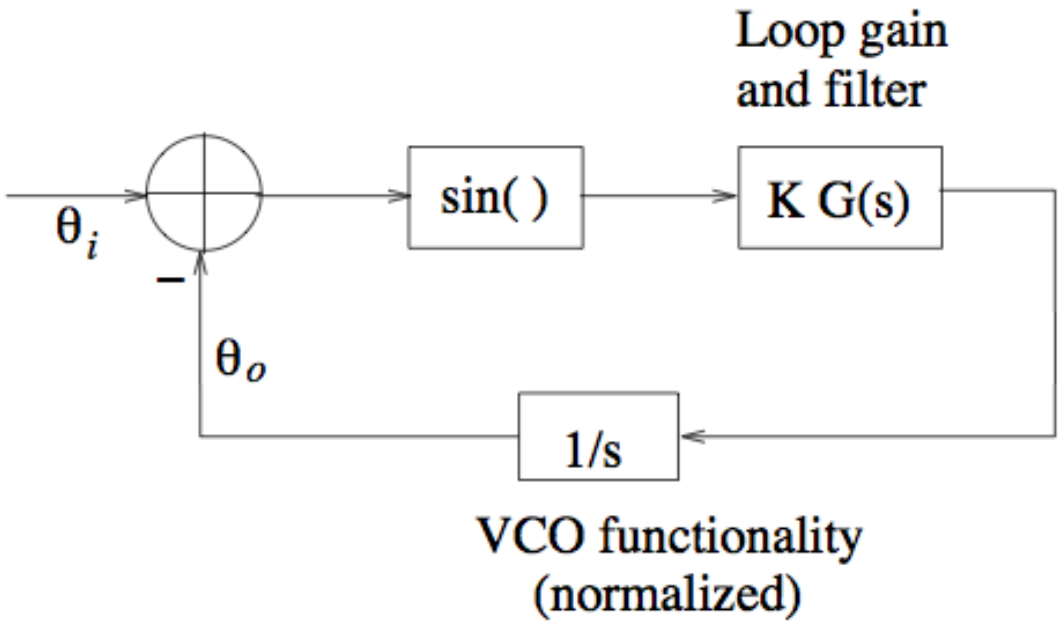
Consider the PLL shown in Fig. assumed to be locked at time zero

1. Suppose that the input phase jumps by $e = 2.72$ radians at time zero assuming $\theta_i(0) = 0$. How long does it take for the difference between the PLL input phase and the VCO output phase to shrink to 1 radian.

2. Find the limiting value of the phase error (in radians) if the frequency jumps by 1 KHz just after time zero.

Actual nonlinear PLL model

Original nonlinear model



- Assuming $G(s) = 1$ (i.e., first order PLL) and for frequency step input, show that

$$\frac{d\theta_e(t)}{dt} = 2\pi\Delta f - K\sin\theta_e(t)$$

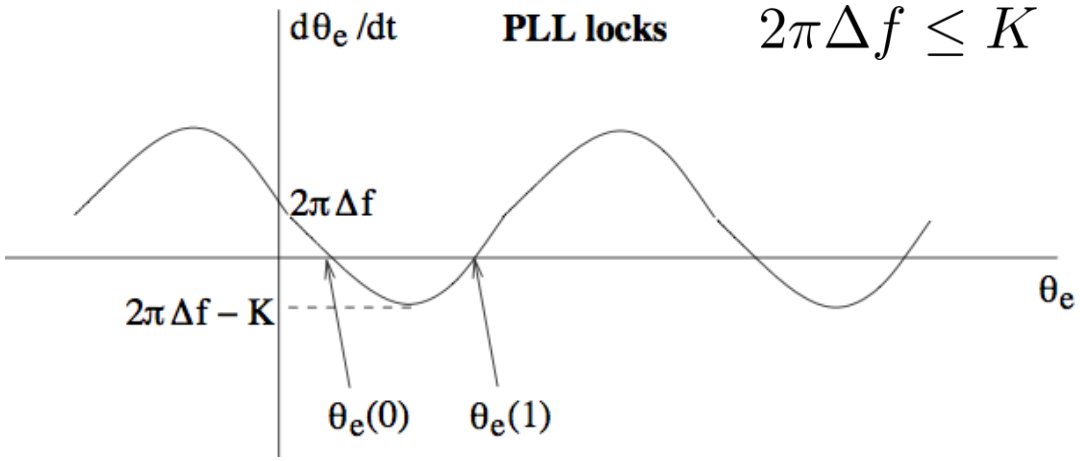
No closed form solution

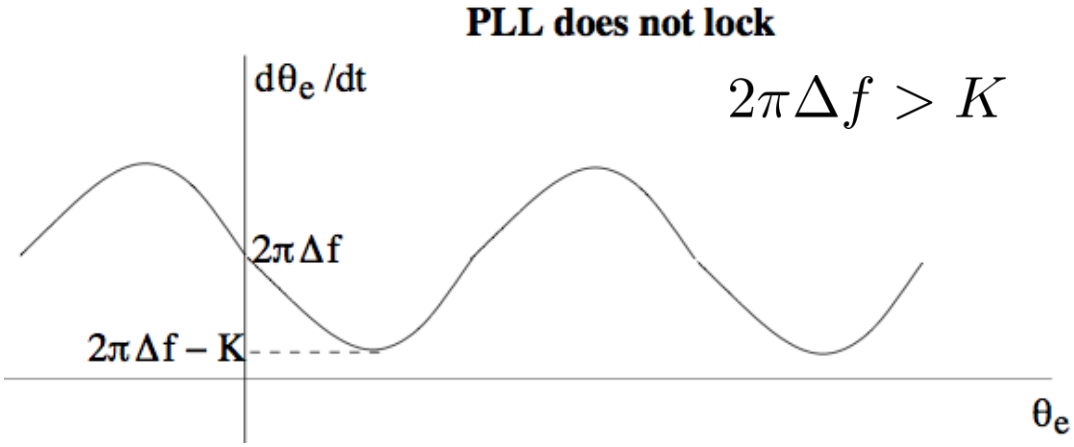
Phase plane plot

$$\frac{d\theta_e(t)}{dt} = 2\pi\Delta f - K\sin\theta_e(t)$$

$$\Downarrow \quad \sin\theta_e(t) \le 1$$

$$\frac{d\theta_e(t)}{dt} \ge 2\pi\Delta f - K$$

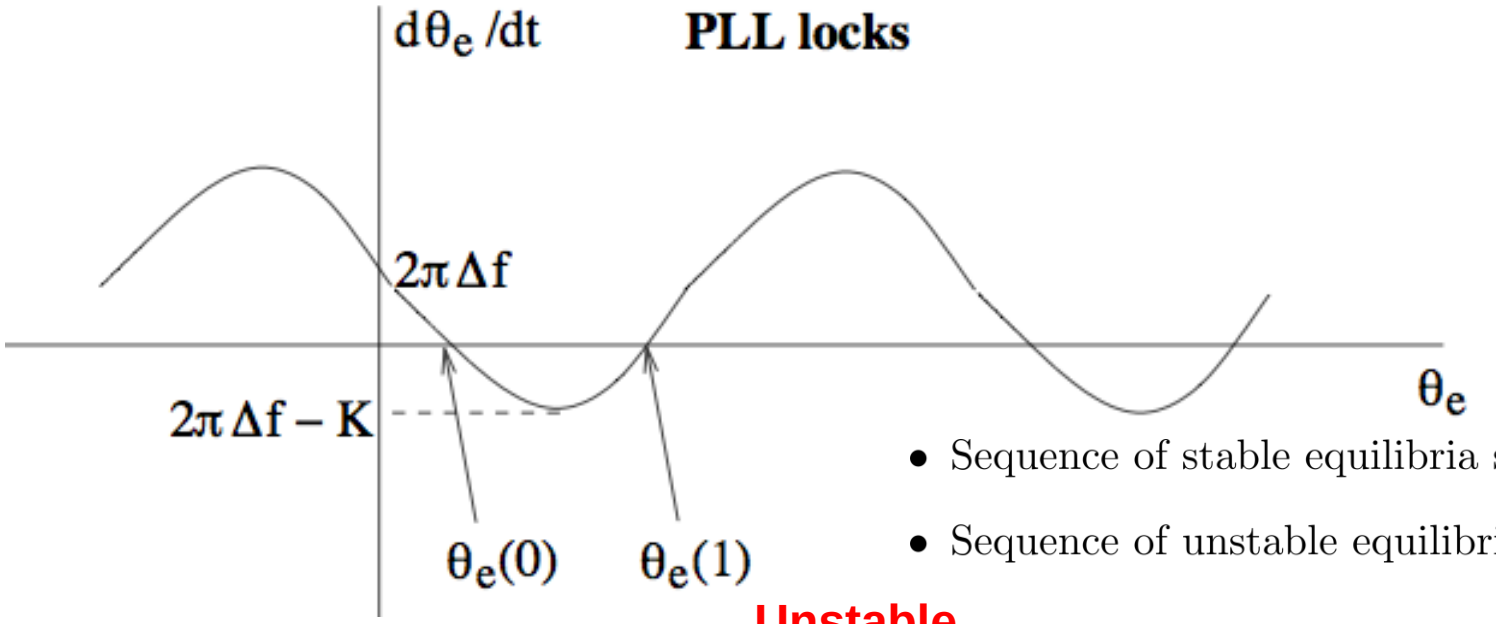




PLL locking

- Find the values of θ_e for which $\frac{d\theta_i}{dt} = 0$
- Investigate their stability.

$$2\pi\Delta f \leq K$$



- Sequence of stable equilibria spaced by 2π
- Sequence of unstable equilibria spaced by 2π

Derivative and error have opposite signs around this, so error is driven back towards zero as it deviates from this equilibrium

Derivative and error have same sign around this so error is driven away from zero as it deviates from this equilibrium.

Nonlinear vs linearized PLL analysis

- Linearized analysis just says that the phase converges to a non-zero value, which gets larger with frequency step.

$$\theta_e(t) \rightarrow \frac{2\pi\Delta f}{K}$$

- For first order PLL, non-linear analysis tells us that the phase does not converge if the frequency step is too large. while there is equilibrium if the frequency step is small enough.

- Linearized analysis gives accurate answers when things are going well, but may miss critical behavior