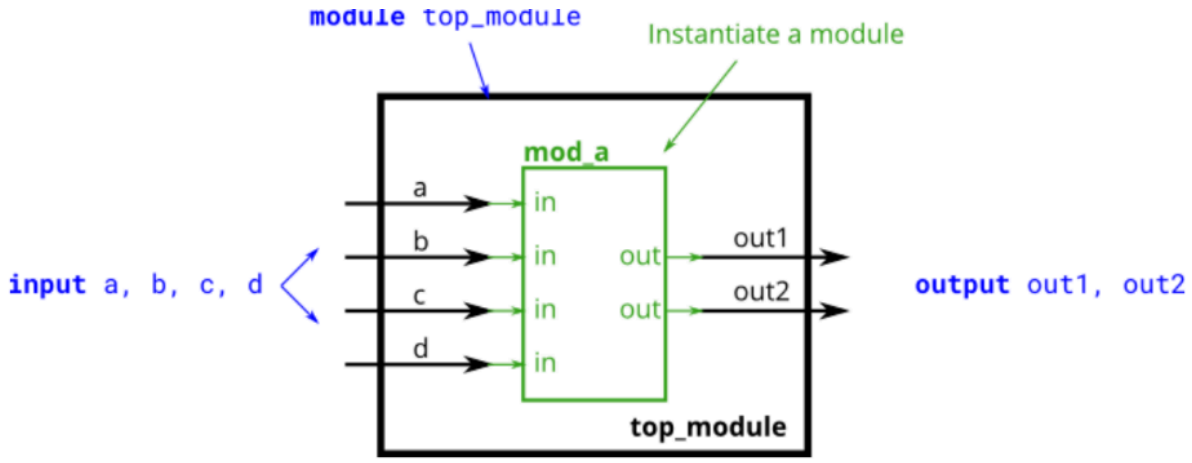
KARTHICK RAJA B
126004121

Given:

You have to design a module named mod_a (you can plan for your own design) that has 2 outputs and 4 inputs, in that order. You must connect the 6 ports by position to your top-level module's ports out1, out2, a, b, c, and d, in that order. You are given the following module:
module mod_a (output, output, input, input, input, input);



Verilog Code:

```
// Given: Choose your own design
// So,Let's choose AND and OR gate

module mod_a(o1,o2,i1,i2,i3,i4);
input i1,i2,i3,i4;
output o1,o2;
assign o1=(i1 & i2); // AND gate
assign o2=(i3 | i4); // OR gate
endmodule

// top module

module top_module_1( out1,out2,a,b,c,d,);
input a,b,c,d;
output out1,out2;
```

```
mod_a m1(.o1(out1),.o2(out2),.i1(a),.i2(b),.i3(c),.i4(d));
endmodule
```

Testbench code:

```
module test_bench_tb6();
reg a,b,c,d;
wire out1,out2;

top_module_1 t1(out1,out2,a,b,c,d,);
initial
begin
a=0; b=0; c=0; d=0; #100;
a=0; b=0; c=1; d=1; #100;
a=0; b=1; c=1; d=1; #100;
a=1; b=1; c=0; d=1; #100;
end
endmodule
```

Functional Simulation: