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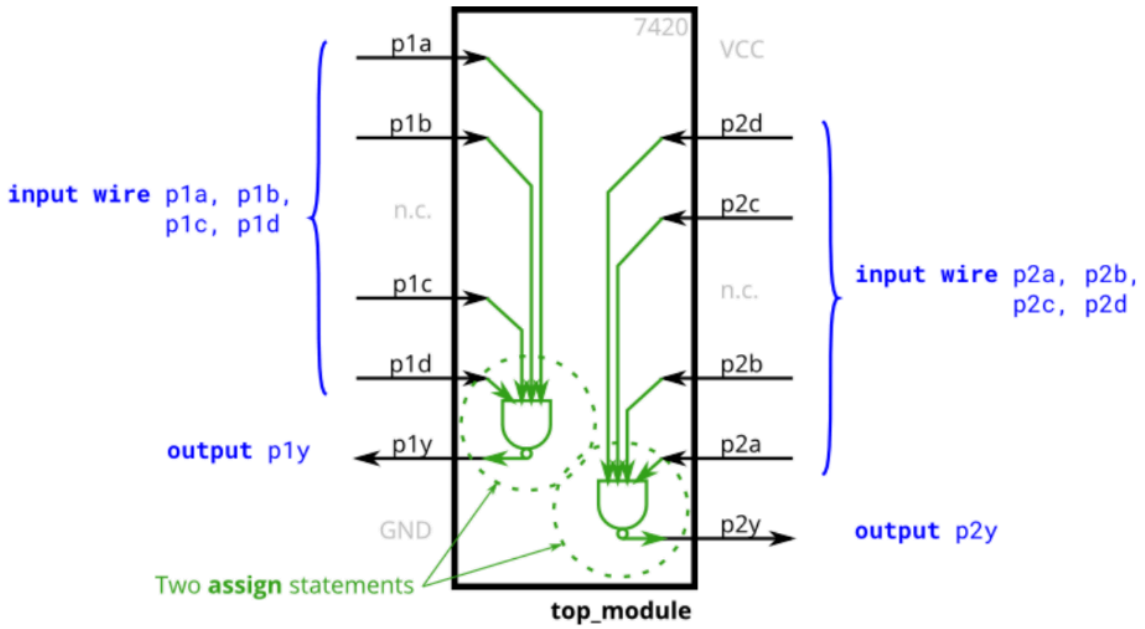
Given:

The 7400-series integrated circuits are a series of digital chips with a few gates each. The 7420 is a chip with two 4-input NAND gates. Create a module with the same functionality as the 7420 chip. It has 8 inputs and 2 outputs.



Verilog Code:

```
module RTL_Day_2 (p1y,p2y,p1a,p1b,p1c,p1d,p2a,p2b,p2c,p2d);
input p1a,p1b,p1c,p1d,p2a,p2b,p2c,p2d;
output p1y,p2y;
assign p1y=~(p1a & p1b & p1c & p1d);
assign p2y=~(p2a & p2b & p2c & p2d);
endmodule
```

Testbench code:

```
module test_bench_tb2();
reg p1a,p1b,p1c,p1d,p2a,p2b,p2c,p2d;
wire p1y,p2y ;
```

```
RTL_Day_2 t2(p1y,p2y,p1a,p1b,p1c,p1d,p2a,p2b,p2c,p2d);
initial
begin

// I have given four combinations for 1st nand gate
p1a=1'b0; p1b=1'b0; p1c=1'b0; p1d=1'b0; #50;        // 0000-0
p1a=1'b0; p1b=1'b0; p1c=1'b0; p1d=1'b1; #50;        // 0001-1
p1a=1'b0; p1b=1'b0; p1c=1'b1; p1d=1'b0; #50;        // 0010-2
p1a=1'b0; p1b=1'b0; p1c=1'b1; p1d=1'b1; #50;        // 0011-3

// I have given  another four combinations for 2nd nand gate
p2a=1'b0; p2b=1'b1; p2c=1'b0; p2d=1'b1; #50;        // 0101-5
p2a=1'b1; p2b=1'b1; p2c=1'b1; p2d=1'b0; #50;        // 1110-14
p2a=1'b1; p2b=1'b1; p2c=1'b1; p2d=1'b1; #50;        // 1111-15
p2a=1'b1; p2b=1'b1; p2c=1'b0; p2d=1'b0;             // 1100-12
end
endmodule
```

Functional Simulation: