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**Given:**

A priority encoder is a combinational circuit that, when given an input bit vector, outputs the position of the first 1 bit in the vector. For example, a 8-bit priority encoder given the input 8'b10010000 would output 3'd4, because bit[4] is first bit that is high. Build a 4-bit priority encoder. For this problem, if none of the input bits are high (i.e., input is zero), output zero. Note that a 4-bit number has 16 possible combinations.

**Verilog code:**

```
module priority_enc(input [3:0]in, output reg[1:0] pos);
always@(*)
begin
if(in==4'b0001 ||in== 4'b0011
||in==4'b0101||in==4'b0111||in==4'b1001||in==4'b1011||in==4'b1101||in==4'b1111)
pos=2'd0;
else if (in==4'b0010|| in==4'b0110||in==4'b1010||in==4'b1110)
pos=2'd1;
else if (in==4'b0100||in==4'b1100)
pos=2'd2;
else if (in==4'b1000)
pos=2'd3;
else
pos=2'd0;
end
endmodule
```

**Testbench Code:**

```
module priority_enc_tb();
reg [3:0] in;
wire [1:0] pos;
priority_enc m1(in,pos);
initial
begin
in=4'b0000; #50;
```

```

in=4'b0001; #50;
in=4'b1001; #50;
in=4'b1110; #50;
in=4'b0010; #50;
in=4'b0100; #50;
in=4'b1100; #50;
in=4'b1000;
end
endmodule

```

### **Functional Simulation:**

Wave - Default		Msgs									
<div> <div></div> <div>/priority_enc_tb/in</div> </div> <div> <div></div> <div>/priority_enc_tb/pos</div> </div>	0000	0000	0001	1001	1110	0010	0100	1100	1000		
	00	00			01		10		11		