KARTHICK RAJA B
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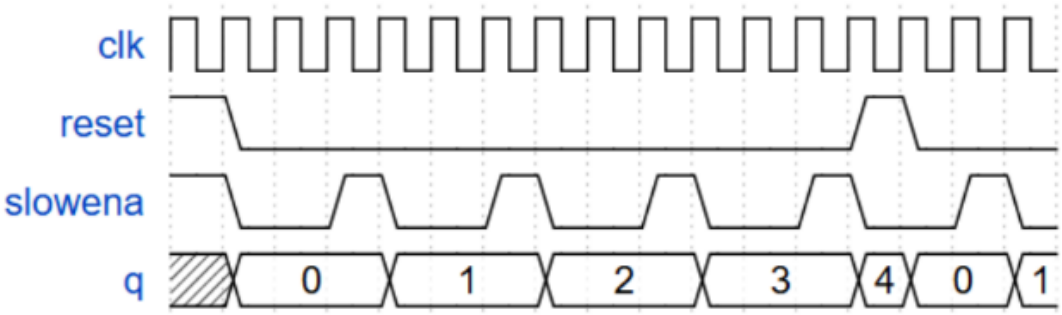
Given:

Build a decade counter that counts from 0 through 9, inclusive, with a period of 10. The reset input is synchronous, and should reset the counter to 0. We want to be able to pause the counter rather than always incrementing every clock cycle, so the slowena input indicates when the counter should increment.



Verilog Code:

```
module RTL_Day_18(clk,q,slowena,rst);
input clk,rst,slowena;
output reg[3:0] q;
always @(posedge clk)
begin
if(rst) begin
q<=4'b0000;
end
else begin
if(slowena)
q<=q+1'b0;
else
begin
if(q<10)
q<=q+1'b1;
else
q<=4'b0000;
end
```

```
end
end
endmodule
```

Testbench Code:

```
module test_bench_tb18();
reg clk,rst,slowena;
wire[3:0]q;
RTL_Day_18 n1(clk,q,slowena,rst);
always
#50
clk=~clk;
initial
begin
clk=1'b0;
rst=1'b1; #100;
rst=1'b0; #100;
slowena=1'b0; #100;
slowena=1'b1; #100;
slowena=1'b0; #100;
slowena=1'b1; #100;
end
endmodule
```

Functional simulation: