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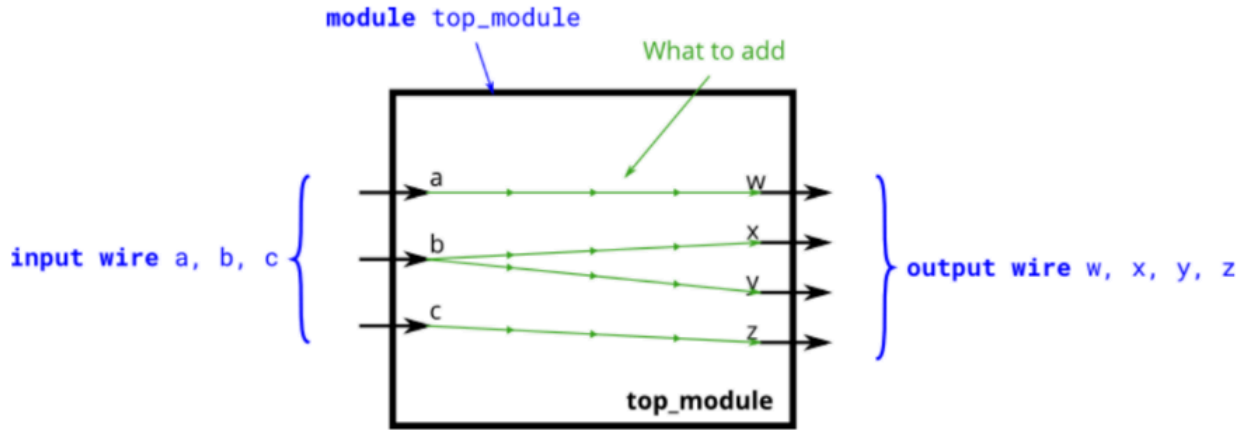
## Given:

Create a module with 3 inputs and 4 outputs that behaves like wires that make these connections. The diagram below illustrates how each part of the circuit corresponds to each bit of Verilog code. From outside the module, there are three input ports and four output ports.




## Verilog HDL code:

```
module top_module(a,b,c,w,x,y,z);
input a,b,c;
output w,x,y,z;
assign w=a;
assign x=b;
assign y=b;
assign z=c;
endmodule
```

## Testbench code:

```
module top_module_tb1();
reg a,b,c;
wire w,x,y,z;
```

```
top_module t1(a,b,c,w,x,y,z);
initial
begin
a=1'b0; b=1'b0; c=1'b0; #50;
a=1'b0; b=1'b0; c=1'b1; #50;
a=1'b0; b=1'b1; c=1'b0; #50;
a=1'b0; b=1'b1; c=1'b1; #50;
a=1'b1; b=1'b0; c=1'b0; #50;
a=1'b1; b=1'b0; c=1'b1; #50;
a=1'b1; b=1'b1; c=1'b0; #50;
a=1'b1; b=1'b1; c=1'b1;
end
endmodule
```

**Functional Simulation:**