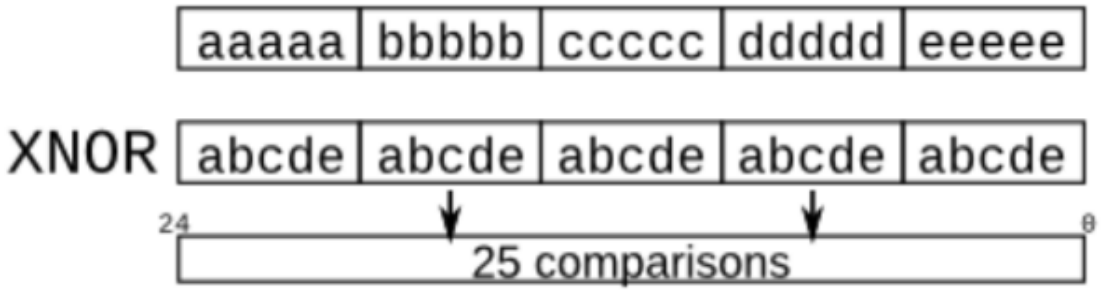
KARTHICK RAJA B
126004121

Given:

Given five 1-bit signals (a, b, c, d, and e), compute all 25 pairwise one-bit comparisons in the 25-bit output vector. The output should be 1 if the two bits being compared are equal.



Verilog code:

```
module rtl_day5(input a,b,c,d,e, output [24:0] out); assign
out=~{{5{a}},{5{b}},{5{c}},{5{d}},{5{e}}}^{5{a,b,c,d,e}};
endmodule
```

Test bench Code:

```
module rt_day5_tb();
reg a,b,c,d,e;
wire [24:0] out;
rt_day5 r1(a,b,c,d,e,out);
Initial
begin
a=0;b=0;c=0;d=0;e=0;#100;
a=0;b=1;c=1;d=1;e=1;#100;
a=1;b=0;c=1;d=0;e=1;#100;
a=1;b=0;c=1;d=1;e=1;#100;
a=1;b=1;c=0;d=1;e=1;#100;
a=1;b=1;c=1;d=0;e=1;#100;
a=1;b=1;c=1;d=1;e=0;#100;
```

a=1;b=1;c=1;d=1;e=1;
end
Endmodule

Functional Simulation: