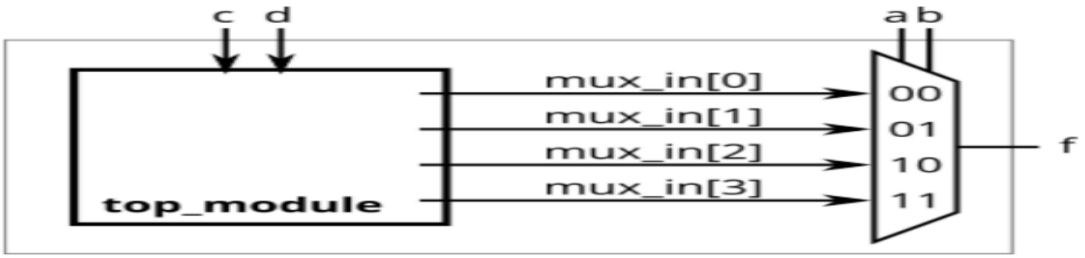
KARTHICK RAJA B
126004121

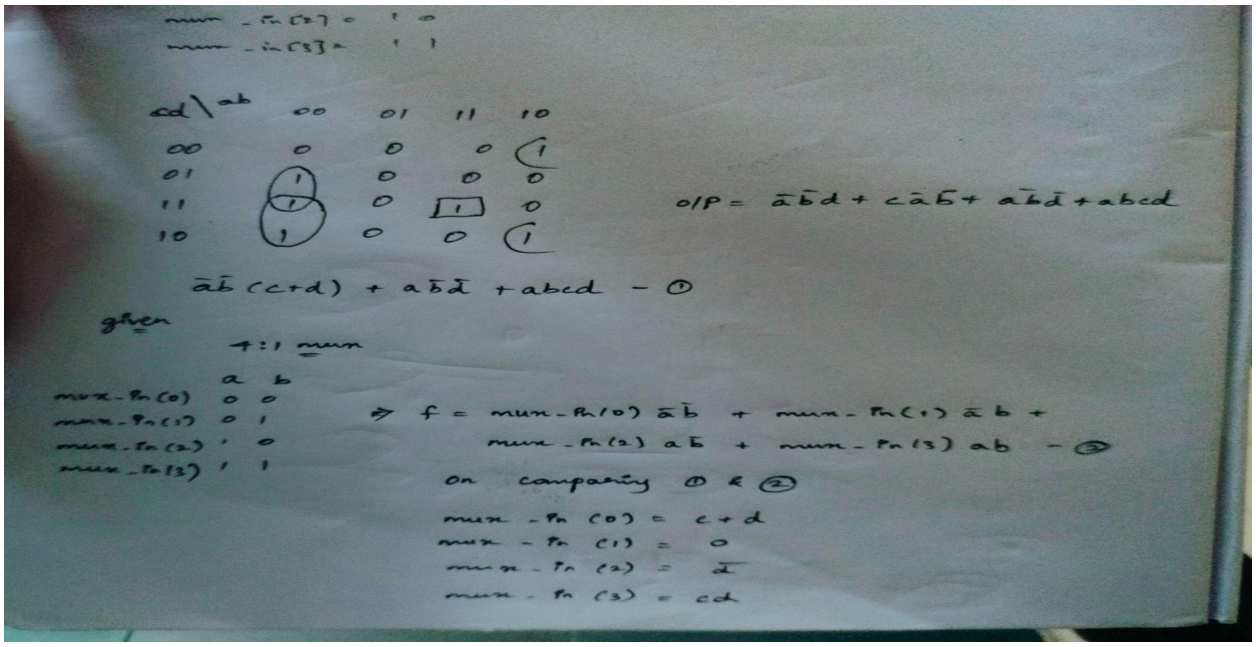
Given:

For the following Karnaugh map, give the circuit implementation using one 4-to-1 multiplexer and as many 2-to-1 multiplexers as required, but using as few as possible. You are not allowed to use any other logic gate and you must use a and b as the multiplexer selector inputs, as shown on the 4-to-1 multiplexer below. You are implementing just the portion labelled top_module, such that the entire circuit (including the 4-to-1 mux) implements the K-map.

cd \ ab	00	01	11	10
00	0	0	0	1
01	1	0	0	0
11	1	0	1	0
10	1	0	0	1



K-Map Simplification:



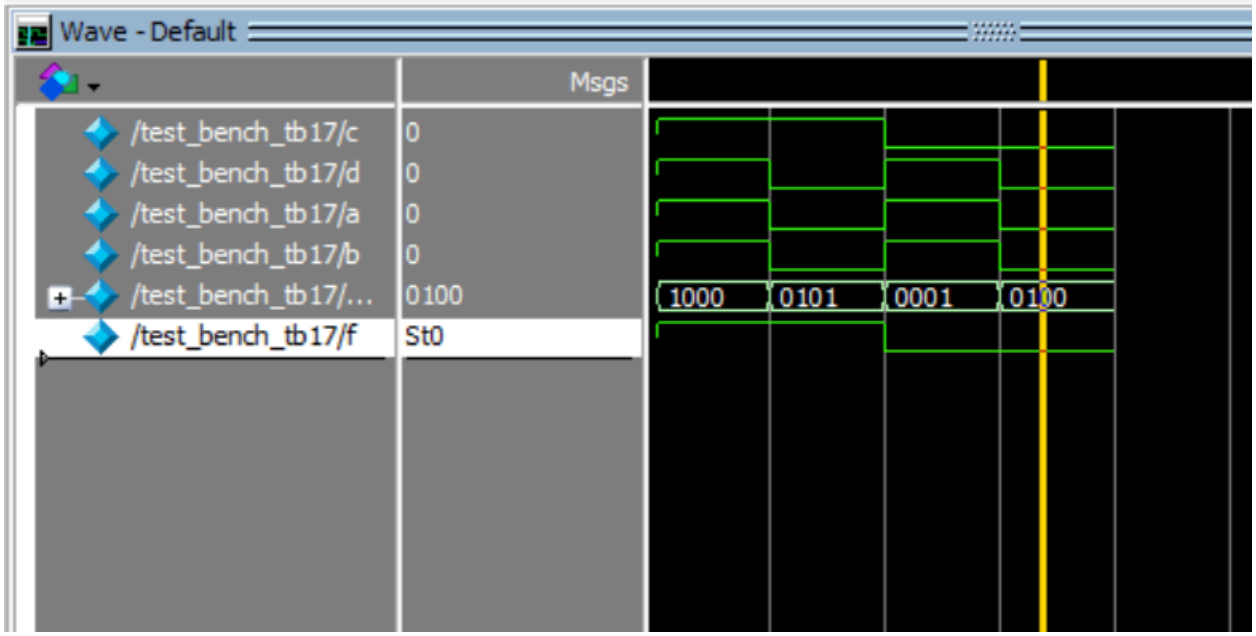
Verilog code:

```
module RTL_Day_17(c,d,a,b,mux_in,f);
input a,b,c,d;
output [3:0] mux_in;
output reg f;
wire w1,w2;
assign w1= c & d;
assign w2= c + d;
assign mux_in={w1,~d,1'b0,w2};
always @ (*)
begin
 case({a,b})
 2'b00:f=mux_in[0];
 2'b01:f=mux_in[1];
 2'b10:f=mux_in[2];
 2'b11:f=mux_in[3]; 1
 endcase
 end
endmodule
```

Testbench code:

```
module test_bench_tb17();
reg c,d,a,b;
wire [3:0]mux_in;
wire f;
RTL_Day_17 f1(c,d,a,b,mux_in,f);
initial
begin
c=1; d=1; a=1; b=1; #50;
c=1; d=1; a=0; b=0; #50;
c=0; d=0; a=1; b=1; #50;
c=0; d=0; a=0; b=0;
end
endmodule
```

Functional Simulation:


Wave - Default
Msgs
/test_bench_tb17/c
/test_bench_tb17/d
/test_bench_tb17/a
/test_bench_tb17/b
/test_bench_tb17/...
/test_bench_tb17/f
0
0
0
0
0100
St0
1000
0101
0001
0100