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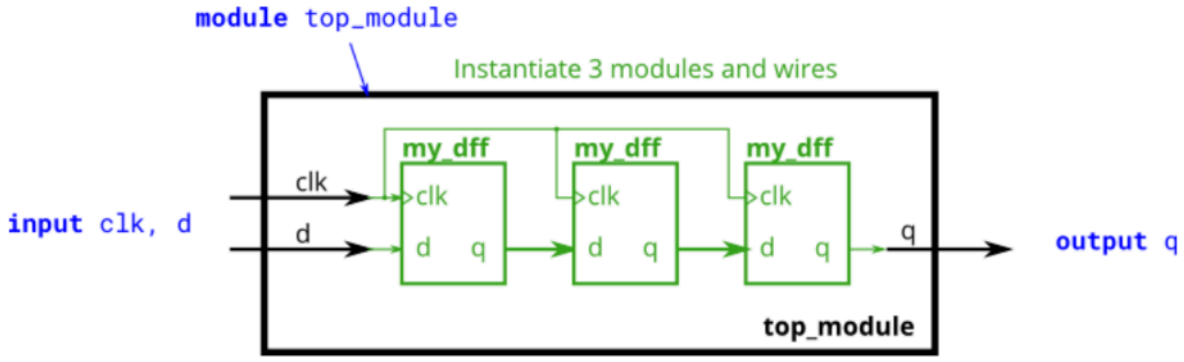
Given:

You have to design a module my_dff with two inputs and one output (that implements a D flip-flop). Instantiate three of them, then chain them together to make a shift register of length 3. The clk port needs to be connected to all instances.



Verilog Code:

```
module dff(q,d,clk);
input clk,d;
output reg q;
always @(posedge clk)
begin
q<=d;
end
endmodule

module RTL_Day_13(q,d,clk);
input clk,d;
output  q;
wire w1,w2;
dff d1(w1,d,clk);
dff d2(w2,w1,clk);
dff d3(q,w2,clk);
endmodule
```

Testbench Code:

```
module test_bench_tb13();
reg clk,d;
wire q;
wire w1,w2;
RTL_Day_13 r1(q,d,clk);
initial
begin
clk=1; d=0; #100;
clk=1; d=1; #100;
end
endmodule
```

Functional Simulation: