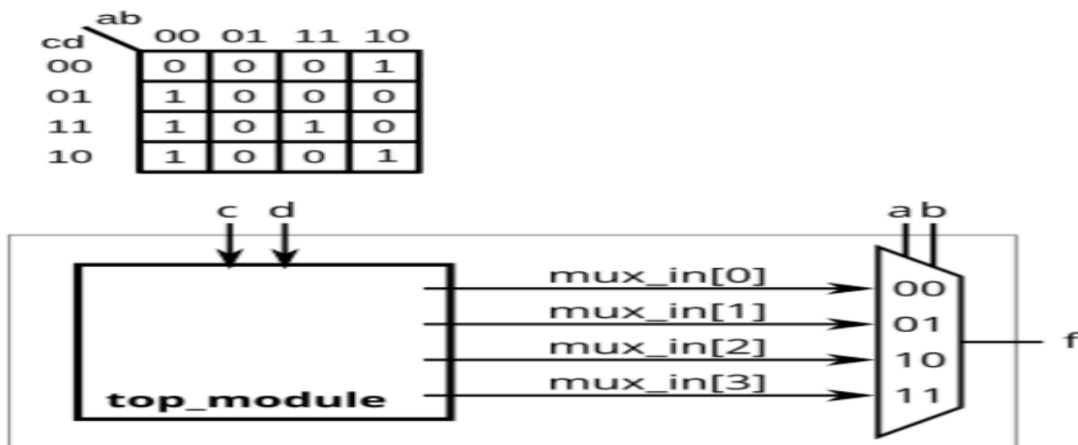


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**Given:**

For the following Karnaugh map, give the circuit implementation using one 4-to-1 multiplexer and as many 2-to-1 multiplexers as required, but using as few as possible. You are not allowed to use any other logic gate and you must use a and b as the multiplexer selector inputs, as shown on the 4-to-1 multiplexer below. You are implementing just the portion labelled top\_module, such that the entire circuit (including the 4-to-1 mux) implements the K-map.



**K-Map Simplification:**

Handwritten K-map simplification and circuit implementation:

K-map (with groupings):

cd \ ab	00	01	11	10
00	0	0	0	1
01	1	0	0	0
11	1	0	1	0
10	1	0	0	1

Groupings: (00,10) column, (01,11) column, (11,10) row, (01,11) row.

o/p =  $\bar{a}\bar{b}d + c\bar{a}\bar{b} + \bar{a}b\bar{d} + abcd$

$\bar{a}\bar{b}(c+d) + a\bar{b}\bar{d} + abcd = \text{①}$

given  $f = \text{mux}$

	a	b
mux - P <sub>0</sub> (0)	0	0
mux - P <sub>0</sub> (1)	0	1
mux - P <sub>0</sub> (2)	1	0
mux - P <sub>0</sub> (3)	1	1

$\Rightarrow f = \text{mux} - P_0(0) \bar{a}\bar{b} + \text{mux} - P_0(1) \bar{a}b + \text{mux} - P_0(2) a\bar{b} + \text{mux} - P_0(3) ab = \text{②}$

On comparing ① & ②

mux - P<sub>0</sub>(0) =  $c + d$   
 mux - P<sub>0</sub>(1) = 0  
 mux - P<sub>0</sub>(2) =  $\bar{d}$   
 mux - P<sub>0</sub>(3) =  $cd$








**Verilog code:**

```
module RTL_Day_17(c,d,a,b,mux_in,f);
input a,b,c,d;
output [3:0] mux_in;
output reg f;
wire w1,w2;
assign w1= c & d;
assign w2= c + d;
assign mux_in={w1,~d,1'b0,w2};
always @ (*)
begin
    case({a,b})
        2'b00:f=mux_in[0];
        2'b01:f=mux_in[1];
        2'b10:f=mux_in[2];
        2'b11:f=mux_in[3];
    endcase
end
endmodule
```

**Testbench code:**

```
module test_bench_tb17();
reg c,d,a,b;
wire [3:0]mux_in;
wire f;
RTL_Day_17 fl(c,d,a,b,mux_in,f);
initial
begin
    c=1; d=1; a=1; b=1; #50;
    c=1; d=1; a=0; b=0; #50;
    c=0; d=0; a=1; b=1; #50;
    c=0; d=0; a=0; b=0;
end
endmodule
```

**Functional Simulation:**

Wave - Default		Msgs			
					
	/test_bench_tb17/c	0			
	/test_bench_tb17/d	0			
	/test_bench_tb17/a	0			
	/test_bench_tb17/b	0			
	/test_bench_tb17/...	0100	1000	0101	0001
	/test_bench_tb17/f	St0			0100