Current Starved Voltage Controlled Oscillator

Karthigaa S

Department of Electronics Engineering, Madras Institute of Technology, Anna University,

Chennai, Tamilnadu 600044, India

karthigaa0722@gmail.com

***Abstract*—This paper introduces a hybrid current-starved ring voltage-controlled oscillator (VCO) employing NMOS and PMOS transistors with a bulk-driven keeper technique to improve high-frequency performance in PLL applications. The circuit consists of NMOS pull-down sleepy stack transistors to minimize leakage, PMOS pull-up sleepy transistors for stable current flow, and bulk-driven PMOS keeper transistors that dynamically adjust threshold voltages to enhance PVT tolerance.**

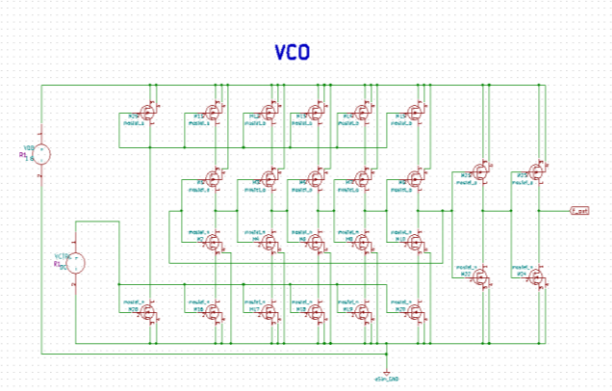
Keywords: *Hybrid VCO, current-starved, NMOS, PMOS, bulk-driven keeper, PVT tolerance, low power, phase noise.*

I. INTRODUCTION

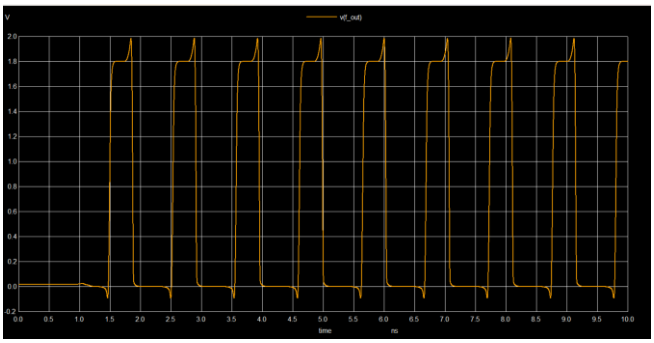
A VCO is central to a PLL and can be based on LC or RC architectures. LC VCOs offer superior phase noise performance but have limited tuning range, larger area, and higher power requirements due to on-chip inductors. Ring VCOs, in contrast, save chip area, provide a wide tuning range, and can produce quadrature-phase outputs. In a "current-starved" design, current is limited by mirroring through each inverter stage, which enhances PVT tolerance and makes it suitable for high-frequency PLLs needing reliable performance under varying conditions.

II.PRINCIPLE OF GENERATION

A VCO is central to a PLL, producing a frequency output based on input voltage, functioning as a voltage-to-frequency converter. Unlike resonator-based oscillators, ring oscillators meet the Barkhausen criteria through sufficient open-loop gain. They work by charging and discharging the gate capacitance across inverter stages, with additional buffer inverters to prevent output loading, which can affect oscillation frequency and VCO gain.



III. RESULTS



The output frequency @ vctrl=0.9V is 961MHz

IV. ISSUES AND IMPROVEMENTS

This VCO circuit faces challenges related to power consumption, and stability. The large transistor count increases area and design complexity, impacting scalability and layout efficiency.

High power consumption due to simultaneous transistor operation could be optimized with enhanced power gating. Signal integrity issues, potentially arising from dense transistor placement, may require improved isolation techniques, while the bulk-driven approach could affect stability, necessitating careful threshold tuning.

V. CONCLUSION

This paper presents a hybrid current-starved ring VCO using bulk-driven keeper and sleepy stack techniques to reduce leakage, power consumption, and enhance PVT tolerance. These optimizations improve frequency stability, making the design suitable for high-performance PLL applications.

VI. REFERENCE

M. Sivasakthi and P. Radhika, "Design and analysis of PVT tolerant hybrid current starved ring VCO with bulk driven keeper technique at 45 nm CMOS technology for the PLL application,"

https://www.researchgate.net/figure/Linearized-current-starved-Voltage-Controlled-Oscillator_fig2_333347988

VII.ACKNOWLEDGEMENT

Kunal Ghosh, Co-Founder of VLSI System Design (VSD) Corp. Pvt. Ltd.