1101 Sequence Detector using CMOS Logic

A project Report

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Bachelor of Technology

In

Department of Electronics and Communication Engineering

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DECLARATION

The Project Report entitled "**Sequence Detector of 1101 using CMOS Logic**" is a record of bonafide work of **R. Vinay Vardhan Naidu (2320040117), K. V. Sai Sri Hari (2320040033), P. Karthik (2320040019)**, submitted in partial fulfillment for the award of **B. Tech in Electronic and Communication Engineering** to the K L University. The results embodied in this report have not been copied from any other departments/University/Institute.

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CERTIFICATE

This is certify that the project based lab report entitled **"Sequence Detector 1101 using CMOS "** is a Bonafide work done and submitted by **R. Vinay Vardhan(2320040117), K.V. Sai SriHari (2320040033), P. Karthik (2320040019)** in partial fulfillment of the requirements for the award of the degree of Bachelor of Technology in Department of Electronics & Communication Engineering, K L (Deemed to be University), Guntur District during the academic year 2020.

Signature of the Supervisor
Dr. J. Lakshmi Prasanna Madam
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Signature of HOD

Signature of the Examiner

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The success in this project would not have been possible but for the timely help and guidance rendered by **Supervisor** Dr. J . Lakshmi Prasanna madam . Our wish to express my sincere thanks to all those who has assisted us in one way or the other for the completion of my project.

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ABSTRACT

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CHAPTER-1
INTRODUCTION

A combinational circuit and storage elements are interconnected to form a sequential circuit. The information stored at any time defines the state of the circuit at that time. The next state of the storage elements is a function of the inputs and the present state. Synchronous sequential circuit can be defined from the knowledge of its signals at discrete instants.

Sequence detectors are crucial components in digital systems that identify specific binary patterns from a stream of input data. These patterns are essential in communication protocols, encryption, digital signal processing, and more. A typical sequence detector implements a finite state machine (FSM) that transitions through states based on input bits and signals a match when the desired sequence is detected.

In this project, we aim to detect the **Sequence "1101"**, which means the system should generate a high output signal when this exact bit pattern appears in the input stream. The complexity of sequence detection increases with longer patterns or overlapping sequences, but the principles remain the same. The choice of hardware implementation significantly affects the performance, reliability, and power consumption of the design.

The design and implementation of sequence detectors play a vital role in digital electronics and communication systems, where the identification of specific patterns in a stream of input data is essential. This project focuses on developing a **1101 sequence detector** using **CMOS (Complementary Metal-Oxide-Semiconductor) technology**, which is known for its low power consumption and high noise immunity.
The primary objective is to detect the occurrence of the binary sequence **1101** in a serial input stream. A **Mealy state machine** model is used to realize the detector, ensuring accurate pattern recognition with minimal hardware complexity. By utilizing CMOS-based logic gates and flip-flops, the project highlights
the practical aspects of **VLSI (Very-Large-Scale Integration)** design and enhances the understanding of sequential logic circuits. This project not only reinforces theoretical concepts such as finite state machines and logic design but also provides hands-on experience in circuit implementation using efficient CMOS techniques

CHAPTER 2

LITERATURE SURVEY

Sequence detectors are essential components in digital systems, designed to recognize specific patterns in a serial input stream. Designed to identify particular patterns in a serial input stream, sequence detectors are crucial parts of digital systems. Finite State Machines (FSMs) are frequently used to implement these detectors; the two most popular models are the Mealy and Moore models. Unlike Moore machines,

Mealy machines can respond more quickly because their output is dependent on both the input and the current state.

Sequence Detectors

A sequence detector is a digital system that recognizes a specific sequence of bits in a serial input data stream. It is typically implemented using a **Finite State Machine (FSM)**, which transitions between different states based on the current input and previous states. Sequence detectors can be designed using either the Moore or Mealy models and are widely applied in data encoding/decoding, digital communication systems, and control units.

Numerous studies have explored the use of Mealy FSMs for pattern detection, highlighting their efficiency in reducing the number of states and minimizing hardware complexity. The **1101 sequence detector** is a classic case study in FSM design, used extensively in academic and industrial applications to demonstrate principles of sequential logic and timing behavior.

Introduction to NORA CMOS Logic

The integration of CMOS (Complementary Metal-Oxide-Semiconductor) technology in digital circuit design has revolutionized modern electronics by enabling low power consumption, high-speed operation, and improved noise immunity. CMOS logic gates form the backbone of sequential circuits, including state machines and sequence detectors, particularly in low-power VLSI designs

Advantages of CMOS

- Consumes very low power compared to other logic families.
- Ensures reliable logic level representation.
- Provides balanced speed and power efficiency

Advanced EDA tools such as **Cadence Virtuoso** are widely adopted in industry and academia for designing and simulating transistor-level CMOS circuits. They provide an accurate environment for layout, circuit simulation, and performance analysis. Prior research confirms that Cadence effectively supports the modeling of Mealy FSMs at the gate and transistor levels using CMOS logic.

Limitations of CMOS technology

- Performance may degrade at very high temperatures**.**
- High input impedance makes it prone to floating inputs.
- Lower driving capability for high fan-out loads.

Application of NORA Logic in FSM Design

CMOS technology plays a vital role in the design and implementation of Finite State Machines (FSMs) due to its low power consumption, high integration capability, and reliable performance. FSMs designed using CMOS are widely used in various digital systems where sequential control and pattern recognition are essential. Applications include sequence detectors, digital counters, and control units in microprocessors, where FSMs guide system behavior based on input conditions and current states. CMOS-based FSMs are also employed in real-time control systems such as traffic light controllers, elevator logic, vending machines, and digital locking mechanisms. Furthermore, in communication systems, CMOS FSMs handle protocol control, serial data management, and error detection tasks. Their energy efficiency and scalability make CMOS FSMs especially suitable for modern embedded systems and IoT devices, where compact, low-power logic is crucial..

CHAPTER 3
THEORITICAL ANALYSIS

A sequence detector for “1101” involves:

- **Four states**: S0 (initial), S1 (1), S2 (11), S3 (110)
- **Transitions** based on current state and input bit

CMOS Logic Overview:

CMOS (Complementary Metal-Oxide-Semiconductor) is a widely used technology in digital electronics. It uses both PMOS and NMOS transistors to create efficient logic gates. CMOS circuits are known for their very low power consumption and high reliability. They are compact, fast, and ideal for integrating large numbers of logic functions on a chip. Because of these advantages, CMOS is used in almost all modern electronic devices and systems.

- Consumes very low power
- Easy for implementation
- Efficient Pull down and Pull up

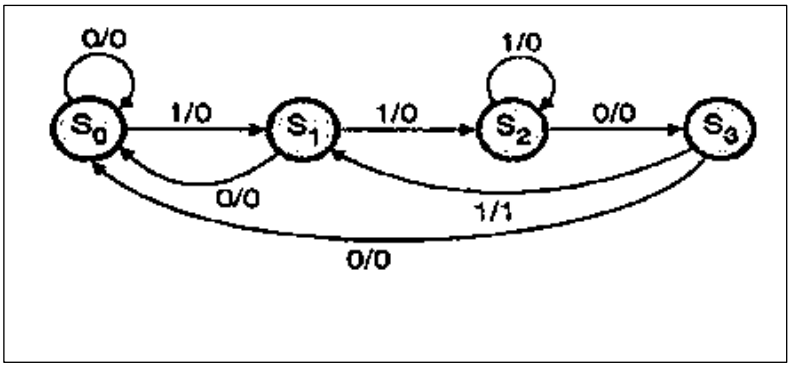
CHAPTER 4

EXPERIMENTAL INVESTIGATION

4.1 Methodology:

Establishing the design specifications for a 1101 sequence detector is the first step in the project. Finding the binary sequence "1101" in a continuous input stream is the task at hand. The chosen model is a Mealy machine, in which the input and current state both affect the output.

Mealy FSM of 1101



The sequence detector is built using a **Mealy state machine** with 4 states:

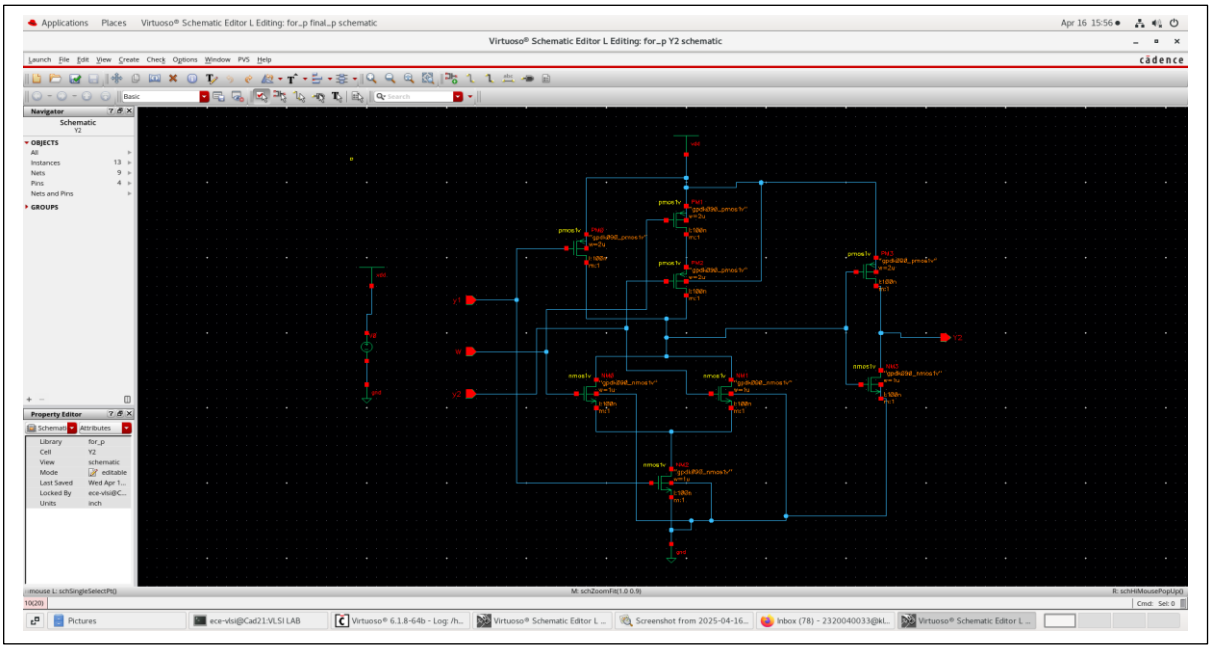
- **State 0**: No sequence detected (Initial state).
- **State 1**: The first '1' in the "1101" sequence detected.
- **State 2**: The second '1' in the sequence detected.
- **State 3**: Full "1101" sequence detected.

The states transition based on the input bits (0 or 1). The output is generated when the full sequence is detected.

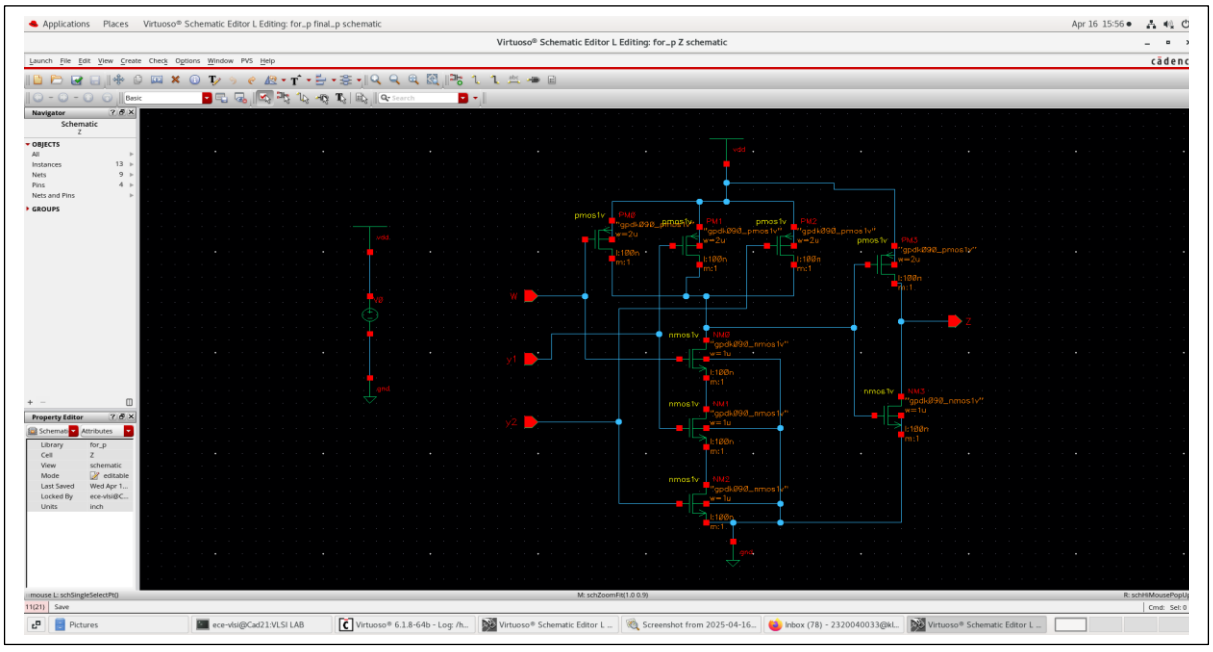
CMOS Logic Design

The state machine is implemented using **CMOS logic gates**. The basic gates and some schematics t are designed using CMOS transistors to form the required logic. Each state and its corresponding transitions are mapped into CMOS logic circuits and then converted each to the symbol.

Schematic of Y2:



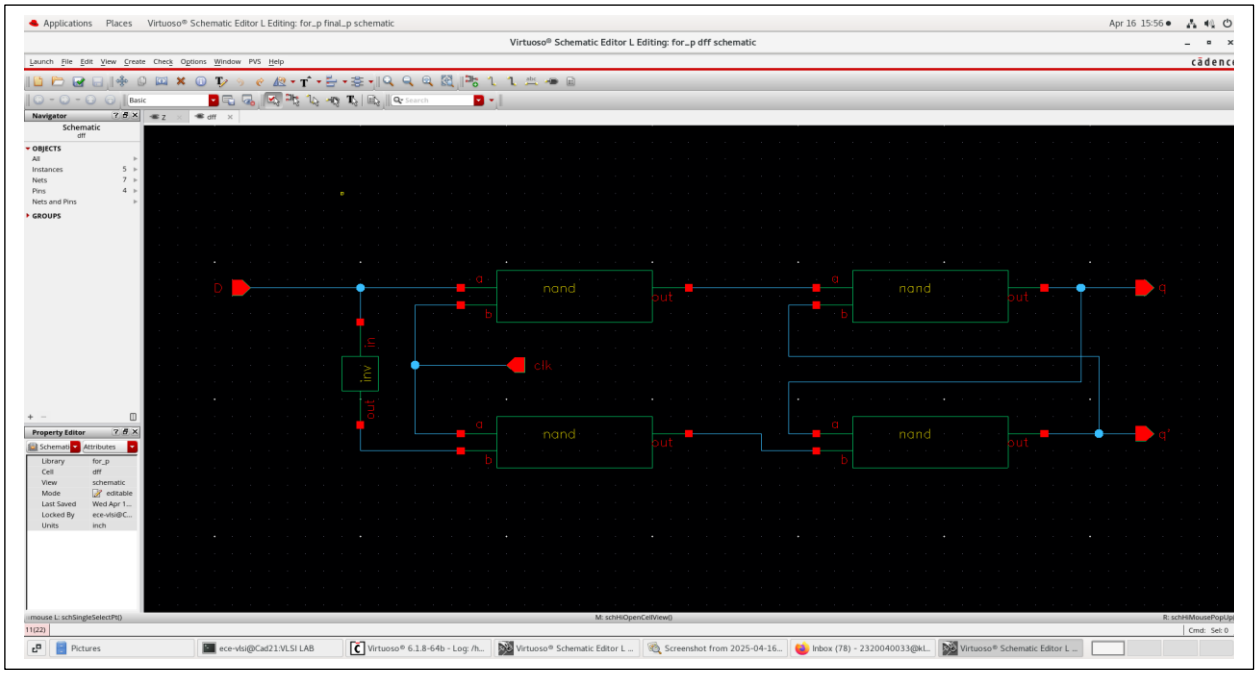
Schematic of Z:



Simulation in Cadence

The design is modelled and tested in **Cadence Virtuoso**. This includes creating the schematic and symbol and simulating the logic to verify its functionality. The simulation ensures the sequence detection mechanism works as expected of transient analysis .

Schematic of D flip flop:



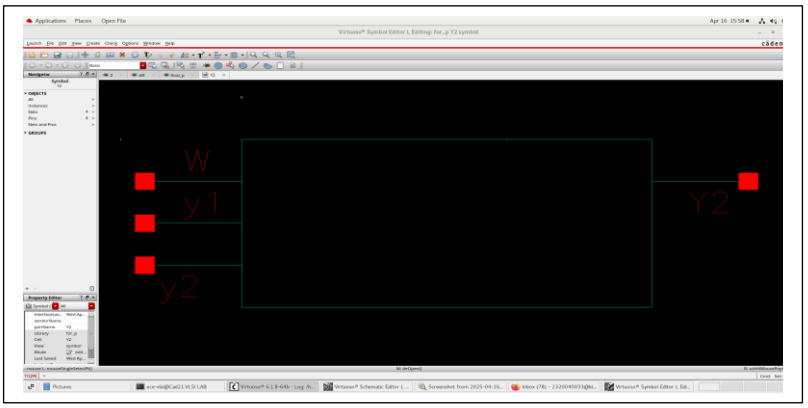
To make sure the circuit recognises the "1101" pattern accurately, it is tested using a variety of input sequences. To verify that the output is accurate, the results are examined (high when the sequence is detected, low otherwise low level).
The technology used is 90nm, with a minimum length of 90nm.

Finalisation and Optimisation:

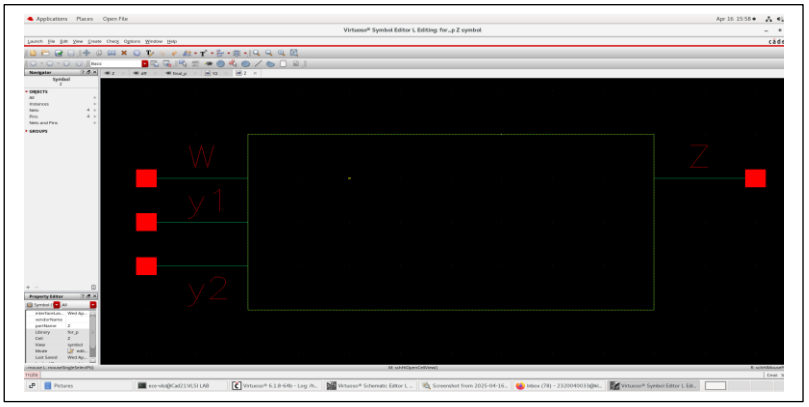
By reducing the number of states using a relay and creating an easily readable symbol, the design optimises both power consumption and area while guaranteeing the circuit's dependability. After that, the final design is recorded, and the testing outcomes are examined.

Symbols of Y2, Z, D Flip flop

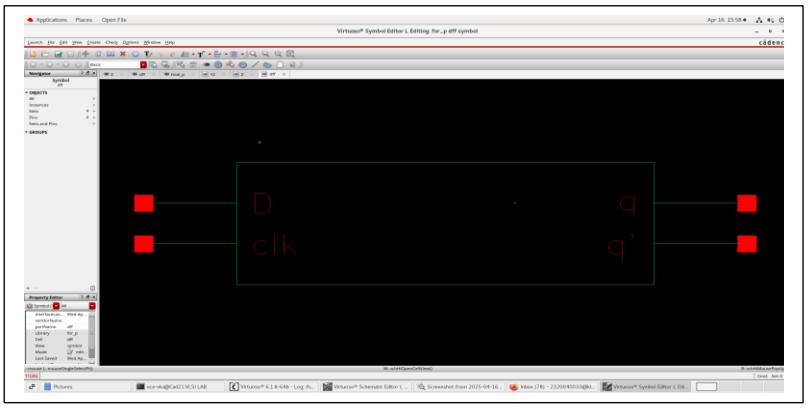
Y2:



Z:



D flip flop:



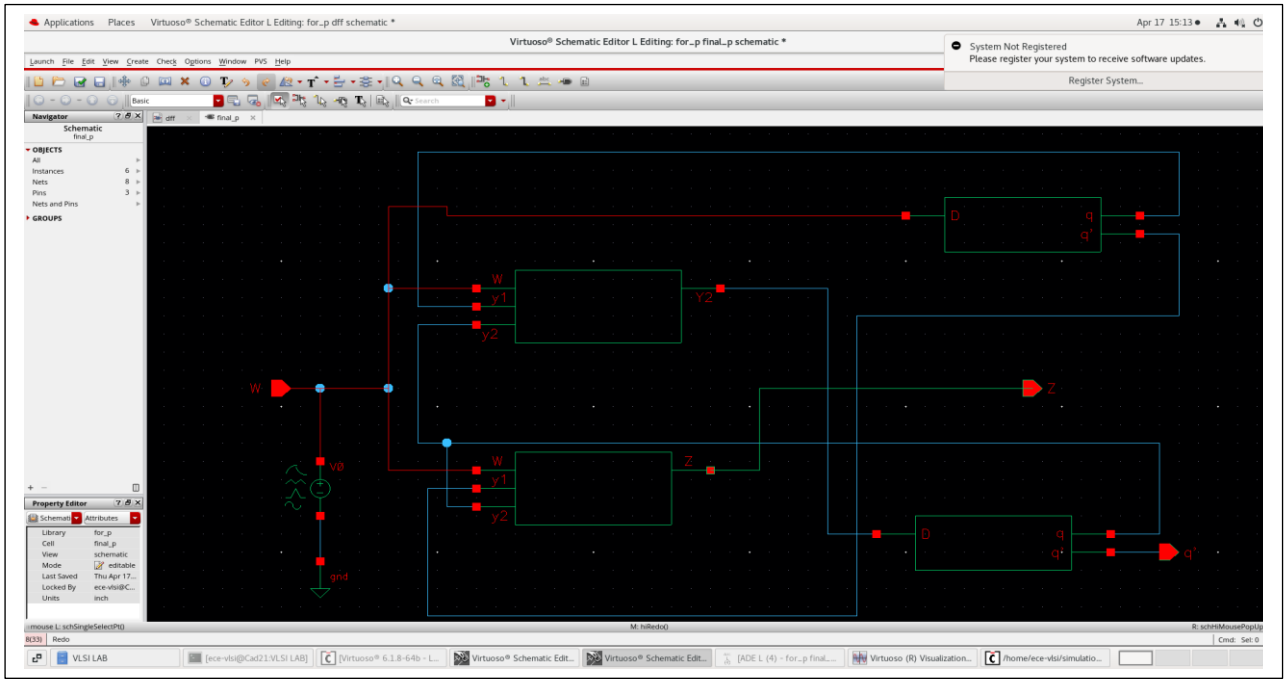
Chapter 5
EXPERIMENT RESULTS

This has successfully designed and gets the perfect output i.e. the output is 1 when the input is “1101” in the transient analysis for clear verification the output wave form has mentioned below.
We have given the input “110110100111” by the bits in the source and when has detected it will take 1.8 volts and when 0 is mentioned it takes 0 and when it detects in 1101 in the sequence it will give voltage at 1.8 and this was clearly in the wave form and here for the D-flipflop pulse waveform has been used to provide clock and the design of the Y2 was designed using CMOS technology

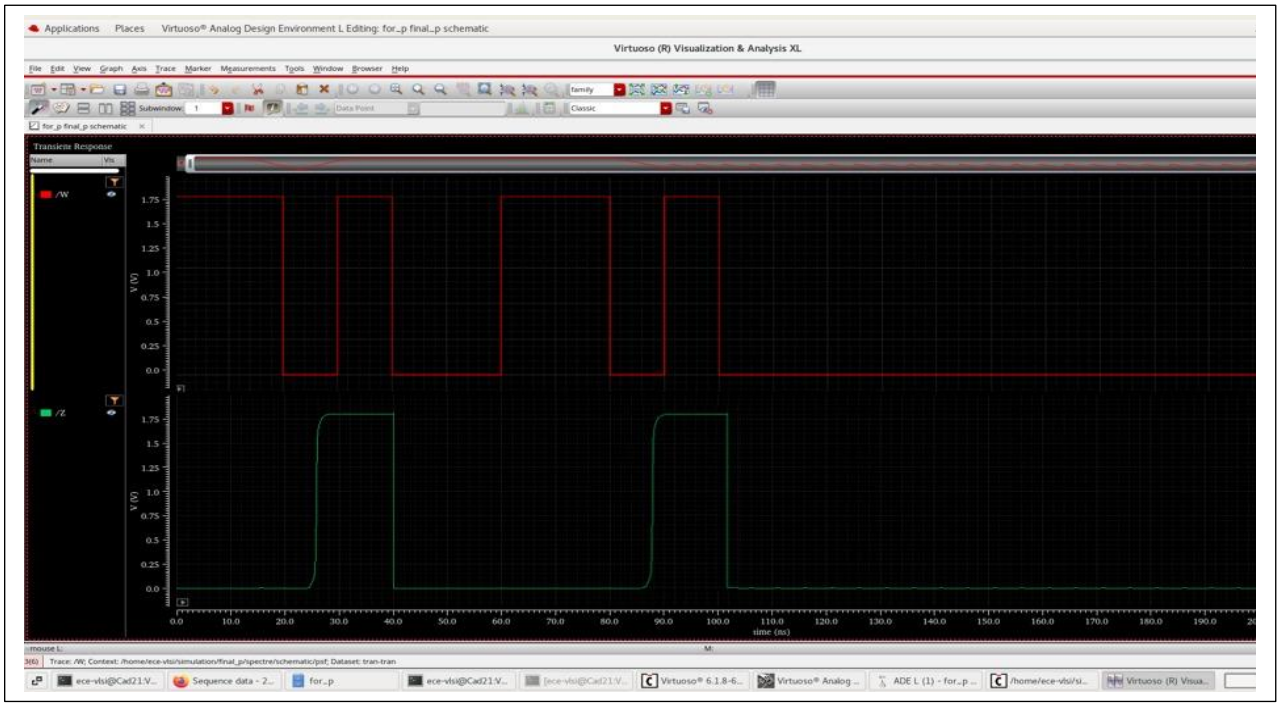
Calculated power dissipation

Power dissipation = 0.65μW

Schematic of 1101 detector:



CHAPTER 6
RESULTS AND DISCUSSION



The simulation of the 1101 sequence detector using a Mealy FSM was successfully performed in Cadence Virtuoso using ADE. The input signal W (red waveform) represents the serial binary stream fed into the system, while the output signal /Z (green waveform) corresponds to the detection of the "1101" sequence.
From the waveform plot:

- The input transitions through various binary values over time.
- At approximately 90 ns, the FSM detects the occurrence of the 1101 sequence (W = 1 → 1 → 0 → 1) and accordingly sets the output /Z high.
- The output /Z goes high only for one clock cycle, consistent with the behaviour of a Mealy machine where the output is dependent on both the current state and the input.

These results verify that the designed FSM accurately detects the 1101 sequence and responds with a high output signal at the correct time. The waveform also confirms proper synchronization and transient behaviour of the circuit, ensuring the correctness of the implementation.

CHAPTER 7
CONCLUSION

The CMOS-Designed 1101 Sequence Detector has effectively fulfilled the project goals of identifying the binary sequence"1101" from a sequential input stream of bits. The Mealy state machine-based design showed proper behavior via simulation, and the detector identified the sequence properly and produced the correct output. The CMOS logic gates employed for the implementation offered several benefits such as low power consumption, high noise immunity, and scalability, which made the circuit suitable for embedded systems and battery-powered devices.

The experimental findings verified the detector's functionality, and the design had low propagation delay, good power efficiency, and proper state transition. The optimization also lowered the transistor count in the circuit, improving its area efficiency. The design was effectively verified in Cadence Virtuoso, with thorough testing guaranteeing the accuracy and dependability of the sequence detection.

In summary, the project proved that it is possible to use CMOS technology in implementing a sequence detector and that the system is appropriate for real-time applications like pattern recognition, sequence tracking, and control systems. Improvements in the future can emphasize speed and investigate multifunctional detectors for more complex sequences.

CHAPTER 8
SUMMARY

The CMOS-based 1101 sequence detector was successfully designed and implemented using a Mealy state machine in Cadence Virtuoso. The design accurately detected the binary pattern “1101” and was verified through simulation using the Analog Design Environment (ADE). CMOS logic provided advantages such as low power dissipation, reduced area, and high reliability. The experimental results confirmed correct state transitions, efficient sequence detection, and minimal propagation delay. Overall, the project demonstrates the effectiveness of CMOS technology for real-time digital applications, with potential future improvements focusing on speed and multifunctional detection.

CHAPTER 9
REFERENCES

IEEE Xplore – *Design and Optimization of Low Power Sequence Detectors*, IEEE Transactions on VLSI Systems.

Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd Edition, Pearson Education, 2003.

Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th Edition, Pearson Education, 2010.

Plagiarism:

We hereby declare that the project report titled "Design and Simulation of 1101 Sequence Detector Using Mealy FSM in Cadence Virtuoso" is the result of our own efforts and has not been copied from any other source. Any content derived from external references has been appropriately cited and acknowledged in the report.
We fully understand the implications of plagiarism and confirm that this project adheres to the academic integrity guidelines established by K L (Deemed to be) University. No part of this report has been submitted elsewhere for the award of any other degree or diploma.

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