Handshake Protocol

Fall 2011

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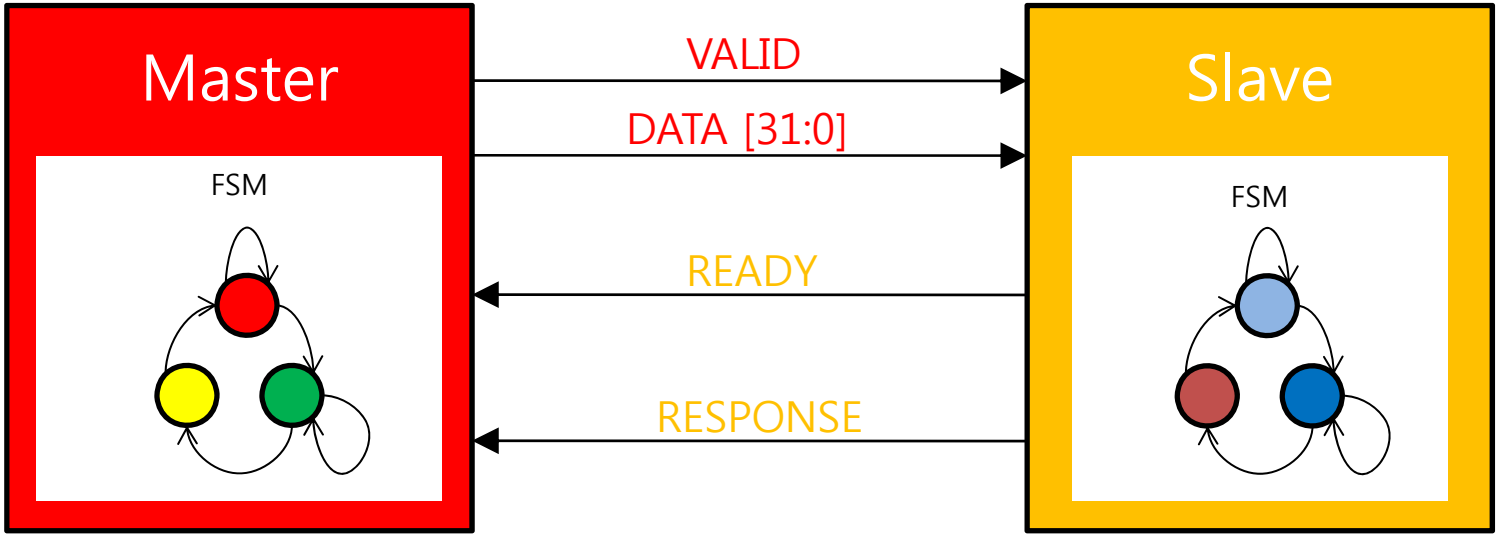
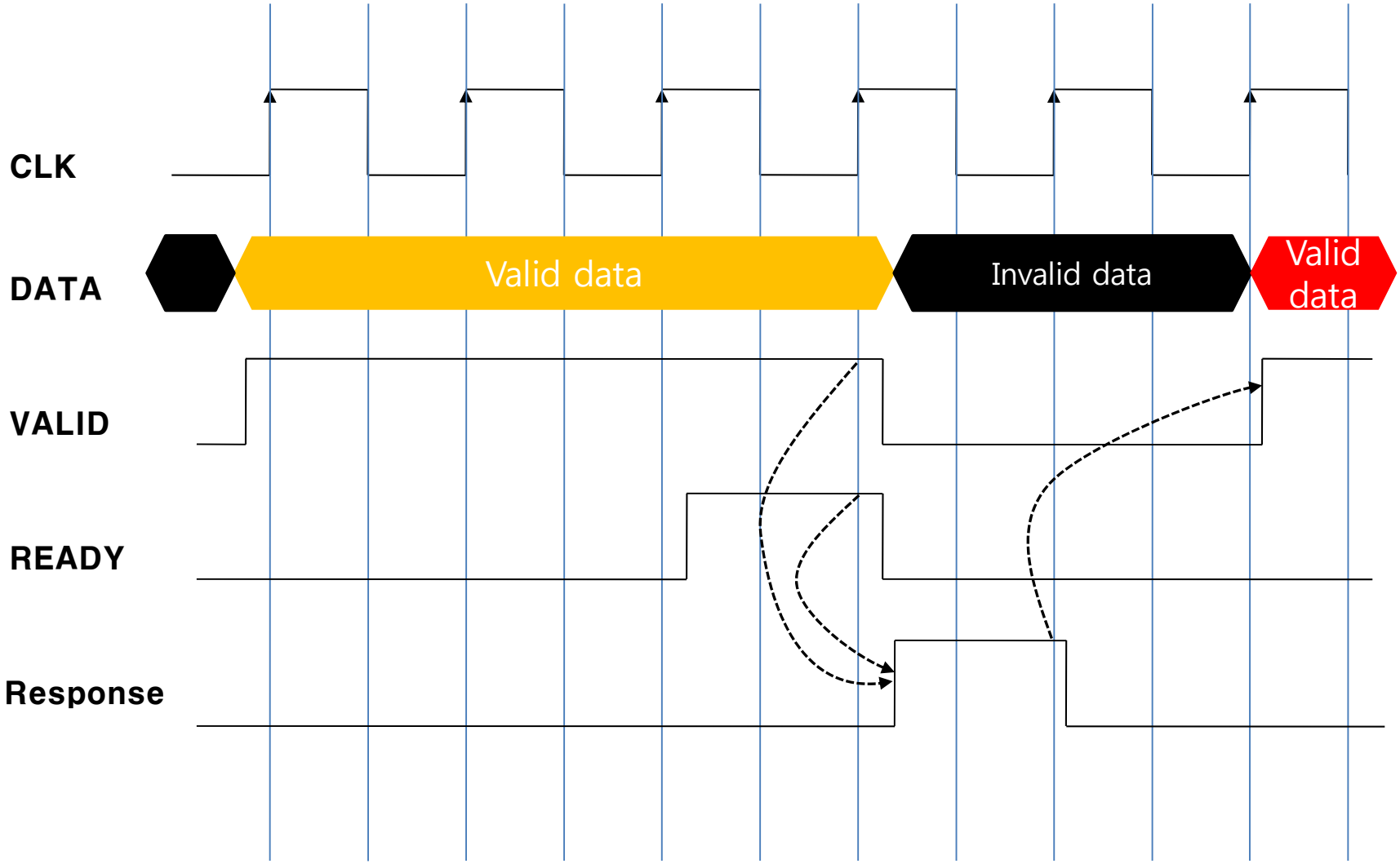
Handshake Process



- The master generates the **VALID signal to indicate when the data is available.**
- The slave generates the **READY signal to indicate that it accepts the data.**
- Transfer occurs only when both the **VALID and READY signals are HIGH.**
- **RESPONSE signal** indicates **one transaction is completed.**

Waveform


CLK
DATA
Valid data
Invalid data
Valid data
VALID
READY
Response

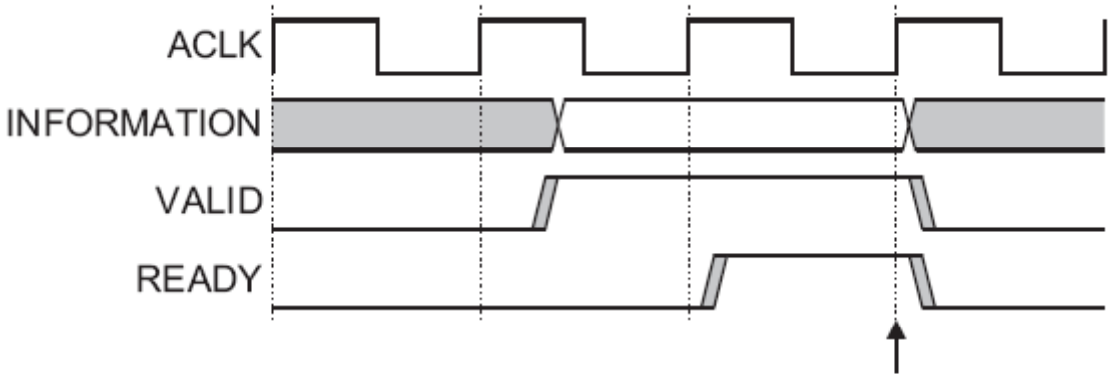


Figure 3-1 VALID before READY handshake

EXAMPLE
AMBA 3.0 AXI protocol

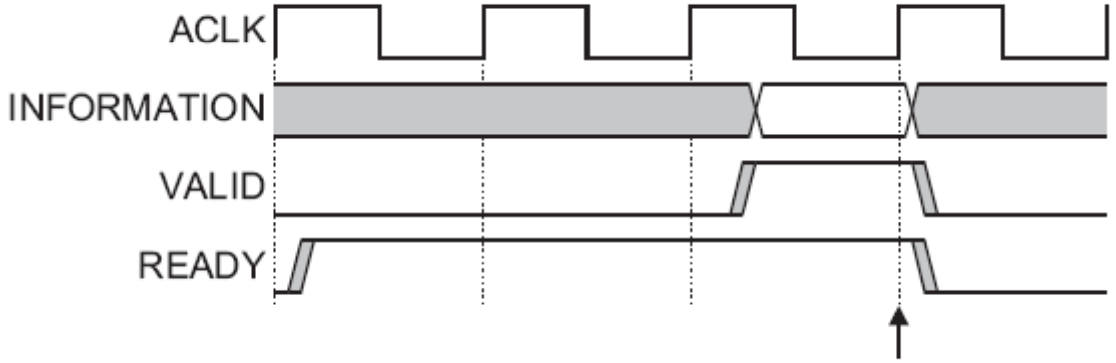


Figure 3-2 READY before VALID handshake

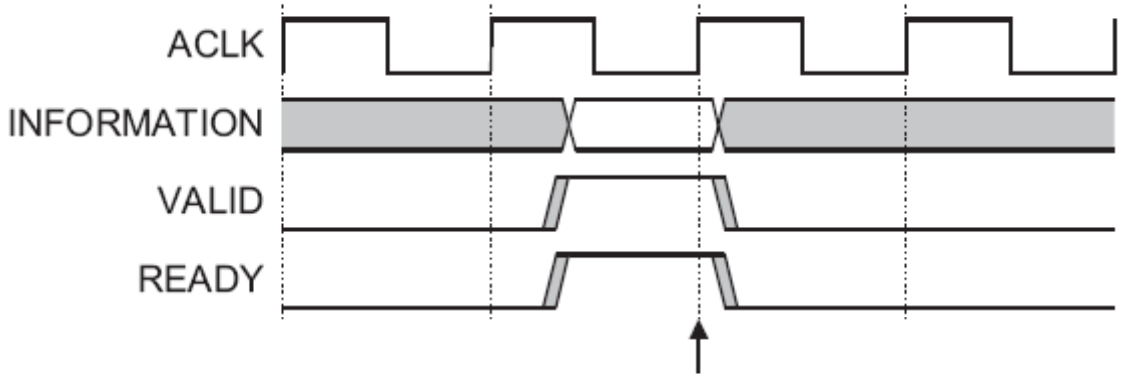
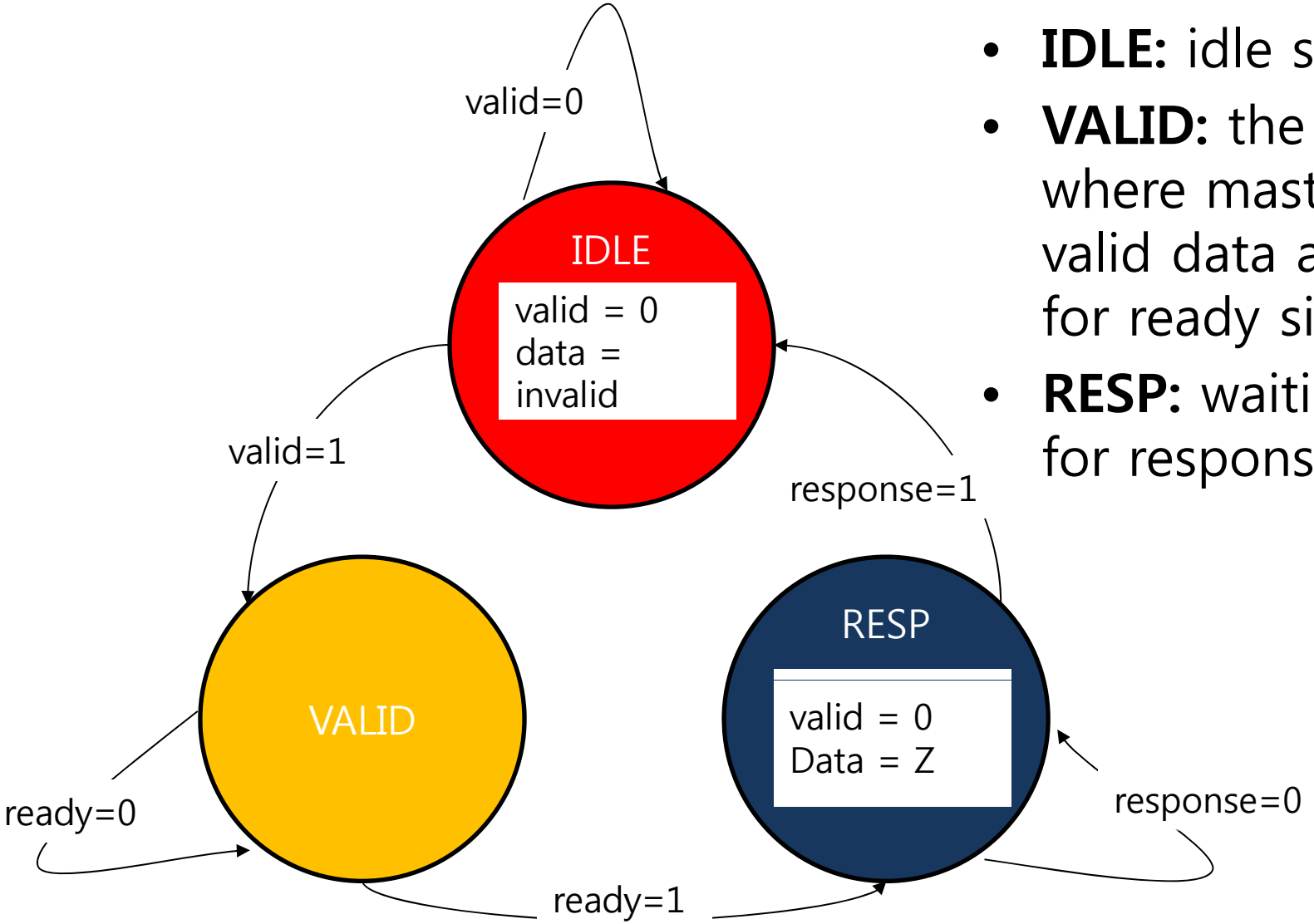


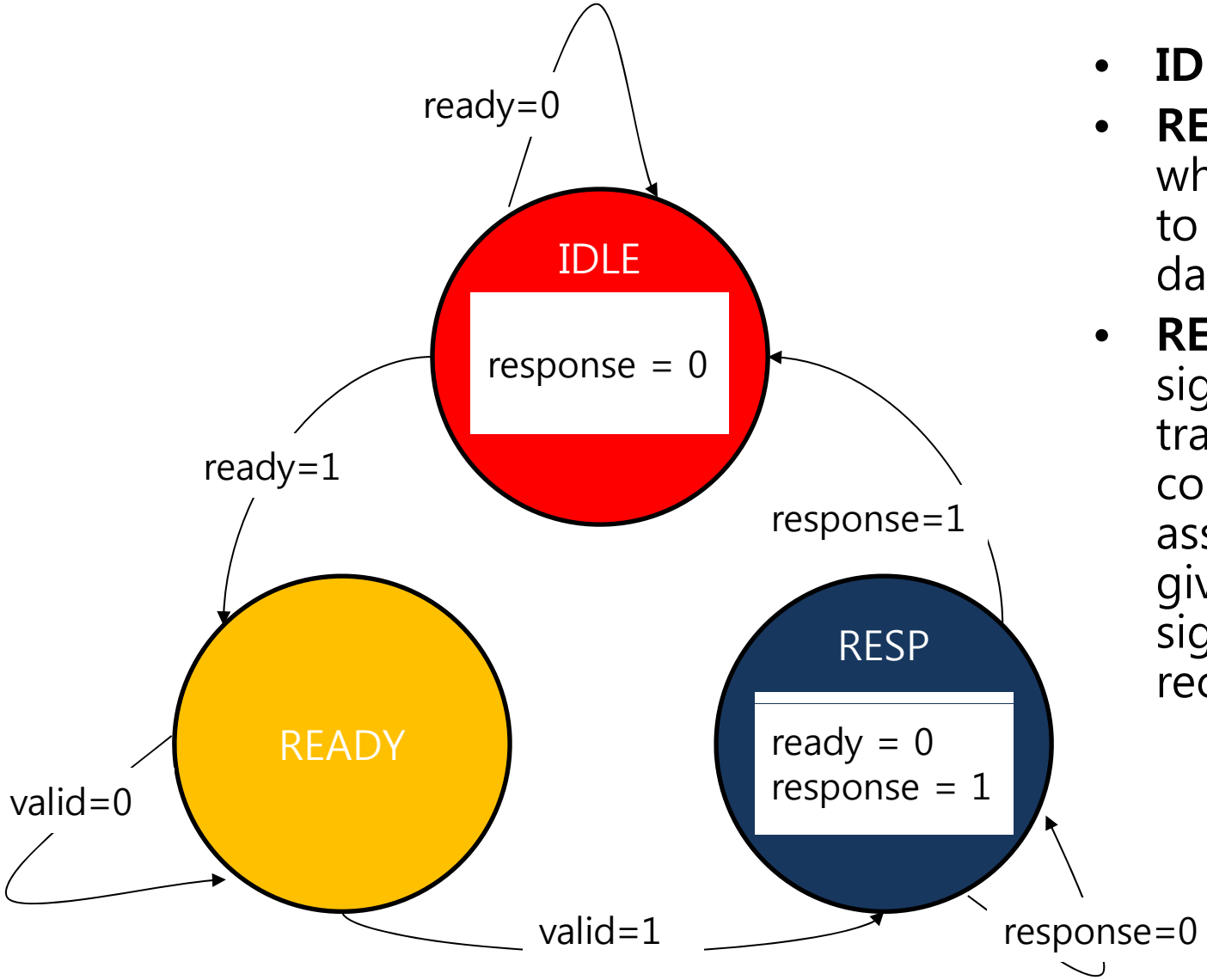
Figure 3-3 VALID with READY handshake

FSM of MASTER



- **IDLE:** idle state
- **VALID:** the state where master sends valid data and waits for ready signal
- **RESP:** waiting state for response signal

FSM of SLAVE



- **IDLE:** idle state
- **READY:** the state where slave is ready to get new valid data from master
- **RESP:** response signal indicates that transaction is completed. (We assume that slave gives OK response signal after receiving valid data.)

Simulation

1) Go down to your 'vlsi1' directory
2) Make your simulation directory

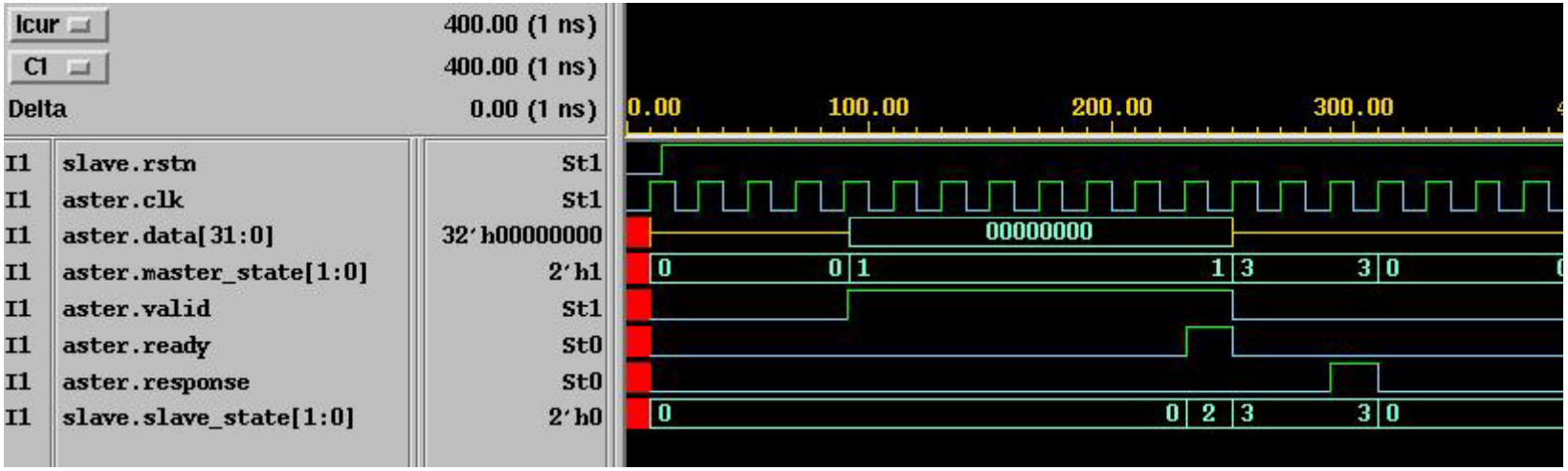
   user@sunapp1> mkdir handshake
3) Copy handshake.tar file to your simulation directory.

   (http://www.cerc.utexas.edu/~jypark/2011_spring_VLSI_I/LAB3_Website/handshake/handshake.tar)
1) Extract the file by using 'tar'

   user@sunapp1> tar –xvf handshake.tar
2) Modify 'USER DEFINED VALUE' section in the handshake.v as a test situation what you want to simulate.
3) user@sunapp1> source :synopsys
4) user@sunapp1> make comp
5) user@sunapp1> make run

- Due to the behavior simulation of master and slave models, this handshake.v file has some un-synthesizable codes (e.g. repeat statement, testbench, initial code).
- You can get a synthesizable code here (http://www.cerc.utexas.edu/~jypark/2011_spring_VLSI_I/LAB3_Website/handshake/syn/handshake.v)

Waveform



- USER DEFINED VALUE
  - SLAVE_READY 10
  - MASTER_VALID 3
  - SLAVE_RESPONSE 2
- MASTER
  - IDLE: 2'b00
  - VALID: 2'b01
  - RESP: 2'b11
- SLAVE
  - IDLE: 2'b00
  - READY: 2'b10
  - RESP: 2'b11