KARTHIK RAJ RAMACHANDRAPPA

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ACADEMIC QUALIFICATIONS

Master of Science in Computer Engineering, December 2018
Stony Brook University, New York, NY

Bachelor of Engineering, June 2014
University Visveswaraya College of Engineering, Bangalore, India

WORK EXPERIENCE

Graduate Research Assistant **March 2018**
Stony Brook University, NY
Research interests: Large scale image retrieval using Deep Local feature(DELF) descriptor for landmark retrieval under Prof. Yuefan Deng (Department of Applied Mathematics and Statistics).

Network Engineer
Ericsson, Bangalore, India March-2017
Responsibilities included integration and troubleshooting of nodes(DTN) in the radio network access.
Technologies used: Mo-Shell Scripting, Python. Received multiple client appreciations (PAT awards) for developing tools which accelerated the productivity of the team.

TECHNICAL EXPERTISE

Programming languages	Python, C, C++ (C++ 11, STL, Multithreading, Boost), Java, System Verilog
Computer Architecture	Multiprocessors, Memory Hierarchy and management, Vector processing and GPU architecture
Related concepts	Parallel, Distributed and Heterogeneous Computing Systems; Digital System Design, RTL logic design; Algorithms and data structures
Fields of interest	High Performance Scientific Computing, Machine learning, Computer Vision
OS and related platforms	Linux, GPFS & PBS
Tools and libraries	CUDA, OpenCL, MPI, OpenMP, OpenCV, Matlab, Modelsim, Git Version Control System Python: Numpy, Matplotlib, Anaconda, Tensorflow,

PROJECTS:

DESIGN AND MODELING OF SPU, A DUAL-ISSUE MULTIMEDIA PROCESSOR BASED ON SONY CELL ARCHITECTURE: (ONGOING)

- SONY CELL is a x64 multicore microprocessor which was based on Broadband Engine Architecture(BEA) and was commercially featured in Playstation 3. The Synergistic Processor Unit (SPU) is the integral part of CELL and is designed to accelerate the media and streaming workloads.
- This project aims to design and implement a SPU-lite multimedia processor in System Verilog. Behavioral design of fundamental modules such as Instruction Line Buffer(ILB), Instruction Decoder, dual pipelined ALU, Data forwarding using forwarding Macro and Local Store needs to be implemented.
- Handling structural hazards and data hazards (RAW, WAR and WAW) & implementing the dynamic branch prediction
- *Tools and tech: Computer Architecture, System Verilog, ModelSim, SPU – ISA, CELL – PowerPC architecture*

HARDWARE GENERATION TOOL FOR A CONFIGURABLE NEURAL NETWORKS:

- A hardware generation tool was implemented in C++ to generate the hardware description script (in System Verilog) for three layered neural networks. The design was capable of generating the hardware script for varying port selection and parallelism. The generated scripts were compiled and synthesized on Design Compiler library.
- *Tools and tech: Digital System Design, System Verilog, Neural networks, C++, ModelSim*

TEMPLATE BASED MURMUR3 HASHING (SUPPORTS BOTH X86_32 AND X86_128 ENCODING)

- MurmurHash3 was written by Austin Appleby and is placed in the public domain. The project implements a wraparound template (and consequently its class) which can take a tuple with unspecified datatypes, as its input and generate a 32 bit or a 128 bit hash key depending on the specified platform.
- *Tools and Technologies: C++ 11 , Linux*

LOCALIZATION AND TRACKING OF AN OBJECT IN A WIRELESS CAMERA NETWORK:

- The motion of an object within a wireless camera network is tracked and the direction of the motion is determined. Through communication between the nodes of WCN the overall traversal of the object is found.
- *Tools and tech: Digital Image processing, Raspberry Pi, Camera module V2 for Pi, Python, OpenCV, WSN*

LICOM: VISIBLE LIGHT COMMUNICATION

- Designed and Implemented a Wireless Visible Light Communication(VLC) system that transferred data bits over the visible light channel. The project was submitted at 'Analog design contest' conducted by Texas Instruments.
- *Tools and tech: Embedded Systems, Analog Circuit design, MSP-430, Code composer studio*