CMOS Schmitt Trigger using 28nm Technology

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***Abstract*—Majorly, most of the portable electronic devices use less power supply to maximize the battery lifetime. Each and every circuit will be tried to implement in such a way that it requires less power. Schmitt Triggers are widely used, and it filters out the noise in the signal and produce the noiseless signal. Here 28nm CMOS technology is used.**

I. Reference Circuit Details

The Schmitt Trigger circuit is widely used in analog and digital circuits to solve the noise problem. Besides that, this circuit is widely design in various styles in order to drive the load with fast switching, low power dissipation, and low supply voltage, especially for high capacitive load problems. Schmitt triggers are bistable networks that are widely used to enhance the immunity of a circuit to noise and disturbances. It is good as a noise rejecter. Schmitt trigger makes use of waves; therefore, it is widely used for converting analog signals into digital ones and to reshape sloppily, or distorted repulses. The output of a Schmitt trigger changes state when a positive-going input passes the upper trigger point (UTP) voltage and when negative-going input passes the lower trigger point (LTP)voltage. Thresholds are dependent on the ratio of NMOS and PMOS. This circuit will exhibit racing phenomena after the transition starts. CMOS Schmitt Trigger circuit here used is capable to operate in low voltages (0.8V- 1.5V), with less propagation delay. The proposed circuit is formed by a combination of two sub-circuits, P sub-circuit (which consists of P1 and P2) and N sub-circuit (which consists of N1 and N2).

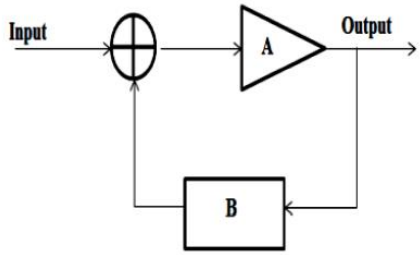
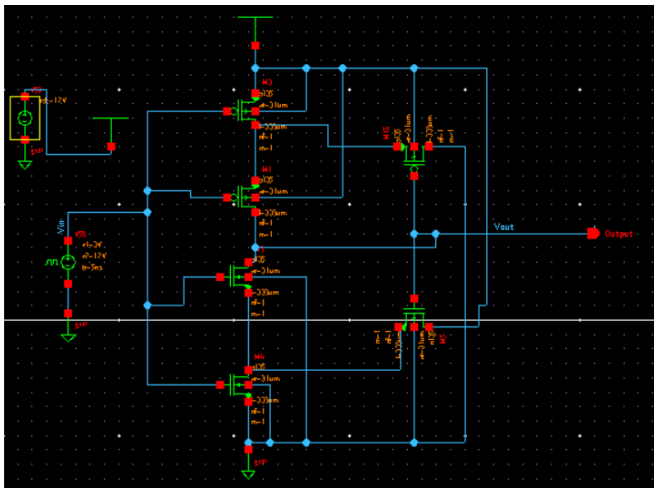


Fig.1: Block diagram of a Schmitt Trigger



There is no direct connection between the source voltage and ground as the P sub-circuit is connected to the path between the source voltage and output while the N sub-circuit is connected between the path of output and ground. Two PMOS (P1and P2) are formed by a parallel connection while two NMOS (N1 and N2) are formed by a series connection. This technique uses aspect ratios for PMOS and NMOS transistors. When the input is low, only the P sub-circuit will be considered and causes the output to be high (equal to VDD). During this condition, both P1 and P2 are on (because Vgs < |Vtp| source voltage and the gate voltage are equal). Therefore, the output voltage is pulled to VDD. When the input increases to Vdd, N1, and N2 are turned on.

II. Reference Circuit Design

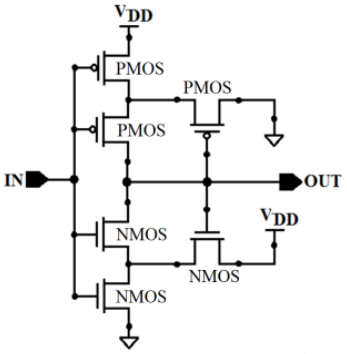
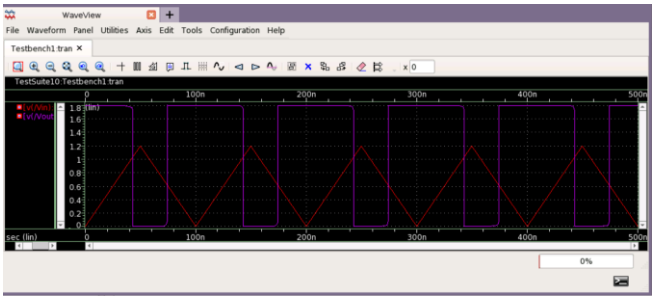


Figure 1: Typical Schmitt Trigger Circuit[3].

After Considering hysterisi and other parameters,W/L ratio for mosftes can be

Transistors	W/L Ratio
M1-PMOS	1.44/0.18
M2-PMOS	1.44/0.18
M3-NMOS	1.8/0.18
M4-NMOS	1.8/0.18
M5-PMOS	0.18/0.18
M6-NMOS	1.44/0.18

III. Reference Waveforms and Area Estimation



The proposed Schmitt trigger design can achieve very low power dissipation and efficient surface at 28nm foundry. This method can minimize power consumption and silicon surface area.

IV. Reference Papers/Journels

- Ghulam Ahmad Raza, Rajesh Mehra, "Area and Power Efficient Layout Design of CMOS Schmitt Trigger" International Journal of Scientific Research Engineering & Technology (IJSRET), ISSN: 2278–0882, pp. 57-60, March 2015.
- Design of Analog CMOS Integrated Circuits by Razavi
- M. Stoopman, S. Member, and S. Keyrouz, "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 622–634, 2014.
- http://ijiset.com/vol3/v3s8/IJISET_V3_I8_40.pdf
- Differential CMOS Schmitt trigger with tunable hysteresis | SpringerLink