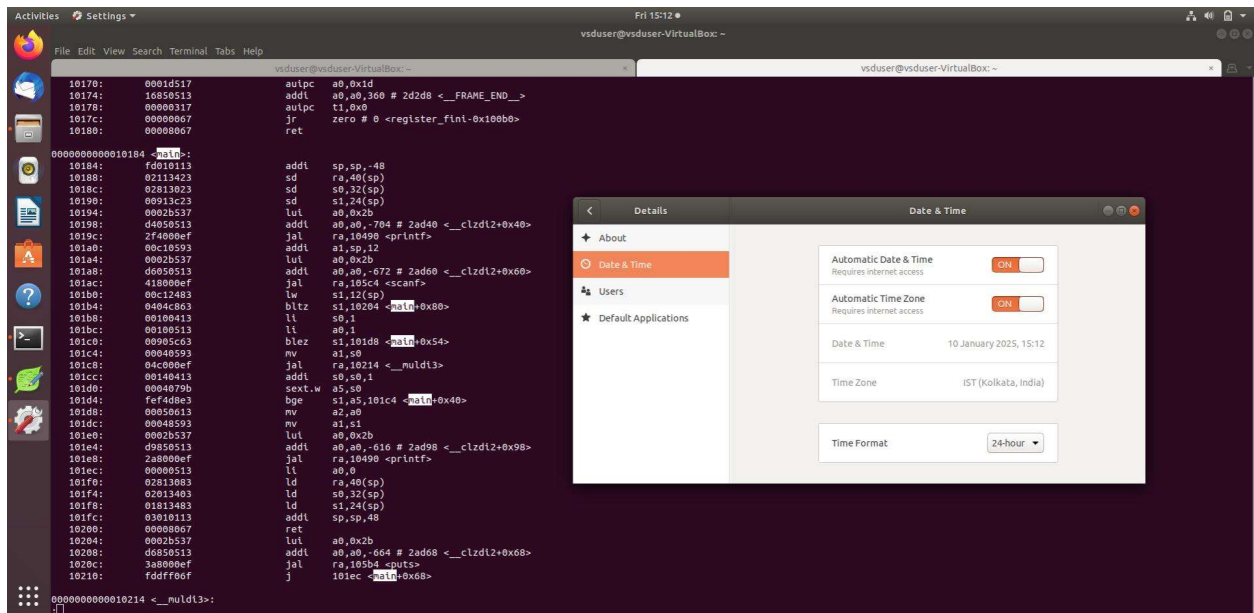


TASK-3



Using factorial of a number(RISC-V)

Instruction Types and Fields:-

The RISC-V instructions are categorized into types based on their field organization. Each type has specific fields like opcode, func3, func7, immediate values, and register numbers. The types include:

R-type: Register type

I-type: Immediate type

S-type: Store type

B-type: Branch type

U-type: Upper immediate type

J-type: Jump type

| 32-bit RISC-V Instruction Formats | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|------------|-----------|----|----|----|----|----|-----|-----|----|----|----|------|------------|----|----|----|--------|--------|----|----------|----------|---|--------|------|--------|---|---|---|---|---|---|
| Instruction Formats | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Register/register | funct7 | | | | | | | rs2 | | | | | rs1 | | | | | funct3 | | | rd | | | opcode | | | | | | | | |
| Immediate | imm[11:0] | | | | | | | | | | | | rs1 | | | | | funct3 | | | rd | | | opcode | | | | | | | | |
| Upper Immediate | imm[31:12] | | | | | | | | | | | | | | | | | | | | rd | | | opcode | | | | | | | | |
| Store | imm[11:5] | | | | | | | rs2 | | | | | rs1 | | | | | funct3 | | | imm[4:0] | | | opcode | | | | | | | | |
| Branch | [12] | imm[10:5] | | | | | | | rs2 | | | | | rs1 | | | | | funct3 | | | imm[4:1] | | | [11] | opcode | | | | | | |
| Jump | [20] | imm[10:1] | | | | | | | | | | | [11] | imm[19:12] | | | | | | | rd | | | opcode | | | | | | | | |
| <ul style="list-style-type: none">● opcode (7 bit): partially specifies which of the 6 types of <i>instruction formats</i>● funct7 + funct3 (10 bit): combined with opcode, these two fields describe what operation to perform● rs1 (5 bit): specifies register containing first operand● rs2 (5 bit): specifies second register operand● rd (5 bit): Destination register specifies register which will receive result of computation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Fig:- RISC-V instruction types

10184:-

Instruction: addi sp, sp, -48

Type: I-type

Opcode: 0010011 (7 bits)

Immediate: 1111111111000000 (12 bits)

Source Register (rs1): 00000 (x0, 5 bits)

Destination Register (rd): 00000 (x0, 5 bits)

Function (funct3): 000 (3 bits)

10188:

Instruction: sd ra, 40(sp)

Type: S-type

Opcode: 0100011 (7 bits)

Immediate: 0000000001010000 (12 bits)

Source Register (rs1): 10010 (x18, 5 bits)

Destination Register (rd): 10001 (x17, 5 bits)

Function (funct3): 010 (3 bits)

1018C:

Instruction: sd s0, 32(sp)

Type: S-type

Opcode: 0100011 (7 bits)

Immediate: 00000000001000000 (12 bits)

Source Register (rs1): 10000 (x16, 5 bits)

Destination Register (rd): 10001 (x17, 5 bits)

Function (funct3): 010 (3 bits)

10190:

Instruction: sd s1, 24(sp)

Type: S-type

Opcode: 0100011 (7 bits)

Immediate: 00000000000110000 (12 bits)

Source Register (rs1): 10001 (x17, 5 bits)

Destination Register (rd): 10001 (x17, 5 bits)

Function (funct3): 010 (3 bits)

10194:

Instruction: lui a0, 0x2b

Type: U-type

Opcode: 0110111 (7 bits)

Immediate: 0000000001011011 (20 bits)

Source Register (rs1): N/A

Destination Register (rd): 01000 (x10, 5 bits)

10198:

Instruction: addi a0, a0, -704

Type: I-type

Opcode: 0010011 (7 bits)

Immediate: 1111111111000000 (12 bits)

Source Register (rs1): 01000 (x10, 5 bits)

Destination Register (rd): 01000 (x10, 5 bits)

Function (funct3): 000 (3 bits)

1019C:

Instruction: jal ra, 10490 <printf>

Type: J-type

Opcode: 1101111 (7 bits)

Immediate: 00000000010001001111010000000000 (20 bits)

Source Register (rs1): N/A

Destination Register (rd): 10010 (x18, 5 bits)

101A0:

Instruction: addi a1, sp, 12

Type: I-type

Opcode: 0010011 (7 bits)

Immediate: 0000000000001100 (12 bits)

Source Register (rs1): 00000 (x0, 5 bits)

Destination Register (rd): 01001 (x11, 5 bits)

Function (funct3): 000 (3 bits)

101A4:

Instruction: lui a0, 0x2b

Type: U-type

Opcode: 0110111 (7 bits)

Immediate: 0000000001011011 (20 bits)

Source Register (rs1): N/A

Destination Register (rd): 01000 (x10, 5 bits)

101A8:

Instruction: addi a0, a0, -672

Type: I-type

Opcode: 0010011 (7 bits)

Immediate: 111111111001100 (12 bits)

Source Register (rs1): 01000 (x10, 5 bits)

Destination Register (rd): 01000 (x10, 5 bits)

Function (funct3): 000 (3 bits)

Machine Code: 111111111001100

101AC:

Machine Code: 418000ef

Instruction: jal ra, 105c4 <scanf>

Type: J-type

Function: Jump to the address 105c4 (which corresponds to the scanf function) and save the current program counter (PC) in register ra for later return.

101B0:

Machine Code: 00c12483

Instruction: lw s1, 12(sp)

Type: I-type

Function: Load the word-sized value from the memory location 12 bytes above the current stack pointer into register s1.

101B4:

Machine Code: 0404c863

Instruction: bltz s1, 10204 <main+0x80>

Type: B-type

Function: Branch to the address 10204 (which corresponds to the label main+0x80) if the value in register s1 is less than zero.

101B8:

Machine Code: 00100413

Instruction: li s0, 1

Type: I-type

Function: Load the immediate value 1 into register s0.

101BC:

Machine Code: 00100513

Instruction: li s1, 1

Type: I-type

Function: Load the immediate value 1 into register s1.

101C0:

Machine Code: 00905c63

Instruction: blez s1, 101D8 <main+0x54>

Type: B-type

Function: Branch to the address 101D8 (which corresponds to the label main+0x54) if the value in register s1 is less than or equal to zero.