

Task 3 4-Stage Pipeline Processor Design using Verilog

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Objective:

The objective of this task is to design and simulate a 4-stage pipelined processor using Verilog HDL. The processor demonstrates instruction pipelining through Instruction Fetch, Decode, Execute, and Write Back stages.

Tools Used:

Verilog HDL
EDA Playground
Icarus Verilog 12.0

Architecture:

The processor consists of instruction memory, register file, data memory, and pipeline registers. Supported instructions include ADD, SUB, LOAD, and NOP. Simulation and Results: Simulation was carried out using Icarus Verilog. The register values after execution matched expected results, confirming correct pipeline operation.

Conclusion:

The designed processor successfully demonstrates pipelined execution and meets requirements.