Karthikeya Sharma M

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Education

Georgia Institute of Technology **August 2023 – May 2025 (Expected)**
Master of Science in Electrical and Computer Engineering *GPA : 3.75/4*

SRM Institute of Science and Technology **July 2019 – May 2023**
Bachelor of Technology in Electronics and Communication Engineering *CGPA : 9.83/10*

Technical Skills

Software: C, CUDA C, C++, Python, MATLAB & LaTeX
Hardware Description Languages: Verilog, SystemVerilog & High Level Synthesis (HLS)
Libraries: OpenGL, OpenMP, OpenMPI, SFML, PyTorch
Tools: Xilinx Vivado & Vitis HLS, Modelsim, Icarus Verilog, Libero 12.5, Microsemi Softconsole, Code Composer Studio
Coursework: Advanced Computer Architecture, Hardware-Software Co-Design for ML Systems, Parallel Programming for FPGA, Advanced Programming Techniques, Machine Learning & Digital Systems Testing.

Research Experience

Research Collaborator **April 2024 – Present**
Synergy Lab @Georgia Tech *Atlanta, GA*

- **Project:** ***Unification of distributed ML modeling frameworks.***
  - Created **APEX**, an automated tool-chain for unifying open-source ML frameworks to study the impact of network configurations on collective algorithms through Design Space Exploration.
  - Translated auto-generated collective algorithm synthesizer outputs (TACOS) into MSCCLang IR, represented collectives as standardized Chakra Execution Traces (ETs), and bypassed the system layer of ASTRA-Sim, reducing engineering effort to create the IR for studying the impact of network parameters on collective algorithms in a distributed setup of GPUs.
  - Developed a configuration file to support the translation of heterogeneous topologies to study the impact of collectives on workloads and an interactive visualizer illustrating collective flows over GPU networks using Chakra ETs for agnostic collective patterns and network configurations.

M.S. Thesis Student **January 2024 – Present**
SHARC Lab @Georgia Tech *Atlanta, GA*

- **Thesis:** ***Correct-by-Design Hardware Accelerator Generation framework for Cryptographic Primitives.***
  - Contributed to building a fully automated and validated framework for generating correct-by-design FPGA accelerators from verified straight-line C implementations of cryptographic primitives.
  - Worked on implementing hardware-specific optimizations using HLS, including loop transformations and memory reorganization with equivalence-preserving loop transformations for enhanced hardware synthesis.
  - Main developer of ***Cryptonite***, a tool-chain that automates generation of correct-by-design hardware accelerators for cryptographic primitives.
  - Developed a DSE Engine and analytical model to estimate the Quality of Results (QoR) of the generated HLS C++ code, providing hardware generation statistics to the loop saturation framework.
  - Achieved scalable designs with up to 88.88% reduced resource usage and a 54.31% improvement in latency compared to naively synthesized straight-line C cryptographic primitives.

Student Assistant **September 2023 – Present**
iSenSys Lab @Georgia Tech *Atlanta, GA*

- ***Project Assisted: An Embedded Gas Sensing System for Industrial Hygiene and Clinical Applications***
  - Assisted in the development of a real-time frequency data acquisition system using Microsemi SmartFusion2 SoC to control a closed-loop system in a battery-powered embedded chemical sensing device to detect volatile organic compounds with sub-parts-per-million (ppm) sensitivity.
  - Interfaced ARM Cortex M3 MCU with SPI-controlled FPGA implementing reciprocal frequency counter to convert signal from the hammerhead resonator into frequency data enabling timed data collection and power-down phases reducing power consumption by 42%.

Research Intern **June 2022 – July 2022**
Indian Institute of Technology *Roorkee, IN*

- **Project:** ***Real-time EV Charging Station monitoring using CAN Communication.***
  - Implemented CAN protocol for real-time communication, reliability, and fault tolerance for EV charging stations.
  - Analyzed CAN module's test modes for network traffic and performance during network bus speed variations.

Projects

A GPU-Accelerated Framework for Hyperspectral Raman Imaging | *Python* **August 2024 - December 2024**

- Developed a GPU-Accelerated pipeline for Raman-Spectroscopic analysis.
- Created a streaming architecture to handle multi-dimensional spectral data and incorporated custom CUDA kernels to perform vectorized mathematical transformations.
- Automated metrics for SVD vector selection, organized post-processing analysis toolkit, and explored UNET phase error correction.

Context-aware Deepfake Detection | *Python* **February 2024 - May 2024**

- Created custom dataset from YouTube and Reddit including metadata such as video description and comment section to provide contextual information for deepfake detection.
- Developed a pre-processing pipeline to clean the metadata, removing unwanted text patterns, translating languages, and applying lemmatization for easier tokenization and feature extraction.
- Applied unsupervised algorithms such as Bertopic, GMM and K-Means clustering to classify contextual deepfake data.
- Implemented **H**ierarchical **M**ulti-modal **C**ontextual **A**ttention **N**etwork model, achieving a training accuracy of 91.7%.

DUT Verification Framework | *SystemVerilog* **December 2023 - January 2023**

- Implemented DUTs including Circular FIFO, SPI, UART, I2C & AXI3 memory.
- Developed a comprehensive verification plan for a hierarchical testbench architecture to ensure robust and reliable functionality of the DUTs.
- Achieved 100% functional coverage for all the DUTs.

Multithreaded 3D Scene Animation | *C++* **November 2023 - December 2023**

- Created an interactive 3D Halloween themed scene using OpenGL, incorporating multiple objects to create scene depth.
- Implemented multithreading using OpenMP to independently calculate the movement and rotation of each animated object, ensuring realistic collisions and interactions within the scene.

CMP Memory Simulator | *C++* **November 2023 - December 2023**

- Engineered a dual-core simulator with a multi-level memory hierarchy encompassing L1, L2 cache, and DRAM, implementing LRU and random eviction policies.
- Optimized L2 shared cache utilization through Static Way Partitioning (SWP) and Dynamic Way Partitioning (DWP).
- Achieved 0.85% performance enhancement after DWP implementation.

MIPS CPU simulator | *C++* **September 2023 - October 2023**

- Developed a 5-stage (8-pipe) MIPS CPU simulator accounting for data and control hazards.
- Supported OoO execution & GShare Branch Prediction, achieving 50% reduction in CPI and 10% reduction in latency.

FaultForge-Sim | *C++* **August 2023 - December 2023**

- Developed a C++ based logic simulator for parsing netlist files, enabling fault-free output evaluation.
- Applied PODEM test generation to produce input vectors for analyzing combinational circuits and verified their correctness using deductive fault simulation.
- Achieved 99.71% fault coverage on average for all the netlists used in testing.

Systolic Array Accelerator | *SystemVerilog* **June 2023 - August 2023**

- Developed a 4x4 Systolic Array Accelerator, with MAC modules supporting pipelined FP32 addition and multiplication.
- Extended the architecture to support CSR and CSC sparse Matrix representations & weight stationary dataflow.

Edge Processing for 3D object Reconstruction | *Python* **July 2022 - November 2022**

- Constructed a cost-effective solution to perform 3D reconstruction of objects in underwater environments by taking stereo images from different perspectives with known deviations in distance and angle.
- Optimized an image processing pipeline using multi-threading to extract features from stereo images for accurate depth estimation and used Epipolar geometry for stitching the 2D images of the object for projection into 3D space.

Teaching Experience

Graduate Teaching Assistant (CS 6340 : Software Analysis and Testing) **August 2024 – December 2024**
Dept. of Computer Science, Georgia Institute of Technology *Atlanta, GA*

- Conducted weekly office hours to support students, providing tutoring and guidance on the final project.
- Led a class session introducing the Static Analysis framework (SVF Framework) and demonstrated a short tutorial on the same, along with tips on debugging the class project with this tool.