KARTIK KULGOD

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FIELD OF INTEREST

I am interested in mathematical aspects of communication and signal processing.

EDUCATION

Birla Institute of Technology and Science, Pilani *August 2015 - Present*
B.E. (Hons.) Electrical & Electronics Engineering
Overall GPA: 8.732/10
Ranked 9th in Dept.

City International School, Pune *March 2015*
High School
Overall Percentage: 96.8%
School Topper

PROJECTS

Long Term Evolution (LTE) & 5G *July 2018 - December 2018*
Student Trainee ***Samsung Research & Development Institute, Bengaluru***

· Designed a simulator in C, based on the Cavium CNF75XX octeon processor for the following features:

- Uplink 256QAM (introduced in 3GPP Rel. 14)
- Frequency Domain Equalization

· Developed tools for analysing log dumps generated by eNB using Python scripts, potentially *saving hundreds of man-hours.*

Satellite Communication *May 2018 - Present*
Telemetry ***Team Pixxel***

· Established communication between transmitter and receiver at 435MHz center frequency and 25 khz bandwidth with MSK modulation.
· Currently investigating S-band communication and inter-satellite communication.

Brain Signal Processing *January 2018 - May 2018*
Prof. Veeky Baths ***BITS Cognitive Neuroscience Lab***

· Worked on left and right hand *motor imagery* (mu-band: 8- 12 Hz) based *brain computer interface*
· Calculated Event Related Desynchronisation (ERD) using Bandpower method and designed *notch*, *bandpass FIR* and *Common Spatial Filters* using *MATLAB* to generate feature vectors
· Tested the scripts on datasets gathered from experiments conducted at the lab, and dataset 2A from BCI Competition IV. Classified the feature vectors using 3 algorithms (LDA,SVM & Logistics Regression) implemented in Python
· Achieved an accuracy of 68% and Cross Validation score of 0.76. [Project Page]

Winter Signal Processing Projects *December 2017 - January 2018*

· ***Estimation of FIR Filter Response***:Estimated the response of a FIR filter using the *method of moments* for a *white* signal, coupled with the *Levinson algorithm* for calculating the inverse of the *autocorrelation toeplitz* matrix. [Project Page]
· ***Spatial Sound Generation:*** Generated spatial sound from a single channel sound using convolutional techniques and Room Impulse Response. [Project Page]

DTMF Decoder *October 2017*

- Developed a software that can decode Dual Tone Multi Frequency Tones.
- Implemented the software using two methods, the *Fast Fourier Transform (FFT)*, and an efficient, less calculation intensive, *Goertzel's algorithm* by developing seven filters for the seven frequencies involved.
- The software can decode signals with mark & space time of 20 ms or 25 digits per second. [Project Page]

Hyperloop India *August 2016 - November 2017*
Electrical & Electronics Engineer ***Goa - Bengaluru - Los Angeles***

- We were the *first* team to have *represented India* and the only two finalists from Asia, who had been selected to race our pod at the SpaceX Hyperloop Pod Competition. The pod was built in a *record time of 3 months*. The pod was later presented to *Indian Prime Minister, Mr. Narendra Modi & advisor to the President of the USA, Ms. Ivanka Trump* at Global Entrepreneurship Summit 2017. We were also the winner of the Hyperloop One Global Challenge.

My various roles as an Electrical and Electronics Engineer were:

- Selecover 30 sensors for measuring attitude (yaw, pitch, roll), kinematic variables $(x, \dot{x}, \ddot{x})$ in X,Y & Z coordinates, temperature, pressure, battery current, voltage and more.
- Wrote drivers for the 30+ sensors and *all* actuators for a Teensy 3.6 MCU (ARM Cortex M4) running FreeRTOS, using *communication protocols* such as $I^2C, SPI, Serial$ and CAN.
- Designed the schematics of the PCBs of the 4 major nodes on *Eagle CAD*. Tested the PCBs and all Electrical and Electronic Components at *DRDO's* vacuum chamber.
- *Assisted* with *industry standard* wiring and connector practices. Performed an exhaustive Failure Mode and Effects Analysis (FMEA) and implemented adequate redundancy. [Project Page]

All Pass Filter Design using Current Feedback Op-Amps *August 2017 - December 2017*
Prof. Dipankar Pal

- Designed a first order all pass filter using a Current Feedback Operational Amplifier.
- Realised the circuit using *45 nm CMOS* technology.
- Simulated the design on *Cadence Virtuoso* from a frequency range of 1 µHz to 1 THz.
- Achieved a gain of 0 dB with variation of 0.023% over the entire frequency range. [Project Page]

Internet of Things *May 2017 - July 2017*
Intern ***Ericsson R&D, Bengaluru***

- Designed a simulacrum of a Smart Irrigation system that can control the movement of irrigation gates depending on the water level in the field.
- Created a web server that displays the water level in the field, while also allowing the user manual control of the gates.

hFE tester *March 2017 - May 2017*
EEE F241, Microprocessors and Interfacing

- Designed and programmed a system to calculate the beta value(h_{FE}) of a transistor, using intel 8086, 2x LED displays & ADC0804 on Proteus using assembly language. [Project Page]

ABU Robocon *March 2016 - March 2017*

- The objective was to deploy a robot that can throw polyurethane frisbees accurately at specified points. My various roles as a member of the team were:
- Wrote the software for the brushless DC motor based throw system and transmitting data among 3 Atmel 8-bit AVR microcontrollers using I2C Protocol.
- Developed the 4 wheel omni-drive base. [Project Page]

TECHNICAL STRENGTHS

Experienced MATLAB, C, Arduino, HTML & CSS, Assembly Language (x86), Orcad PSpice
Familiar Eagle CAD, Proteus, Cadence Virtuso, Python, Simulink, C++, Verilog, LaTeX
Comfortable with Linux and Windows OS

RELEVANT COURSEWORK

Major courses: Signals & Systems, Communication Systems, Digital Signal Processing, Data Communication and Networking, Mobile Telecom Networks, Microprocessor and Interfacing, Digital Design, Analog & Digital VLSI Design.

Math: Statistical Inference & Application, Calculus, Probability & Statistics, Linear Algebra & Complex Analysis, Ordinary & Partial Differential Equations, Optimization.

SCHOLASTIC ACHIEVEMENTS

- **KVPY** *(Kishore Vaigyanik Protsahan Yojana)* 2015 Scholar *selected among 200,000 students.*
- **All India Rank 1091** among 1.5 million students in *JEE (Mains)* 2015
- **School topper** in National Science Olympiad & International Mathematics Olympiad for several years

MENTORING & MANAGING EXPERIENCE

- **Teaching Assistant** for the course **Microprocessors & Interfacing** for the *Spring semester* of the academic year 2017-2018
- **Panel Coordinator** for *Electrify* during Quark (the Technical Festival), which consists of events related to Electrical Engineering concepts. Managed a team of *13 people*, and *introduced a new headliner event, The IoT hackathon.*
- Member of **IEEE** Student body
- **Mentored 30+ students** about communication principles using the Arduino and Raspberry Pi development boards, as a part of Quark Summer Technical Project.
- **Mentored 50+ students** as a part of an Introduction to Robotics, and designed the capstone project: *Micro Servo Robotic Arm*