6KS04 - Computer Architecture (10335)

* Required

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Instructions:
1. All 40 MCQ questions are compulsory.
2. Every question carries two (02) marks.
3. Exam time : 60 Minutes (1 Hr.).
4. No negative marking.

*

2 points

A

- [x] B
- [ ] C
- [ ] D

*

2 points

2) ARM processors where basically designed for ------

A) Main frame systems B) Distributed systems

C) Mobile systems D) Super computers

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

3) The address space in ARM is ------

A) 2^{24} B) 2^{64}

C) 2^{16} D) 2^{32}

- A
- B
- C
- D

*

2 points

4) The bit present in the op code, indicating which of the operands is the source is called as ----

A) SRC bit B) Indirection bit

C) Direction bit D) FRM bit

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

5) The CPU of a Computer takes instruction from the memory and executes them. This process is called

A) Load cycle
B) Time sequence
C) Fetch-execute cycle
D) None of these

- ○ A
- ○ B
- ◉ C
- ○ D

*

2 points

6) Run time mapping from virtual to physical address is done by ------

A) Memory Management Unit B) CPU

C) PCI D) None of the above

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

7) Operating System maintains the page table for --------

A) Each data element

B) Each instruction

C) Each address

D) Each process

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

8) Serial Peripheral Interface bus allows -------

A) Half/full

B) Synchronous

C) Serial communication with external devices

D) All of the above

- ○ A
- ○ B
- ○ C
- ◉ D

*

2 points

9) A process is thrashing if -------

A) it is spending more time paging management than executing

B) it is spending less time paging than executing

C) page fault occurs very infrequently

D) swapping could not take place

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

10) The average time required to reach a storage location in memory and obtain its contents is called ------.

A) Latency time
B) Access time
C) Turnaround time
D) Response time

- [ ] A
- [x] B
- [ ] C
- [ ] D

*

2 points

11) Which of the following register in ARM7 is used to point to the location of currently executing instruction in a program?

A) R1 B) R5

C) R15 D) R8

- ○ A
- ○ B
- ◉ C
- ○ D

*

2 points

12) Evaluate the following statements

i) R13 is traditionally used as the stack pointer and stores the head of the stack in the current processor mode.

ii) R14 is the link register where the core puts the return address on executing a subroutine.

iii) R15 is the program counter and contains the address of the next instruction to be fetched

A) All the options are true
B) i and ii are true
C) ii and iii are true
D) i and iii are true

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

13) If an instruction takes 3 cycles for execution, then how many cycles are needed for executing 4 instructions of the same type in a sequence using a 3-stage pipeline? Assume that there are no interrupts or exceptions while executing them.

A) 12 cycles B) 6 cycles

C) 9 cycles D) 4 cycles

- ○ A
- ◉ B
- ○ C
- ○ D

*

2 points

14) Which of the following processor belong to Reduced Instruction Set Computers (RISC) family?

A) ARM
B) AVR
C) MIPS
D) All of the above

- ○ A
- ○ B
- ○ C
- ◉ D

*

2 points

15) The fetch and execution cycles are interleaved with the help of ------

A) Modification in processor architecture B) Clock

C) Special unit D) Control unit

- ○ A
- ◉ B
- ○ C
- ○ D

*

2 points

16) Each stage in pipelining should be completed within ------ cycle.

A) 1 B) 2

C) 3 D) 4

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

17) To increase the speed of memory access in pipelining, we make use of ------

A) Special memory locations
B) Special purpose registers
C) Cache
D) Buffers

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

18) The situation wherein the data of operands are not available is called ------

A) Data hazard
B) Stock
C) Deadlock
D) Structural hazard

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

19) Which of the following is not a visible register?

A) General Purpose Registers B) Address Register

C) Status Register D) MAR

- ○ A
- ○ B
- ○ C
- ◉ D

*

2 points

20) Which of the following is a data transfer instruction?

A) STA 16-bit address

B) ADD A, B

C) MUL C, D

D) RET

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

21) Pipelining strategy is called implement.

A) instruction execution B) instruction prefetch

C) instruction decoding D) instruction manipulation

- A
- B
- C
- D

*

2 points

22) The computer architecture aimed at reducing the time of execution of instructions is -----

A) CISC B) RISC

C) ISA D) ANNA

- ○ A
- ◉ B
- ○ C
- ○ D

*

2 points

23) Out of the following which is not a CISC machine.

A) IBM 370/168 B) VAX 11/780

C) Intel 80486 D) Motorola A567

- ○ A
- ○ B
- ○ C
- ◉ D

*

2 points

24) What are the significant designing issues/factors taken into consideration for RISC Processors?

A) Simplicity in instruction set
B) Pipeline Instruction Optimization
C) Register Usage Optimization
D) All of the above

- ○ A
- ○ B
- ○ C
- ◉ D

*

2 points

25) Which register of current procedure resemble physically similar to the parameter register of called procedure during register to register operation in an overlapping window of RISC Processors?

A) Local Register
B) Temporary Register
C) Parameter Register
D) All of the above

- [ ] A
- [x] B
- [ ] C
- [ ] D

*

2 points

26) The iconic feature of the RISC machine among the following are

A) Reduced number of addressing modes B) Increased memory size

C) Having a branch delay slot D) All of the above

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

27) The stalling of the processor due to the unavailability of the instructions is called as -------

A) Control hazard
B) Structure hazard
C) Input hazard
D) None of the mentioned

- (●) A
- ( ) B
- ( ) C
- ( ) D

*

2 points

28) The concept of pipelining is most effective in improving performance if the tasks being performed in different stages:

A) require different amount of time

B) require about the same amount of time

C) require different amount of time with time difference between any two tasks being same

D) require different amount with time difference between any two tasks being different

- ○ A
- ○ B
- ◉ C
- ○ D

*

2 points

29) The average number of steps taken to execute the set of instructions can be made to be less than one by following --------.

A) ISA
B) Pipe-lining
C) Super-scaling
D) Sequential

- ○ A
- ○ B
- ◉ C
- ○ D

*

2 points

30) Both the CISC and RISC architectures have been developed to reduce the -------

A) Cost
B) Time delay
C) Semantic gap
D) All of the mentioned

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

31) What is the control unit's function in the CPU?

A) to transfer data to primary storage B) to store program instruction

C) to perform logic operations D) to decode program instruction

- ○ A
- ○ B
- ○ C
- ◉ D

*

2 points

32) Memory access in RISC architecture is limited to instructions.

A) CALL and RET B) PUSH and POP

C) STA and LDA D) MOV and JMP

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

33) If the control signals are generated by combinational logic, then they are generated by a type of ------- controlled unit.

A) Micro programmed
B) Software
C) Logic
D) Hardwired

- ○ A
- ○ B
- ○ C
- ◉ D

*

2 points

34) Broader concept offers Cloud computing to select which of the following.

A) Parallel computing
B) Centralized computing
C) Utility computing
D) Decentralized computing

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

35) Virtualization that creates one single address space architecture that of, is called

A) Loosely coupled
B) Peer-to-Peer
C) Space-based
D) Tightly coupled

- [ ] A
- [ ] B
- [x] C
- [ ] D

*

2 points

36) Dynamic networks of networks, is a dynamic connection that grows is called

A) Multithreading
B) Cyber cycle
C) Internet of things
D) Cyber-physical system

- [ ] A
- [x] B
- [ ] C
- [ ] D

*

2 points

37) What kind of a flag is the sign flag?

A) General Purpose B) Status

C) Address D) Instruction

- [ ] A
- [x] B
- [ ] C
- [ ] D

*

2 points

38) The iconic feature of the RISC machine among the following are

A) Reduced number of addressing modes B) Increased memory size

C) Having a branch delay slot D) All of the above

- ○ A
- ○ B
- ◉ C
- ○ D

*

2 points

39) The length of a register is called -------

A) word limit
B) word size
C) register limit
D) register size

- [ ] A
- [x] B
- [ ] C
- [ ] D

*

2 points

40) The time lost due to the branch instruction is often referred to as ------

A) Latency
B) Delay
C) Branch penalty
D) None of the mentioned

- [ ] A
- [ ] B
- [x] C
- [ ] D

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