CHAPTER-3 I

INTERFACING: Memory and I/O Mapped I/O

1. I/O Interfacing Techniques

- Microprocessor, isolates memory and IO system
- It provides instruction for addressing memory and IO system. This is done by $M/\overline{IO}$ signal in 8085.

  $M/\overline{IO} = 1$; microprocessor communicating with memory system.

  $M/\overline{IO} = 0$; microprocessor communicating with IO system.
- In IO addressing mode 8085 has capability of 8 bit IO address, through which it can address 255 IO ports.
- Microprocessor also provides facility to, treat I/O devices as memory location. In this case, one can map IO devices in memory map.
- Thus, due to above two methods of interfacing IO devices, we have two techniques of IO mapping i.e

  1. I/o mapped I/O 2. Memory mapped I/O

I/O Mapped I/O [I/O PORT ADDRESSING]

- In this case the I/o device is treated as I/o device only
- Each I/o device uses eight bits of address line and control signals $\overline{IOR}$ (Input output read) and $\overline{IOW}$ (Input output Write)
- The address bus of 8085 microprocessor is of 16 bits, but for I/O devices only 8 bits address is used. So to implement this the 8 bit address is transferred on both address groups ie A_0 to A_7 and A_8 to A_{15}.
- The contents available are same, so one can use any one group ie A_{15} to A_7 or A_7 to A_0 or combination

of two groups.

- Let us consider an example if address of I/O device is 50H.

The contents transferred on A_0 to A_{15} will be as follow:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7
0	1	0	1	0	0	0	0	0

50

A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	1	0	0	0	0

50

So we can use 50H address given by A_7 to A_0 or A_{15} to A_7 or we can use A_0 or A_8, A_1 or A_9 and so on A_7 or A_{15}.

This will be represented as follow:

$$\underbrace{A_{7|15} \quad A_{6/14} \quad A_{5|13} \quad A_{3|12} \quad A_{2|10} \quad A_{1|9} \quad A_{0|8}}$$

- The above representation specifies that line contents are same. So to address an I/O device we can use A_0 or A_8.
- There are two special instructions available for data transfer b/w an I/O device and microprocessor.

In I/O mapped I/O:

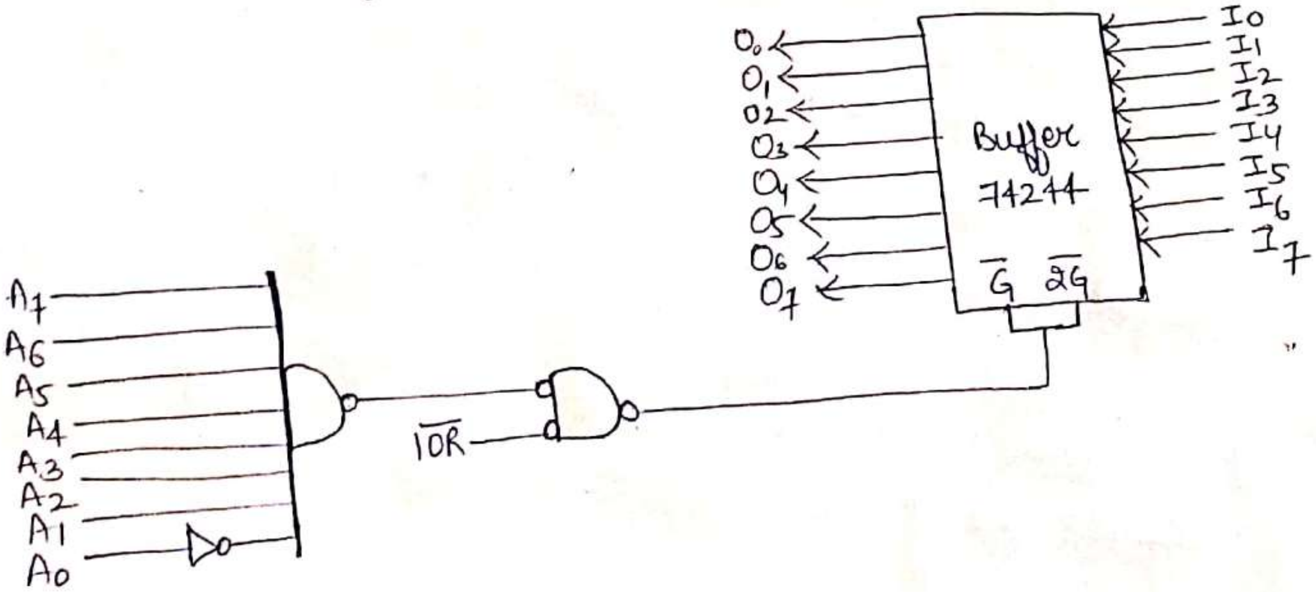
(1) IN address

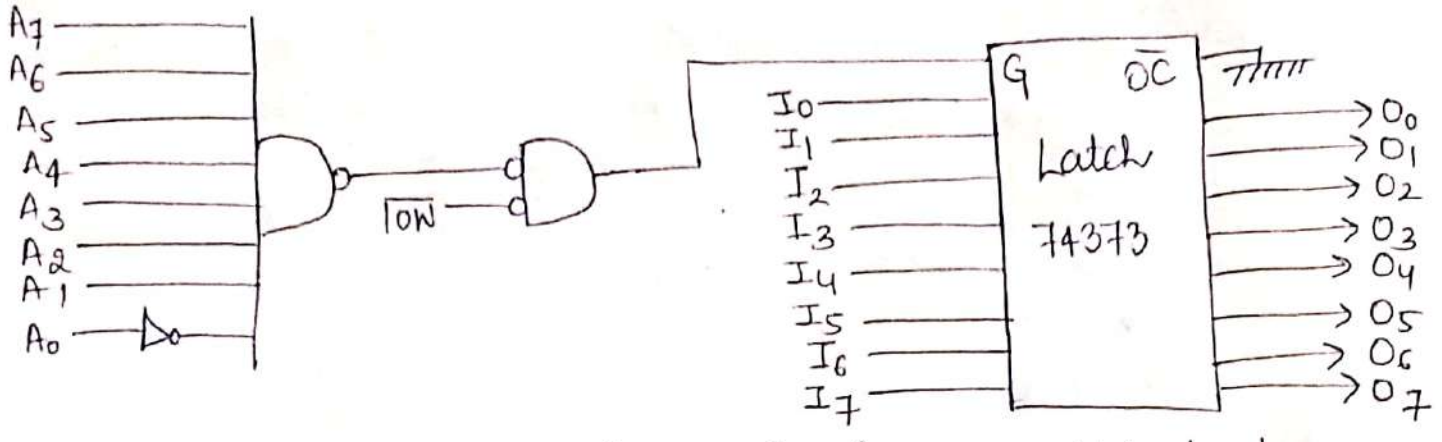
(2) OUT address.

INPUT OUTPUT INTERFACING IN I/O MAPPED I/O

- The address for I/O devices is of 8 bits. So $2^8 = 256$ I/O devices can be connected to system

- For input device we require $\overline{IOR}$ signal and for output device $\overline{IOW}$ signal. As with $\overline{IOR}$ and $\overline{IOW}$ one can differentiate between input and output devices, so even if both the devices have same address there will be no problem.
- The number of devices which can be connected are 256 input and 256 output devices.
- Now to interface these devices to 8085, the control pins of I/O devices should be synchronised with 8085.
- The input device control pins $\overline{1G}$ and $\overline{2G}$ should be connected to combination of address and control signal $\overline{IOR}$. When $\overline{1G}$ and $\overline{2G}$ are active the buffer will get enabled and transfer data on to the data bus.
- Similarly for output device we connect $\overline{OC}$ to ground and use enable G input to control the latch. So the G input is connected to combination of address and control signal $\overline{IOW}$.
- The interfacing of input and output device will be a shown





Input Output interfacing in IO mapped I/O

- The interfacing diagram is divided in two separate parts: 1) for input device i.e buffer 2) for output device i.e latch.
- For both the interfacing diagrams combination of address lines is done by 8 input NAND gate. The address lines used are A_0 to A_7 (or we can use A_8 to A_{15})
- When the combination of input get satisfied the output will be low and for all other combinations it will be high. This output is then combined with control signal $\overline{IOR}$ or $\overline{IOW}$ to generate signals to enable buffer and latch.
- The output of buffer is connected to data bus and input of latch is connected to data bus.
- The address of input and output device is calculated from combination of address lines as follows:

Input device = 1111 1111 = FFH
Output device = 1111 1110 = FEH

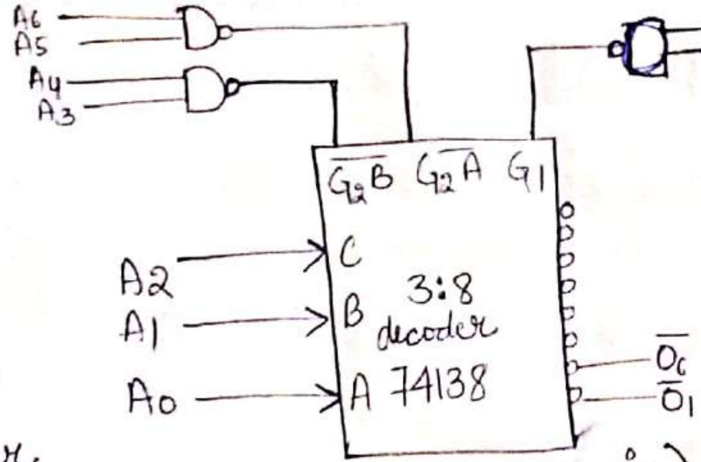
- Instead of logic gates a decoder logic can be used to do the same function. When the decoder logic is used from its many outputs one of the output is used to enable one device.
- The general interfacing of I/O device is shown:

The two cases of address selection logic:

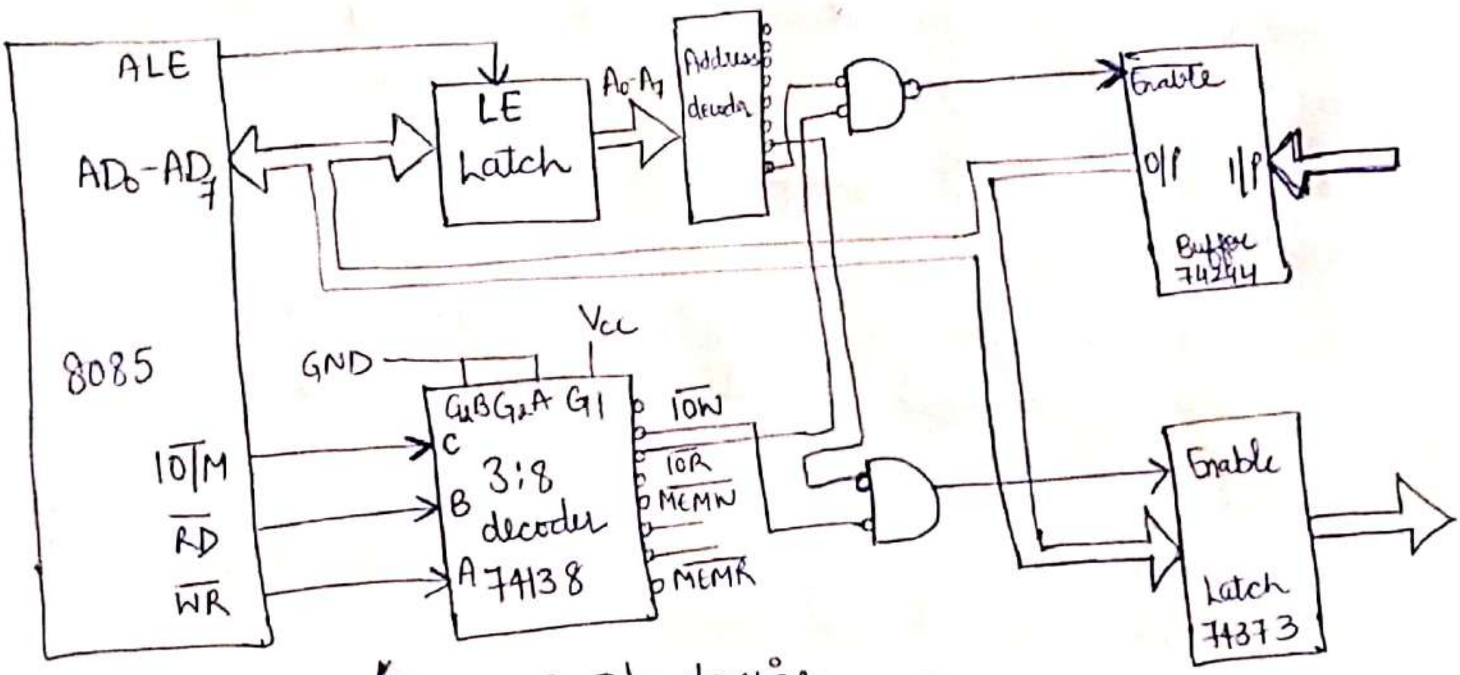
(1) Using logic gates

(2) Using 3:8 decoder

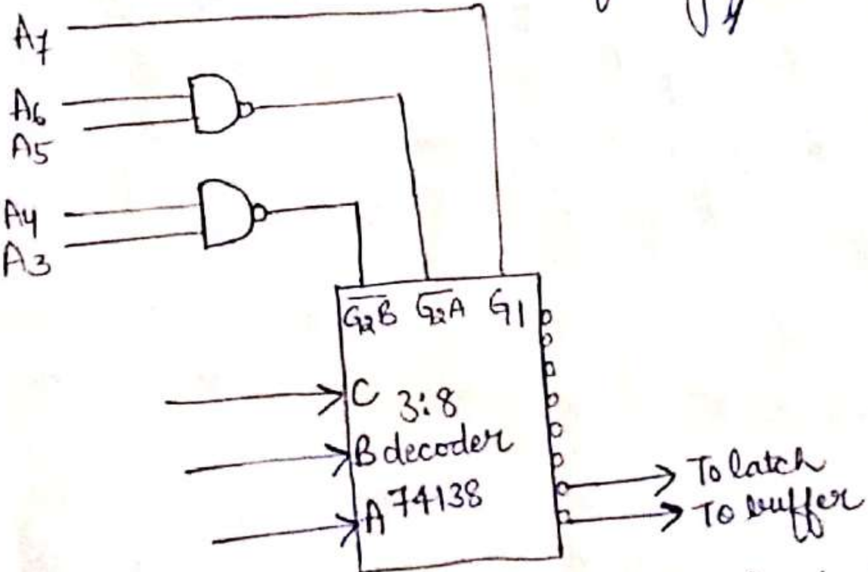
are shown



(Decoder logic)



(General I/O device interfacing)



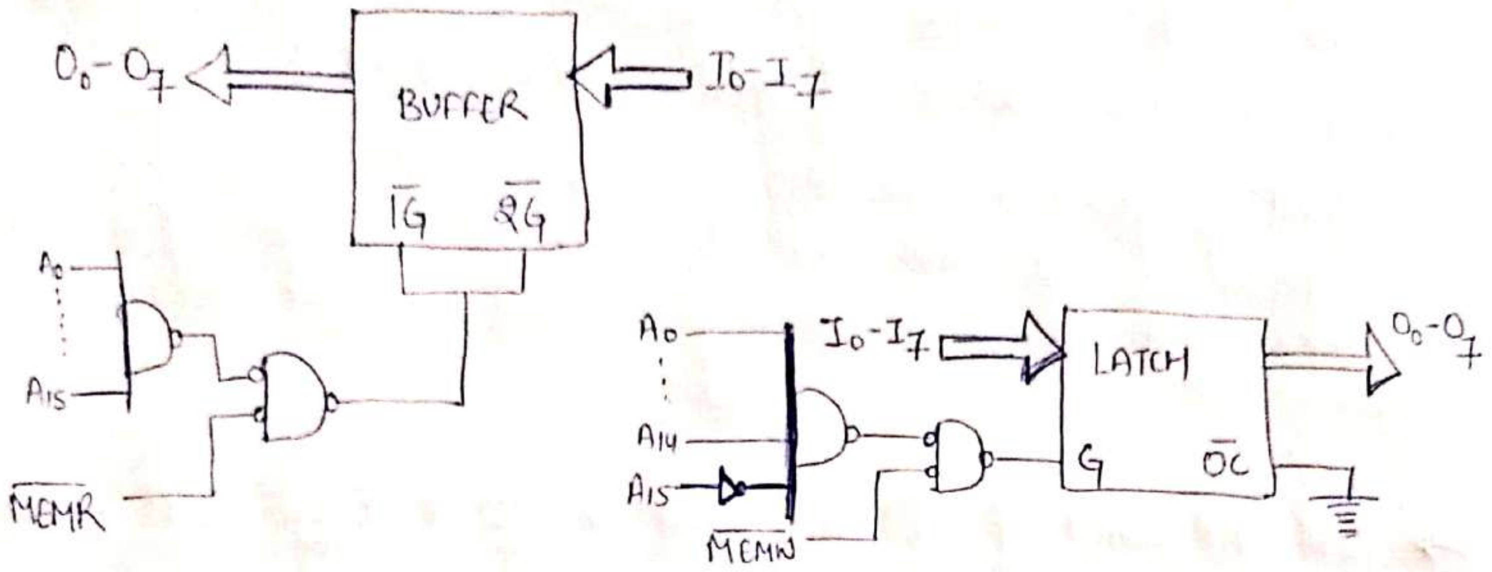
(3:8 decoder selection logic)

MEMORY MAPPED I/O

- In this case the I/O device are treated as memory location. There will be no separation like memory or I/O.
- Each device (I/O) will have 16 bit address.
- The control signals used will be same as memory i.e $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$.
- The interfacing between the I/O and microprocessor will be same as single memory location. Because of this the instructions for I/O device will be memory related instruction for ex. LDA, STA, LDAX, STAX, MOV A etc
- The number of I/O device will be 64KB shared by I/O and memory.
- For data transfer, microprocessor will send address on A_0 to A_{15} lines and generates control signals or $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$.
- In $\overline{\text{MEMR}}$ it accept data from I/O device while in $\overline{\text{MEMW}}$ it transfer data to I/O device.

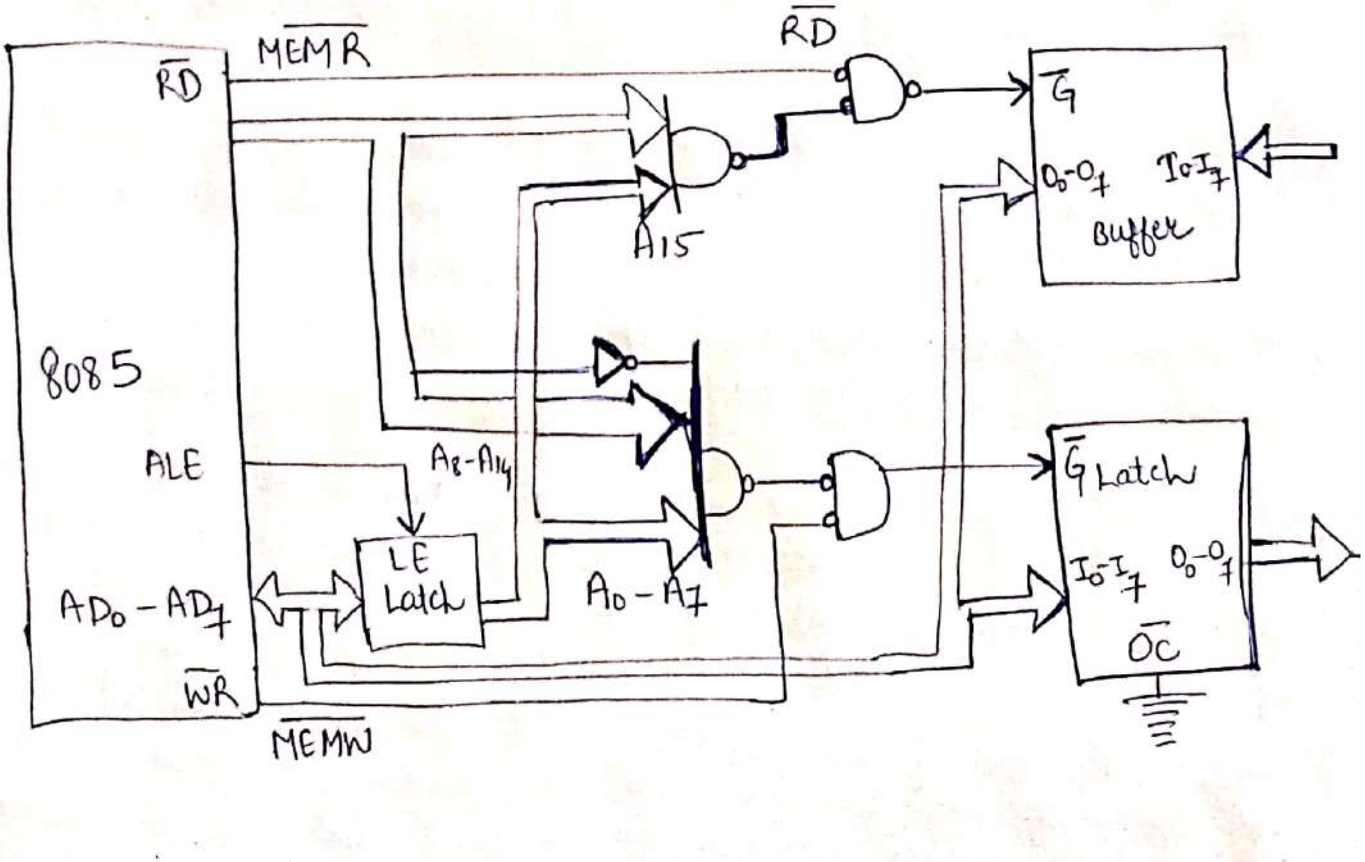
INPUT/OUTPUT INTERFACING IN MEMORY MAPPED I/O

- The simple input output device is a buffer and output device is latch. To interface these devices to 8085, the control lines $\overline{1G}$, $\overline{2G}$ of buffer and G input of latch is controlled from 8085.
- The address is of 16 bits A_0 to A_{15} and control signal $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ are used to control the buffer latch.
- The combination of address lines A_0 to A_{15} can be done by using NAND gates and then it is combined with $\overline{\text{MEMR}}$ and $\overline{\text{MEMW}}$ signal.
- The interfacing diagram is



(Input/output interfacing in memory mapped I/O)

For buffer when A_0 to A_{15} are all 1's the output of NAND gate will be low. It is then combined with MEMR using NAND gate with inverted inputs and connected to 1G and 2G. So the address of buffer will be FFFF H.



- For latch when A_0 to A_{14} all are 1's and the line A_{15} $\overline{MEMW} = 0$ the output of NAND gate will be low, it is then combined with MEMW Using AND gate with inverted inputs and connected to G, so the address of latch will be 7FFFH.
- Instead of gates a 3:8 decoder logic can be used to select appropriate device. The general interfacing diagram of an I/O device with 8085 in memory mapped I/O scheme is shown.

→ COMPARISON OF MEMORY MAPPED I/O and I/O MAPPED I/O

I/O Mapped I/O	Memory mapped I/O
1. I/O devices are treated as I/O and memory as memory.	1. Both the devices i.e I/O and memory are treated as memory.
2. Device address is 8/16 bits.	2. Device address is 20 bits.
3. Control signals used for I/O are $\overline{IOR}$ and $\overline{IOW}$.	3. control signals used for I/O are MEMR and MEMW.
4. Special instructions ore available such as IN and OUT	4. All memory related instruction can be used to communicate with IO.
5. Data transfer is possible b/w accumulator and I/O only.	5. Data transfer is possible b/w any register and I/O.
6. The total devices which can be connected will be 1MB memory and maximum 65,535 Input & maximum 65,535 out	6. The total devices will be only 1MB as it is shared b/w memory and I/O.
7. The arithmetic and logical operations are not possible with direct data from I/O device.	7. The arithmetic and logical operations can be performed on direct data from I/O device.