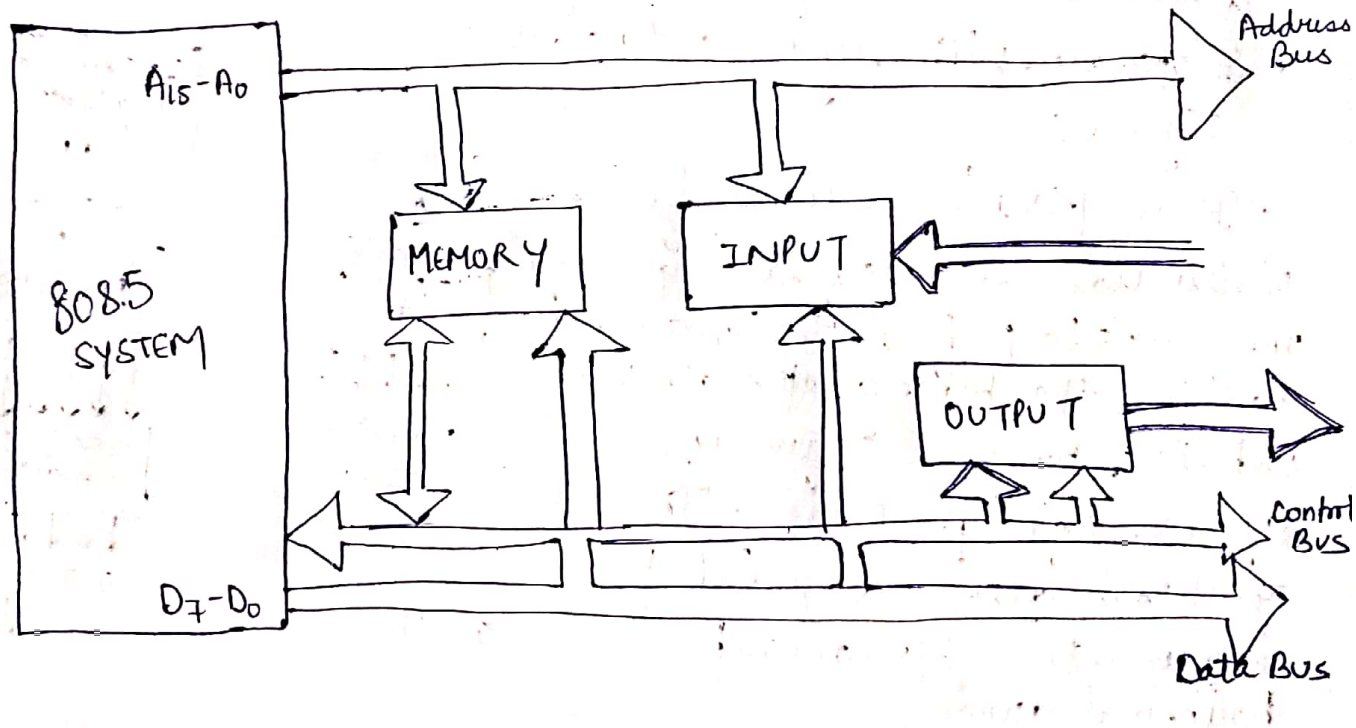
8085 BUS STRUCTURE

- A set of pins, wires or signals having common function is called as bus.
- A bus is a bundle of wires that are grouped together to serve a single purpose in the 8085 microprocessor there are three sets of communication lines that are called buses. They are the address bus, the data bus and control bus. The three buses together form the "SYSTEM BUS".



ADDRESS BUS

- The bus over which the microprocessor sends out the address of a memory location or I/O location is called as the address bus.
- The address bus carries the address of the memory or I/O location to be read or written form.
- In 8085 the address bus is 16 bit ($A_0 - A_{15}$). So the microprocessor can be used to access 16 bit address & is capable of addressing $2^{16} = 65536$.
- The address bus is unidirectional i.e bits flow only in one direction from the microprocessor unit to memory and I/O device.
- The address bus is also used to send the port address on address bus.

DATA BUS

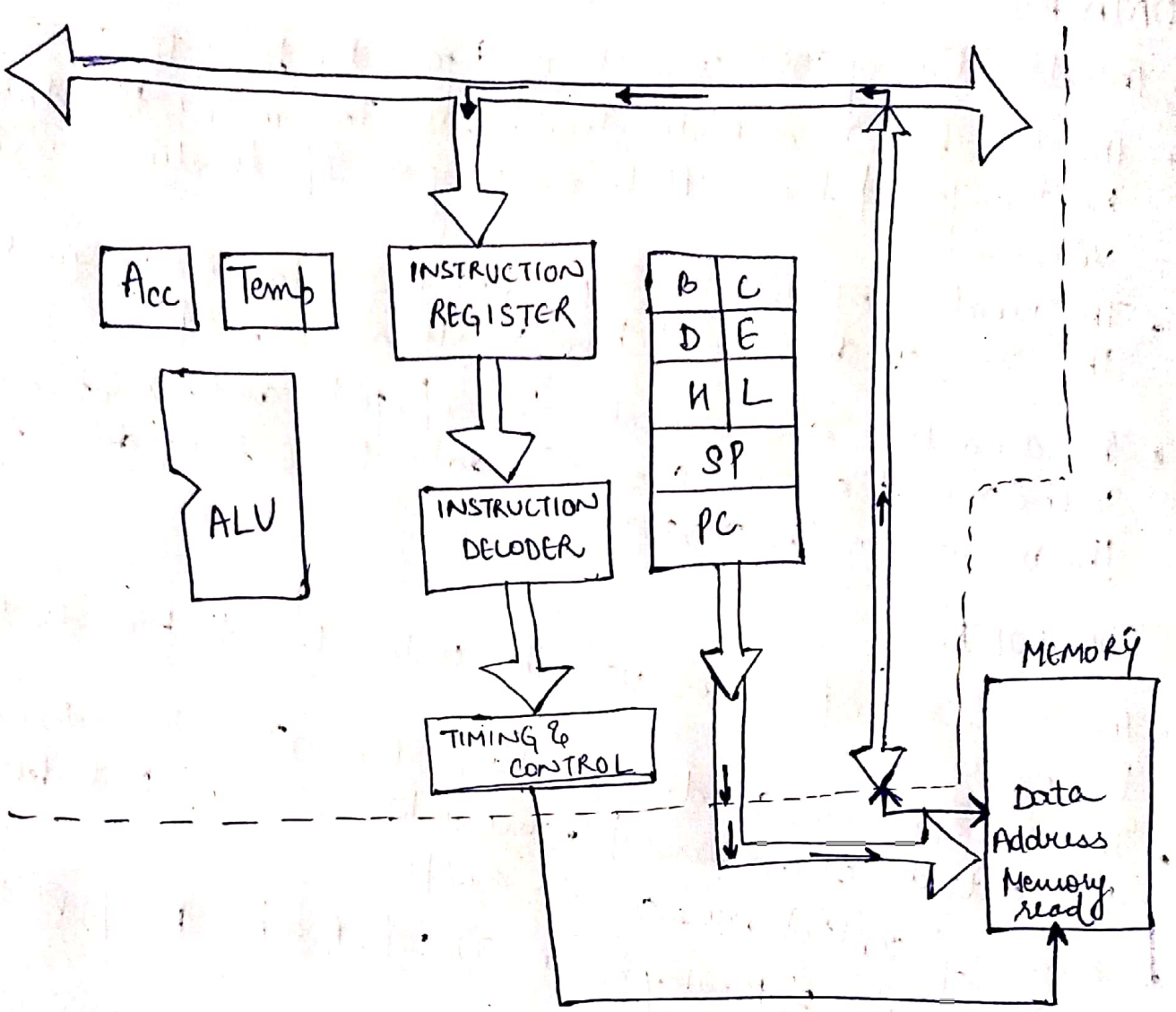
- The data bus of 8085 consists of 8 parallel lines $D_0 - D_7$
- The data bus is a bi-directional bus. This means the data can be transferred from CPU to memory or I/O locations and viceversa.
- The number of data lines used in the data bus is equal to the size of data word being written or read.
- The data bus also connects the I/O ports and microprocessor. So the microprocessor can write data to or read data from the memory or the I/O ports.

CONTROL BUS

- The 8085 microprocessor uses the control bus to provide the timing signals.
- The microprocessor sends signals on the control bus to enable the outputs of addressed memory devices or I/O port devices.
- Some of control bus signals are as follows:
  1) Memory read 2) Memory Write 3) I/O Read 4) I/O Write
- These signals are used to identify a device type with which the microprocessor intends to communicate.

8085 INSTRUCTION FETCHING AND EXECUTION OPERATION

- The basic function of 8085 is to execute a program. For executing a program, 8085 treats each instruction separately.
- For each instruction 8085 requires 2 steps:
  (1) Fetch an instruction from memory.
  (2) Execute the instruction.
- For fetching an instruction, 8085 places the contents of PC on A_0 to A_{15} address lines, makes data bus available and activates a memory read control signal. Becz. of this, the instruction code from memory is available on D_0 to D_7 lines. The microprocessor accepts the contents of D_0 to D_7 and transfers them to internal data bus.

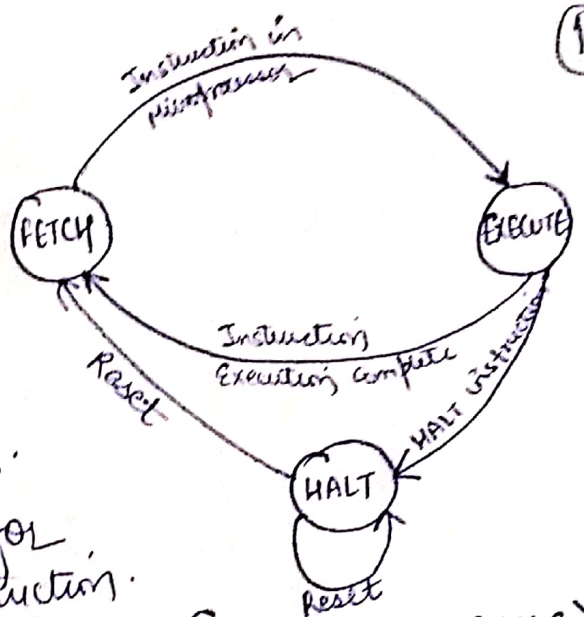


[INSTRUCTION FETCH OPERATION]

From there it is only accepted by instruction register and fetch operation is complete.

- The bit pattern concerning to instruction i.e OPCODE is then transferred to instruction decoder, there it is decoded and supplied to timing and control.
- The timing and control gets all the information about the operation specified. The timing and control will perform the operation, this is called as EXECUTION OF AN INSTRUCTION.
- If instruction specifies to read the data from memory, the address will be given by instruction or specified by instruction. So it will read data from memory, the operation will be execution instruction. The microprocessor will complete this and then go for fetching OPCODE of next instruction.

- The fetch and execute cycles of instruction will toggle among one to other. First fetch operation is completed then the instruction code is available. The microprocessor then executes this instruction and will go for the fetch operation of next instruction.



(FETCH-EXECUTE CYCLE)

- The above switching is applicable for all instructions except HALT instruction. When HALT instruction is executed, the microprocessor enters HALT loop so will not go for fetch operation. The microprocessor will remain in HALT loop and check reset signal. When a reset is applied, it will return back to fetch operation.

FETCH CYCLE	EXECUTION CYCLE
1. The microprocessor perform fetch cycle to access instruction codes from program memory.	1. The microprocessor performs execution cycles to access data memory, stack memory and I/O devices.
2. During fetch cycle, the microprocessor performs only read operation.	2. During execution cycle the microprocessor performs either read or write operation.
3. PC is incremented by 1.	3. PC is not incremented.
4. Contents of PC are placed on the address bus.	4. Contents of SP, general purpose register pair or temporary register pair are place on the address bus.