8085 ARCHITECTURE

- **INTRODUCTION :-** A microprocessor is a semiconductor chip that implements the central processor of a computer. The microprocessor works as a brain of a computer. It consists of an ALU and a control unit. The microprocessor are usually characterised by speed, word length, architecture and instruction set. This central processing unit built into single chip is called as Microprocessor.

- **8085 FEATURES :-** The features of a processor can be divided into three broad groups viz. basic features, special features & miscellaneous features.

  Basic features of 8085 :-
  - Processor size
  - Address bus size for memory
  - Speed of processor
  - Address bus size for I/O

1. 8085 is a 8 bit microprocessor. This implies that:
   a) It has 8 bit ALU that can perform 8 bit operations.
   b) It has 8 bit internal data bus and registers.
   c) It has 8 bit external data bus.
2. It has three versions based on frequency of operation.
   a) 8085 → 3MHz
   b) 8085-2 → 5MHz
   c) 8085-1 → 6MHz
3. 8085 has 16 bit address bus to access memory, hence it can access $2^{16} = 2^6 \times 2^{10} = 64 \times 1k = 64KB$ memory locations.
4. It has 8-bit address bus to access I/O locations.

SPECIAL FEATURES OF 8085:-
- Single +5V power supply
- On-Chip clock generator
- Duplex Serial port

1. 8085 was the first processor that required only single +5V power supply.
2. 8085 has a duplex serial port with 2 pins to receive and transmit serial data.
3. It has an on-chip clock generator. Hence there is no need for external clock generators.

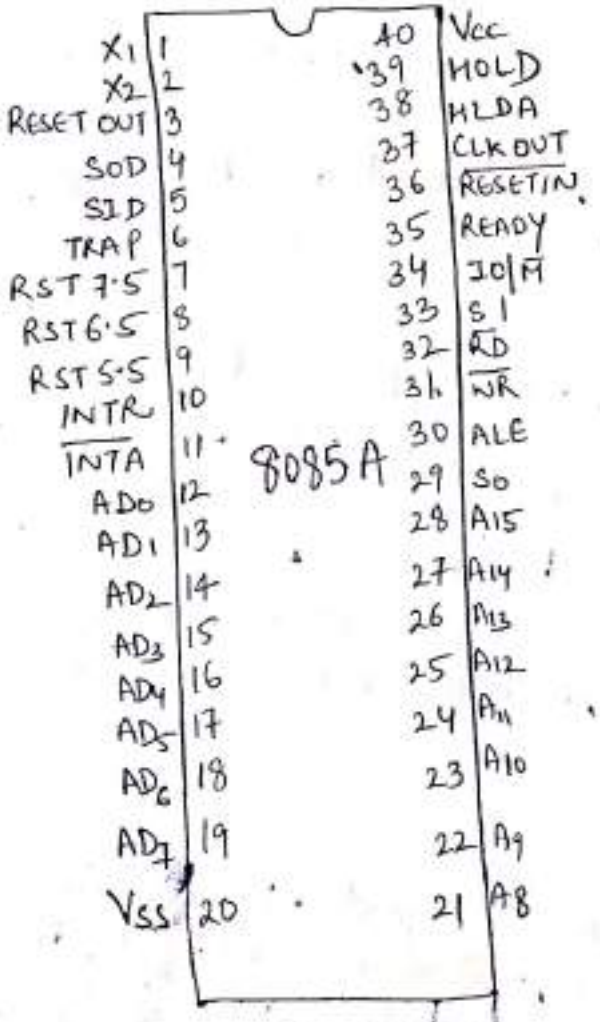
MISCELLANEOUS FEATURES of 8085:-
- Interrupts
- Instruction set
- Registers
- Data types for ALU

1. 8085 has 5 hardware interrupts and 8 software interrupts.
2. 8085 has following registers
   a. 8 bit accumulator
   b. Six 8 bit general purpose registers named as B, C, D, E, H and L
   c. Flag Register
   d. 16 bit program counter.
   e. 16 bit stack pointer.

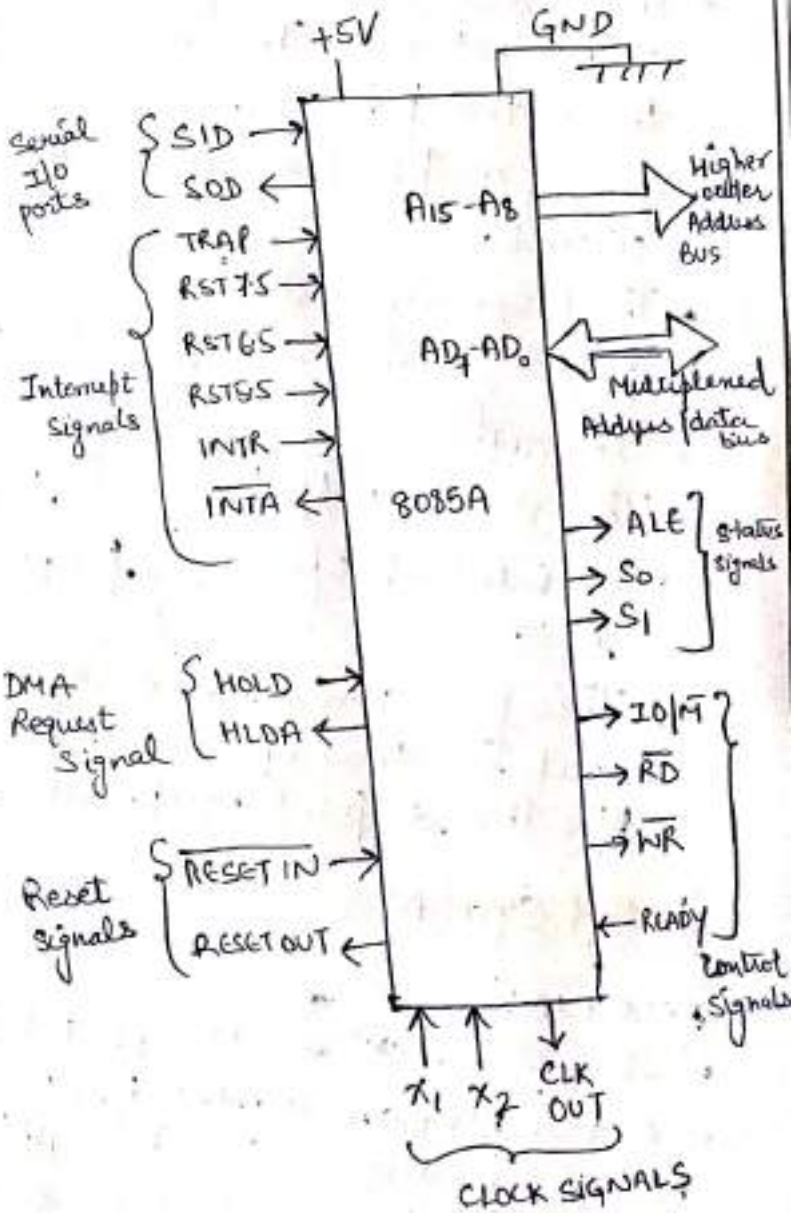
3. 8085 has a powerful instruction set that can do various arithmetic operations.
4. 8085 can perform operation on bit, byte and some word data.

PIN DEFINITIONS OF 8085

The 8085A is an 8 bit general purpose microprocessor having 40 pins and works on single power supply.



PIN DIAGRAM OF 8085



GROUPS OF 8085 SIGNALS

We group the signals as:

(1) Power supply signals.
(2) clock signals
(3) Reset Signals
(4) Interrupt Signals
(5) Address bus and data bus
(6) Status Signals and control Signals
(7) Serial input/output Signals.
(8) DMA Request Signals.

POWER SUPPLY SIGNALS

V_{cc} and V_{ss}

- V_{cc} is to be connected to +5V power supply.
- V_{ss} Ground Reference.

CLOCK SIGNALS

(1) X_1 X_2

- These are clock input signals, connected to crystal, LC or RC network. The crystal, LC or RC is connected b/w these two pins..
- The X_1 and X_2 pins drive the internal clock generator circuit.
- The frequency is divided by 2 and used as operating frequency.

(2) CLK OUT

- This is an output signal, used as system clock.
- The internal operating frequency is available on CLK OUT pin.
- This pin can be used by the peripherals as a system clock input for their operation. Hence there will be synchronization b/w the different peripherals and the microprocessor.

RESET SIGNALS

$\overline{\text{RESET IN}}$

- This is an active low, input reset signal. When $\overline{\text{RESET IN}}$ = 0 it clears program counter i.e 0000 and makes address, data and control lines tristated. After reset the status of internal register and flag are unpredictable.
- The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
- After reset the microprocessor starts executing instructions from 0000H onwards.

RESET OUT

- This is an active high, output signal used to indicate that the microprocessor is reset.
- This signal is used as system reset, to reset other devices connected in system.

INTERRUPT SIGNALS

1) TRAP

- This is an active high level and edge triggered, non maskable, vectored highest priority interrupt.
- When TRAP line is active microprocessor performs internal restart automatically at vector address 0024 H

2) RESTART INTERRUPTS (RST 7.5, RST 6.5, RST 5.5)

- These are active high level, triggered, vectored, maskable interrupt. They cause an internal restart to be automatically inserted.
- The priorities of these are RST 7.5, RST 6.5, RST 5.5
- When RST 7.5, RST 6.5 or RST 5.5 is active microprocessor performs internal restart automatically at vector address 003C H, 0034 H, 002C H respectively.

3) INTR

- INTR is an active high, level triggered, general purpose non-vectored interrupt.
- It has the lowest priority.
- Whenever a device requires a service it has to request service on this pin by making it logic "1".
- The interrupting device has to state where the interrupt service routine is placed in memory.

4) $\overline{\text{INTA}}$

- It is an output signal.
- $\overline{INTA}$ is used to indicate that the microprocessor has received an INTR interrupt.

ADDRESS BUS AND DATA BUS

1) ADDRESS BUS ($A_8 - A_{15}$)
- These are output, tristate signals used as higher order 8 bits of 16 bit address.
- The address bus is always unidirectional meaning that the address is given by 8085 to select a memory or an I/O location.
- It is used to identify a memory location or peripheral device.

2) MULTIPLEXED ADDRESS / DATA BUS ($AD_0 - AD_7$)
- These are input/output, tristate signals having two set of signals. They are address and data.
- The lower order 8 bits, 16 bit address is multiplexed or time shared with data bus.
- They are demultiplexed with the help of ALE signal.
- The address and data buses are multiplexed to reduce the number of pins of the chip.

STATUS AND CONTROL SIGNALS

1) ADDRESS LATCH ENABLE (ALE)
- This is an output signal, used to give information of $AD_0 - AD_7$ contents.
- It is a positive going pulse generated during the first clock cycle of a machine cycle.
- When pulse is high it indicates that the contents of $AD_0 - AD_7$ are address. When it is low it indicates that the contents are data.
- The ALE signal is used to separate $AD_0 - AD_7$ to $A_0 - A_7$ and $D_0 - D_7$. To do this seperation an external latch is

connected to $AD_0 - AD_7$ lines.

2) INPUT OUTPUT / MEMORY ($IO/\overline{M}$)

- This is an output status signal, used to give information of operation to be performed with memory or I/O device.
- If $IO/\overline{M} = 0$, the microprocessor is performing a memory related operation.
- If $IO/\overline{M} = 1$ the microprocessor is performing an I/O device related operation.

3) STATUS SIGNALS (S_1 & S_0)

- These are output status signals used to give information of operation performed by microprocessor.
- When S_1 and S_0 is combined with $IO/\overline{M}$ we get status of all the machine cycles performed by 8085 as shown:

STATUS SIGNALS			OPERATION	CONTROL SIGNALS USED
$IO/\overline{M}$	S_1	S_0		
0	0	0	—	—
0	0	1	Memory write	$\overline{WR}$
0	1	0	Memory read	$\overline{RD}$
0	1	1	Opcode fetch	$\overline{RD}$
1	0	0	—	—
1	0	1	I/O Write	$\overline{WR}$
1	1	0	I/O Read	$\overline{RD}$
1	1	1	Interrupt acknowledge	$\overline{INTA}$
Z	0	0	Halt	—
Z	X	X	Hold	—
Z	X	X	Reset	—

Z - Tristate (High impedence condition)

X - Unspecified Condition

4) READ ($\overline{RD}$)

- This is an active low signal.
- It is an output control signal that is used to read data from the selected memory location or an I/O location via the data bus.
- A low on this pin indicated that a operation performed is a read operation.

5) WRITE ($\overline{WR}$)

- This is an active low signal
- It is an output control signal used to write data to selected memory location or an I/O location via data bus.
- A low on this pin indicated that a operation performed is a write operation.

6) READY

- This is an active high input control signal;
- It is used by microprocessor to detect whether a peripheral is ready for the data transfer or not. If not the processor waits till the signal goes high.
- The main function of this pin is to synchronize the microprocessor 8085 with slower peripherals.

DMA REQUEST SIGNALS

HOLD and HLDA

- HOLD is an active high, input signal used by the other controller to request microprocessor about use of address, data and control signals.
- The HOLD and HLDA signals are used for DMA (Direct Memory Access).

- The DMA Controller receives a request from a device & in turn issues the HOLD signal to the microprocessor.
- The processor releases the system bus and then acknowledges the HOLD signal with HLDA signal. The DMA transfer thus begins.
- The DMA controller will use the buses. On completion of work will disable HOLD signal.

SERIAL I/O SIGNALS

1) SID (Serial Input Data)
   - This is an active high, serial input port pin, used to accept serial 1-bit data under software control.
   - When a RIM instruction is executed the SID pin data is loaded in bit D_7 of accumulator.

2) SOD (Serial output Data)
   - This is an active high, serial output port pin, used to transfer serial 1-bit data under software control.
   - When a SIM instruction is executed the SOD pin is set or reset depending on D_7 and D_6 bits of accumulator.