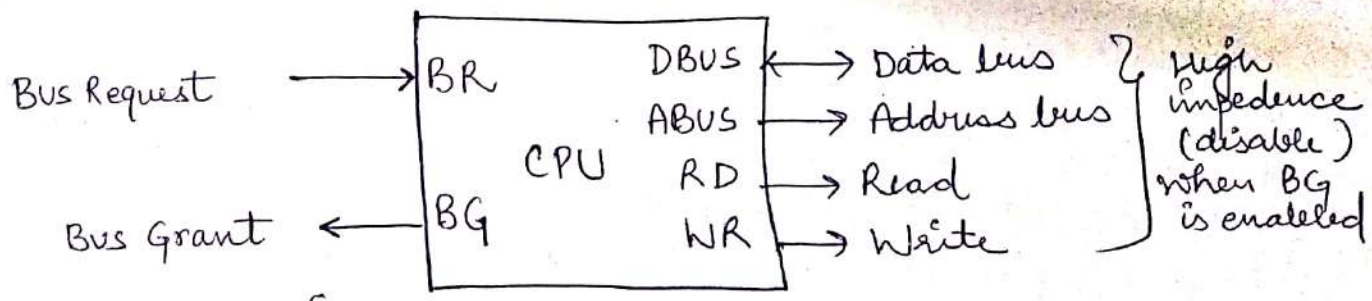
DMA (Direct Memory Access) :-

The transfer of data b/w a fast storage device such as magnetic disk and memory is limited by the speed of the CPU. Removing the CPU from the path and letting peripheral device manage the memory buses directly would improve speed of transfer. This transfer technique is called direct memory access (DMA).

During DMA transfer, the CPU is idle and has no control of the memory buses. A DMA controller takes over the buses to manage the transfer directly b/w the I/O device and memory.

The CPU may be placed in an idle state in variety of ways. One common method used in microprocessors is to disable the buses through special control signals.



(CPU bus signals for DMA transfer)

Diagram shows the two control signals in the CPU that facilitates the DMA transfer.

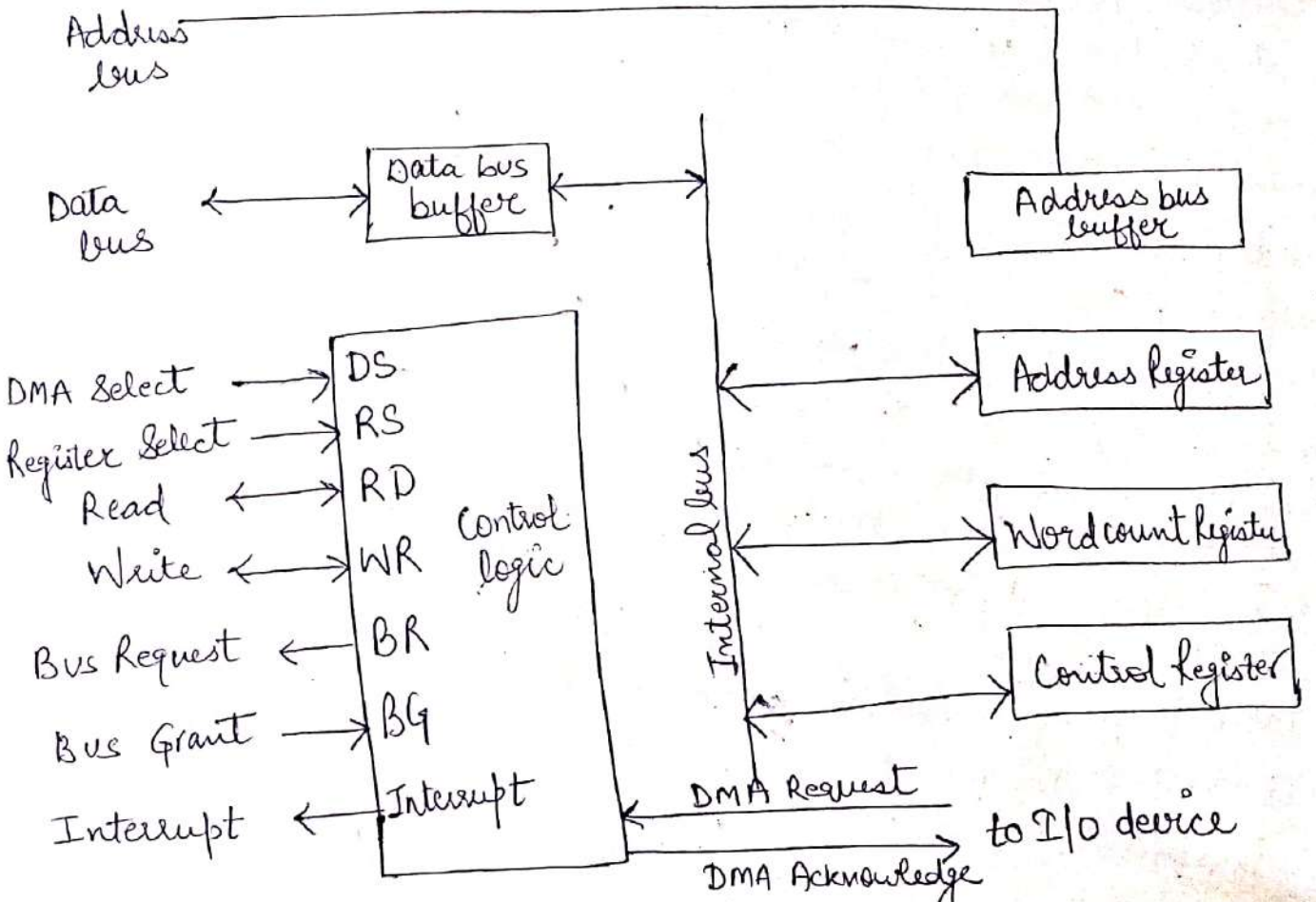
The BUS REQUEST (BR) input is used by the DMA controller to request the CPU to give away the control of the buses. When this input is active, the CPU terminates the execution of current instruction and places the address bus, data bus and the read and write lines into the high impedance state. The CPU activates the bus Grant (BG) output to inform the external DMA that the buses are in high-impedence state. The DMA that originated the bus request can now take control of the buses to conduct memory transfer. When DMA terminates the transfer, it disables the bus request line. The CPU disables the bus grant, take control of buses & return to its normal operation.

When DMA takes control of the bus system, it communicates directly with the memory. In DMA burst transfer, a block sequence consisting of a number of memory words is transferred in a continuous burst while the DMA controller is master of the memory buses. This mode of transfer is needed for fast devices such as magnetic disks. An alternative technique called cycle stealing allows the DMA controller to transfer one data word at a time, after which it must return control of the buses to CPU. The CPU delays its operation for one memory cycle to allow the direct memory I/O transfer to "steal" one memory cycle.

DMA CONTROLLER

The DMA controller needs the circuits of an interface to communicate with the CPU and I/O device. In addition it needs an address register, a word count register and a set of address lines. The address register and address lines are used for direct communication with the memory.

The word count register specifies the number of words that must be transferred. The data transfer may be done directly between the device and memory under control of the DMA.



(BLOCK DIAGRAM OF DMA CONTROLLER)

The unit communicates with CPU via the data bus and control lines. The registers in the DMA are selected by the CPU through the address bus by enabling the DS (DMA select) and RS (Register select) inputs. The read (RD) and write (WR) inputs are bidirectional. When BG (bus grant) input is 0, the CPU can communicate with the DMA register through the data bus to read from or write to the DMA register. When BG = 1, the CPU has given away the buses & the DMA can communicate directly with the memory by specifying an address in address bus and activating the RD or WR control. The DMA communicate with the external

peripheral through the request and acknowledge lines by using a handshaking procedure.

The DMA controller has three registers: an address register, a word count register and control register.

The address Register contains an address to specify the desired location in memory. The address bits go through bus buffer into the address bus. The address register is incremented after each word that is transferred to memory.

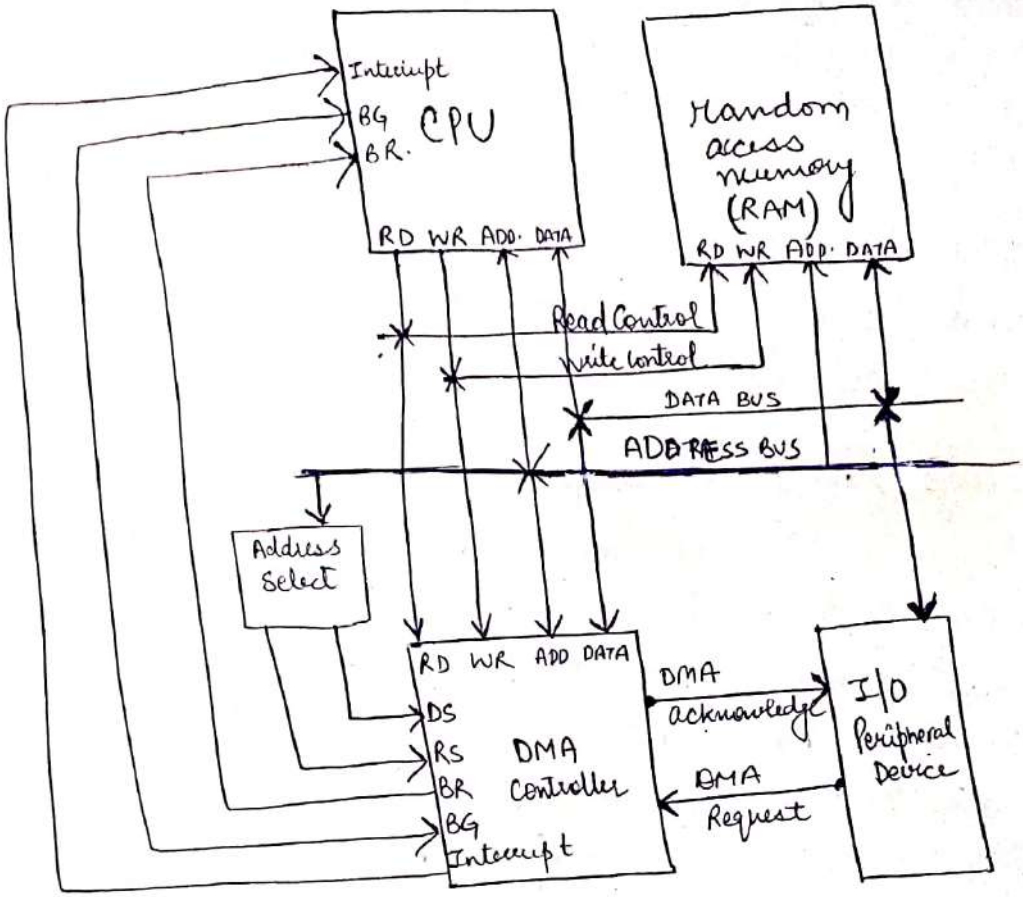
The word count register holds the number of words to be transferred. This register is decremented by one after each word transfer and internally tested for zero.

The control register specifies the mode of transfer. All registers in the DMA appear to the CPU as I/O interface registers. Thus the CPU can read from or write into the DMA registers under program control via the data bus.

The DMA is first initialized by the CPU. After that, the DMA starts and continues to transfer data between memory and peripheral unit until an entire block is transferred. The CPU initializes the DMA by sending the following information through the data bus:

1. The starting address of the memory block where data are available (for read) or where data are to be stored (for write)
   The starting address is stored in address register.
2. The word count, which is the number of words in the memory block.
   The word count is stored in wordcount Register.
3. Control to specify the mode of transfer such as read or write
   Control Information is stored in control Register.
4. A control To start the DMA transfer.

DMA TRANSFER



(DMA Transfer in a computer System)

The CPU communicates with the DMA through the address and data buses with any interface unit. The DMA has its own address, which activates the DS and RS lines. The CPU initializes the DMA through the data bus. Once the DMA receives the start control command it can start the transfer b/w the peripheral devices & memory.

When peripheral device sends a DMA request, the DMA controller activates the BR line, informing the CPU to give away the buses. The CPU responds with its BG line, informing DMA that its buses are disabled. The DMA then puts the current value of its address Register into the address bus, initiates the RD or WR signal and sends a DMA acknowledge to the peripheral devices. When BG=0 the RD and WR are input lines allowing the CPU to communicate

with the internal DMA registers. When BG=1, the RD and WR are output lines from the DMA controller to RAM to specify the read or write operations for the data.

When the peripheral devices receives a DMA acknowledge it puts a word in the data bus (for write) or receives a word from the data bus (for read). Thus the DMA controls the read or write operations and supplies the address for memory. The peripheral unit can then communicate with memory through the data bus for direct transfer between the two units while CPU is disabled.

For each word that is transferred, the DMA increments its address Register and decrements its word count Register. If the word count doesnot reach zero, the DMA checks the request line coming from peripheral. For high speed device, the line will be active as soon as previous transfer is completed. A second transfer is then initiated and the process continues until the entire block is transferred.

If word count register reaches zero, the DMA stops any further transfer and removes its bus request. It also informs the CPU of the termination by means of an interrupt. When CPU responds to the interrupt, it reads the content of word count register. The zero value indicates that all the words were transferred successfully. The CPU can read this register at any time to check the number of words already transferred.

DMA transfer is used in many applications:-

1. It is used for fast transfer of information b/w magnetic disks & memory.
2. It is also useful for updating the display in an interactive terminal
3. The content of memory can be transferred to the screen periodically by means of DMA transfer.