DATA TRANSFER GROUP :-

INTRODUCTION:-

Data transfer group of instruction copies data from source to destination without modifying the content of the source. The various types of data transfer that are possible b/w direct data, registers and memory locations as follows:

Sr. NO.	Data Transfer	Example
1.	Between registers.	Register B → Register D
2.	Specific data byte to register or a memory location	Data byte → Register B
3.	Between Memory location and register.	Memory Location → Register A
4.	Between an I/O device and the accumulator	Input device → Register A
5.	Between a register pair & the stack	Register pair stack → Stack locations.

The data transfer group of instructions include the following instructions:

1.	MOV R_d, R_s	2.	MOV R, M
3.	MOV M, R	4.	MVI R, data
5.	MVI M, data	6.	LXI Rp, 16 bit data
7.	LDA address	8.	STA address
9.	LHLD address	10.	SHLD address
11.	LDAX Rp	12.	STAX Rp
13.	XCHG		

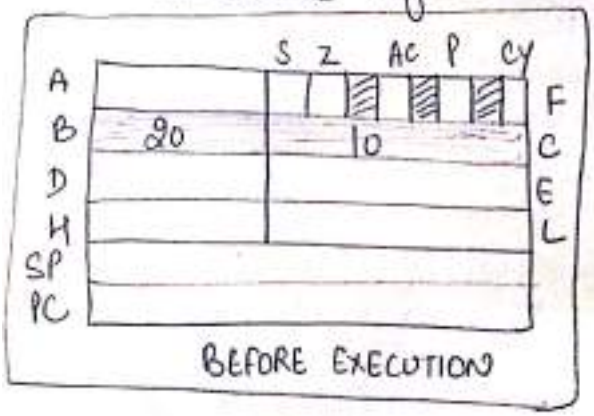
1: MOV R_d, R_s

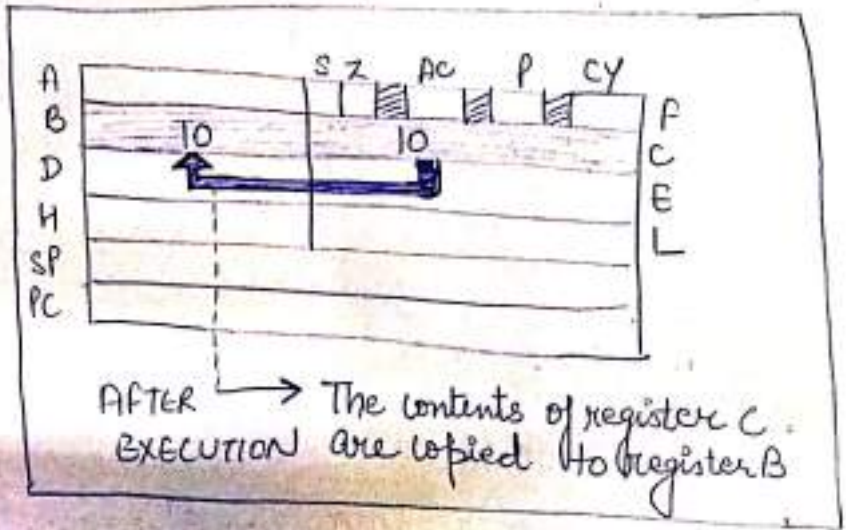
Mnemonic	MOV R_d, R_s
Operation	$R_d = R_s$
No of Bytes	1 byte
Machine cycles	1 (OF)

ALGORITHM	$R_d \leftarrow R_s$
FLAGS	No flags are modified
Addressing Mode	Register addressing Mode
T-States	4

Description:- This instruction copies data from source register R_s to the destination register R_d.
The source register R_s and destination register R_d can be any general purpose register like A, B, C, D, E, H or L
The contents of source register remain uncharged.

Example:- MOV B, C
This instruction will copy the contents of register C to register B
The contents of register C remains unchanged.
Suppose B = 20H, C = 10H and the instruction MOV B, C is executed. After the execution B = 10H and C = 10H





2: MOV R, M

Mnemonic	MOV R, M
Operation	R = M or R = (HL)
No of Bytes	1 byte
Machine cycles	2 (OF + MR)

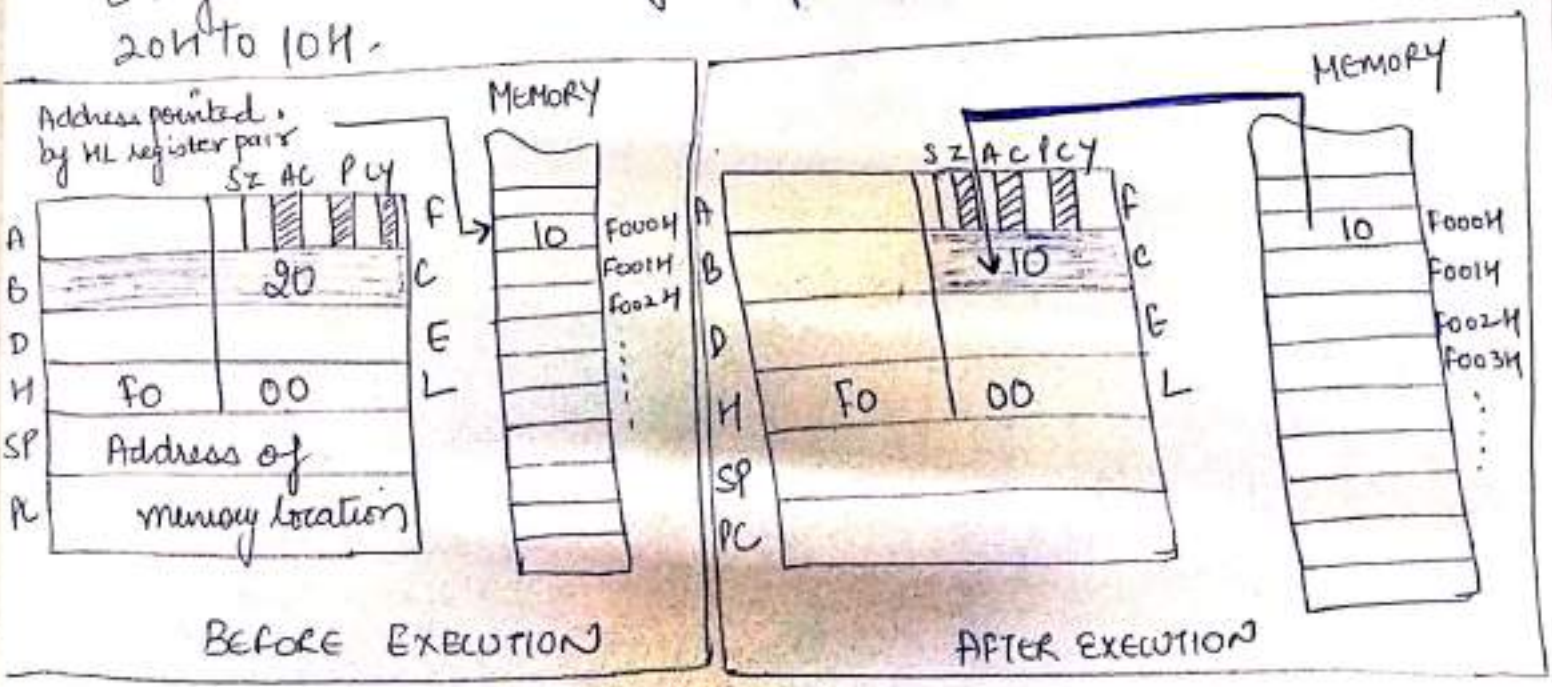
ALGORITHM	$R \leftarrow M$
FLAGS	No flags are modified
ADDRESSING MODES	Indirect addressing mode
T-State	4 + 3 = 7

Description:- This instruction copies data from memory M to register R.

- The term M specifies the HL memory pointer. The contents of HL register pair are used as the address of the memory location. The contents of that memory location are transferred to the specified register R.
- The Register R can be any general purpose register like A, B, C, D, E, H or L

EXAMPLE :- MOV C, M

- This instruction will copy the data from the memory location pointed by HL register pair to C register.
- Let the contents of HL register pair be F000H, register C=20H
- At the address F000H : 10H is stored. The HL register pair contents are used as address ie HL=F000H
- The content of memory location F000H are copied to the C register. So contents of C register will change from 20H to 10H.



3. MOV M,R

MNEMONIC	MOV M, R
Operation	M = R or (HL) = R
No of Bytes	1 byte
Machine Cycles	2 (OF + MW)

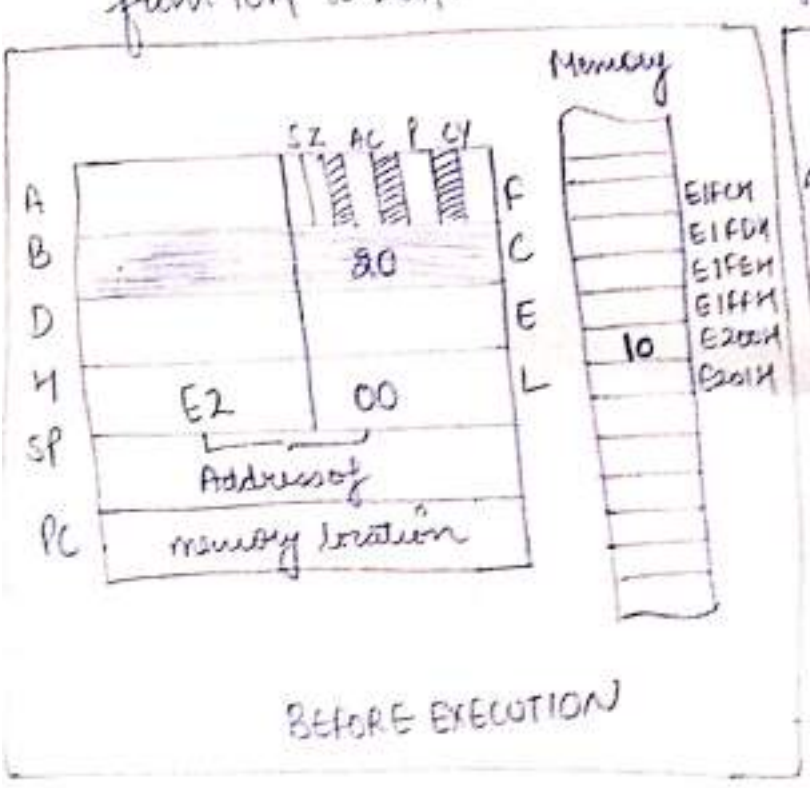
ALGORITHM	M ← R or (HL) ← R
FLAGS	No flags are modified
ADDR. MODE	Indirect addressing mode
T-States	4+3=7

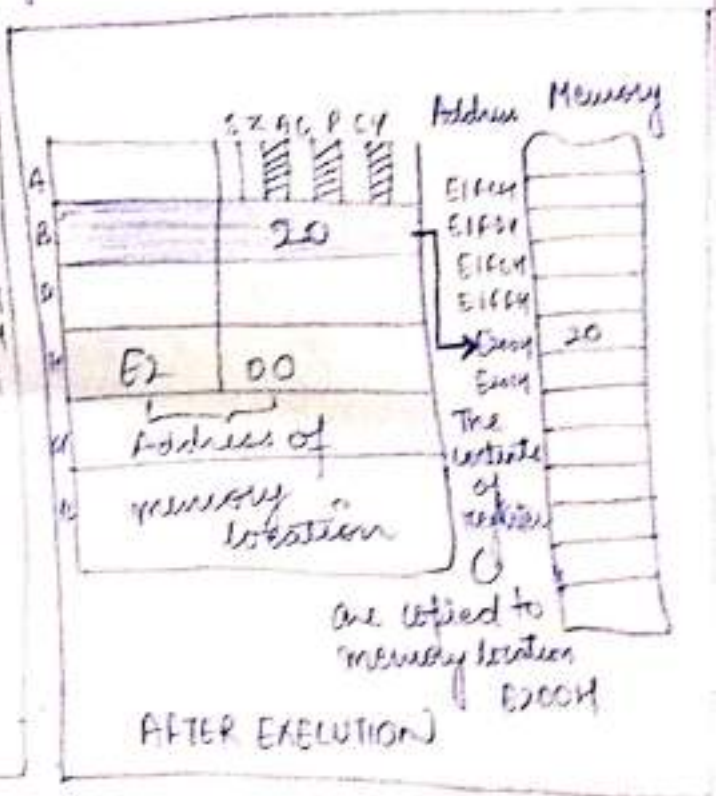
DESCRIPTION :- This instruction will copy the data from the register to memory M.

- The HL register pair is used as the memory pointer. The contents of the specified register are copied to that memory location pointed by the HL register pair.
- The specified register may be any general purpose register A, B, C, D, E, H or L

EXAMPLE :- MOV M, C

- Let the contents of HL pair are E200H, register C = 20H, at address E200 : 10H is stored. On the instruction MOV M, C the data is transfered from C register to memory
- The contents of the register C are copied to memory location E200H, so the contents of memory location E200H will change from 10H to 20H.





4. MVI R, Data

Mnemonic	MVI R, Data
Operation	R = data
No of bytes	2 bytes
Machine cycles	2 (OF + MR)

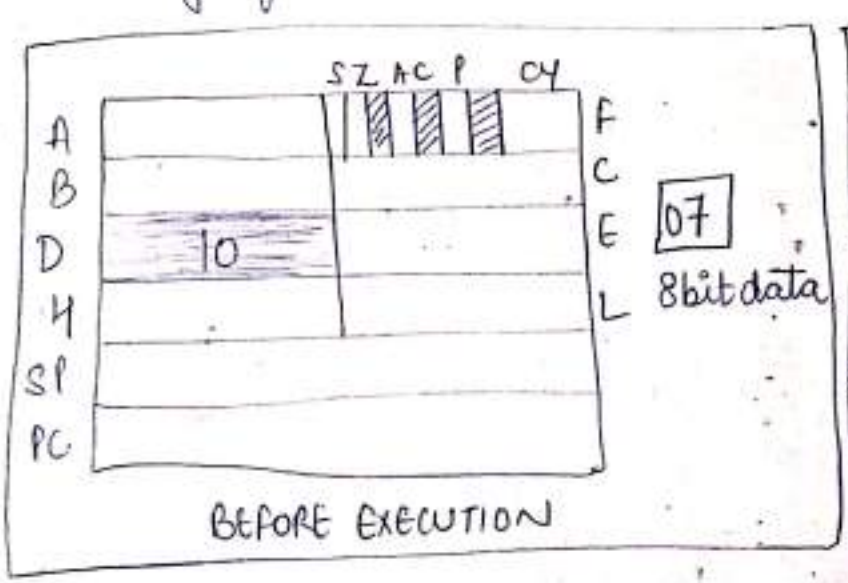
ALGORITHM	R ← data
FLAGS	NO flags are affected
ADDR. MODE	Immediate addressing mode
T-States	7 (4+3)

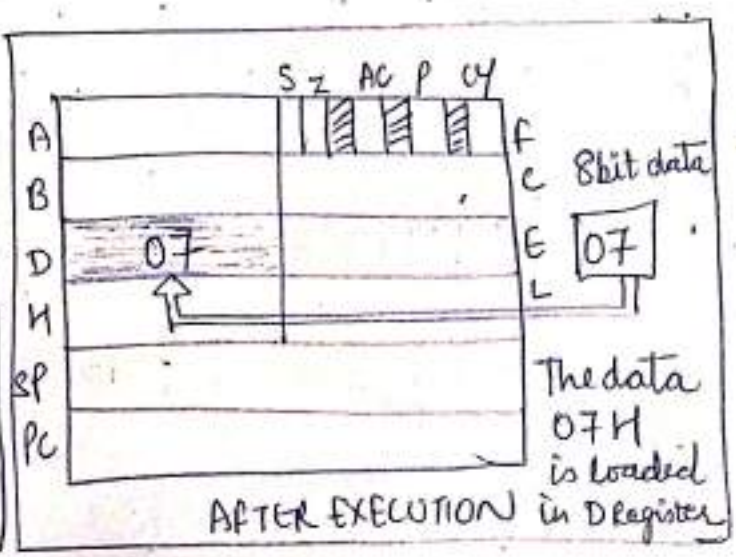
DESCRIPTION :- This instruction moves the 8 bit immediate data to the specified register.

- The data is specified within the instruction.
- It is a two byte instruction, so first byte of instruction will be OPCODE and second byte will be 8 bit data.
- The register R may be any General purpose register like A, B, C, D, E, H or L.

EXAMPLE :- MVI D, 07H

- This instruction will load the immediate data 07H in register D.
- Let the contents of register D = 10H. Then after the execution of instruction MVI D, 07H the contents of register D will be change from 10H to 07H.





5. MVI M, DATA

Mnemonic	MVI M, Data
Operation	M = data or (HL) = data
No of Bytes	2 bytes
Machine Cycles	3 (OF + MR + MW)

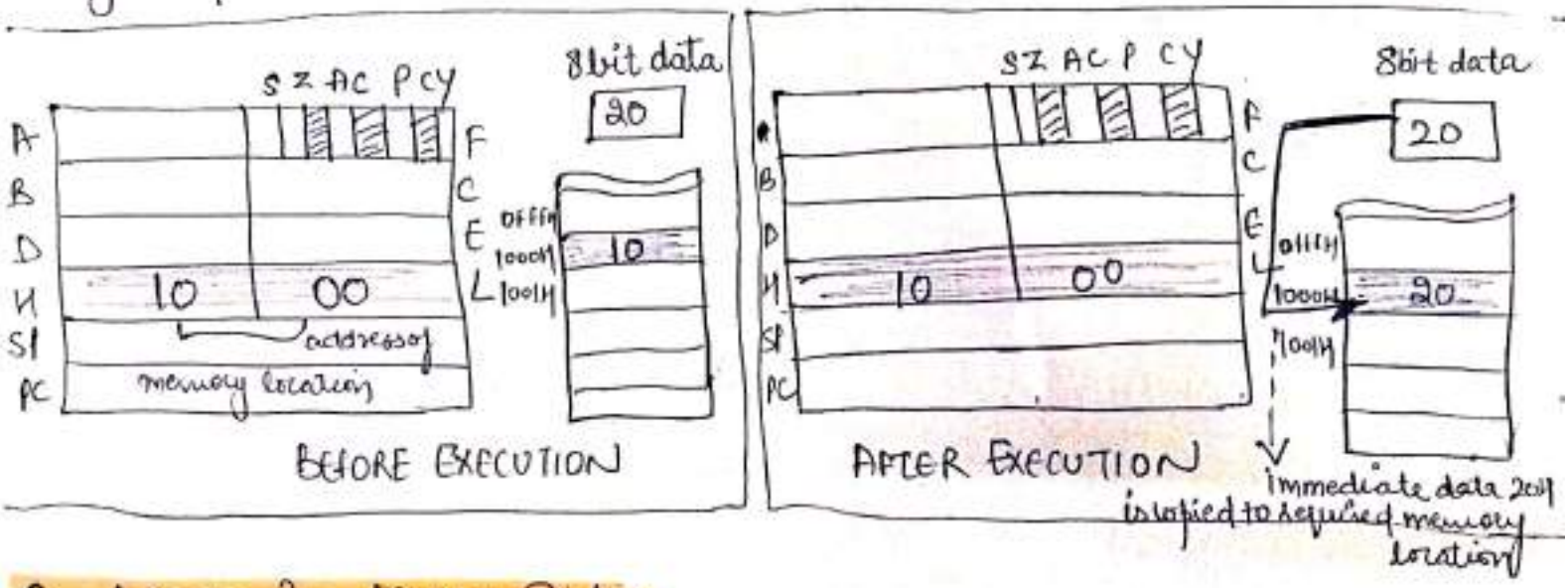
ALGORITHM	M ← data or (HL) ← data
FLAGS	No flags are affected
ADDR. MODE	Indirect addressing Mode / Immediate addr. mode
T-STATE	10 (4+3+3)

DESCRIPTION :- This instruction moves immediate data to memory.

- The HL register pair is used as memory pointer. The contents of HL register pair are used as memory address and the immediate data is transferred to that memory location.

EXAMPLE :-
```
MVI H, 10H
MVI L, 00H
MVI M, 20H
```

- 10H is transferred to H register
- 00H is transferred to L register
- 20H is transferred to memory
- When the instruction MVI M, 20H is executed the data 20H will be stored in the memory location addressed by the HL register pair i.e 1000H



6. LXI Rp, 16 bit Data

Mnemonic	LXI Rp, 16bit data
operation	Rp = 16 bit data
No of Bytes	3 bytes
Machine cycle	3 (OF+MR+MR)

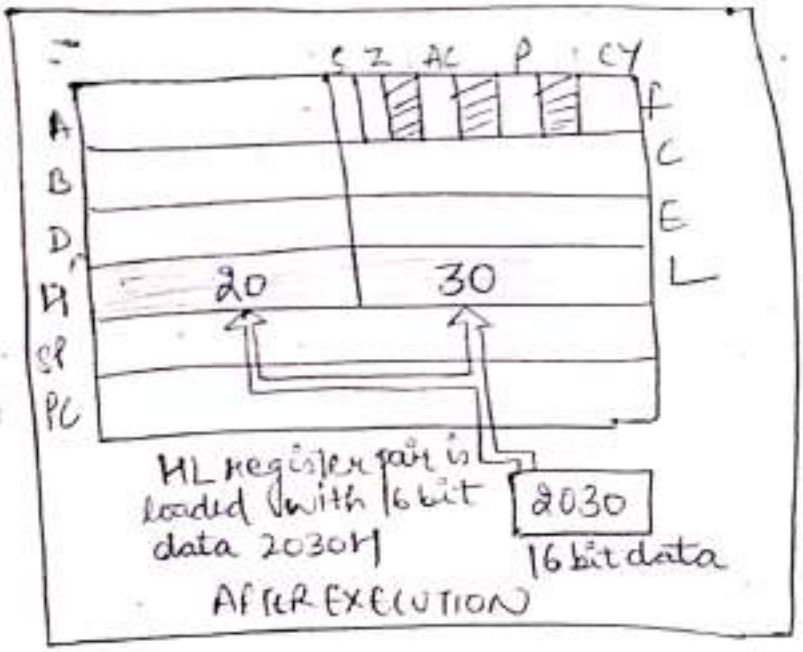
Algorithm	Rp ← 16 bit data
FLAGS	No flags are affected
ADDR. MODE	Immediate addressing mode
T States	10 (4+3+3)

DESCRIPTION :- This instruction will load register pair with 16 bit data.

- This instruction loads 16 bit data specified within the instruction to the specified register pair or stack pointer
- In the instruction only high order register is specified for register pair ie if HL pair is to be loaded only H register will be specified in the instruction.
- The register pair Rp can be BC, DE, HL register pair or the stack pointer SP.

EXAMPLE :- LXI H, 2030H

Load HL pair with 2030H. 20H will be loaded in the H register and 30H in the L register.



7. LDA Address

Mnemonic	LDA address
Operation	A=(address)
No of Bytes	3 bytes
Machine cycles	4(OF+MR+MR+MR)

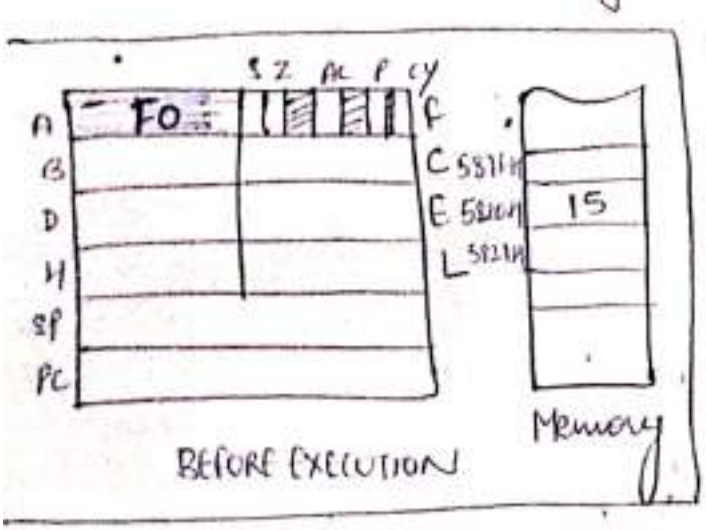
Algorithm	A ← (address)
Flags	No flags are affected
Addr. Mode	Direct addressing mode
T-states	13(4+3+3+3)

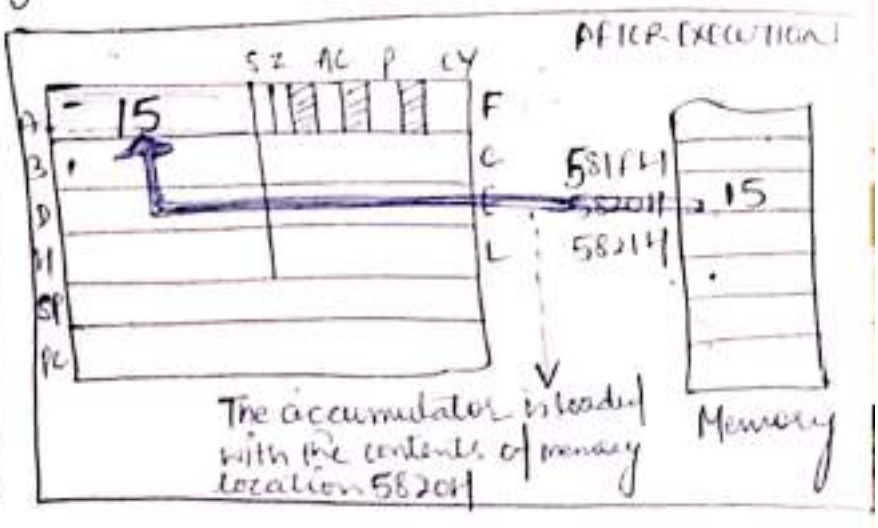
DESCRIPTION :- Load accumulator direct from memory

- This instruction copies the contents of the memory location whose address is specified in the instruction to the accumulator.
- The contents of memory location remains unchanged.

EXAMPLE :- LDA 5820H

- This instruction will load the accumulator with the contents of memory location 5820H.
- Let initially A = 10H, content of memory location 5820H = 15H
- Then after the execution of instruction LDA 5820H, the accumulator will be loaded with 15H. The contents of accumulator will change from F0H to 15H.





8. STA Address

Mnemonic	STA address
Operation	(address) = A
Byte	3 bytes
Machine cycle	4 (OF + MR + MR + MW)

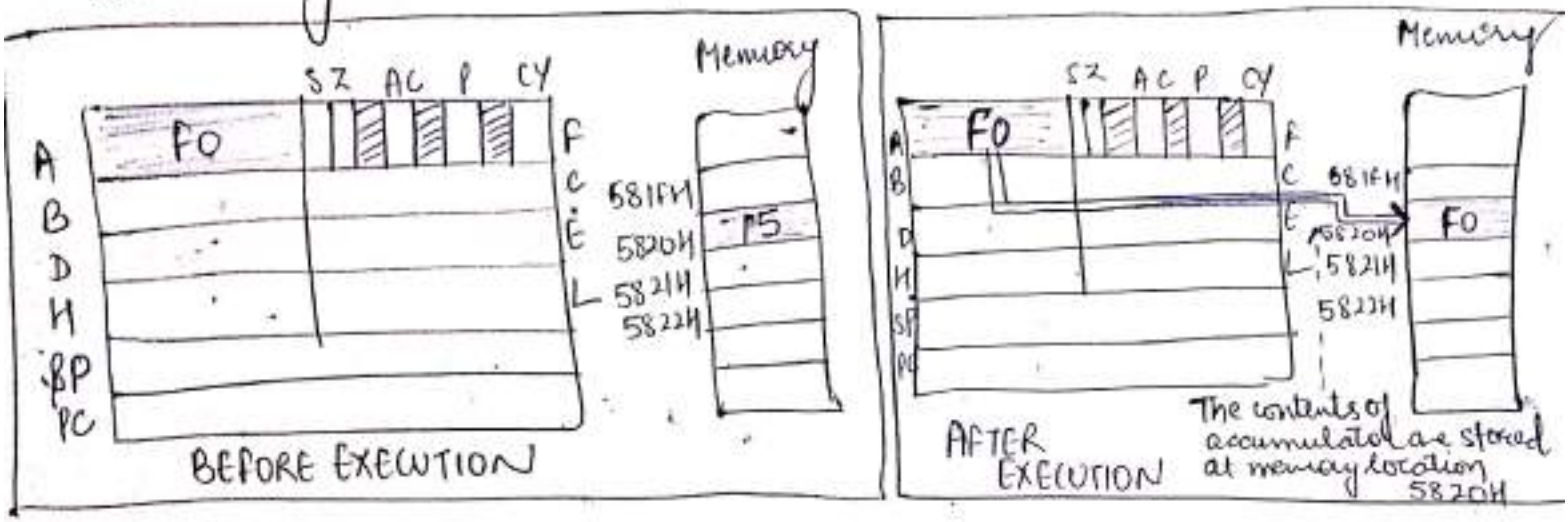
Algorithm	(Address) ← A
Flags	No flags are affected
Addr. Mode	Direct addressing mode
T-States	13 (4 + 3 + 3 + 3)

DESCRIPTION :- Store accumulator direct to memory.

- This instruction will store the contents of the accumulator to the memory location specified in the instruction.
- The contents of the memory location remains unchanged.
- It is a 3 byte instruction. The first byte is opcode, second byte is lower order address and third byte is higher order address.

EXAMPLE:- STA 5820H

- This instruction will store the contents of accumulator at memory location 5820H.



9. LHLD Address

Mnemonic	LHLD address
Operation	L = (address) H = (address+1)
No of Bytes	3 bytes
Machine cycles	5 (OF+MR+MR+MR+MR)

Algorithm	L ← (address) H ← (address+1)
Flags	No flags are affected
Addr. Mode	Direct Addressing mode
T-states	16 (4+3+3+3+3)

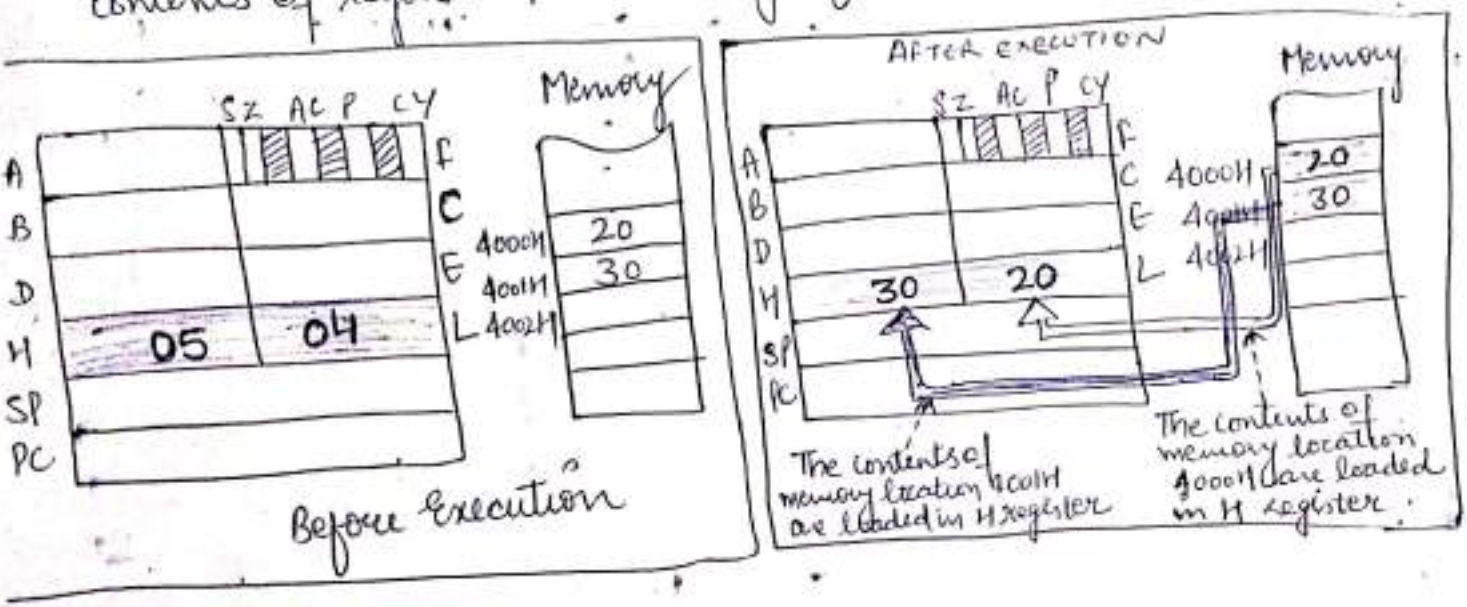
DESCRIPTION:- Load HL pair directly from memory

- This instruction loads the contents of the memory location to the H and registers. The address of memory is specified along with the instruction.
- The contents of memory location whose address is specified in the instruction are transferred to L register and the contents of the next memory location i.e (address+1) to the H register.
- This instruction is used to load the H and L registers from memory.
- It is a 3 byte instruction. The first byte is the opcode, second byte is lower order address and third byte is higher order address.

EXAMPLE:- LHLD 4000H.

- Load HL pair from memory locations 4000H and 4001H
- Let H=05H, L=04H, at memory locations 4000H and 4001H the data 20H, 30H is stored.

- The instruction LHLD will load the contents of memory location 4000H to the L register and the contents of memory location 4001H to the H register.
- So the contents of register L will change from 04 to 20H and contents of register H will change from 05H to 30H.



10. SHLD Address

Mnemonic	SHLD address
Operation	(Address) = L register (Address+1) = H register
No of Bytes	3 bytes
Machine cycles	5 (OF+MR+MR+MW+MW)

Algorithm	(Address) ← L (Address+1) ← H
Flags	No flags are affected
Addr. Mode	Direct addressing mode
T-states	16 (4+3+3+3+3)

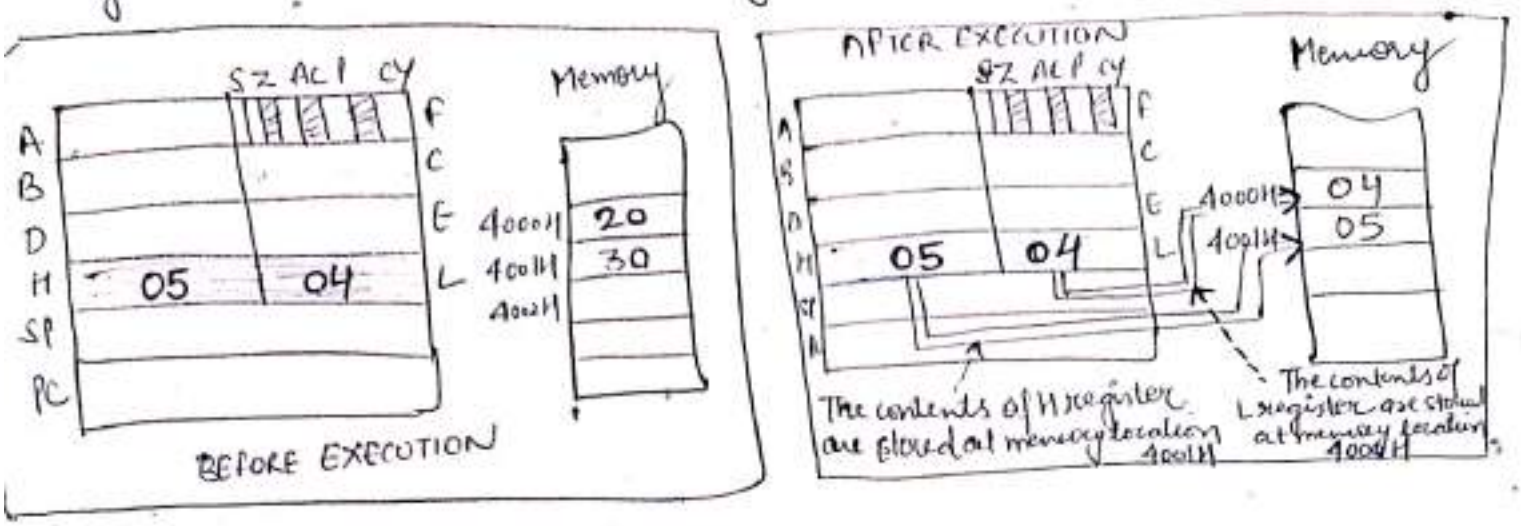
DESCRIPTION :- Store HL pair direct in memory

- This instruction copies the contents of registers H and L to the memory location. The address of memory location is specified along with the instruction.
- The contents of L register are stored at the memory location whose address is specified and the contents of the H register to the (address+1) location.

EXAMPLE :- SHLD 4000H

- Store HL pair to memory locations 4000 and 4001
- Let H = 05H, L = 04H, at memory location 4000H and 4001H the data 20H and 30H is stored and the instruction

SHLD 4000H is executed, the contents of register L are copied to memory location 4000H and the contents of register H are copied to memory location 4001H.



11. LDAX Rp

Mnemonic	LDAX Rp
Operation	A = (Rp)
No. of Bytes	1 byte
Machine cycle	2(OF+MR)

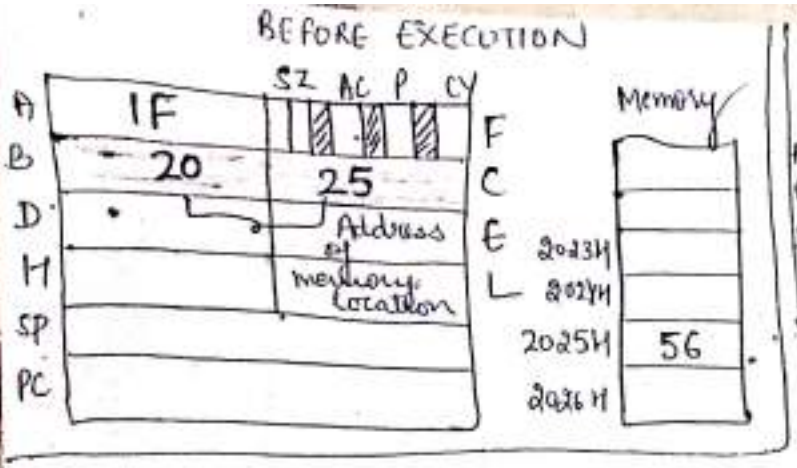
Algorithm	A ← (Rp)
Flags	No flags are affected
Addr. Mode	Indirect addressing mode
T-state	7(4+3)

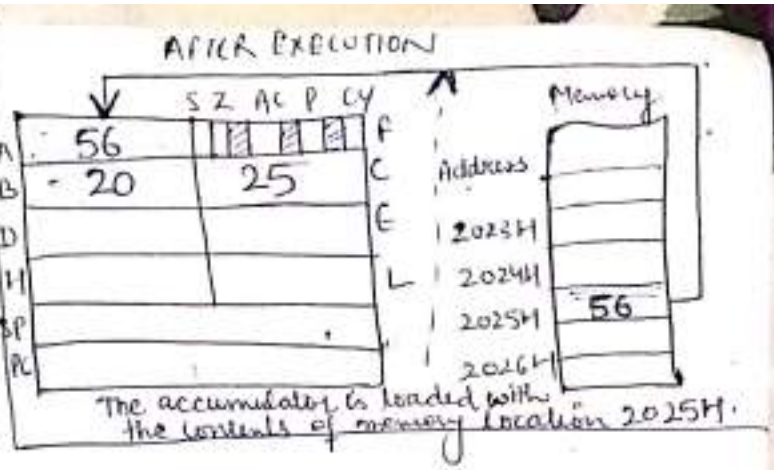
DESCRIPTION:- Load accumulator indirect by using a memory pointer.

- This instruction copies the contents of the memory location to the accumulator.
- The address of memory location is given by Rp register pair specified along with the instruction.
- The register pair Rp can be BC or DE only.
- The contents of the memory location remains unchanged.

EXAMPLE:- LDAX B

- This instruction will load accumulator with the contents of memory location whose address is given by BC register pair.
- Let A = 1F H, B = 20H, C = 25 H at memory location 2025 : 56H is stored.
- Then after the execution of instruction LDAX B, the accumulator will be loaded with the contents of memory location 2025.





12: STAX Rp

Mnemonic	STAX Rp
Operation	(Rp) = A
No of Bytes	1 byte
Machine cycles	2(OF+MW)

Algorithm	(Rp) ← A
flags	No flags are affected
Addr. Mode	Indirect addressing mode
T-state	7(4+3)

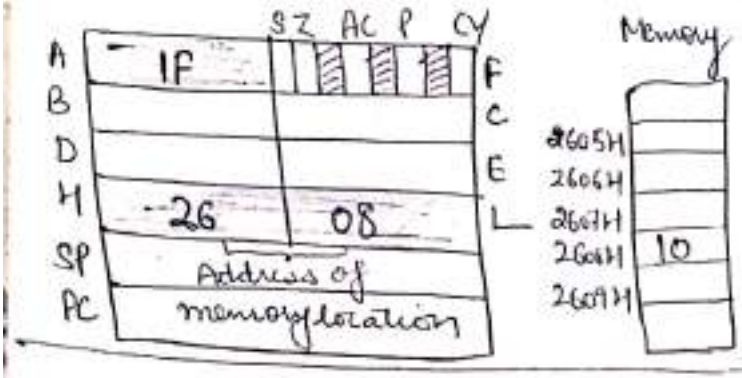
DESCRIPTION :- Store accumulator indirect by using a memory pointer.

- This instruction copies the contents of accumulator to memory location.
- The address of the memory location is given by the Rp register pair specified in the instruction.
- The register pair Rp can be a valid register pair like BC or DE only.
- The contents of accumulator remain unchanged.

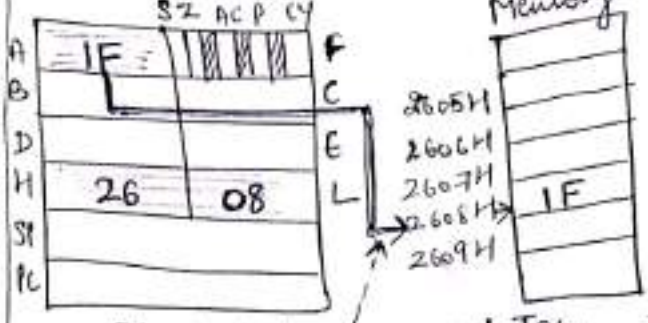
EXAMPLE: STAX D

- This instruction will store the contents of accumulator to the memory location, whose address is given by the DE register pair.
- Let A = 1FH, D = 26H, E = 08H, at memory location 2608:10 is stored.
- Then after the execution of STAX D instruction, the memory location 2608 will contain 1FH.

BEFORE EXECUTION



AFTER EXECUTION



The contents of accumulator are copied to memory location 2608H

13. XCHG

Mnemonic	XCHG
Operation	H↔D L↔E
No° of Bytes	1 byte
Machine cycles	1(OF)

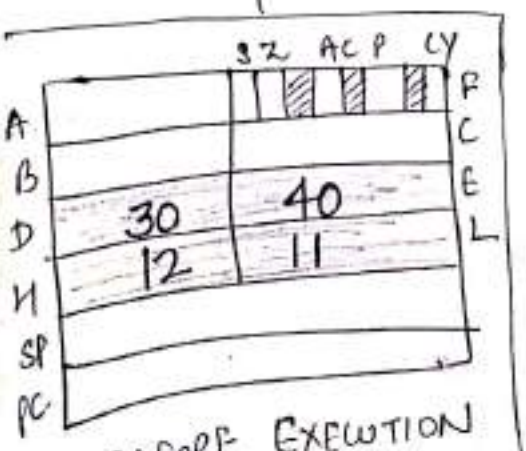
Algorithm	H↔D L↔E
Flags	No flags are affected
Addr. Mode	Register addressing mode
T-state	4

DESCRIPTION: Exchange the contents of HL with DE pair

- This instruction exchanges the contents of H register with D register and L register with E register.

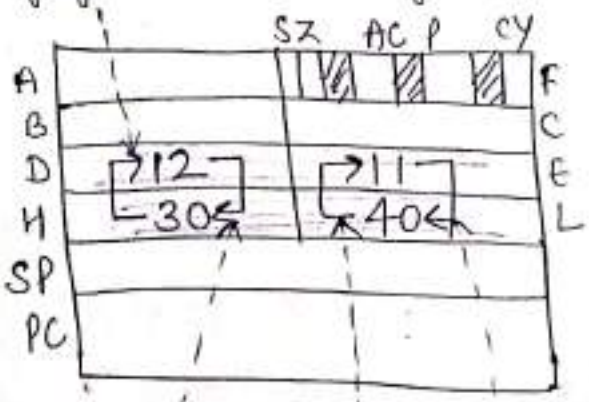
EXAMPLE : XCHG

- Let H=12H, L=11H, D=30H, E=40H and the instruction XCHG is executed.



BEFORE EXECUTION

The contents of register H are loaded in register D.



The contents of register D are loaded in register H

The contents of register L are loaded in register E

The contents of register E are loaded in register L