MODULE 4.2 Peripheral Device, Input-Output Interface, Asynchronous Bata 7 Transfer, Modes of Transfer, Priority Interrupt, DMA, I/O Promo PERIPHERAL DEVICE The input-output subsystem of a computer, referred to as I/o, provides an efficient model of communication between the central system and the outside environment. Devices that are under the direct control of the computer are said to be connected on line. These during are designed to read information into or out of memory unit upor command from the CPU and are considered to the part of the Total computer system. Input or output devices attached to the computer are also called peripherals. Among the most common peripherals are keyboards, display limits and Printers. Peripherals that provide aunitiony storage for the system are magnetic disks and takes. Poulpherals are electromechanical and electromagnetic devices of some complexity, Video Monitors we the most commonly used peripherals. They consist of a keywoard as the input devide and a display unit as the disput device. There are different types of video (monitore but the most popular is cathode lay tube (CRT) The CRT contains an electronic gun that sends an electronic beam to a phospherescent socien in front of the tube. The beam can be defected hoursontally and vertically. To produce a patter on screen, aigned inside the CRT receiped a variable yortage that causes the beam to hit the screen and make it glove at selected stots. Horizontal and vertical signal deflect the bean to make the sweet across the tube, country the visual pattern to appear on the screen. (Vacuum) ☐ -> electrons. plates + E light

Printers provide a permanent record on paper of computer of data or text. There are thru basic types of Character printers: The Daisywheel printer contains a wheel with the Character placed Valong the circumference. The Dot Marine printer contains a set of dots along the puntag mechanism: The Laser Printer was a ristating photographic drum that is used to imprint the character grages. Magnetic takes are used mostly for storing files of data: for Example, a company's paylote record. I Access is sequential and consists of records that can be accessed one after another as the take moves along a stationary read-write mechanism. It is cheapest & stowest method () for storage Other Input and output devices encountered in computer system are digital incumental plotlers, optical and magnetic character readers, and various data acquisition equipment The input-output organization of a computer is a function of the Size of the computer and the devices connected to it ASCII Alphanumeric Characters:-Input and output devices that communicate with people and the computer are usually involved in transfer of alphanemeric information to and from the device and the computer. The Standard binary code for the alphanumeric character is ASCII. It uses form bits to code 128 characters. The ASCII code centains 94 characteres that can be printed and 34 nonprinting characters used for various control functions. The pountfy characters consist of 26 uppercase letters A to Z, The 26 lowercase letters, the 10 numerals 0 to 9, and 32 special printable characters such as %, *, 1 and \$. The 34 control characters are used for nouting data and overanging the brunted text into a presorbed format:

FORMAT EFFECTORS INFORMATION SEPARATURS COMMUNICATION CONTROL CHARACTERS

format effectors are characters that control the layout of printing. They include controls such as backspace (BS), cavaige Return (CR). Information Seperators are used to separate the data into divisions like Poragraphs and pages. They include character such as second separator (RS) and file seperator (FS). The communication Control characteris are useful during the transmission of text between securite terminals. Example due STX ((start of text) and ETX (sind of text).

INPUT-OUTPUT INTERFACE

Input Output interface provides a method for transferring information between internal storage and enternal Input output devices Peripherals connected to a computer need special communication links for interfacing them with the CPU. The purpose of communication link is to resolve the difference that exist b/w the central computer and each peripheral.

The differences are:

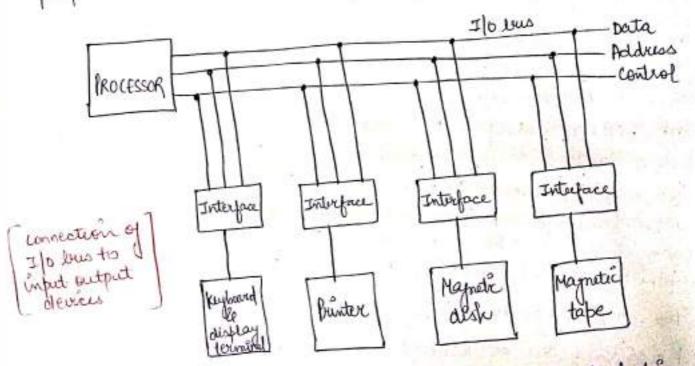
1. Peripherals are electromechanical and electromagnetic devices and their manner of operation is different from operation of CPU and menory and : conversion of signal values may be required.

2. The data transfer rate of perépherals is slower than the toansfer rate of CPU and synchronization mechanism may be needed.

- 3. Pata wedes and formats in purpheral differ from the word format in cov and miniony.
- 4. The operating modes of peripherals are different from each other and each must be controlled so as not to disturb the operation of other perapherals connected to CPU.

To resolve these differences, computer system includes special hordware components by the CPU and peripherals to supervise and synchronize all input and output transfers. These components are called INTERFACE UNITS because they interface components are called INTERFACE UNITS because they interface that processor lows and the peripheral device. In addition both the processor lows and the pulpheral device. In addition each device may have its own controller that supervises the operations of particular mechanism in peripheral.

I/O BUS AND INTERFACE MODULES A communication link between the processor and several posiphurals is shown:



The I/O bus consists of data lines, addies lines and control lines.

The majnetic disk, printer, terminal are employed in general purpose computer. The majnetic take is used in computer for purpose computer. The majnetic take is used in computer for backup street. Each peruphrical olevice has associated with it backup street. Each peruphrical olevice has associated with it controller interface unit each interface alecades the address of the control received from the I/O bus, interprets them for the controller peruphrical and provides signals for the peruphrical controller. It also appropriates the data flow and arguments the transfer of also appropriates the data flow and arguments the transfer of the peruphrical has its between the peruphrical and provisions. Peach peruphrical has its between the peruphrical that operates the particular electromechanical onen controller that operates the particular electromechanical device. Covample, the Printer Controller control the paper device. Covample, the Printer Controller may be housed motion, the print timing. A controlled may be housed separately or integerated with perphiral.

The I/o bus from the processor is attached to all peripheral interfaces. To communicate with particular device peripheral interface advice endness on the address line. The processor places a device endness on the address line trach interface attached to the I/o bus contains an address trach interface decoder that monitors the address line. When the interface decoder that monitors the address line when the path b/w the bus detects its own address, it activates the path b/w the bus detects its own address, it controls. All the peripherals lines and the device that it controls. All the peripherals whose address does not correspond to the address in the bus whose address does not correspond to the address in the bus whose address does not correspond to the address in the bus.

At the same time that the address is made available in the address line, the processor provides a function to the central lines. The interface selected responds to the function took and proceed to execute it. The function took is referred to as an I/o command. The interpretation of the command depends on the perupheral that the processor is addressing.

There are four types of commands that interface may receive.

1. CONTROL COMMAND: - It is issued to activate the peripheral and to inform it what to do.

Example: Magnetic take unit may be instructed to backspace the take by one record, to swind the take. The particular control command issued depends on the particular control command issued depends on the

2. STATUS COMMAND: — It is used to test various status condition in the interface and the peruphreal.

Example: The computer may wish to thick the status of the peripheral before the transfer is initiated. During the transfer one or more error may occur which are detected by the interface. These errors face clisiquated by setting laits in a status register that the processor can bread at certain tidervals.

3. OUTPUT COMMAND: - It causes the interface to respond by transferring data from the less into one of its registers Consider an Example with a taker unit. The computer storts the lape moving by issuing a control command. The Processor then monitors the status of the tape by means of a status command when take is in docust position, the phocusor issues a data curput command.

4. Input Command: It is opposite of the data output. In this case the interface receives an item of data from the perioheral and places it in its buffer register. The processor Checks if data are available by means of a status command and their issues a data input command The interface places the data on the datalines, when they are accepted by processor.

I O VERSUS MEMORY BUS

In addition to communicating with I/o, the processor must Communicate with the mentby unit. Like the I/o lows, the meniony leus centains data, address, and read wente central lines. There are three ways that computer lowers can be used to communicate with mentiony and I/o:

1. Use two seperate buses, one for memory and the other for 110.

2. Use one common bus for both memory and I/O but have seperate control lines for each. ((Isolated 1/0 method)

3. Use one common bus for memory and I/o with common control lines. (Memory mapped I/O)

Un find method, the computer has independent set of data, address and central buses, one for accessing memory and other for I/O. This is done in computers that provide a (seperate I/O processor (IOP) in addition to CPU. The memory communicates with both-the CPU and-the IOP through mining thus. The Top also communicates with the input and output devices through a seperate I/o lous with its own address, data and controlline The purpose of IOP is to provide an independent pathway for transfer of information b/w enternal devices re internal of medicing. The I/o processor is also called as data

2) Goblated VERSUS MEMORY-MAPPED I/O Many computers use one common bus to transfer information b w mentay or I/O and the CPU. The distinction b/rs a meniory transfile and Tobiansfer is made theory's seperate read Jand write lines. The CPU specifies whether the doldress on the address line is for a memory word or for an interface register. The I/o read and I/o (write control lines are enabled dwang an I/o transfer. The memory read and memory write control lines are enabled during memoritionsfer. This configuration isolates all I/O interface address from the address assigned to mining and is referred to as isolated I/O method. In isolated I/o configuration, the CPU has distinct input & output instructions and each of these instructions is associated with the address of an interfalse register. When cru fetches and decodes the operation code of an input and off instruction, it places the address associated with the instruction into the common addiess lines. At same times it enables the I/O read (for input) or I/O wite (for output) control lines. This informs the external component that are attached to the common bus that the address in the address line is for the interface register & not for memory word. On other hand When UV is fitching an instruction of an operand from minory, it placed the meniory address on the address times & enabled the memory read or memory write control line. This informs the external component Athat the address is for meliony word 4 not for I/o interface.) The other alternature is to use the same address space for both memory and I/O. This is the case in computer that empl only one set (by read and white signals and not distinguish ble menery and I/O address. This configuration is referred to as miniony-mapped I/O. In a memory-mapped I/O organization there are not specific input or off instruction. The CPU can manipulate I/o data residy in interface register with the same instructions that are used to manipulate members words lack interface is organized as a set of registers that responds to read and write requests. Computers with munorymapped I/o can use memory-type instructions to access I/o data It allows the computere to () we the same instructions for either input-output transfers or for memory transfers. An example of an I/O interface 110 data Register control Ilonite Register TO CPU To I) odevice Register selected RSI None: data lous in high impedence X X 0 Pout A Register Pout B Register Control Register Status Register

It consists of two data registers called ports, a control register, a status register, bus buffers and timing and control concuits. The interface communicates with the CPU through the data bus. The chip select and register select inputs determine the address assigned to the interface. The Plo read and write are two control lines that Specify an input or output respectively. The four registers communicated directly with the I/o device attached to the interface.

The I/O data to and from the device can be transferred into (3) either port A or ports. The interface may operate with an output device or with a device that requires both input and output. If the interface is connected to printer, it will only output data, and if it sources a character reader, it will only output data.

A magnetic disk unit transfers data in both directions but not at the same time, so the interface can use bidirectional lines.

The central register receives control information from the CPU.

By loading appropriate bits into the control register, the
interfoce and the I/o device attached to it can be placed
interfoce and the I/o device attached to it can be placed
interfoce and the I/o device attached to it can be placed
in a variety of operating modes. For Example, poet A may be
defined as an input poet and poet B as an output poet.

A magnetic tape limit may be instructed to reusing the tape or
to start the tope moving in the forward direction

The lits in the status register are used for status conditions

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and for recording errors that may occur always the data transfer
and for recording errors that may indicate that poet A has
for grample, a status bit may indicate that poet A has
for grample, a status register may indicate that a parity error has
lift in the status register may indicate that a parity error has
occured during the transfer.

The interface registers communicate with the CPU through the bidirectional data bus. The address bus selects the interface unit through the chip select and two register select inputs. A circuit through the chip select and two registers. This circuit enables the address must be provided externally (usually a dicoder) to detect the address must be provided externally (usually a dicoder) to detect the address chip select (CS) input when the interface is selected by the address thus. The two register select inputs RSI and RSO are usually connected to the two least significant lines of address bus. These two inputs select one of the four registers in the These two inputs select one of the four registers in the interface as specified in table. The content of selected interface as specified in table. The content of selected register is transfer into the CPU via the data bus when the