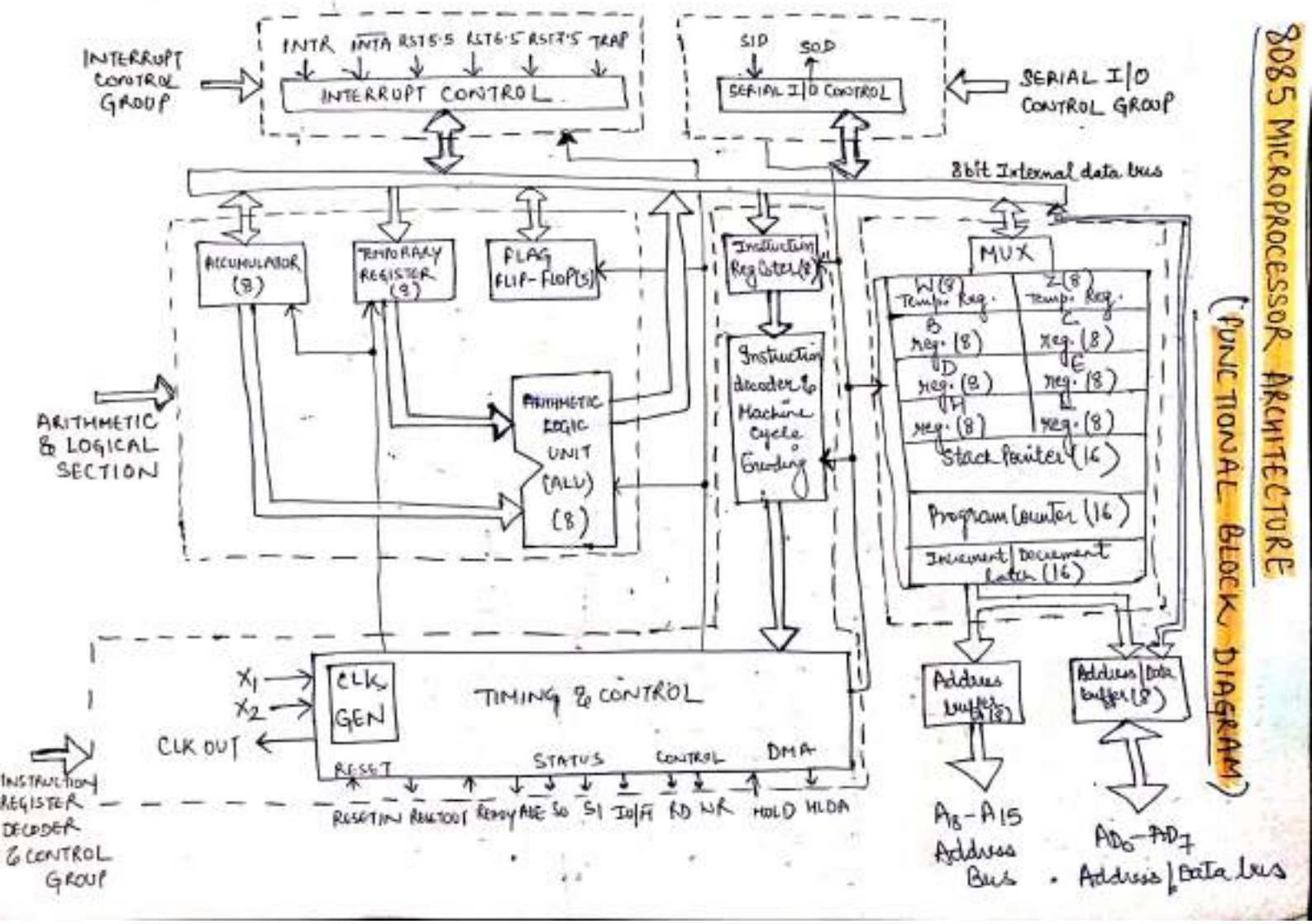
8085 MICROPROCESSOR ARCHITECTURE (FUNCTIONAL BLOCK DIAGRAM)

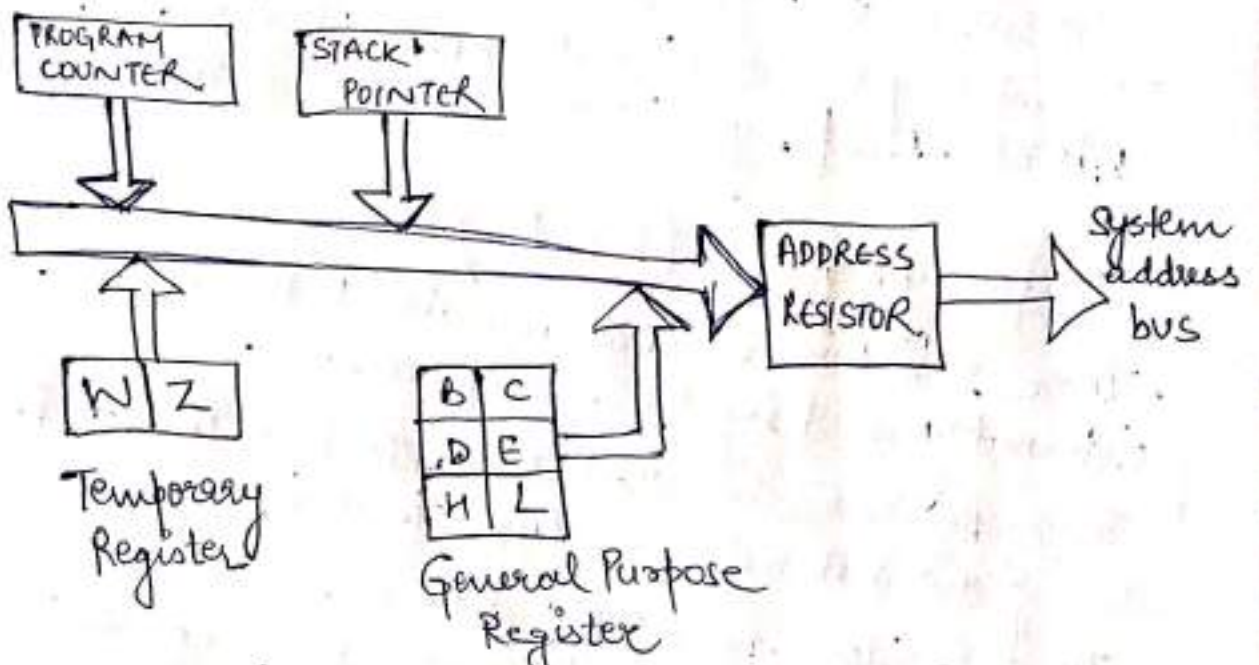


This architecture is divided in following groups:

- Register group
- Arithmetic and logical section
- Instruction Register, decoder & control gp.
- Address and Address/Data Buffers
- Interrupt control gp.
- Serial I/O control gp.

REGISTER SECTION

- It consists of PIPO ('parallel in parallel out) Registers.
- The Register contains a set of binary storage cells/flip flops with reading and writing facilities. It is used for temporary storage of instructions and data/address. Hence, the no of bits in a register is equal to data or address or instruction size depending on the application.



(REGISTER SECTION OF 8085)

The architecture of 8085 consists of following register:

a) Temporary data register.
b) Temporary registers W and Z (8 bit each)
c) 8 bit accumulator

(d) Flag Register
(e) Six General purpose Registers viz B, C, D, E, H and L
(f) 16 bit program Counter.
(g) 16 bit stack pointer.
(h) Instruction Register.

TEMPORARY REGISTERS

1) Temporary data Register
- It is also known as operand register (8 Bit). It provides operands to the ALU.
- The temporary register serve as one input to the ALU. The other input to the ALU is from the accumulator.
- Example: ADD B instruction add A register and B register contents, the result is stored in A register. The other data is available in B register. The data from B register is transfered to temporary register. Contents of A register and temporary register will be added by ALU and result is stored in Accumulator.

2) Temporary Registers (W and Z)
- These registers are not available to the users. They are internally used by the microprocessor.
- These Registers are used by control section to hold data during an arithmetic or logic operation.
- These registers hold 8 bit data each.

W and Z registers are used by 8085 for swaps instruction eg:
(i) XCHG (exchange)
This instruction swaps the contents of H and L registers with that of D and E. Hence W and Z register are used as temporary storage while swapping.
(ii) XTHL (exchange top of stack with registers H and L)

This instruction swaps the contents of H and L registers with that of the two stack top locations. Hence again W and Z registers are used as temporary storage while swapping.

GENERAL PURPOSE REGISTERS

- The 8085 contains 6 general purpose registers of 8 bits each named as B, C, D, E, H and L.
- B, C, D, E, H and L can be used to store 8 bits of data or can be used to form a register pair to store 16 bit of data. The valid register pairs available are BC, DE and HL. The user cannot form a register pair of his/her choice.
- These registers are programmable by user. These registers are available to the user. They are used to hold data, results of arithmetic and logical operations and address of data memory.
- The HL register pair functions as default data pointer. If used as data pointer memory pointer it holds the address of a 16 bit address of memory location. The L register stores the lower byte of address and the H register stores the higher byte of address.

USE OF GENERAL PURPOSE REGISTERS & HOW DO THEY INCREASE THE SPEED OF OPERATION?

- The main use is to hold data which is frequently used.
- It increases the speed of program execution. The main reason is as follows. The data in microprocessor can be stored in memory or general purpose register. If the data is present in memory the microprocessor has to perform an operation of memory read. This data is taken by microprocessor, the required operation is performed & result is stored back to memory. To store result in memory the microprocessor has to perform one more operation of memory write. Thus there are two operations involved in using memory to hold data.

SPECIAL PURPOSE REGISTERS

These registers are used for special use. The special purpose registers are:

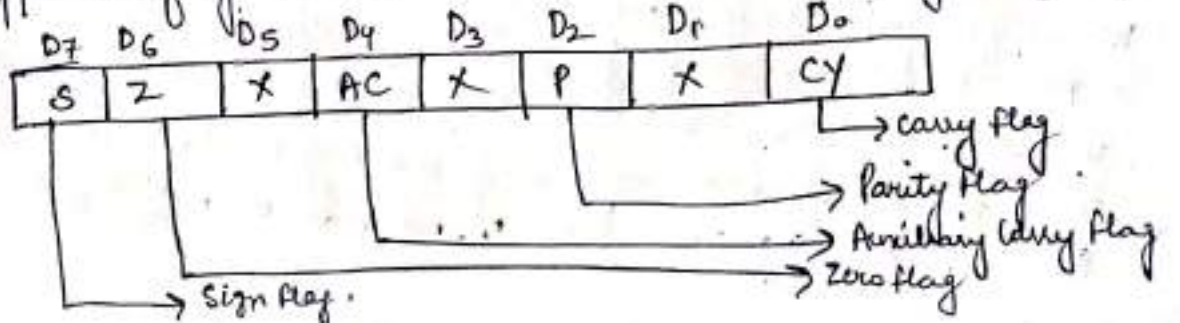
- Accumulator
- Flag Register
- Instruction Register
- Program counter
- Stack Pointer

Accumulator:

- It is an 8 bit register of 8085.
- It has some special functions and it is a special register.
- Accumulator has following special function
  (i) It has to private one of the operand, for any ALU operation.
  (ii) It has to accumulate the result of ALU operation.
  (iii) It also works as a via register for I/O accesses i.e. Whenever a data is read from input devices, it comes in accumulator & similarly O/P device gets data from accumulator.

STATUS OR FLAG REGISTER:

- A flag is a flip flop. It indicates some condition produced by the execution of an instruction. For eg:, the zero flag (ZF) will set if the result of execution of an instruction is zero.
- The flag register of 8085 microprocessor consists of five flags. The flag register is connected to ALU.
- When an operation is performed by ALU the result is transferred on internal data bus and states of result will be stored in flip flops.
- The different flags and their positions in flag register are as:



a) The Carry Flag (CF):

(i) This flag is set whenever there has been a carry out of, or a borrow into, the higher order bit of the result (8 or 16 bit).

(ii) The flag is used by the instructions that add and subtract multibyte numbers.

(iii) Rotate instructions can also isolate a bit in memory or a register by placing it in the carry flag.

1 - there is a carry out from the most significant bit

0 - no carry out from msb.

b) The Parity Flag (PF):

(i) This flag is set when the result has even parity, an even number of 1 bits.

(ii) If parity is odd, PF is resetted.

(iii) This flag is normally used to check for data transmission errors

1 - low byte has an even number of 1 bits

0 - low byte has odd parity

c) The Auxiliary Carry Flag (AF):

(i) This flag is set, whenever there has been a carry out of the lower nibble into the highest nibble or a borrow from higher nibble into lower nibble of an 8 bit quantity.

(ii) This flag is used by decimal arithmetic instructions

1 - carryout from bit 3 on addition or borrow into bit 3 on addition.

0 - Otherwise.

d) The Zero Flag (ZF):

This flag is set, when the result of operation is zero, else it is reset.

1 - zero result 0 - msb is 0 (positive)

c) The sign flag (SF):

(i) This flag is set, when MSB of the result is 1.

(ii) Since negative binary numbers are represented in the 8085 CPU in standard two's complement notation, SF indicates sign of the result

1 – msb is 1 (negative) 0 – msb is 0 (positive)

INSTRUCTION REGISTER:

- This register is not accessible to the user.
- The instruction register holds the opcode of the instruction that is decoded and executed.
- This opcode is further sent to the instruction decoder to select one of the 256 alternative (operations). The contents of the instruction decoder are in the form of 0's and 1's.

PROGRAM COUNTER (PC):

- It is used to hold the address of program memory.
- When reset is activated, the program counter is set to 0000H i.e the address of the first instruction to be fetched and executed.
- It always points to the next instruction to be fetched i.e it holds the memory address of the next instruction to be executed.

STACK POINTER (SP):

- Stack is reserved portion of memory where information can be stored or taken back under software control. This memory area is referred to as stack area.
- SP is a 16 bit register used to define the stack starting address. It always points of the top of the stack.
- It is used to keep track of data stored on stack.
- The stack pointer is decremented after each stack write operation and incremented after each stack read operation

ARITHMETIC AND LOGICAL SECTION

This section processes data i.e it performs arithmetic & logical operations.

- It performs arithmetic operations like addition, subtraction and logical operations like ANDing, ORing, EX-ORing etc
- The ALU is not available to the user. Its word length depends upon the width of an internal data bus i.e 8 bit.
- The ALU is always controlled by timing and control circuits.
- It accepts operands from accumulator and temporary register. It stores result of arithmetic and logic operations in accumulator.
- It provides status of result to the flag register.

INSTRUCTION DECODER AND MACHINE CYCLE ENCODER

This accepts a bit pattern (OPCODE) from instruction register, decodes it and gives the decoded information to control logic. It is a 8, 256 decoder.

The information includes what operation is to be performed, who is going to perform it, how many operand bytes the instruction contains etc. It means that it will understand the instruction in this block.

The decoded information is given to the Timing and control unit that provides control signals.

The 8085 executes seven types of machine cycles. The status signal gives information about which machine cycle is currently being executed.

ADDRESS BUFFER

- This is an 8 bit unidirectional buffer used for address lines.
- A buffer is used to isolate the microprocessor from getting loaded due to high current in the other peripherals connected to the microprocessor.
- These are used to drive the higher order address bus.

- When they are not in use or under certain conditions such as reset, hold, halt; this buffer is used to tri-state to address lines.

ADDRESS/DATA BUFFER

- This is an 8 bit bidirectional buffer used for address & data.
- It is used to drive the lower order address and data bus.
- Under certain condition such as reset, hold, halt this buffer is used to tri-state to address/data lines.

INCREMENTER/DECREMENTER ADDRESS LATCH

This 16 bit register is used to increment or decrement address i.e the contents of PC, HL, BC, DE and SP registers. They are also used to latch the address.

INTERRUPT CONTROL

- This block accepts different interrupt request inputs such as TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR.
- $\overline{\text{INTA}}$ is an acknowledgent pin for maskable and non-vectored interrupt.
- When a valid interrupt request is present it informs control logic to take action in response to each signal. In such a case the processor has to be interrupted in order to service the interrupt.
- The interrupt control unit job is to service the interrupt & after completion of the interrupt service routine return back the control to the main prgm where it was interrupted.

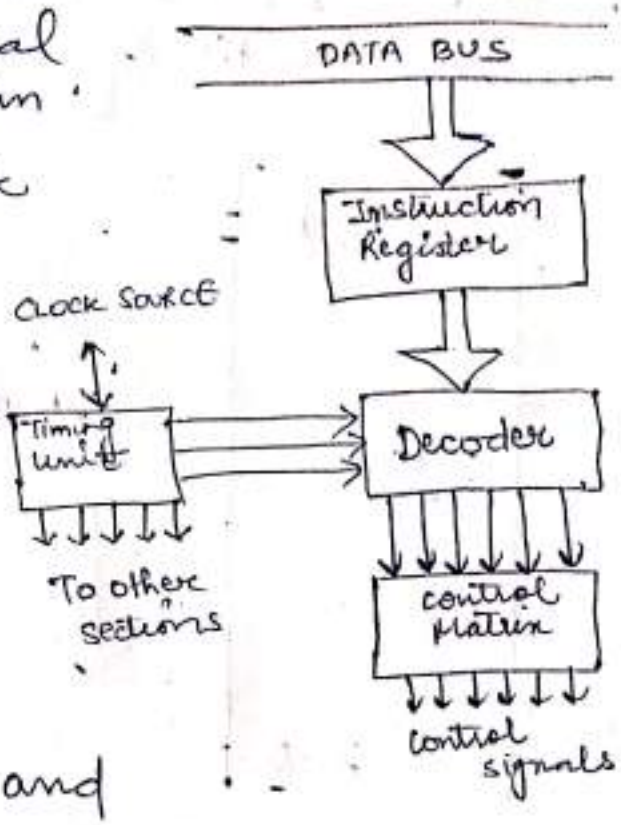
SERIAL I/O CONTROL GROUP

- The data transferred on to data bus is a parallel data, but under certain condition it is advantageous to use serial data transfer. 8085 implements this by using SID & SOD signals.

- The data on these lines is accepted or transferred under software control by serial I/O control block.
- In 8085 to perform serial data transfer there are two special instructions RIM and SIM.

TIMING AND CONTROL

- This is control section of 8085 made up of synchronous sequential logic circuit.
- It controls all internal and external circuits in the microprocessor system.
- It operates with reference to clock signal.
- It accepts information from instruction decoder and generates microsteps to perform it. In addition to this, the block accepts clock inputs, perform sequencing & synchronising operations. The synchronization is required for communication b/w microprocessor and peripheral devices.



- Figure shows the control section of microprocessor.
- The content of instruction Register are in the form of 0's and 1's. They are converted to meaningful form by the decoding network called matrices. The control matrices provide internal signals for controlling operation & data b/w registers.
- The control unit also generates timing signals essential for microprocessor to operate.
- The microprocessor uses a quartz crystal (LC or RC circuit) to determine clock frequency.
- Speed of microprocessor $\propto$ Speed of crystal.