Silicon Architects

The HDL Hackathon

Ingenium — IIT Indore

Competition Overview

Theme: Digital Design, Computer Architecture, and FPGA Prototyping

Silicon Architects is a high-performance digital design hackathon designed to test participants' understanding of logic design, processor architecture, and hardware synthesis. Unlike conventional coding hackathons, this event focuses on Hardware Description Languages such as Verilog and VHDL.

The objective of the competition is to bridge the gap between theoretical digital logic and physical FPGA implementation, encouraging participants to optimize designs for speed, power, and area.

Competition Structure

The event will be conducted in **two rounds**.

Round 1: The Soft Core Challenge (Online Qualifier)

Format: Online

Task:

Teams will be provided with a problem statement to design a specific module of a processor with integrated peripherals and a custom application to be showcased. An example includes using a RISC-V core with integrated peripherals and an application demonstration.

Submission Requirements:

- Synthesizable RTL code written in Verilog, SystemVerilog, VHDL, or C (HLS)
- Project must be packaged as a ZIP file containing a Vivado or Quartus project
- Only Vivado or Quartus design tools are supported
- Participants must validate their design using their own testbench
- Corresponding C code for peripheral integration must be validated through simulation
- A report detailing:
  - Processor architecture

- Peripheral integration
- Waveforms of simulated results

Selection:
The top 10 teams will be shortlisted to advance to Round 2.

Round 2: The Physical Implementation (On-Site Finals)

Format: Presentation with live FPGA demonstration

Hardware:
Shortlisted teams must deploy their project on an FPGA board of their choice. The selected application must be demonstrated live during the presentation.

Task:

- Synthesize and deploy the Round 1 design onto a physical FPGA
- Demonstrate real-time functionality through a live hardware setup

Judging Criteria

Criterion	Weightage	Description
Functionality	40%	Correct operation on real-time hardware and successful execution of all test cases
Resource Utilization	20%	Efficient usage of LUTs, Flip-Flops, and BRAM
Presentation	20%	Overall understanding and clarity of the project and implementation
Innovation	20%	Creativity in architecture design and application implementation

Further instructions will be communicated to shortlisted teams.