# Kartik Nagar

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| **PERSONAL PARTICULARS** | Postdoctoral Research Associate, Department of Computer Science, Purdue University, West Lafayette, Indiana, USA. Email: nagark@purdue.edu, kartik.n.nagar@gmail.com |

**EMPLOYMENT**

**Purdue University**                                          **Aug 2016 - present**
Postdoctoral Research Associate
Mentor : Suresh Jagannathan

**EDUCATION**

**Indian Institute of Science, Bangalore**          **Aug 2012 - June 2016**
**Ph.D.** Computer Science, Department of CSA, IISc.

- Thesis : Precise Analysis of Private and Shared caches for tight WCET Estimates.
- Advisor : Y.N. Srikant

**Indian Institute of Science, Bangalore**          **Aug 2010 - July 2012**
**M.E.** Computer Science, Department of CSA, IISc.

- CGPA : 7.4/8
- Thesis : Cache analysis for multi-level data caches.
- Advisor : Y.N. Srikant

**Dhirubhai Ambani Institute of Information and Communication Technology, Gandhinagar**          **Aug 2006 - July 2010**
**B.Tech.** Information and Communication Technology, DAIICT.

- CGPA : 9.94/10

**RESEARCH INTERESTS**

Program Analysis, Automated Verification, Concurrency, Distributed Systems, Real-time Systems.

**PUBLICATIONS**

**Under Submission**

- CLOTHO: Directed Test Generation for Weakly Consistent Database Systems. Kia Rahmani, Kartik Nagar, Benjamin Delaware and Suresh Jagannathan. *Submitted*

**Peer-reviewed Journal Papers**

- [**POPL**] Alone Together: Compositional Reasoning and Inference for Weak Isolation.
  Gowtham Kaki, Kartik Nagar, Mahsa Najafzadeh and Suresh Jagannathan.
  PACMPL 2(POPL) 2018.
- [**TECS**] Refining Cache Behaviour Prediction using Cache Miss Paths.
  Kartik Nagar and Y.N. Srikant.
  ACM Transactions on Embedded Computing Systems 16(4), 2017
- [**TECS**] Fast and Precise Worst Case Interference Placement for Shared Cache Analysis.

Kartik Nagar and Y.N. Srikant.
ACM Transactions on Embedded Computing Systems 15(3), 2016.

**Peer-reviewed Conference Papers**

- [**CAV**] Automated Parametrized Verification of CRDTs.
Kartik Nagar and Suresh Jagannathan.
International Conference on Computer-Aided Verification, 2019.

- [**CONCUR**] Automated Detection of Serializability Violations under Weak Consistency.
Kartik Nagar and Suresh Jagannathan.
International Conference on Concurrency Theory, 2018.

- [**VMCAI**] Path-sensitive Cache Analysis using Cache Miss Paths.
Kartik Nagar and Y.N. Srikant.
International Conference on Verification, Model Checking, and Abstract Interpretation, 2015.

- [**RTAS**] Precise Shared Cache Analysis using Optimal Interference Placement.
Kartik Nagar and Y.N. Srikant.
IEEE Real Time and Embedded Technology and Applications Symposium, 2014.

- [**MEMOCODE**] Interdependent Cache Analyses for better precision and safety.
Kartik Nagar and Y.N. Srikant.
ACM/IEEE International Conference on Formal Methods and Models for Codesign, 2012.

**PROFESSIONAL ACTIVITIES**

- PC : WCET (International Workshop on Worst Case Execution Time Analysis) 2017, 2018, 2019

- Reviewer : ESOP 18, POPL 19, PLDI 19, JACM, JSA

**TALKS**

- *Static Analysis and Automated Verification for Replicated Systems*, IIT-Delhi, Delhi, India, April 2019.

- *Static Analysis and Automated Verification for Replicated Systems*, IIT-Bombay, Mumbai, India, April 2019.

- *Automated Detection of Serializability Violations under Weak Consistency.*, International Conference on Concurrency Theory (CONCUR) 2018, Beijing, China, September 2018.

- *Path sensitive cache analysis using cache miss paths*, International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI) 2015, Mumbai, India, January 2015.

- *Precise shared cache analysis using optimal interference placement*, IEEE Real Time and Embedded Technology and Applications Symposium (RTAS), Berlin, Germany, April 2014.

- *A Comprehensive cache analysis for multi-level caches*, IMPECS-CSA Workshop on Program Analysis, Indian Institute of Science, Bangalore, September 2012.

- *Interdependent cache analyses for better precision and safety*, ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Arlington, Virginia, USA, July 2012.

**RESEARCH VISITS**

- Saarland University, Germany (hosted by Jan Reineke and Reinhard Wilhelm) Sep-Oct 2015

**AWARDS AND HONORS**

- Awarded Microsoft Research India PhD fellowship, 2013.
- Secured an all India rank of 19 in Graduate Aptitude Test in Engineering (GATE) 2010.
- Gold medal for best academic performance in B.Tech., DAIICT, Gandhinagar, 2011.

**TEACHING EXPERIENCE**

Teaching Assistant for 'Algorithms and Programming' (Aug-Dec 2014), 'Compiler Design' (Jan-Apr 2013), 'Program Analysis and Verification' (Aug-Dec 2012) at Indian Institute of Science, Bangalore.

**SKILLS**

Languages : English (fluent), Gujarati (Native), Hindi.
Programming : C, Java, C++, Z3, LLVM, LaTeX, Shell programming.

**REFERENCES**

Prof. Y. N. Srikant
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