Kartik Nagar

PERSONAL PARTICULARS
Assistant Professor,
Department of Computer Science and Engineering,
Indian Institute of Technology Madras,
Chennai, India.
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EMPLOYMENT

IIT Madras **Jan 2020 - present**
Postdoctoral Research Associate
Mentor : Suresh Jagannathan

Purdue University **Aug 2016 - Dec 2019**
Postdoctoral Research Associate
Mentor : Suresh Jagannathan

EDUCATION

Indian Institute of Science, Bangalore **Aug 2012 - June 2016**
Ph.D. Computer Science, Department of CSA, IISc.

- Thesis : Precise Analysis of Private and Shared caches for tight WCET Estimates.
- Advisor : Y.N. Srikant

Indian Institute of Science, Bangalore **Aug 2010 - July 2012**
M.E. Computer Science, Department of CSA, IISc.

- CGPA : 7.4/8
- Thesis : Cache analysis for multi-level data caches.
- Advisor : Y.N. Srikant

Dhirubhai Ambani Institute of Information and Communication Technology, Gandhinagar **Aug 2006 - July 2010**
B.Tech. Information and Communication Technology, DAIICT.

- CGPA : 9.94/10

RESEARCH INTERESTS
Formal Verification, Program Analysis, Programming Languages, Formal Methods, Concurrent and Distributed Systems, Real-time Systems.

PUBLICATIONS

Peer-reviewed Journal Papers

- [**OOPSLA**] CLOTHO: Directed Test Generation for Weakly Consistent Database Systems.
  Kia Rahmani, Kartik Nagar, Benjamin Delaware and Suresh Jagannathan. PACMPL 3(OOPSLA), 117:1-117:28, 2019.
- [**TECS**] Refining Cache Behaviour Prediction using Cache Miss Paths.
  Kartik Nagar and Y.N. Srikant.
  ACM Transactions on Embedded Computing Systems 16(4), 103:1-103:26, 2017
- [**TECS**] Fast and Precise Worst Case Interference Placement for Shared Cache Analysis.
  Kartik Nagar and Y.N. Srikant.
  ACM Transactions on Embedded Computing Systems 15(3), 45:1-45:26, 2016.

Peer-reviewed Conference Papers

- [**CAV**] Semantics, Specification and Bounded Verification of Concurrent Libraries in Replicated Systems.
  Kartik Nagar, Prasita Mukherjee and Suresh Jagannathan.
  International Conference on Computer-Aided Verification, 2020.
- [**CAV**] Automated Parametrized Verification of CRDTs.
  Kartik Nagar and Suresh Jagannathan.
  International Conference on Computer-Aided Verification, 2019.
- [**CONCUR**] Automated Detection of Serializability Violations under Weak Consistency.
  Kartik Nagar and Suresh Jagannathan.
  International Conference on Concurrency Theory, 2018.
- [**POPL**] Alone Together: Compositional Reasoning and Inference for Weak Isolation.
  Gowtham Kaki, Kartik Nagar, Mahsa Najafzadeh and Suresh Jagannathan.
  Symposium on Principles of Programming Languages, 2018.
- [**VMCAI**] Path-sensitive Cache Analysis using Cache Miss Paths.
  Kartik Nagar and Y.N. Srikant.
  International Conference on Verification, Model Checking, and Abstract Interpretation, 2015.
- [**RTAS**] Precise Shared Cache Analysis using Optimal Interference Placement.
  Kartik Nagar and Y.N. Srikant.
  IEEE Real Time and Embedded Technology and Applications Symposium, 2014.
- [**MEMOCODE**] Interdependent Cache Analyses for better precision and safety.
  Kartik Nagar and Y.N. Srikant.
  ACM/IEEE International Conference on Formal Methods and Models for Codesign, 2012.

PROFESSIONAL ACTIVITIES

- PC : WCET (International Workshop on Worst Case Execution Time Analysis) 2017, 2018, 2019
- Reviewer : ESOP 18, POPL 19, PLDI 19, Journal of ACM, Journal of Systems Architecture, IEEE Transcations on Computers, Science of Computer Programming, Journal of Logical and Algebraic Methods in Programming

TALKS

- *Semantics, Specification and Bounded Verification of Concurrent Libraries in Replicated Systems*, International Conference on Computer-Aided Verification (CAV), 2020, Online, July 2020.
- *Automated Parametrized Verification of CRDTs*, International Conference on Computer-Aided Verification (CAV), 2019, New York, USA, July 2019.
- *Automated Detection of Serializability Violations under Weak Consistency.*, International Conference on Concurrency Theory (CONCUR) 2018, Beijing, China, September 2018.
- *Path sensitive cache analysis using cache miss paths*, International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI) 2015, Mumbai, India, January 2015.
- *Precise shared cache analysis using optimal interference placement*, IEEE Real Time and Embedded Technology and Applications Symposium (RTAS), Berlin, Germany, April 2014.

- *A Comprehensive cache analysis for multi-level caches*, IMPECS-CSA Workshop on Program Analysis, Indian Institute of Science, Bangalore, September 2012.
- *Interdependent cache analyses for better precision and safety*, ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Arlington, Virginia, USA, July 2012.

AWARDS AND HONORS

- Awarded Microsoft Research India PhD fellowship, 2013.
- Secured an all India rank of 19 in Graduate Aptitude Test in Engineering (GATE) 2010.
- Gold medal for best academic performance in B.Tech., DAIICT, Gandhinagar, 2011.

SKILLS

Languages : English, Gujarati (Native), Hindi.
Programming and Tools: C, Java, C++, Z3, Dafny, Coq, LLVM, LaTeX, Shell programming.