10. FLIP-FLOPS AND RELATED DEVICES

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10.3 *R-S* Flip-Flop

A flip-flop is a bistable circuit i.e. both of its output states are stable. The circuit remains in a particular output state indefinitely until something is done to change that output status. These devices offer complementary outputs usually designated as Q and $\bar{Q}$. The R-S flip-flop is the most basic of all flip-flops. The letters 'R' and 'S' here stand for RESET and SET. When the flip-flop is SET, its Q output goes to a '1' state, and when it is RESET it goes to a '0' state. The $\bar{Q}$ output is the complement of the Q output at all times.

10.3.1 R-S *Flip-Flop with Active LOW Inputs*

Figure 10.17(a) shows a NAND gate implementation of an R-S flip-flop with active LOW inputs. The two NAND gates are cross-coupled. That is, the output of NAND 1 is fed back to one of the inputs of NAND 2, and the output of NAND 2 is fed back to one of the inputs of NAND 1. The remaining inputs of NAND 1 and NAND 2 are the S and R inputs. The outputs of NAND 1 and NAND 2 are respectively Q and $\bar{Q}$ outputs.

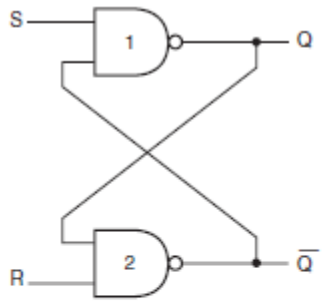
The fact that this configuration follows the function table of Fig. 10.17(c) can be explained. We will look at different entries of the function table, one at a time.

Let us take the case of R = S = 1 (the first entry in the function table). We will prove that, for R = S = 1, the Q output remains in its existing state. In the truth table, Q_n represents the existing state and Q_{n+1} represents the state of the flip-flop after it has been triggered by an appropriate pulse at the R or S input. Let us assume that Q = 0 initially. This '0' state fed back to one of the inputs of gate 2 ensures that $\bar{Q}$= 1. The '1' state of $\bar{Q}$ fed back to one of the inputs of gate 1 along with S = 1 ensures that Q = 0. Thus, R = S = 1 holds the existing state. Now, if Q was initially in the '1' state and not the '0' state, this '1' fed back to one of the inputs of gate 2 along with R = 1 forces Q to be in the '0' state. The '0' state, when fed back to one of the inputs of gate 1, ensures that Q remains in its existing state of logic '1'. Thus, whatever the state of Q, R = S = 1 holds the existing state.

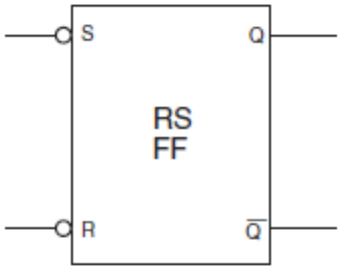
Let us now look at the second entry of the function table where S = 0 and R = 1. We can see that such an input combination forces the Q output to the '1' state. On similar lines, the input combination S = 1 and R = 0 (third entry of the truth table) forces the Q output to the '0' state. It would be interesting to analyse what happens when S = R = 0. This implies that both Q and Q outputs should go to the '1' state, as one of the inputs of a NAND gate being a logic '0' should force its output to the logic '1' state irrespective of the status of the other input. This is an undesired state as Q and $\bar{Q}$ outputs are to be the complement of each other. The input condition (i.e. R=S =0) that causes such a situation is therefore considered to be an invalid condition and is forbidden. Figure 10.17(b) shows the logic symbol of such a flip-flop. The R and S inputs here have been shown as active LOW inputs, which is obvious as this flip-flop of Fig. 10.17(a) is SET (that is, Q=1) when S =0 and RESET (that is, Q=0) when R = 0. Thus, R and S are active when LOW. The term CLEAR input is also used sometimes in place of RESET. The operation of the R-S flip-flop of Fig. 10.17(a) can be summarized as follows:

1. SET=RESET= 1 is the normal resting condition of the flip-flop. It has no effect on the output state of the flip-flop. Both Q and Q outputs remain in the logic state they were in prior to this input condition.
2. SET = 0 and RESET = 1 sets the flip-flop. Q and $\bar{Q}$ respectively go to the '1' and '0' state.
3. SET =1 and RESET =0 resets or clears the flip-flop. Q and $\bar{Q}$ respectively go to the '0' and '1' state.
4. SET = RESET = 0 is forbidden as such a condition tries to set (that is, Q = 1) and reset (that is, Q = 1) the flip-flop at the same time. To be more precise, SET and RESET inputs in the R-S flip-flop cannot be active at the same time.

The R-S flip-flop of Fig. 10.17(a) is also referred to as an R-S latch. This is because any combination at the inputs immediately manifests itself at the output as per the truth table.



(a)



(b)

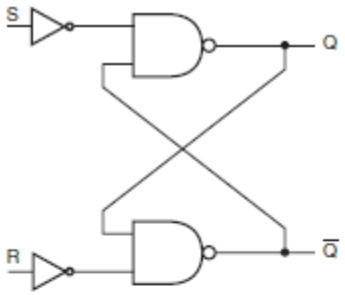
Operation Mode	S	R	Q_{n+1}
No change	1	1	Qn
SET	0	1	1
RESET	1	0	0
Forbidden	0	0	—

(c)

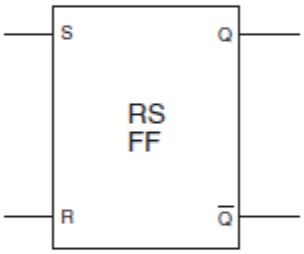
Figure 10.17 *R-S* flip-flop with active LOW inputs.

10.3.2 R-S *Flip-Flop with Active HIGH Inputs*

Figure 10.18(a) shows another NAND gate implementation of the R-S flip-flop. Figures 10.18(b) and (c) respectively show its circuit symbol and function table. Such a circuit would have active HIGH inputs. The input combination R = S = 1 would be forbidden as SET and RESET inputs in an R-S flip-flop cannot be active at the same time.



(a)



(b)

Operation Mode	S	R	Q_{n+1}
No change	0	0	Q_n
SET	1	0	1
RESET	0	1	0
Forbidden	1	1	—

(c)

Figure 10.18 *R-S* flip-flop with active HIGH inputs.

The R-S flip-flops (or latches) of Figs 10.17(a) and 10.18 (a) may also be implemented with NOR gates. The NOR gate counterparts of Fig. 10.17(a) and Fig. 10.18(a) are respectively shown in Figs 10.19(a) and (b).

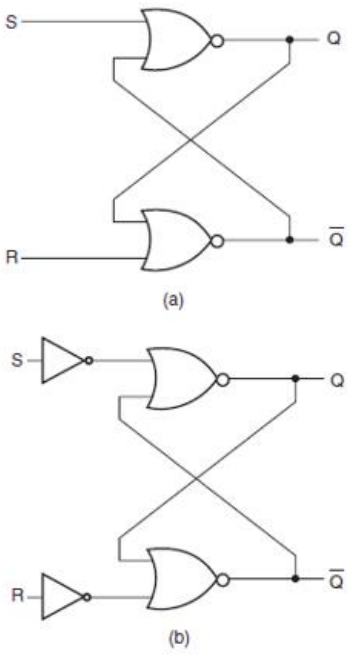


Figure 10.19 NOR implementation of an *R-S* flip-flop.

So far we have discussed the operation of an R-S flip-flop with the help of its logic diagram and the function table on lines similar to the case of combinational circuits. We do, however, appreciate that a sequential circuit would be better explained if we expressed its output (immediately after it was clocked) in terms of its present output and its inputs. The function tables of Figs 10.17(c) and 10.18(c) may be redrawn as shown in Figs 10.20(a) and (b) respectively. This new form of representation is known as the characteristic table. Having done this, we could even write simplified Boolean expressions, called characteristic equations, using any of the minimization techniques, such as Karnaugh mapping.
The K-maps for the characteristic tables of Figs 10.20(a) and (b) are given in Figs 10.20(c) and (d) respectively. Characteristic equations for R-S flip-flops with active LOW and active HIGH inputs are given by the equations

$$Q_{n+1} = \overline{S} + R.Q_n \quad \text{and} \quad S + R = 1 \qquad (10.15)$$

$$Q_{n+1} = S + \overline{R}.Q_n \quad \text{and} \quad S.R = 0 \qquad (10.16)$$

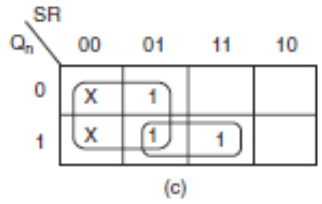
S+R=1 indicates that R=S =0 is a prohibited entry. Similarly, S.R=0 only indicates that R=S =1 is a prohibited entry.

Qn	S	R	Q_{n+1}
0	0	0	Indeter
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	Indeter
1	0	1	1
1	1	0	0
1	1	1	1

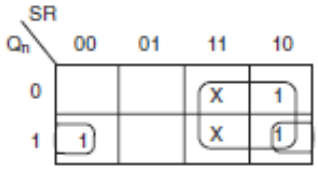
(a)

Qn	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeter
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeter

(b)



(c)

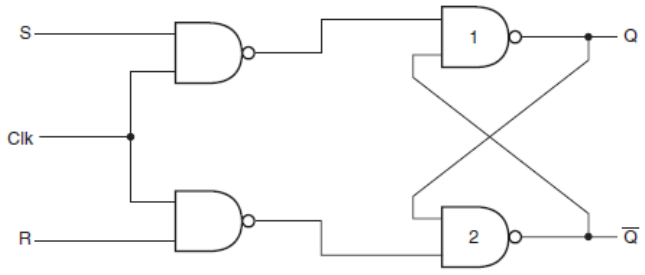


(d)

Figure 10.20 (a) Characteristic table of an *R-S* flip-flop with active LOW inputs, (b) the characteristic table of an *R-S* flip-flop with active HIGH inputs, (c) the K-map solution of an *R-S* flip-flop with active LOW inputs and (d) the K-map solution of an *R-S* flip-flop with active HIGH inputs.

10.3.3 Clocked R-S *Flip-Flop*

In the case of a clocked R-S flip-flop, or for that matter any clocked flip-flop, the outputs change states as per the inputs only on the occurrence of a clock pulse. The clocked flip-flop could be a level-triggered one or an edge-triggered one. The two types are discussed in the next section. For the time being, let us first see how the flip-flop of the previous section can be transformed into a clocked flip-flop. Figure 10.21(a) shows the logic implementation of a clocked flip-flop that has active HIGH inputs. The function table for the same is shown in Fig. 10.21(b) and is self-explanatory.

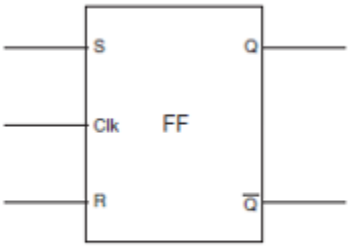


(a)

S	R	Clk	Q_{n+1}
0	0	0	Q_n
0	0	1	Q_n
0	1	0	Q_n
0	1	1	0
1	0	0	Q_n
1	0	1	1
1	1	0	Q_n
1	1	1	Invalid

(b)

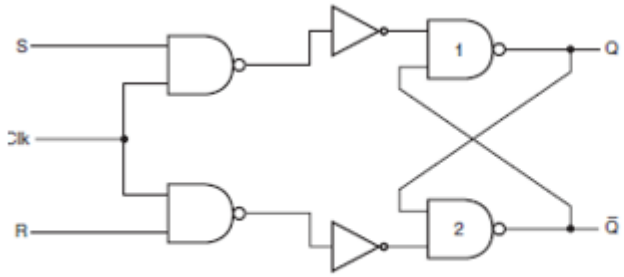
Figure 10.21 Clocked *R-S* flip-flop with active HIGH inputs.



(c)

Figure 10.21 *(continued).*

The basic flip-flop is the same as that shown in Fig. 10.17(a). The two NAND gates at the input have been used to couple the R and S inputs to the flip-flop inputs under the control of the clock signal. When the clock signal is HIGH, the two NAND gates are enabled and the S and R inputs are passed on to flip-flop inputs with their status complemented. The outputs can now change states as per the status of R and S at the flip-flop inputs. For instance, when S = 1 and R = 0 it will be passed on as 0 and 1 respectively when the clock is HIGH. When the clock is LOW, the two NAND gates produce a '1' at their outputs, irrespective of the S and R status. This produces a logic '1' at both inputs of the flip-flop, with the result that there is no effect on the output states. Figure 10.22(a) shows the clocked R-S flip-flop with active LOW R and S inputs. The logic implementation here is a modification of the basic R-S flip-flop in Fig. 10.18(a). The truth table of this flip-flop, as given in Fig. 10.22(b), is self-explanatory.

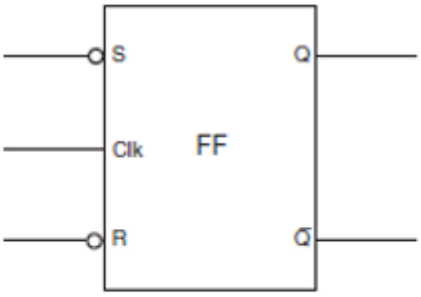


(a)

S	R	Clk	Q_{n+1}
0	0	0	Q_n
0	0	1	Invalid
0	1	0	Q_n
0	1	1	1
1	0	0	Q_n
1	0	1	0
1	1	0	Q_n
1	1	1	Q_n

(b)

Figure 10.22 Clocked *R-S* flip-flop with active LOW inputs.



(c)

Figure 10.22 *(continued).*

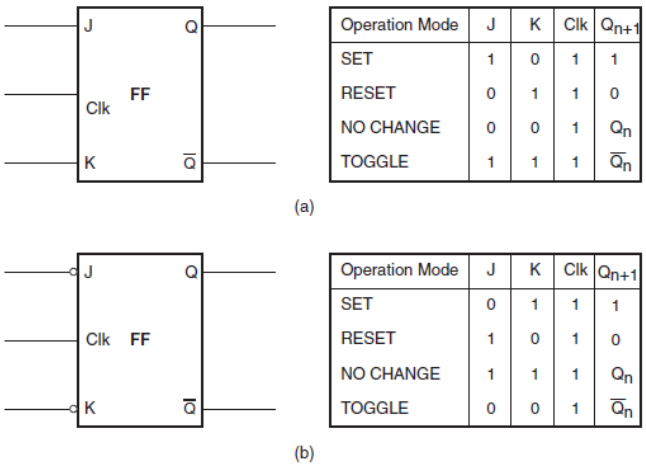
10.4 Level-Triggered and Edge-Triggered Flip-Flops

In a *level-triggered* flip-flop, the output responds to the data present at the inputs during the time the clock pulse level is HIGH (or LOW). That is, any changes at the input during the time the clock is active (HIGH or LOW) are reflected at the output as per its function table. The clocked R-S flip-flop described in the preceding paragraphs is a level-triggered flip-flop that is active when the clock is HIGH.

In an *edge-triggered* flip-flop, the output responds to the data at the inputs only on LOW-to-HIGH or HIGH-to-LOW transition of the clock signal. The flip-flop in the two cases is referred to as positive edge triggered and negative edge triggered respectively. Any changes in the input during the time the clock pulse is HIGH (or LOW) do not have any effect on the output.

10.5 *J-K* Flip-Flop

A J-K flip-flop behaves in the same fashion as an R-S flip-flop except for one of the entries in the function table. In the case of an R-S flip-flop, the input combination S = R = 1 (in the case of a flip-flop with active HIGH inputs) and the input combination S = R = 0 (in the case of a flip-flop with active LOW inputs) are prohibited. In the case of a J-K flip-flop with active HIGH inputs, the output of the flip-flop toggles, that is, it goes to the other state, for J = K = 1 . The output toggles for J = K = 0 in the case of the flip-flop having active LOW inputs. Thus, a J-K flip-flop overcomes the problem of a forbidden input combination of the R-S flip-flop. Figures 10.26(a) and (b) respectively show the circuit symbol of level-triggered J-K flip-flops with active HIGH and active LOW inputs, along with their function tables.



Operation Mode	J	K	Clk	Q_{n+1}
SET	1	0	1	1
RESET	0	1	1	0
NO CHANGE	0	0	1	Q_n
TOGGLE	1	1	1	$\overline{Q}_n$

Operation Mode	J	K	Clk	Q_{n+1}
SET	0	1	1	1
RESET	1	0	1	0
NO CHANGE	1	1	1	Q_n
TOGGLE	0	0	1	$\overline{Q}_n$

Figure 10.26 (a) *J-K* flip-flop active HIGH inputs and (b) *J-K* flip-flop active LOW inputs.

Figure 10.27 shows the realization of a J-K flip-flop with an R-S flip-flop.

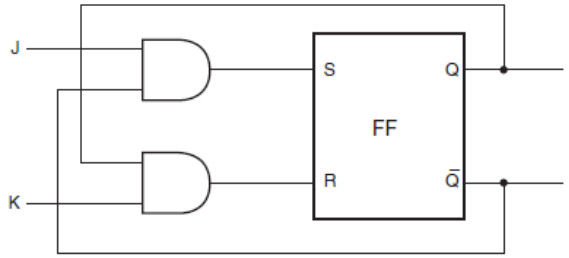


Figure 10.27 Realization of a *J-K* flip-flop using an *R-S* flip-flop.

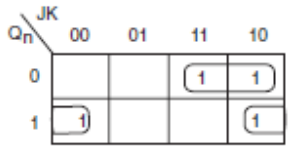
The characteristic tables for a J-K flip-flop with active HIGH J and K inputs and a J-K flip-flop with active LOW J and K inputs are respectively shown in Figs 10.28(a) and (b). The corresponding Karnaugh maps are shown in Fig. 10.28(c) for the characteristics table of Fig. 10.28(a) and in Fig. 10.28(d) for the characteristic table of Fig. 10.28(b).

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

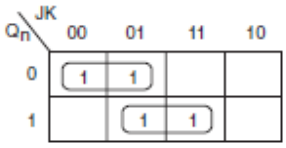
(a)

Q_n	J	K	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(b)



(c)



(d)

Figure 10.28 (a) Characteristic table of a *J-K* flip-flop with active HIGH inputs, (b) the characteristic table of a *J-K* flip-flop with active LOW inputs, (c) the K-map solution of a *J-K* flip-flop with active HIGH inputs and (d) the K-map solution of a *J-K* flip-flop with active LOW inputs.

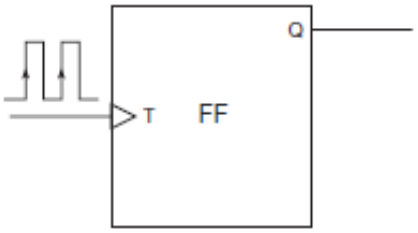
The characteristic equations for the Karnaugh maps of Figs 10.28(c) and (d) are respectively

$$Q_{n+1} = J.\overline{Q_n} + \overline{K}.Q_n \qquad (10.17)$$

$$Q_{n+1} = \overline{J}.\overline{Q_n} + K.Q_n \qquad (10.18)$$

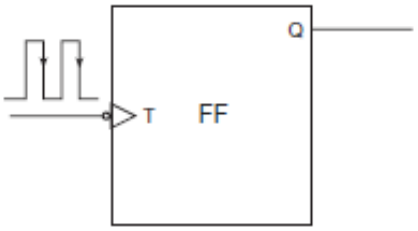
10.6 Toggle Flip-Flop (*T* Flip-Flop)

The output of a *toggle flip-flop*, also called a T flip-flop, changes state every time it is triggered at its T input, called the toggle input. That is, the output becomes '1' if it was '0' and '0' if it was '1'. Figures 10.34(a) and (b) respectively show the circuit symbols of positive edge-triggered and negative edge-triggered T flip-flops, along with their function tables.



T	Q_n	Q_{n+1}
↑	0	1
↑	1	0

(a)



T	Q_n	Q_{n+1}
↓	0	1
↓	1	0

(b)

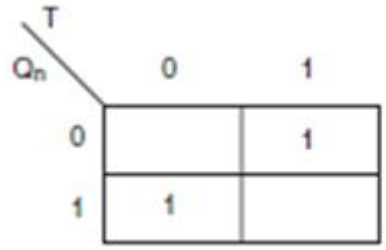
Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

(c)

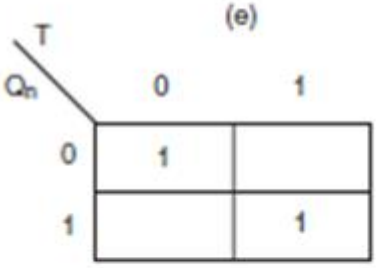
Q_n	T	Q_{n+1}
0	0	1
0	1	0
1	0	0
1	1	1

(d)

Figure 10.34 (a) Positive edge-triggered toggle flip-flop, (b) a negative edge-triggered toggle flip-flop, (c, d) characteristic tables of level-triggered toggle flip-flops and (e, f) Karnaugh maps for characteristic tables (c, d).



(e)



(f)

Figure 10.34 *(continued).*

If we consider the T input as active when HIGH, the characteristic table of such a flip-flop is shown in Fig. 10.34(c). If the T input were active when LOW, then the characteristic table would be as shown in Fig. 10.34(d). The Karnaugh maps for the characteristic tables of Figs 10.34(c) and (d) are shown in Figs 10.34(e) and (f) respectively. The characteristic equations as written from the Karnaugh maps are as follows:

$$Q_{n+1} = T.\overline{Q_n} + \overline{T}.Q_n \qquad (10.19)$$

$$Q_{n+1} = \overline{T}.\overline{Q_n} + T.Q_n \qquad (10.20)$$

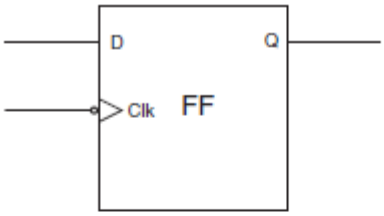
It is obvious from the operational principle of the T flip-flop that the frequency of the signal at the Q output is half the frequency of the signal applied at the T input.

10.7 *D* Flip-Flop

A D flip-flop, also called a *delay flip-flop*, can be used to provide temporary storage of one bit of information. Figure 10.39(a) shows the circuit symbol and function table of a negative edge-triggered D flip-flop. When the clock is active, the data bit (0 or 1) present at the D input is transferred to the output. In the D flip-flop of Fig. 10.39, the data transfer from D input to Q output occurs on the negative-going (HIGH-to-LOW) transition of the clock input. The D input can acquire new status when the clock is inactive, which is the time period between successive HIGH-to-LOW transitions. The D flip-flop can provide a maximum delay of one clock period.

The characteristic table and the corresponding Karnaugh map for the D flip-flop of Fig. 10.39(a) are shown in Figs 10.39(c) and (d) respectively. The characteristic equation is as follows:

$$Q_{n+1} = D \qquad (10.21)$$



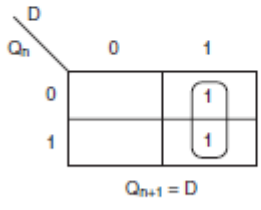
(a)

D	Clk	Q
0	↓	0
1	↓	1

(b)

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

(c)



(d)

Figure 10.39 *D* flip-flop.