UGANDA MARTYRS UNIVERSITY

UNIVERSITY EXAMINATIONS

FACULTY OF SCIENCES

DEPARTMENT OF NATURAL

SEMESTER1, 2023/24 FINAL ASSESSMENT

ELECTRONICS II

DATE : 15/12/2023

TIME : :00 - 5:00PM

DURATION: 3 Hrs

Instructions

1. *Carefully read through ALL the questions before attempting.*
2. The examination has a total of eight (8) questions. *ANSWER FIVE (5) Questions (All questions carry equal marks).*
3. *Ensure that your **Reg. number Name** and **Programme of study** are indicated on all pages of your work.*
4. *Ensure that your work is **clear** and **readable**. Untidy work will be penalized.*
5. *Any type of examination Malpractice will lead to automatic disqualification.*

Where necessary Assume:

Electron charge e	=	$1.6\times10^{-19}C$
Permittivity of free space ε_0	=	$8.85\times10^{-12}Fm^{-1}$
Speed of light in a vacuum c	=	$3.0\times10^{8}m/s$
Permeability of free space μ_0	=	$4\pi\times10^{-7}Hm^{-1}$
Boltzmann's constant κ	=	$1.4\times10^{-23}JK^{-1}$
Planck's constant h	=	$6.6\times10^{-34}JS$
Avogadro's number N_A	=	$6.02\times10^{23}(mole)^{-1}$
Universal gas constant R	=	$8.31JK^{-1}mole^{-1}$
Gravitational constant G	=	$6.67\times10^{-11}Nm^2kg^{-2}$
Electron mass m	=	$9.11\times10^{-31}kg$
Acceleration due to gravity, g	=	$9.8ms^{-2}$

Question 1

a) i) How do you understand with the term field effect transistor. (1mk)

ii) Mention the main types of field effect transistors. (1mk)

iii) Describe the major composition of junction field effect transistor. (2mks)

b) i) With aid of labeled diagram, explain the working of n- type junction field effect transistor. (5mks)

ii) Sketch an I-V out-put characteristics of n- type junction field effect transistor and indicate on it Ohmic region, pinch off line and saturation region. (3mks)

c) An n- channel JFET with saturation current $I_{DSS} = 6mA$ and pinch off voltage $V_p = -6v$ is used in the self – bias circuit of figure 1. Given that $V_{DD} = 12v$, $R_D = 1.5k\Omega$ and $R_S = 500\Omega$. Determine the operating point (determine I_D, V_{DS}, V_{GS}) (8mks)

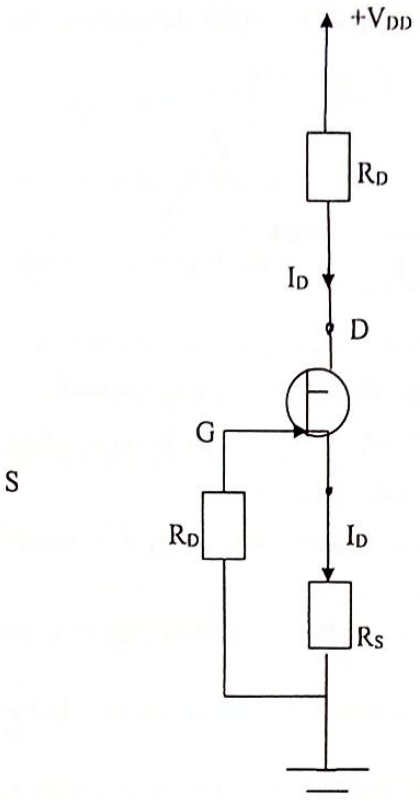


Fig. 1

Question 2

2 a) i) Distinguish between cut off and pinch off voltage. (2mks)

ii) Identify the major types of metal oxide semi-conductor field effect transistor (MOSFET) (2mks)

iii) State the common metal oxide used in MOSFET to separate the gate and the channel. (1mk)

b) i) with aid of a diagram explain the working of depletion mode MOSFET. (5mks)

ii) Sketch I-V transfer characteristic for enhancement mode n-MOSFET. (2mks)

iii) Define the term threshold voltage as applied in MOSFET. (1mk)

iv) How does the threshold voltage vary in the different MOSFET. (2mks)

c) Given that the drain current I_D of a JFET in absence of gate current is a function of V_{GS} and V_{DS},

i) Write down the changes in I_D (2mks)

ii) Suppose $\delta I_D = i_d$ $\delta V_{GS} = V_{gs}$ and $\delta V_{DS} = V_{ds}$, write the small- signal equivalent circuit equation hence define the major variables in the equation. (3mks)

Question 3

a) i) How do you understand the term resonance circuit. (1mk)

b) i) identify any two application of tuned circuit. (1mk)

ii) State the two types of resonators. (1mk)

iii) Explain how the performance of oscillator circuit can be improved. (2mks)

iv) Mention the fundamental parameter used to describe the behavior of RLC circuit. (1mk)

v) Distinguish between bandwidth and quality factor. (2mks)

c) A series RLC circuit has the following components $R = 100\Omega$, $L = 10mH$ and $C = 25nF$. Calculate the following parameters;

i) Resonance frequency. (2mks)

ii) Damping factor. (2mks)

iii) Band width. (2mks)

iv) Q- factor. (2mks)

d) The figure 2 shows a resonant circuit (2mks)

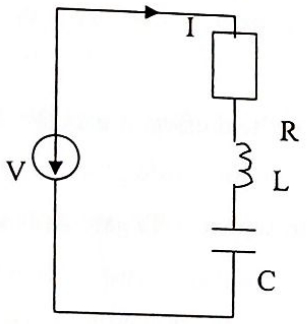


Figure 2

Determine a second order differential equation for the voltage in the circuit at any time; also determine the maximum current of the amplitude of current for the circuit. (4mks)

Question 4

a) i) what is a filter. (1mk)

ii) Distinguish the major categories of filters. (2mks)

b) i) Define the four common filters you know. (4mks)

ii) Draw the frequency response of any two of the filters defined in b (i). (4mks)

c) i) Define the term voltage transfer function. (1mk)

ii) With reference to low pass filter, derive the voltage transfer function. (3mks)

iii) A low pass filter circuit consisting of resistor of 4.7 kΩ in series with a capacitor of 47nF is connected across 10v sinusoidal supply. Calculate the output voltage and the voltage transfer function at a frequency of 100Hz. (Take $Z_C = \frac{1}{2\pi fC}$) (5mks)

Question 5

a) i) Define the term operational amplifier. (1mk)

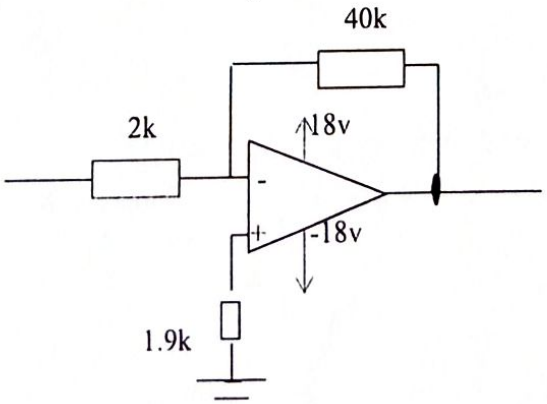
ii) Draw a well labeled circuit symbol of an operational amplifier. (3mks)

b) i) Explain the major characteristics of ideal operational amplifier. (6mks)

ii) When is an operational amplifier said to be inverting or non-inverting. (2mk)

c i) with reference to an inverting operational amplifier, show that the differential $gain = \frac{-R_F}{R_{in}}$ (3mks)

ii) Given an inverting operational amplifier below with an input voltage of 10mv, determine the differential gain and output voltage. (5mks)



Question 6

a) With aid of a labelled diagram explain the operation of a feedback circuit. (5mks)

b) i) State a major reason why positive feedback is un-desirable in amplifiers. (2mks)

ii) With reference to one application of positive feedback, demonstrate the conditions necessary for it to occur. (3mks)

c) i) With suitable equations describe a negative feedback. (2mks)

ii) State one fundamental characteristic of negative feedback amplifier. (1mk)

iii) Identify any three advantages of negative feedback in amplifiers. (3mks)

d) i) Distinguish between series and shunt- feedback circuits. (2mks)

ii) Draw a circuit diagram showing a series feedback amplifier. (2mks)

Question 7

a) i) what is a logic gate? (1mk)

ii) Name the three basic gates and draw their circuit symbol. (3mks)

iii) Explain the term truth table with the characteristics of its components. (3mks)

b) i) write down the logic equations for the following gates AND, OR, NOT. Assume two inputs A and B for the AND and OR gates. (3mks)

ii) Consider three input signals A, B and C, generate a truth table of their AND & OR gates. (5mks)

iii) Draw the truth tables for the following gates NAND, NOR and EXOR with two inputs A and B. (5mks)

Question 8

a) i) what is Boolean algebra. (1mk)

ii) State any five laws of Boolean algebra. (5mks)

iii) State how the laws mentioned in a) ii) can be proved. (2mks)

iv) Use the mentioned approaches in a) iii) above with three input signals A, B & C to prove the distributive law. (8mks)

c) Determine the simplest form of the following.

i) $F = \overline{A}B + AB + A\overline{B} + AB$ (2mks)

ii) $G = \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}C + ABC$ (2mks)