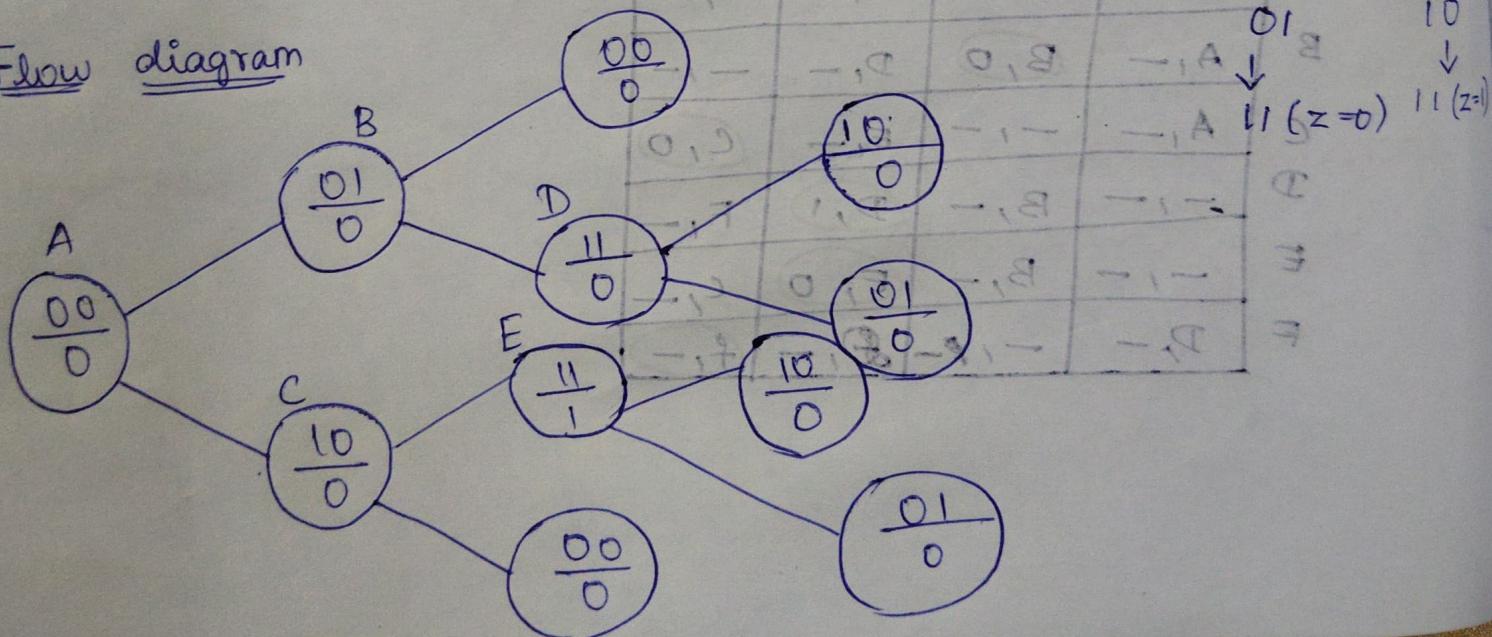


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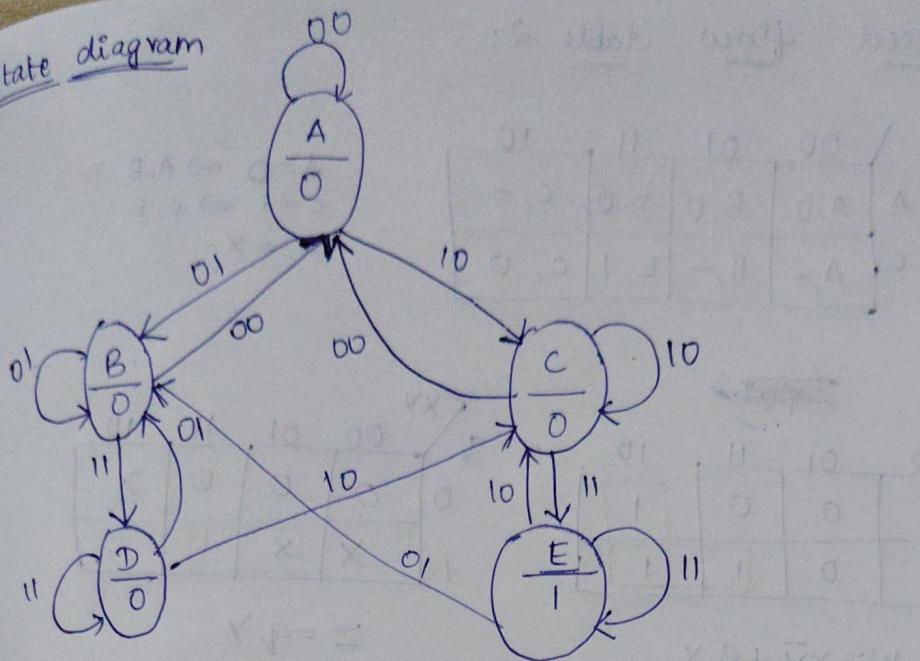
Q.B (16m)

1) Develop a circuit with 2 input x and y to give an out $z=1$ when $x \geq y$ by flow drawing, state diagram, primitive, flow table and output map in which transition state is included.

Flow diagram



state diagram



Primitive flow table:

	00	01	11	10
A	(A, 0)	B, -	-,-	C, -
B	A, -	(B, 0)	D, -	-,-
C	A, -	D, -	E, -	C, 0
D	-,-	B, -	(D, 0)	C, -
E	-,-	B, -	(E, 1)	C, -

Implication table:

	B	C	D	E
B	✓			
C	✓	✗		
D	✓	✓	✗	
E	✓	✗	✓	✗

(A, B), (A, C), (A, D), A(E), (B, D), (C, E).

Reduced flow table 1:

	00	01	11	10
A, B, D	A, 0	B, 0	D, 0	C, -
C, E.	A, -	B, -	E, 1	C, 0

Reduced flow table 2:

	00	01	11	10
A	A, D	B, D	D, 0	C, -
C	A, -	B, -	E, 1	C, 0

$A = 0 \Rightarrow A, B, D$
 $C = 1 \Rightarrow C, E$
 $- = X$.

K-map

~~Input~~:

x, y

q	00	01	11	10
0	0	0	0	1
1	0	0	1	1

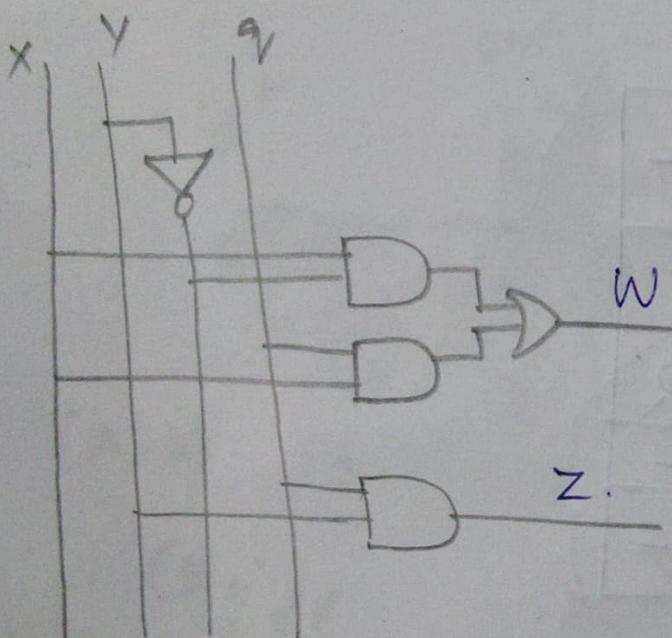
$$W = x\bar{y} + q_1x$$

x, y

q	00	01	11	10
0	0	0	0	X
1	X	X	1	0

$$Z = q_1y$$

Logic circuit



2) construct and explain the steps in designing
Asynchronous sequential circuit with suitable
example: (Refer 1 question fully). ② Q.B (16m)

4) find a static and dynamic hazard free realization for the following function using

i) NAND gate. (Q.B (1bm))

ii) NOR gate.

$$f(A, B, C, D) = \sum_m (1, 5, 7, 14, 15)$$

Using 4 variable K-map.

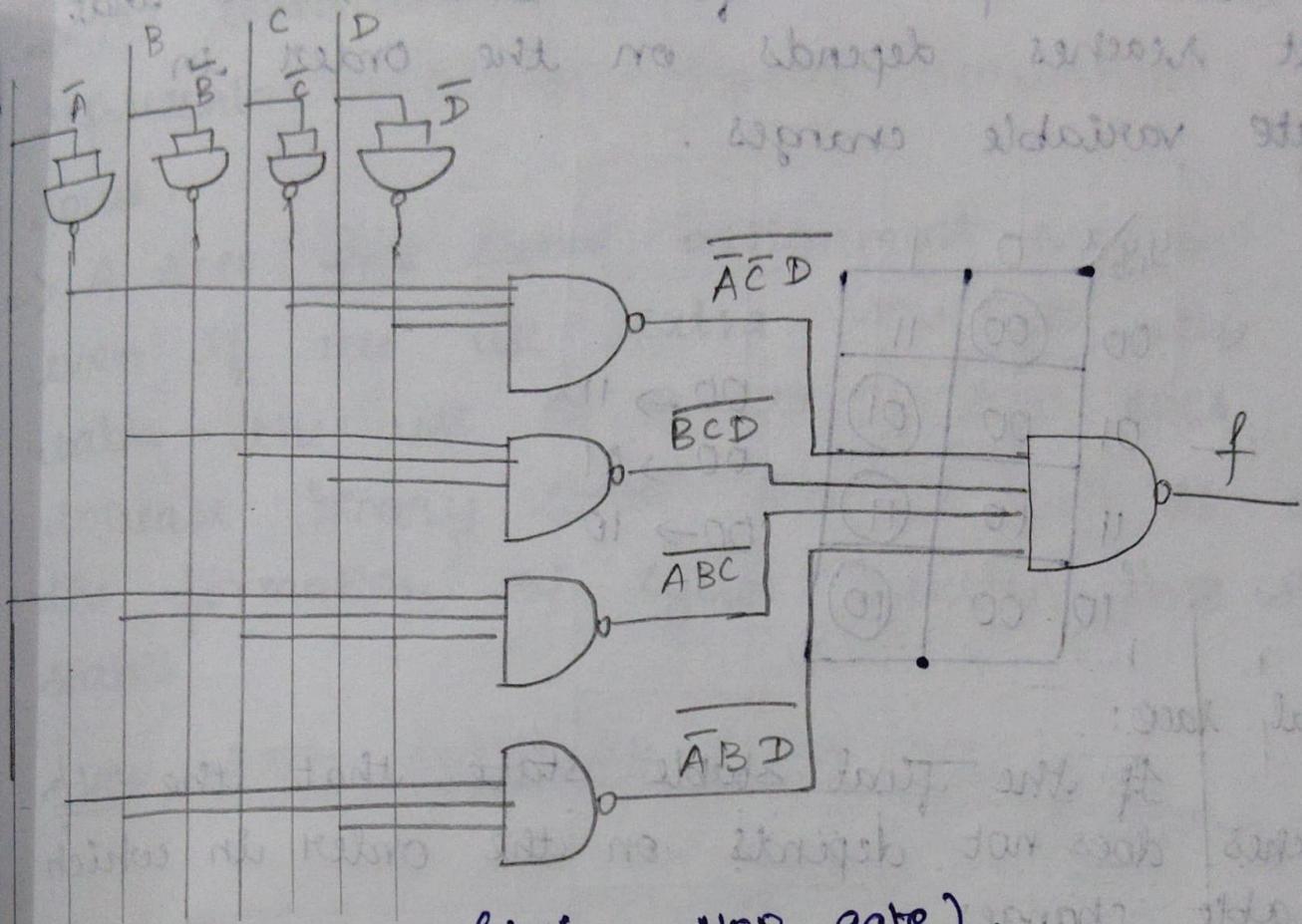
AB \ CD	00	01	11	10
00		1		
01		1	1	
11	1	1	1	1
10	1	0	1	0

$$F(A, B, C, D) = \bar{A}\bar{C}D + BCD + ABC.$$

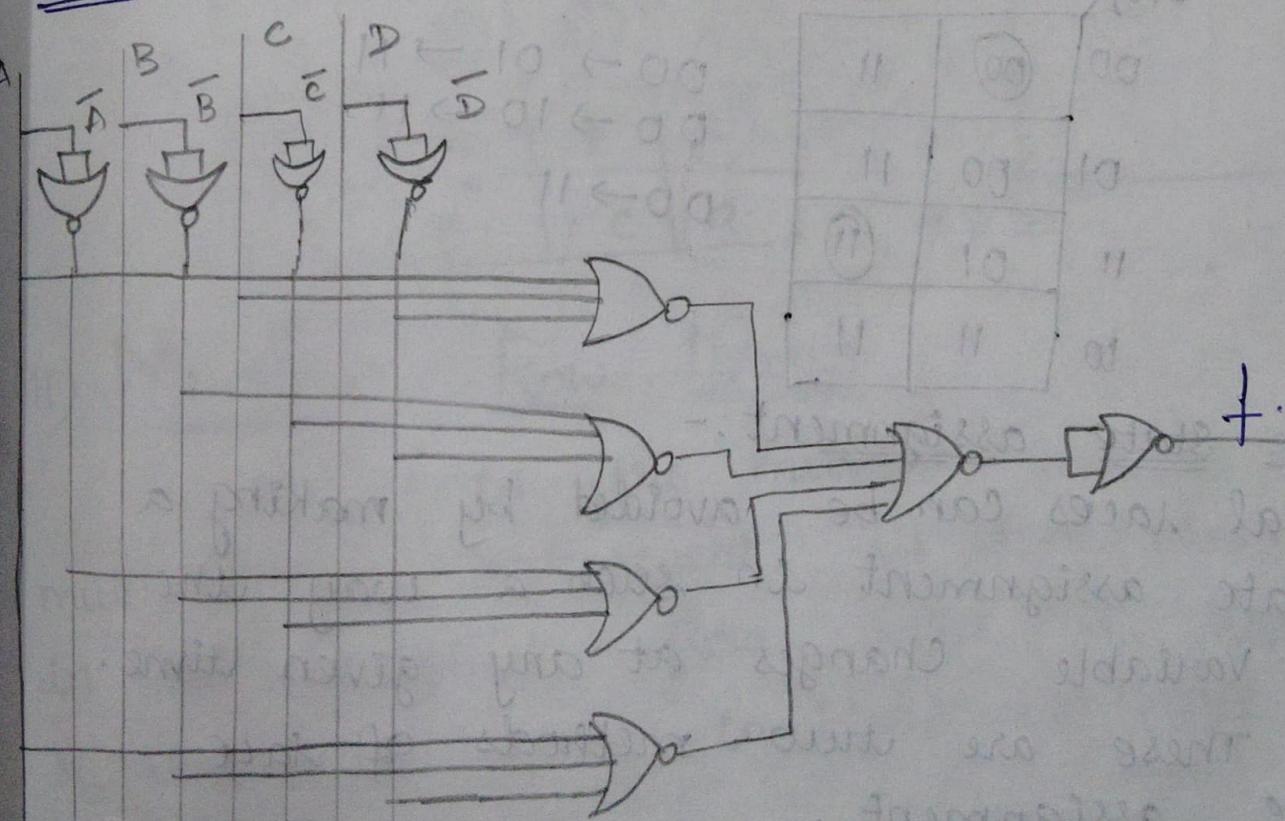
But to remove static and dynamic hazards one more term has to be, include which is shown as dotted lines in K-map.

LOGIC CIRCUIT: (using only NAND gate).

fast. 9 bits adders long with 16 → 32 bits (16 bits with no changes in both. Thus it will be faster than older one. This is due to

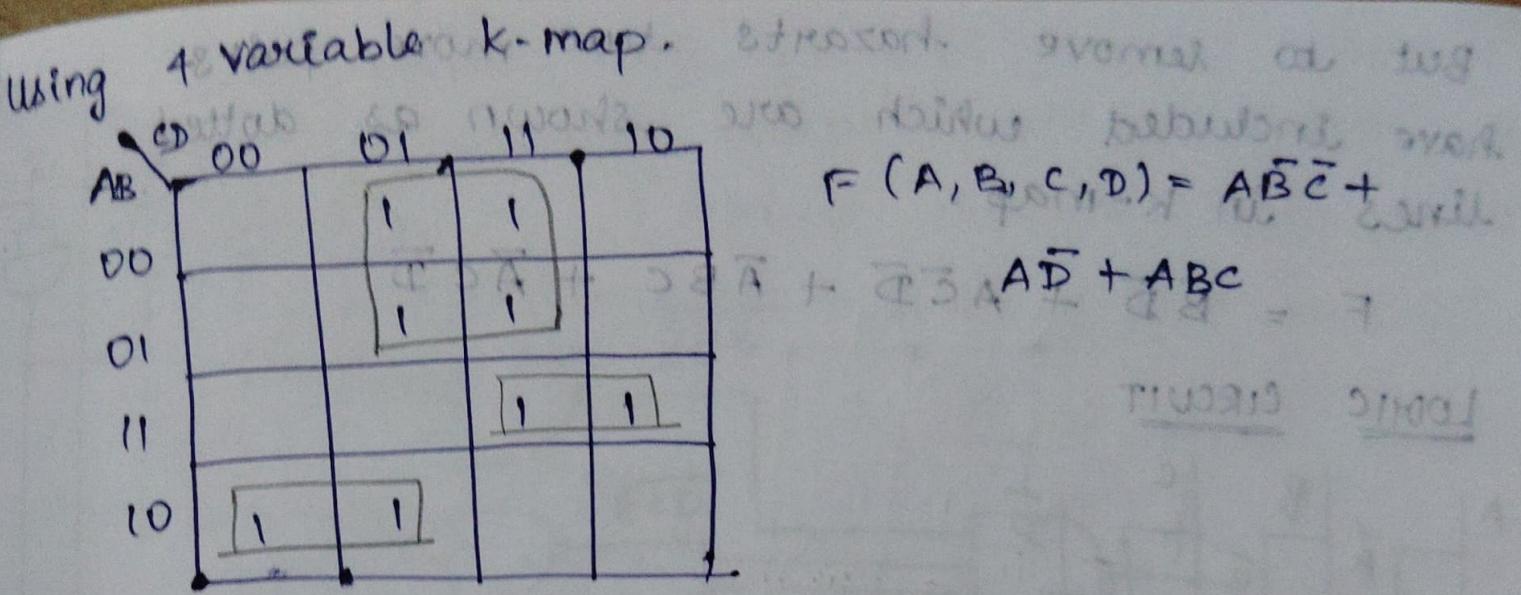


LOGIC CIRCUIT : (Using NOR gate)



2) Implement the switching function $f = \sum m_{(1, 3, 5, 7, 8, 9, 14, 15)}$ by a static hazard free 2 level and R gate net work.

(A) Q.B (16m)



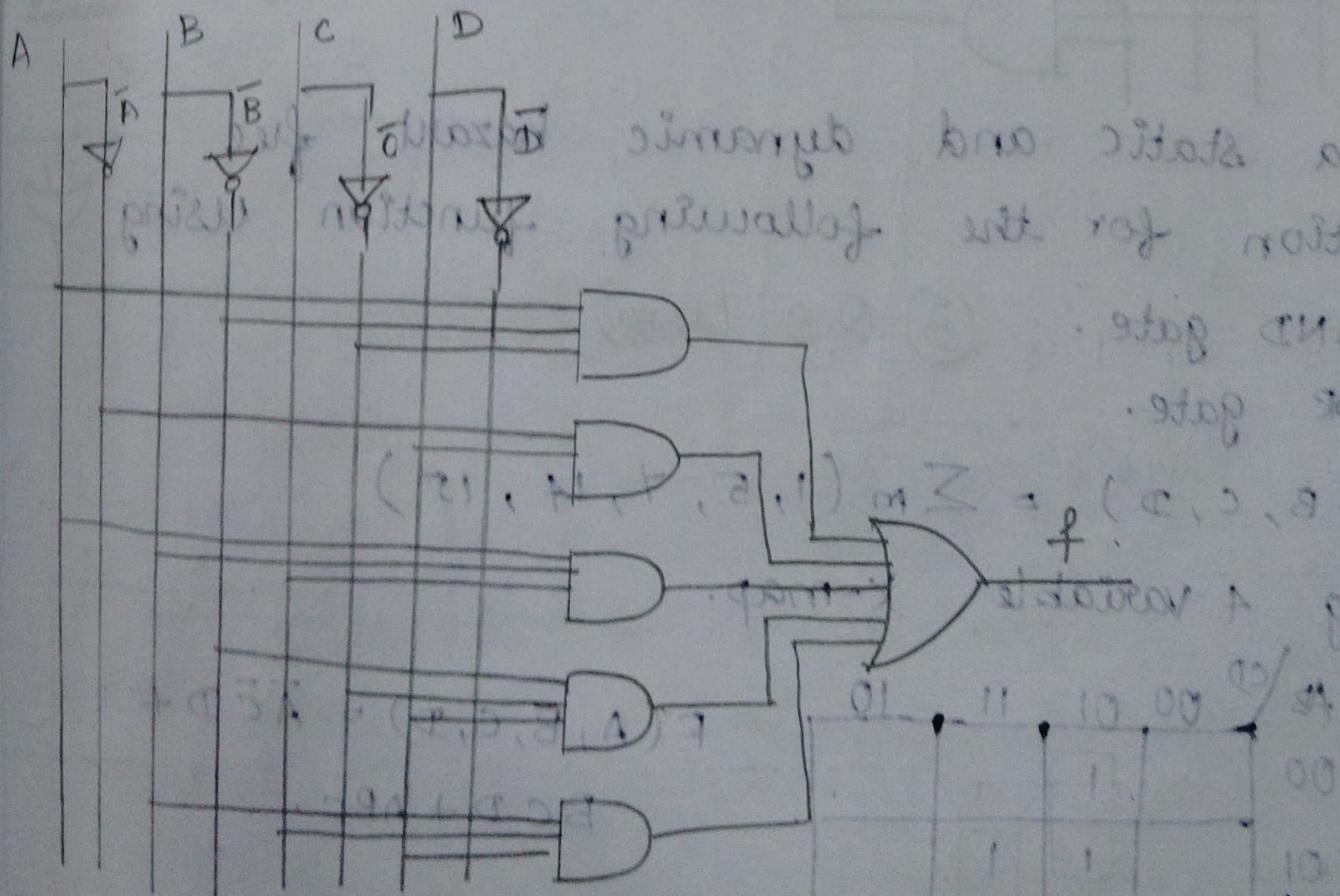
$$F(A, B, C, D) = \overline{ABC} + \overline{AD} + ABC$$

THREE GATES

But to remove hazards two more pairs have include which are shown as dotted lines in K-map.

$$F = \overline{ABC} + \overline{AD} + ABC + \overline{BC}D + BCD.$$

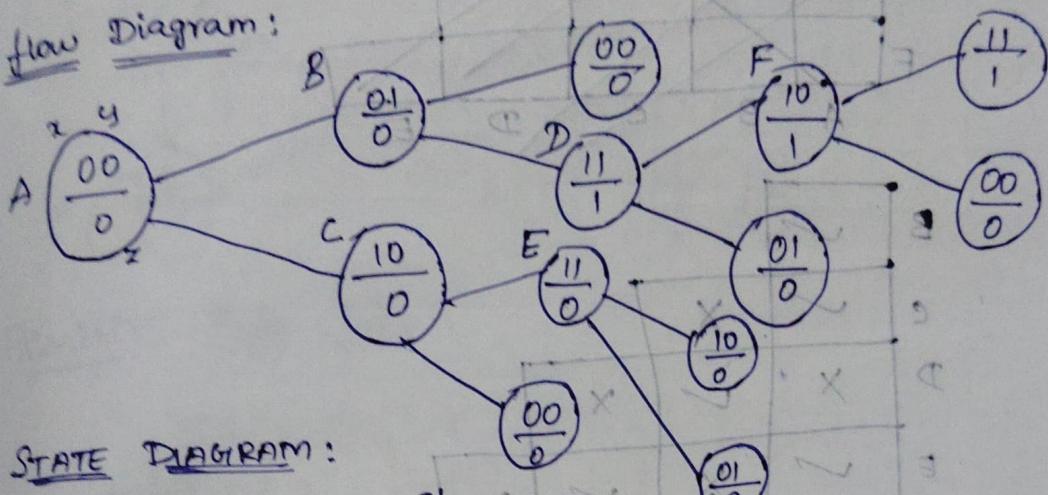
LOGIC CIRCUIT:



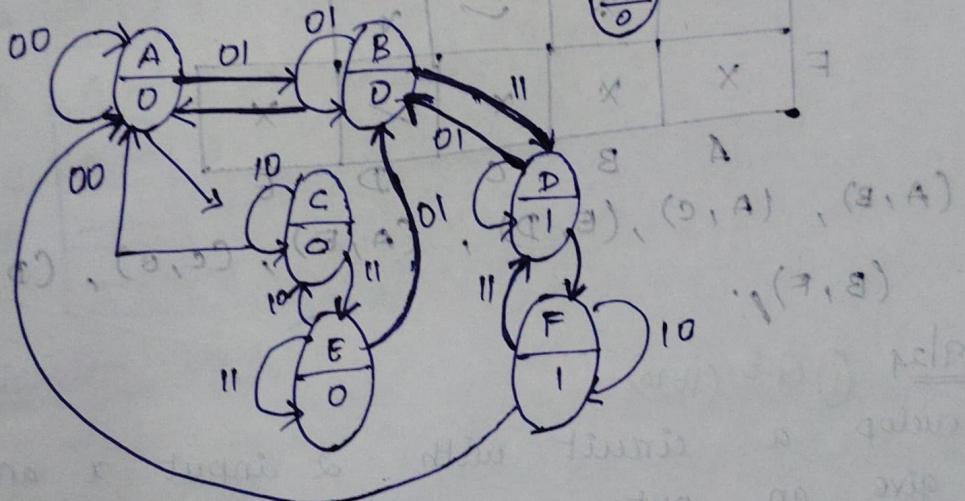
18/09/24 Q.B (16m)

Solve a circuit with 2 inputs x and y and with one output $z=1$ when x becomes 1, if y is already 1. Once $z=1$ it will remain 1 until x goes to 0. Draw the total state diagram and primitive flow table.

flow Diagram:



STATE DIAGRAM:



PRIMITIVE FLOW TABLE:

	00	01	11	10
A	(A, 0)	B, -	-, -	C, -
B	A, -	(B, 0)	D, -	-, -
C	A, -	-, -	E, -	(C, 0)
D	-, -	B, -	(D, 1)	F, -
E	-, -	B, -	(E, 0)	C, -
F	D, -	-, -	(F, 1)	-, -

Implication table:

B	X	X	X	X
C	X	X	X	X
D	X	X	X	X
E	X	X	X	X
F	X	X	X	X

B	✓	X	X	X
C	✓	X	X	X
D	X	✓	X	X
E	✓	X	✓	X
F	X	X	X	X

$(A, B), (A, C), (E, D), (A, E), (C, E), (D, F), (B, F)$

5) Built the types of races and explain race free statement with an example. (6) Q.B (1bm)

RACE CONDITION:

A race condition is said to exist in an Asynchronous sequential circuit when two or more binary state variable change value in response to change in input variable types:-

- i) Critical race
- ii) Non critical race

i) Critical race :- If the final stable state that the circuit reaches depends on the order in which state variable changes.

y_1, y_2	0	1
00	(00)	11
01	00	(01)
11	10	(11)
10	00	(10)

$$\begin{aligned} 00 &\rightarrow 11 \\ 00 &\rightarrow 01 \\ 00 &\rightarrow 10 \end{aligned}$$

ii) Non-Critical race:

If the final stable state that the circuit reaches does not depend on the order in which state variable changes (up to 9th point) : THUS913 31100

y_1, y_2	0	1
00	(00)	11
01	00	11
11	01	(11)
10	11	11

$$\begin{aligned} 00 &\rightarrow 01 \rightarrow 11 \\ 00 &\rightarrow 10 \rightarrow 11 \\ 00 &\rightarrow 11 \end{aligned}$$

Race free state assignment:-

Critical races can be avoided by making a binary state assignment in such a way that only one variable changes at any given time.

These are two methods of race free state assignment.

i) Shared row method.

ii) Multiple row method.

i) SHARED Row METHOD

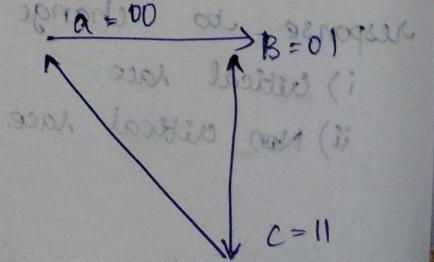
The assignment of a single binary variable into a flow table with two rows which does not cause critical race problem.

Three row flow table

	00	01	11	10 $\leftarrow x_1, x_2$
A	(A)	B	(A)	c
B	c	(B)	A	(B)
c	(C)	A	(C)	B

flow diagram

Transition Diagram

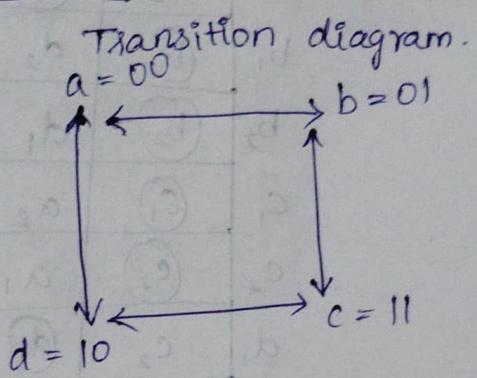


⇒ The transition diagram is the pictorial representation of all required transition between rows.

⇒ A race free state assignment can be obtained even if we use extra row to the flow table. The use of an extra row does not increase binary state variable but it allows the formation of cycles between two stable states.

Flow table with an extra row :-

a	@	b	c	@
b	c	(b)	(b)	d
c	(c)	a	b	(c)
d	b	(d)	c	a



ii) MULTIPLE Row METHOD :

In the multiple row method multiple row assignment is done each state in the original flow table is replaced by two or more combinational off state variable.

⇒ The state assignment map shows a multiple row assignment that can be done with any number of rows in a flow table.

⇒ There are two binary state variables for each table state being the logical complement of each others.

Binary assignment :-

	00	01	11	10
0	a ₁	b ₁	c ₁	d ₁
1	c ₂	d ₂	a ₂	b ₂

Flow table :

	00	01	11	10
a ₁	b ₁	a ₁	d ₁	a ₁
a ₂	b ₂	a ₂	d ₂	a ₂
b ₁	b	d ₂	b	a ₁
b ₂	b ₂	d ₁	b ₂	a ₂
c ₁	c ₁	a ₂	b ₁	c ₁
c ₂	c ₂	a ₁	c ₂	b ₁
d ₁	c ₂	d ₁	a ₂	d ₁
d ₂	b ₁	d ₂	a ₁	d ₂

000

100

001

101

010

110

011

111

In a multiple row assignment the change from one stable state to another will always cause a change of only one binary state variable. Each table state has two binary assignment with Exactly the same output at any given time only one of the assignment is in else.

3) Draw a circuit that has NO static hazard
and implement the boolean function. 7 Q.B (8m)

$$f(A, B, C, D) = \sum (0, 2, 6, 7, 8, 10, 12)$$

AB\CD	00	01	11	10
00	1			1
01			1	1
11	1			
10	1			1

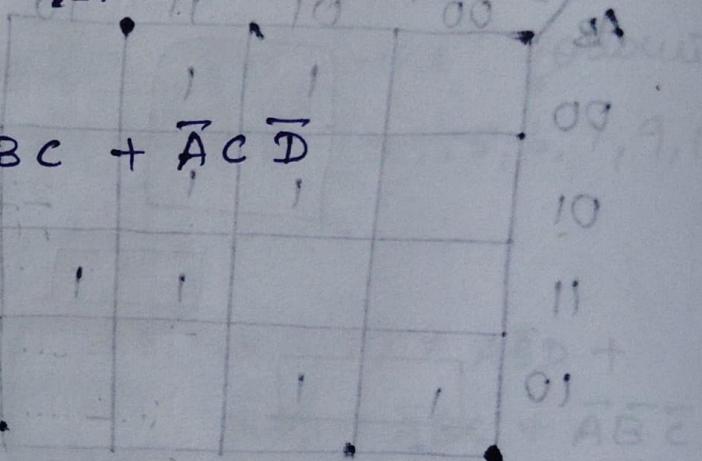
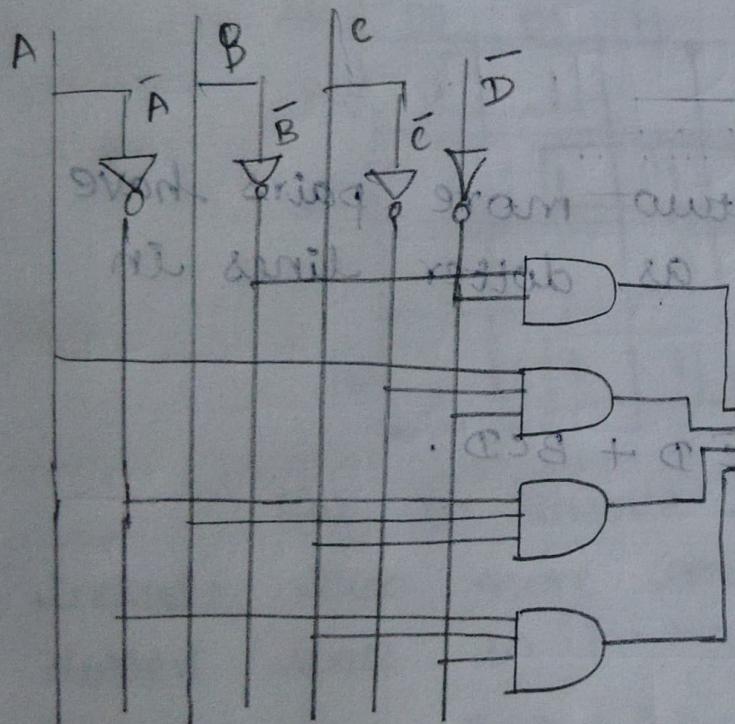
$$F(A, B, C, D) = \overline{BD} + \overline{AD}$$

$$A \overline{C} \overline{D} + \overline{ABC}$$

But to remove hazards two more pairs have included which are shown as dotted lines in K-map.

$$F = \overline{B}\overline{D} + A\overline{C}\overline{D} + \overline{A}BC + \overline{A}C\overline{D}$$

LOGIC CIRCUIT



$$f = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C} + A\overline{B}C + AB\overline{C} + ABC$$

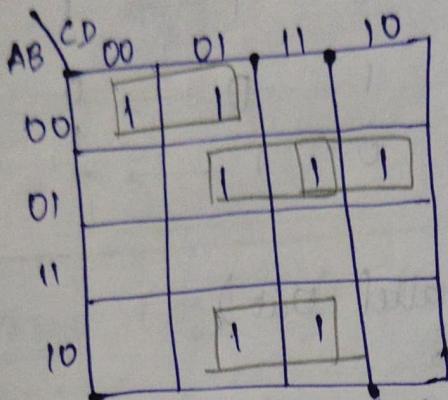
LOGIC CIRCUIT

UNIT CIRCUIT

A SYNCHRONOUS SEQUENTIAL

1) Give hazard free realisation for the following boolean function $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 9, 11)$ Q.B (8m)

K-map:



$$F(A, B, C, D) = A\bar{B}D + \bar{A}BD + \bar{A}BC + \bar{A}\bar{B}C$$

But to remove hazards we have to include two more terms that are shown as dotted lines in K-map.

$$= A\bar{B}D + \bar{A}BD + \bar{ABC} + \bar{ABC} + \bar{AC}D + \bar{BC}D$$

LOGIC CIRCUIT:

