Department of Computer Science and Engineering			
23CS404 - COMPUTER ARCHITECTURE			
Second Year / Fourth Semester			
Unit I			
QNo	**Questions**	**COs**	**Bloom's Level**
PART - A			
1	Define computer architecture.	CO1	K1
2	Define computer organization.	CO1	K1
3	Define RISC and CISC.	CO1	K1
4	Define MIPS.	CO1	K1
5	What are the components of a computer?	CO1	K1
6	What are the functions of control unit?	CO1	K1
7	Define MAR and MDR.	CO1	K1
8	What is program counter and instruction register?	CO1	K1
9	Compare clock cycle and clock period.	CO1	K2
10	How performance is measured in computing.	CO1	K1
11	Write the formula for CPU execution time for a program. .	CO1	K1
12	Define CPI (Cycles Per Instruction).	CO1	K2
13	What is a computer instruction?	CO1	K1
14	State the various types of operations required for instructions?	CO1	K1
15	Name various registers available in MIPS.	CO1	K1
16	Define instruction format.	CO1	K1
17	Write MIPS code for the given C code. if (i == j) f = g + h; else f = g – h	CO1	K1
18	Define addressing modes and list its types.	CO1	K1
19	Compare register and immediate addressing mode.	CO1	K2
20	State the use of offset in base or displacement addressing mode.	CO1	K1
Part – B			
1	Explain the various components of computer system with neat diagram.	CO1	K2
2	Explain in detail about the basic operational concepts of a computer.	CO1	K2
3	Explain various instruction formats and illustrate the same with an example.	CO1	K2
4	Explain the various control operations available in MIPS and explain the instructions supporting the control operations?	CO1	K2
5	What are the various logical operations in MIPS and explain the instructions supporting the logical operations?	CO1	K2

6	Explain in detail about addressing modes with an example.	CO1	K2
7	Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. a) Which processor has the highest performance expresses in instructions per second? (7) b) If the processors each execute a program in 10 seconds. Find the number of cycles and the number of instructions in each processor. (8)	CO1	K3

8	Translate the following C code to MIPS assemble code. Use a minimum number of instructions. Assume that i and k correspond to registers $s3 and $s5 and the base of the array save in $s6.
	While (save[i] == k)
	i+=1;
		CO1	K3

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UNIT II

QNo	Questions	COs	Bloom's Level
	PART - A		
1	Define half adder.	CO2	K1
2	Define full adder.	CO2	K1
3	Draw 4-bit full ripple carry adder.	CO2	K2
4	How subtraction happens using adder?	CO2	K1
5	Differentiate carry and overflow.	CO2	K2
6	What is Booth's algorithm?	CO2	K1
7	Define division.	CO2	K1
8	What is divide overflow?	CO2	K1
9	Add 6_{10} to 7_{10} in binary.	CO2	K1
10	Subtract 6_{10} from 7_{10} in binary.	CO2	K1
11	Multiply 100010_2 **x** 100110_2	CO2	K1
12	Divide $(1001010)_2 \div (1000)_2$.	CO2	K1
13	Explain about the floating point number.	CO2	K2
14	Give the representation of single precision floating point number.	CO2	K1
15	Give the representation of double precision floating point number.	CO2	K1
16	Write 82.125_{10} in single and double precision format.	CO2	K1
17	What is floating point normalization?	CO2	K1
18	State the purpose of guard bits used in floating point arithmetic.	CO2	K1
19	What are the ways to truncate the guard bits?	CO2	K1
20	Define overflow and underflow with examples	CO2	K1
	Part – B		
1	Explain the design of ALU in detail.	CO2	K2
2	Explain with an example how to multiply two unsigned binary numbers.	CO2	K2
3	Explain with an example how to multiply two signed binary numbers.	CO2	K2
4	Explain the algorithm for restoring integer division with suitable example.	CO2	K2
5	Explain the algorithm for non-restoring integer division with suitable example.	CO2	K2

6	Explain with an algorithm how to do addition and subtraction of two floating-point binary numbers.	CO2	K2
7	Describe in detail about Booth's multiplication algorithm and perform the booth's operation for the 5-bit signed operand, -12 is the multiplicand, and it's multiplied by –11 the multiplier.	CO2	K3
8	Mr. John has been assigned a project by his team leader in ALS Technologies. His project is to design an algorithm for 2's complement division using addition and subtraction operations. Help Mr. John is in designing an algorithm by sketching the flowchart for non-restoring division and also check the working of it with the following numbers: 24÷4	CO2	K3

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UNIT III

QNo	Questions	COs	Bloom's Level
	PART - A		
1	Define data path in the processor unit.	CO3	K1
2	List seven single-bit and one two-bit control lines present in control unit.	CO3	K1
3	Name any two signals and write its effects.	CO3	K1
4	Define pipelining.	CO3	K1
5	What is pipeline bubble?	CO3	K1
6	What is the advantage of using a pipeline?	CO3	K1
7	Define pipeline speedup.	CO3	K1
8	What is a hazard and list its types?	CO3	K1
9	Define structural hazards.	CO3	K1
10	What is data hazard?	CO3	K1
11	What is control hazard?	CO3	K1
12	What is branch target address?	CO3	K1
13	What do you mean by branch penalty?	CO3	K1
14	What is branch folding?	CO3	K1
15	What do you mean by delayed branching?	CO3	K1
16	What are the two types of branch prediction?	CO3	K1
17	Why branch prediction algorithm needed?	CO3	K1
18	What is an interrupt?	CO3	K1
19	What is meant by vectored interrupt?	CO3	K1
20	What is precise exception?	CO3	K1
	Part – B		
1	Explain the basic MIPS implementation with necessary diagrams.	CO3	K2
2	Explain in detail about building a data path for various instructions.	CO3	K2
3	Explain in detail about designing a control unit for MIPS.	CO3	K2
4	Explain in detail about five stage pipelining. Also write its advantage and disadvantage.	CO3	K2
5	Explain in detail about the methods for dealing with the data hazards.	CO3	K2

6	Explain the techniques for handling control hazards in pipelining.	CO3	K2
7	A pipelined processor uses the delayed branch technique. You are asked to recommend one of two possibilities for the design of the processor. In the first possibility, the processor has a 4-stage pipeline and one delay slot, and in the second possibility it has a 6-stage pipeline with two delay slots. Assume that 20% of the instructions are branch instructions and that an optimizing compiler succeeds in filling 80% of the single delay slot. For the second alternative, the compiler is able to fill the second slot 25% of the time.	CO3	K3
8	Find out the hazards in the following instructions and eliminate them by using stalls: LW R_1 , 0(R_2) SUB R_4 , R_1 , R_5 AND R_6 , R_1 , R_7 OR R_8 , R_1 , R_9	CO3	K3

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UNIT IV

QNo	Questions	COs	Bloom's Level
	PART - A		
1	What is principle of locality?	CO4	K1
2	What is locality of reference?	CO4	K1
3	Define the term memory latency.	CO4	K1
4	What is the need to implement memory as hierarchy?	CO4	K1
5	What is cache memory?	CO4	K1
6	Why is cache memory faster than main memory?	CO4	K1
7	Define hit and miss in cache.	CO4	K1
8	What are the methods used to reduce cache misses?	CO4	K1
9	Define write through.	CO4	K1
10	Define write buffer.	CO4	K1
11	What is write-back?	CO4	K1
12	What is direct mapped cache?	CO4	K1
13	What is virtual memory?	CO4	K1
14	Compare memory mapped I/O and I/O mapped I/O.	CO4	K2
15	What is the purpose of dirty/modified bit in cache memory?	CO4	K1
16	What is Small Computer System Interface (SCSI)?	CO4	K1
17	What is a Universal Serial Bus (USB)?	CO4	K1
18	How does a parallel bus differ from a serial bus?	CO4	K1
19	How does a processor handle an interrupt?	CO4	K1
20	Define vectored interrupts.	CO4	K1
	Part – B		
1	Explain in detail about memory technologies.	CO4	K2
2	Explain the basic operations of cache memory in detail with diagram.	CO4	K2
3	Explain the virtual memory address translation and TLB with necessary diagram.	CO4	K2
4	Explain in detail about parallel and serial bus architectures.	CO4	K2
5	Explain in detail about internal communication methodologies	CO4	K2
6	Explain the design of a typical input and output interface.	CO4	K2

7	Consider a system, which transfers 2MB file from memory to pen drive. i) If memory is using handshaking protocol to send the file, depict clearly how the data transfer takes place in case of source initiated and destination-initiated data transfer. (7) ii) When the file is being transferred there should be minimal intervention of the processor. Suggest a suitable technique for the above operation and explain it with proper justification and diagrams. (8)	CO4	K3
8	Consider a cache of 256 blocks in size, each block has 2^4 words. The main memory size is 2^{12} blocks, each block has 2^4 words. How many bits are required for each of the TAG, SET/BLOCK and WORD FIELDS for different mapping techniques? Wherever needed assume that there are 8 ways in each set.	CO4	K3

UNIT V

QNo	Questions	COs	Bloom's Level
	PART - A		
1	Name two major challenges in parallel processing.	CO5	K1
2	How does Amdahl's Law impact the speedup of parallel programs?	CO5	K1
3	What is load balancing in parallel computing, and why is it important?	CO5	K1
4	What is the main goal of hardware multithreading?	CO5	K1
5	How does fine-grained multithreading differ from coarse-grained multithreading?	CO5	K1
6	What is the advantage of simultaneous multithreading (SMT)?	CO5	K1
7	What is the primary advantage of multicore processors over single-core processors?	CO5	K1
8	How do shared memory multiprocessors communicate between cores?	CO5	K1
9	What is cache coherence in shared memory multiprocessors?	CO5	K1
10	What is a multiprocessor network topology?	CO5	K1
11	How does a GPU differ from a CPU in terms of architecture?	CO6	K1
12	What is the purpose of CUDA in GPU programming?	CO6	K1
13	Why are GPUs well-suited for parallel computing tasks?	CO6	K1
14	What is the role of shaders in a GPU?	CO6	K1
15	What is the role of parallelism in GPU computing?	CO6	K1
16	What is the main purpose of a computer cluster?	CO6	K1
17	What is the main difference between a cluster and a warehouse-scale computer?	CO6	K1
18	Why is load balancing important in cluster computing?	CO6	K1
19	Name one key challenge in managing warehouse-scale computers.	CO6	K1
20	What type of network interconnect is commonly used in cluster computing.	CO6	K1
	Part – B		
1	Explain in detail about hardware multithreading.	CO5	K2
2	Explain about the motivation of multi-core computing.	CO5	K2
3	Explain about shared memory multiprocessors.	CO5	K2
4	Explain about the multiprocessor network topologies.	CO5	K2

5	Explain in detail about Graphics Processing Units.	CO6	K2
6	Explain in detail about cluster computing.	CO6	K2
7	Explain in detail about warehouse scale computers.	CO6	K2
8	Compare and contrast clusters and warehouse-scale computers.	CO6	K2

Course Coordinator **HOD** **CHIEF AUDITOR**