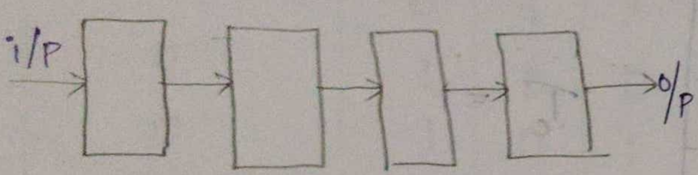
3) Analyse different types of shift register in detail using suitable diagram. (16 m) Q.P (1)

REGISTERS: A collection of flip flop is called registers. The register which performes the data moment operation is know shift register. The register that moves the binary information from one flip flop to its neighbouring flip flop depending upon the clock pluse.

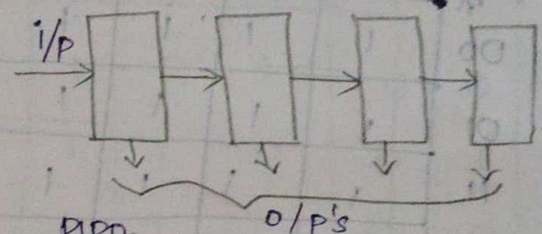
TYPES OF REGISTERS:

i) Serial in serial out. (SISO)
ii) Serial in parallel out (SIPO)
iii) parallel in serial out (PISO)
iv) parallel in parallel out (PIOP)

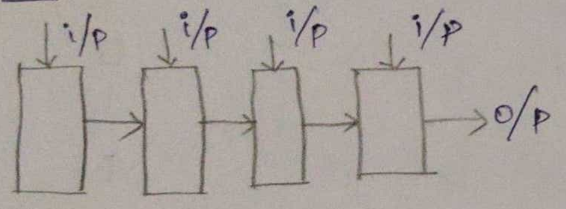
SISO



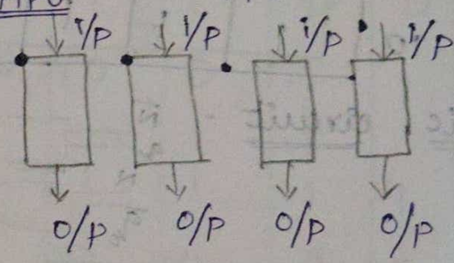
SIPO



PISO

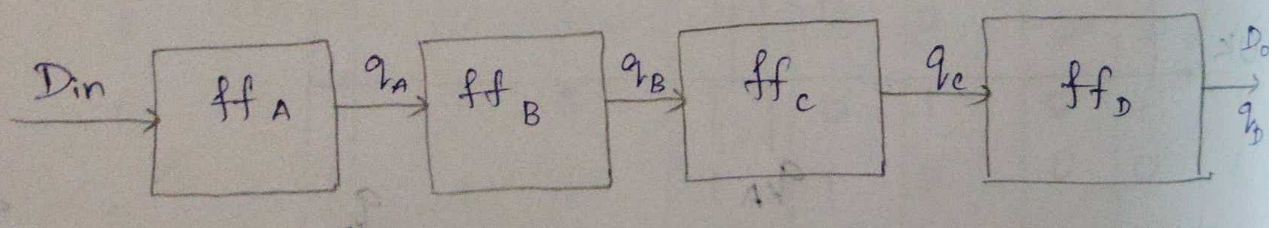


PIPO



1) **SISO** (serial in Serial out)

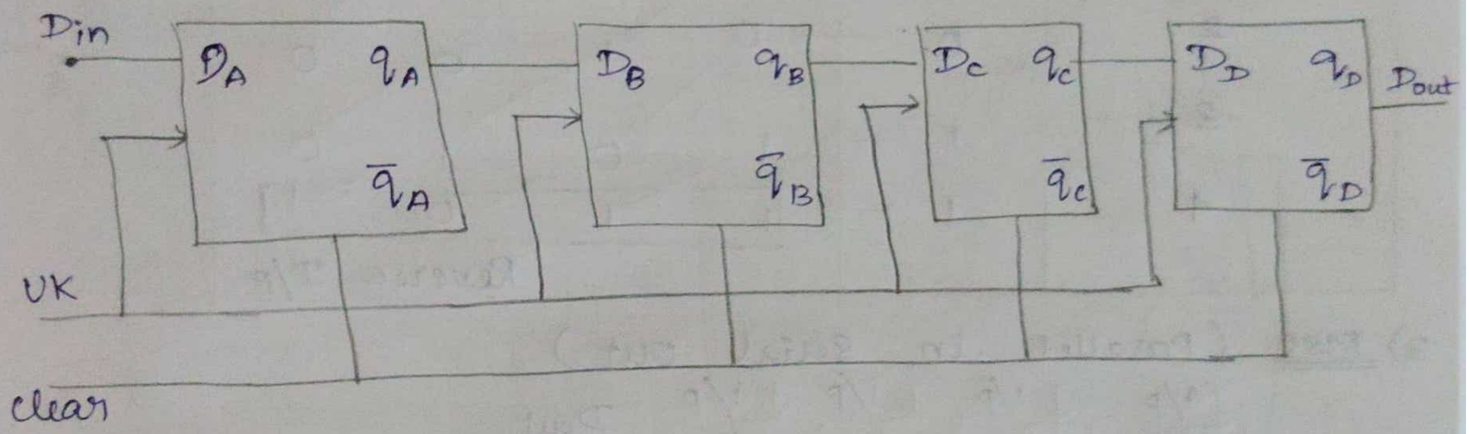
i/p ⇒ Left most ff
o/p ⇒ Right most ff
(eg) i/p data 1011



TRUTH TABLE

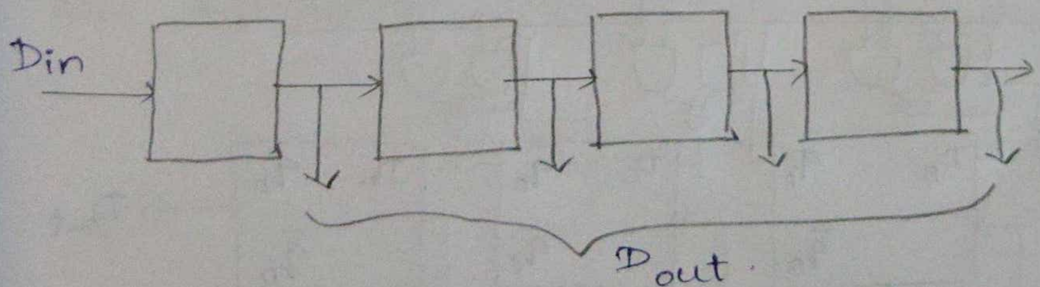
clock pulse	D_{in}	q_A	q_B	q_C	q_D	O/P
1	1	1	0	0	0	0
2	0	0	1	0	0	0
3	1	1	0	1	0	0
4	1	1	1	0	1	1
5	0	0	1	1	0	0
6	0	0	0	1	1	1
7	0	0	0	0	1	1

ff Diagram :

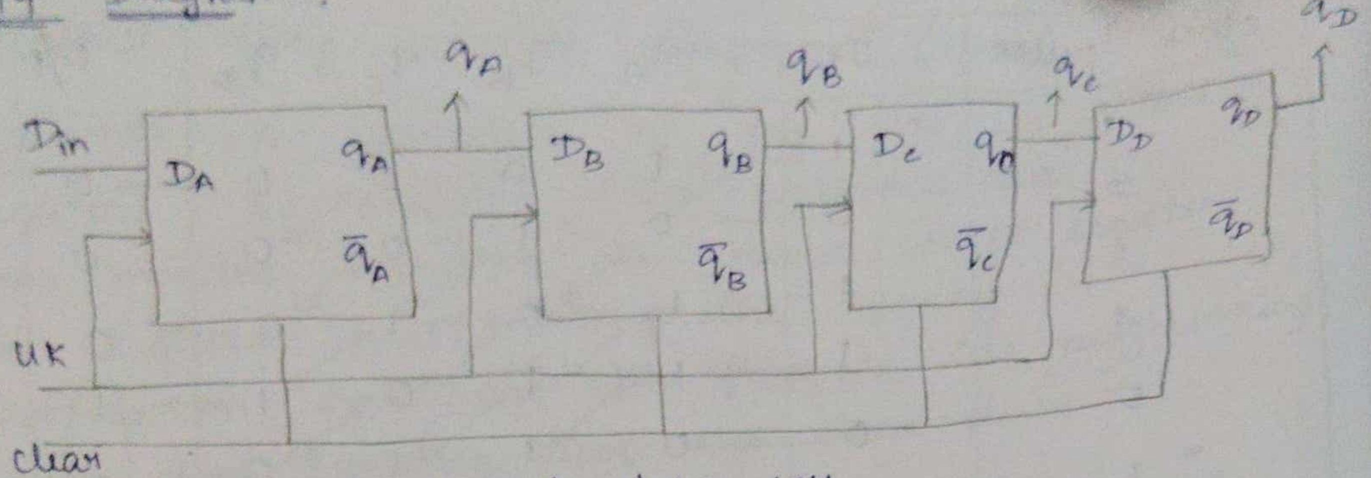


2) SIPO (serial in Parallel out)

* LSB is entered first
* After fourth clock pulse data can be taken simultaneously.



ff Diagram :

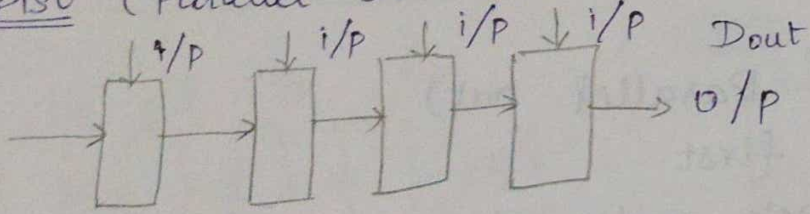


TRUTH TABLE (eg) I/P data 1011

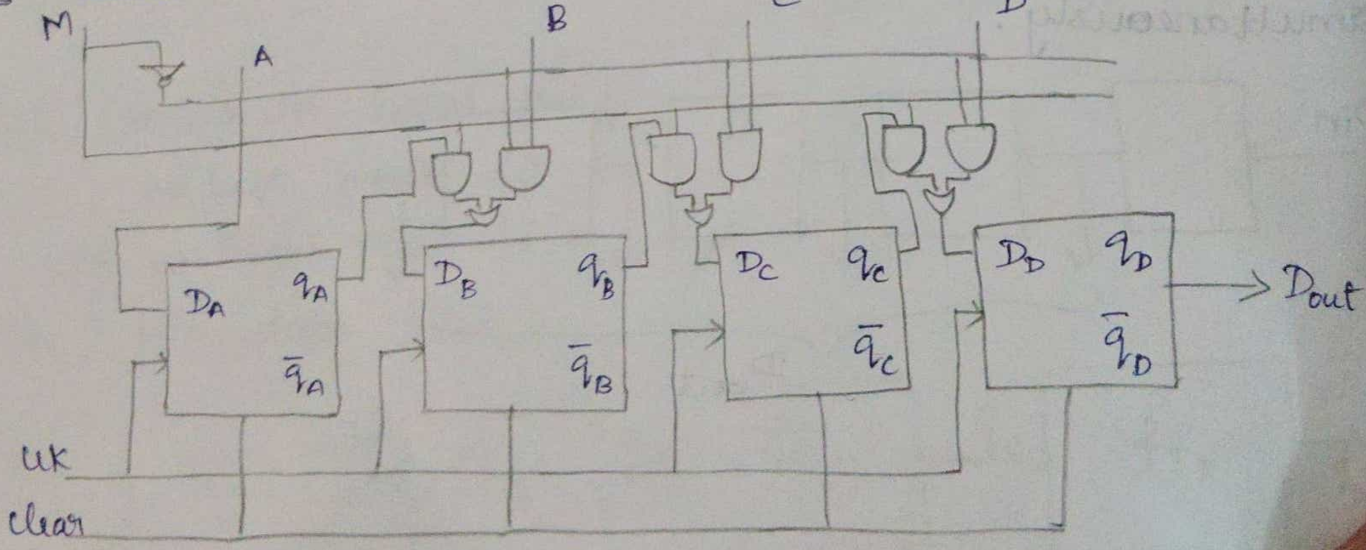
clock pulse	D_{in}	Dout			
		q_A	q_B	q_C	q_D
1	1	1	0	0	0
2	0	0	1	0	0
3	1	1	0	1	0
4	1	1	1	0	1

Reverse I/P

3) PISO (Parallel in Serial out)



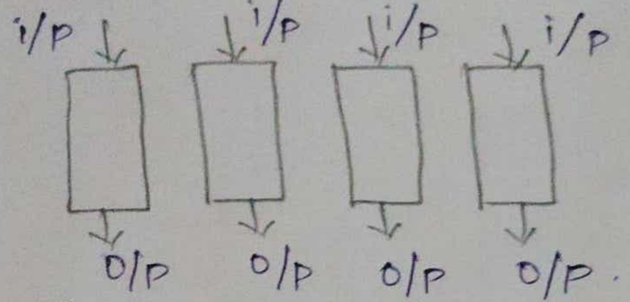
ff Diagram :



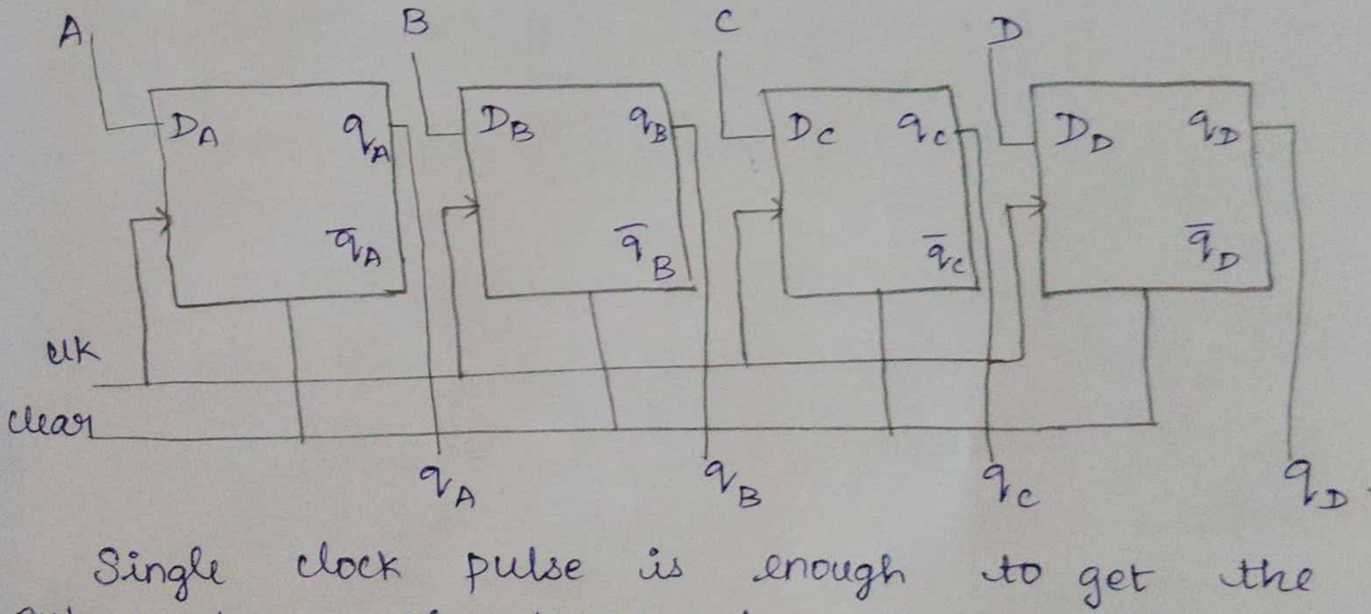
TRUTH TABLE

clk	Din	D_A	D_B	D_C	D_D	Dout
1		1	0	1	1 →	1
2		0	1	0	1 →	1
3		0	0	1	0 →	0
4		0	0	0	1 →	1

4) PIPO (Parallel in Parallel Out)



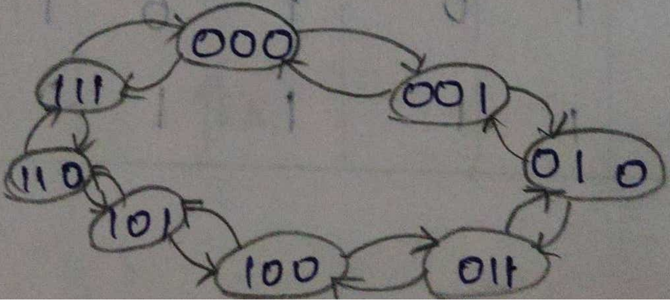
ff Diagram :



Single clock pulse is enough to get the output data simultaneously. Input data is also simultaneously apply.

2) Analyse 3-bit synchronous up down counter using k-map. (16 m) Q.B 2.

<u>Soln</u>: 3 bit synchronous up down counter using T flip flop.



EXCITATION TABLE

q_n	q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE

Numbers	Present State			Next State			flip flop inputs		
up or Down	q_A	q_B	q_C	q_{A+1}	q_{B+1}	q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

K-map T_A

$Nq_A \backslash q_Bq_C$	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	1	0	0	0
10	1	0	0	0

$$T_A = N\bar{q}_B\bar{q}_C + \bar{N}q_Bq_C$$

T_B

$Nq_A \backslash q_Bq_C$	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

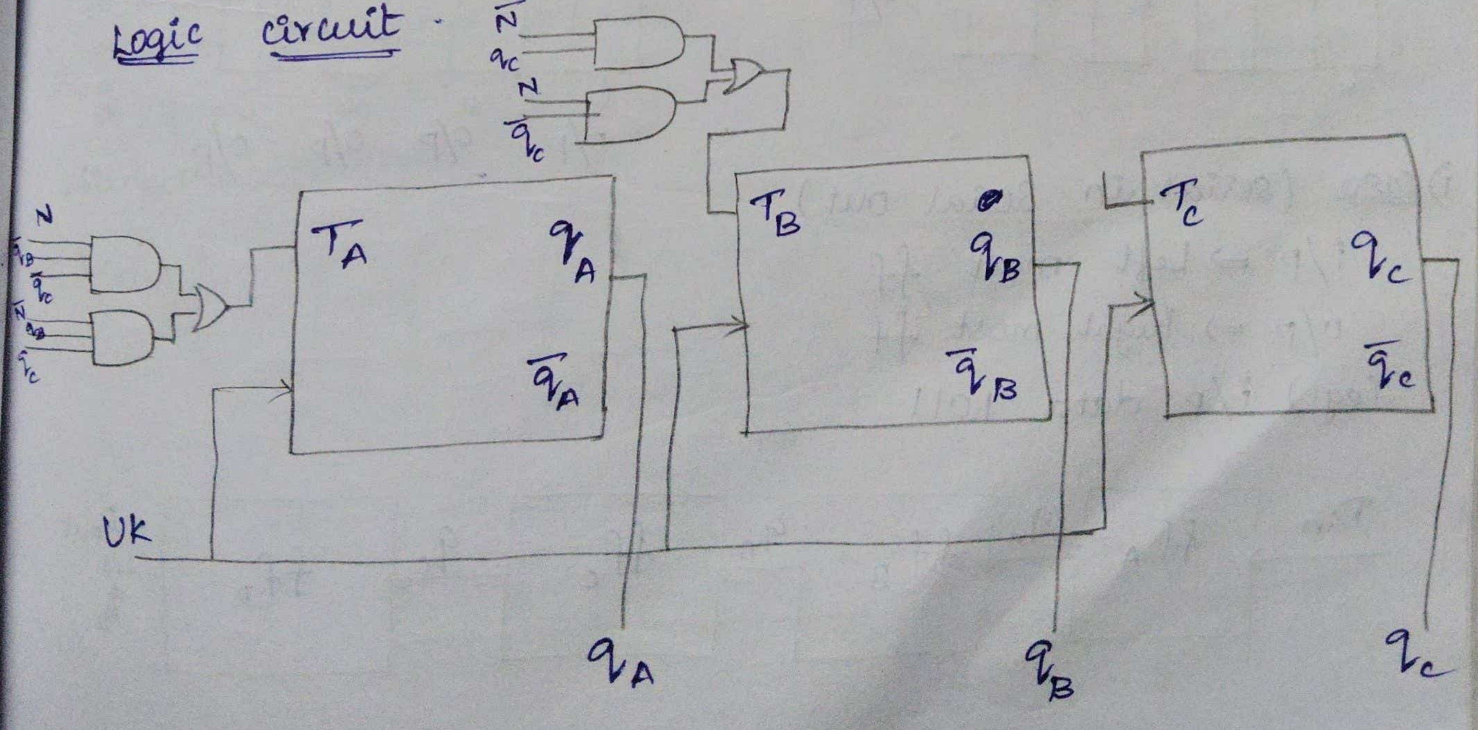
$$T_B = \bar{N}q_c + N\bar{q}_c$$

T_c

$Nq_A \backslash q_Bq_C$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

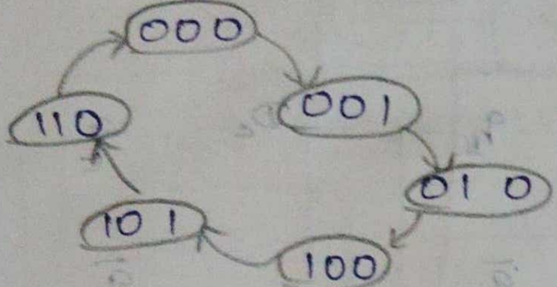
$$T_c = 1$$

Logic circuit :



2) Examine a Synchronous sequential circuit using D flip flop to generate the following sequence and repeat '0, 1, 2, 4, 5, 6 Q.B 3 (16m)

State Diagram



EXCITATION TABLE

q_n	q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

TRUTH TABLE

Present State			Next State			flip flop Inputs		
A	B	C	A_{t+1}	B_{t+1}	C_{t+1}	D_A	D_B	D_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	0	0	0	0	0	0

K-map

D_A

A \ BC	00	01	11	10
0	0	0	X	1
1	1	1	X	0

$D_A = \bar{A}B + A\bar{B}$

D_B

A \ BC	00	01	11	10
0	0	1	X	0
1	0	1	X	0

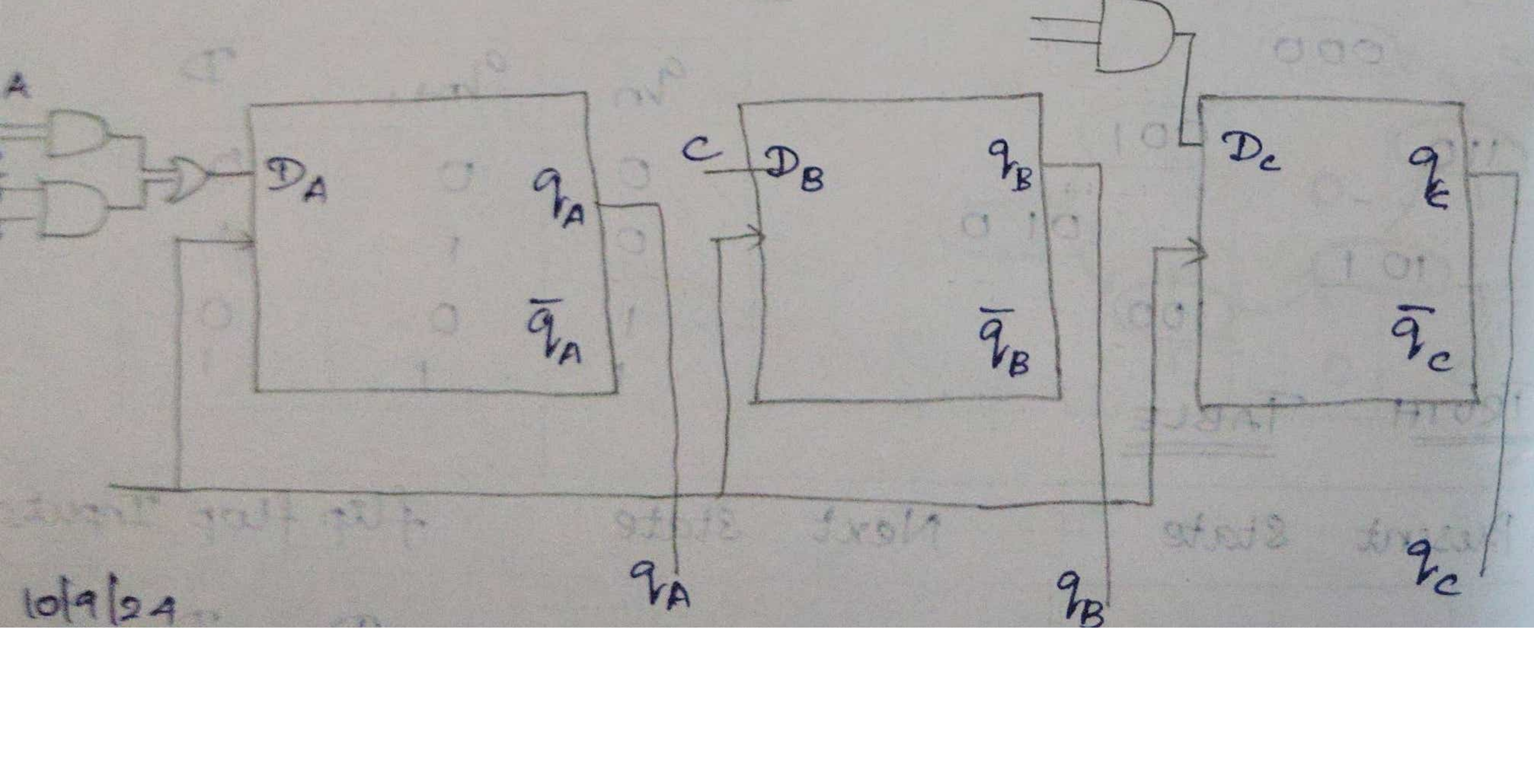
$D_B = C$

D_C

A \ BC	00	01	11	10
0	1	0	X	0
1	1	0	X	0

$D_C = \bar{B}\,\bar{C}$

Circuit Diagram.



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1) Analyse MOD-5 Synchronous counter using T flip flop. Q.B (4) (16m)

EXCITATION TABLE:

q_n	q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

mod 5

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4$

TRUTH TABLE

Present State			Next State			flipflop Inputs		
A	B	C	A_{t+1}	B_{t+1}	C_{t+1}	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	0	0	0	1	0	0

K-map

T_A

A \ BC	00	01	11	10
0	0	0	1	0
1	1	X	X	X

$T_A = A + BC$

T_B

A \ BC	00	01	11	10
0	0	1	1	0
1	0	X	X	X

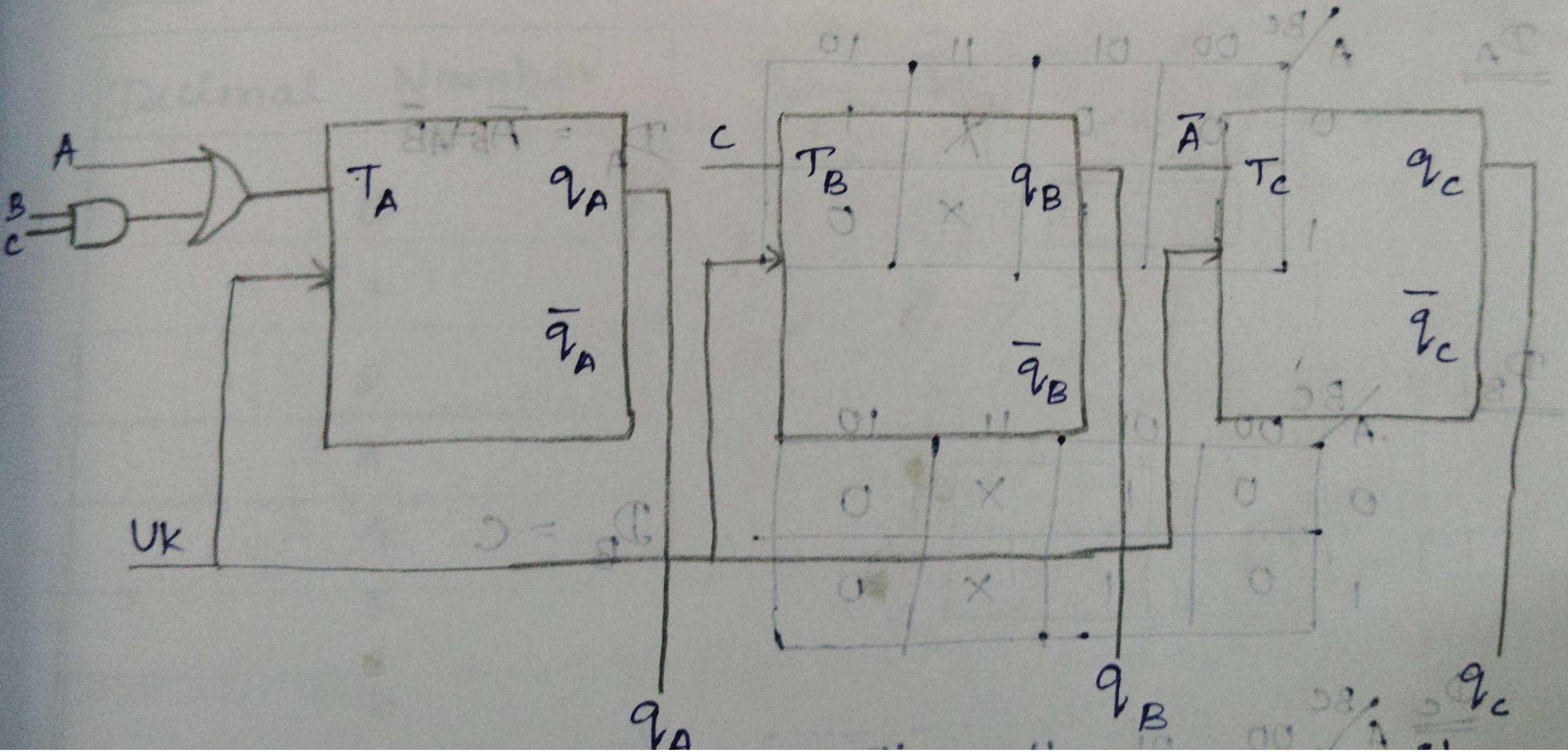
$T_B = C$

T_C

A \ BC	00	01	11	10
0	1	1	1	1
1	0	X	X	X

$T_C = \overline{A}$

Logic circuit



1) Examine a singular counter that counts the sequences :

1 - 3 - 15 - 5 - 8 - 2 - 0 - 12 - 6 - 9 using JK flip flop. Q.B (5) (16m)

EXCITATION TABLE :

q_n	q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

TRUTH TABLE :

NUMBER	PRESENT STATE				NEXT STATE				EXCITATION INPUTS			
	q_D	q_C	q_B	q_A	q_{D+1}	q_{C+1}	q_{B+1}	q_{A+1}	$J_D K_D$	$J_C K_C$	$J_B K_B$	$J_A K_A$
1	0	0	0	1	0	0	1	1	0X	0X	1X	X0
3	0	0	1	1	1	1	1	1	1X	1X	X0	X0
~~3~~15	1	1	1	1	0	1	0	1	X1	X0	X1	X0
5	0	1	0	1	1	0	0	0	1X	X1	0X	X1

8	1 0 0 0	0 0 1 0	1X	0X	1X	0X
2	0 0 1 0	0 0 0 0	0X	0X	X1	0X
0	0 0 0 0	1 1 0 0	1X	1X	0X	0X
12	1 1 0 0	0 1 1 0	X1	X0	X0	0X
6	0 1 1 0	1 0 0 1	1X	X1	X1	1X
9	1 0 0 1	0 0 0 1	X1	0X	0X	X0

K-map.

J_D

$q_D q_C \backslash q_B q_A$	00	01	11	10
00	1	0	1	0
01	X	1	X	1
11	X	X	X	X
10	X	X	X	X

$$J_D = q_C + \bar{q}_B \bar{q}_A + q_B q_A$$

K_D

$q_D q_C \backslash q_B q_A$	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	X	1	X
10	1	1	X	X

$$K_D = 1$$

J_C

$q_D q_C \backslash q_B q_A$	00	01	11	10
00	1	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	X	X

$$J_C = \bar{q}_D + \bar{q}_B \bar{q}_A + q_B q_A$$

K_C

$q_D q_C \backslash q_B q_A$	00	01	11	10
00	X	X	X	X
01	X	1	X	1
11	0	X	X	X
10	X	X	X	X

$$K_C = \bar{q}_D$$

q_Dq_C \ q_Bq_A	00	01	11	10
00	0	1	X	X
01	X	0	X	X
11	1	X	X	X
10	1	0	X	X

$$J_B = \bar{q}_D \bar{q}_C q_A + q_D \bar{q}_A$$

K_B

q_Dq_C \ q_Bq_A	00	01	11	10
00	X	X	0	1
01	X	X	X	1
11	X	X	1	X
10	X	X	X	X

$$K_B = q_B \bar{q}_A + q_C$$

J_A

q_Dq_C \ q_Bq_A	00	01	11	10
00	0	X	X	0
01	X	X	X	1
11	0	X	X	X
10	0	X	X	X

$$J_A = q_C + q_B$$

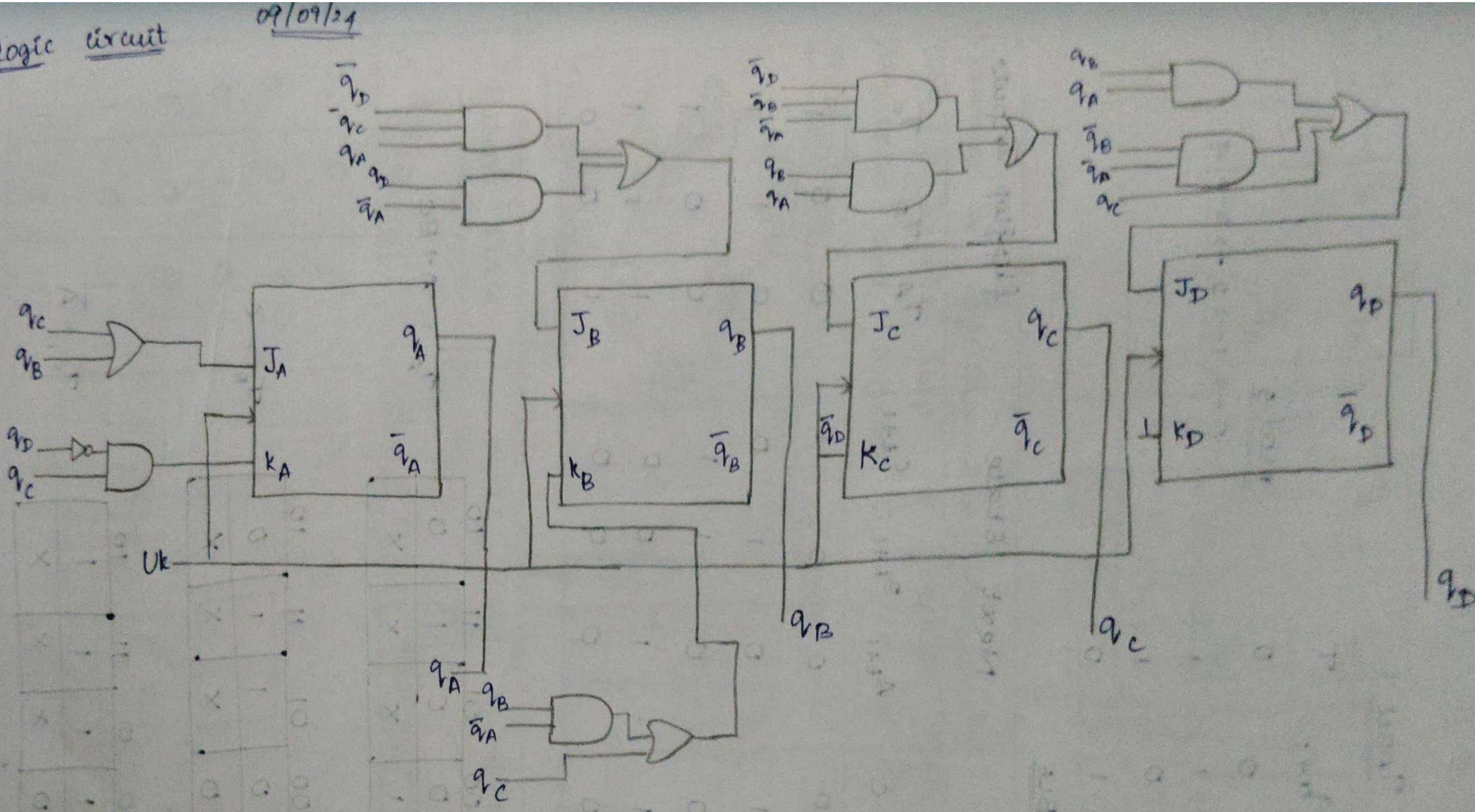
K_A

q_Dq_C \ q_Bq_A	00	01	11	10
00	X	0	0	X
01	X	1	X	X
11	X	X	0	X
10	X	0	X	X

$$K_A = \bar{q}_D q_C$$

Logic circuit

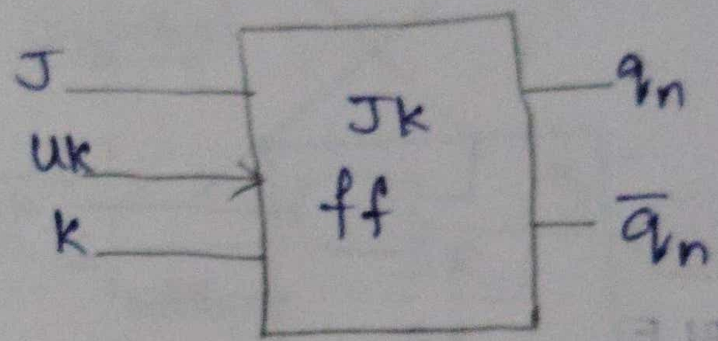
09/09/24



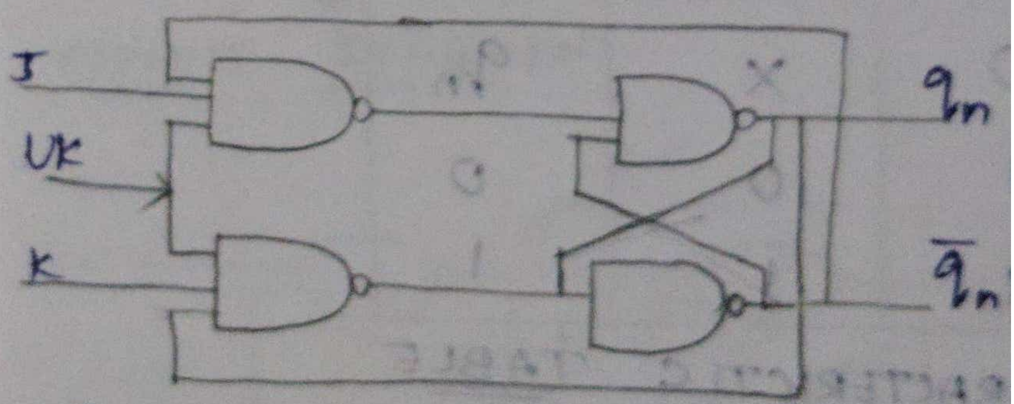
3) JK FLIP FLOP:

It is used to over come the invalid state of SR flip flop (S=1 & R=1) by some useful action (Toggling)

SYMBOL:



CIRCUIT DIAGRAM:



TRUTH TABLE:

UK	J	K	q_{n+1}
0	x	x	q_n
1	0	0	q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{q}_n$

CHARACTERISTIC TABLE

J	K	q_n	q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

To Find q_{n+1}:

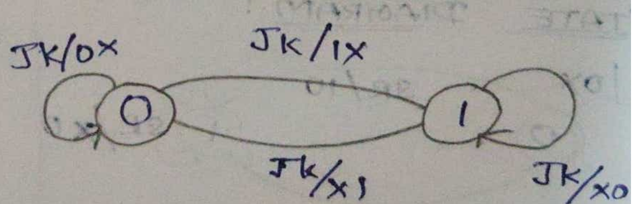
J \ Kq_n	00	01	11	10
0	0	1	0	0
1	1	1	0	1

$$\boxed{q_{n+1} = J\bar{q}_n + \bar{K} q_n}$$

EXCITATION TABLE :

q_n	q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

STATE DIAGRAM :



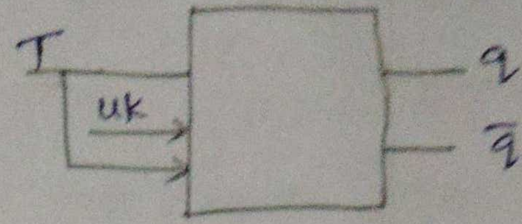
for charac table

J K	q_{n+1}
0 0	q_n
0 1	J (0)
1 0	J (1)
1 1	$\bar{q}_n$

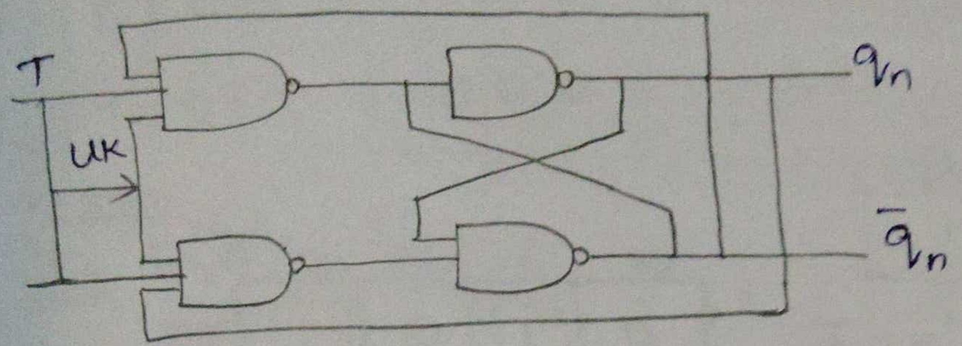
T- FLIP FLOP (Toggling)

T flip flop is used when we want only Toggling action. JK flip flop is used to obtain T flip flop.

Symbol



CIRCUIT DIAGRAM



TRUTH TABLE

ck	T	q_{n+1}
0	X	q_n
1	0	q_n
1	1	$\bar{q}_n$ (Toggle state)

CHARACTERISTIC TABLE

T	q_n	q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

EXCITATION TABLE

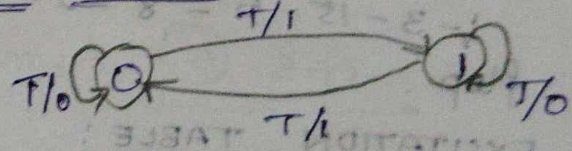
q_n	q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

TO find q_{n+1}

$$q_{n+1} = \bar{T} q_n + T \bar{q}_n$$

$$\boxed{q_{n+1} = T \oplus q_n}$$

STATE DIAGRAM:



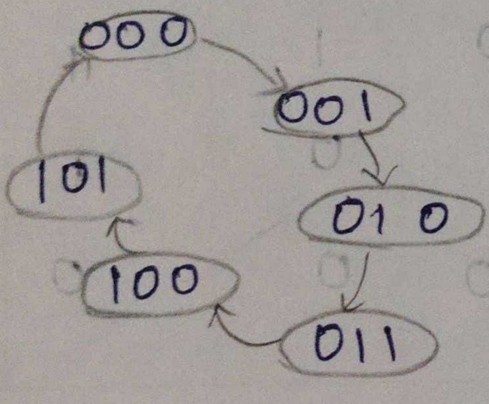
~~MASTER~~ ~~S/~~

10/9/24

1) Analyse modulo 6 Asynchronous counter in detail (8m) Q.B (8m) 8

State diagram

0 → 1 → 2 → 3 → 4 → 5



Truth Table:

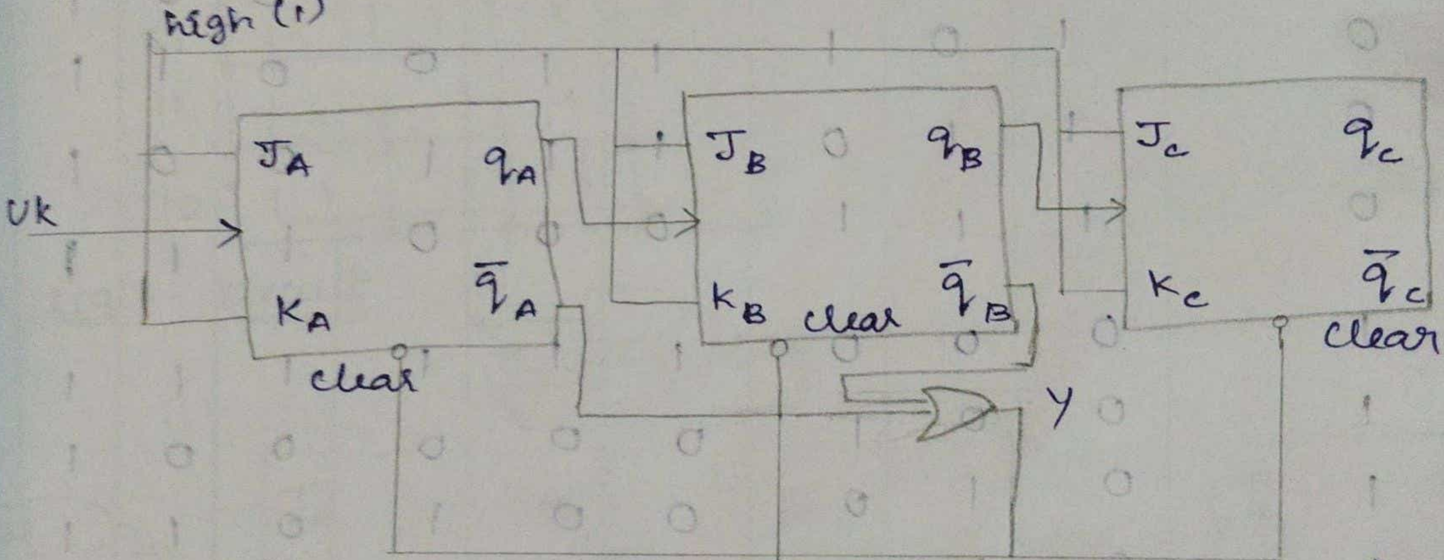
Decimal Number	q_A	q_B	q_C	Y
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	1	1	1	X

K-map

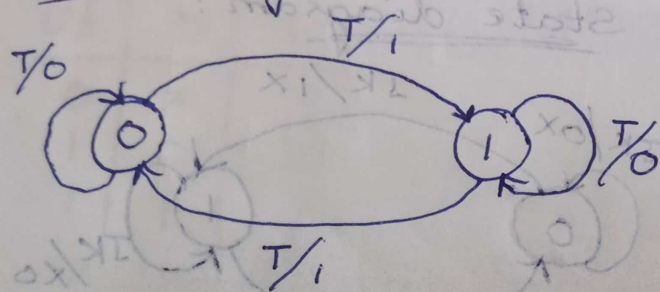
$q_A \backslash q_B q_C$	00	01	11	10
0	1	1	1	1
1	1	1	X	0

$$Y = \bar{q}_B + \bar{q}_A$$

Logic Circuit Diagram:



State diagram:



[16 mark]

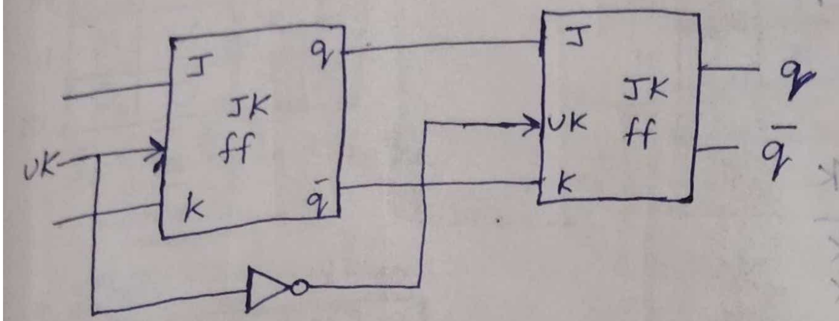
(1) Master Slave JK - flip flop : [16 marks]

Q.B

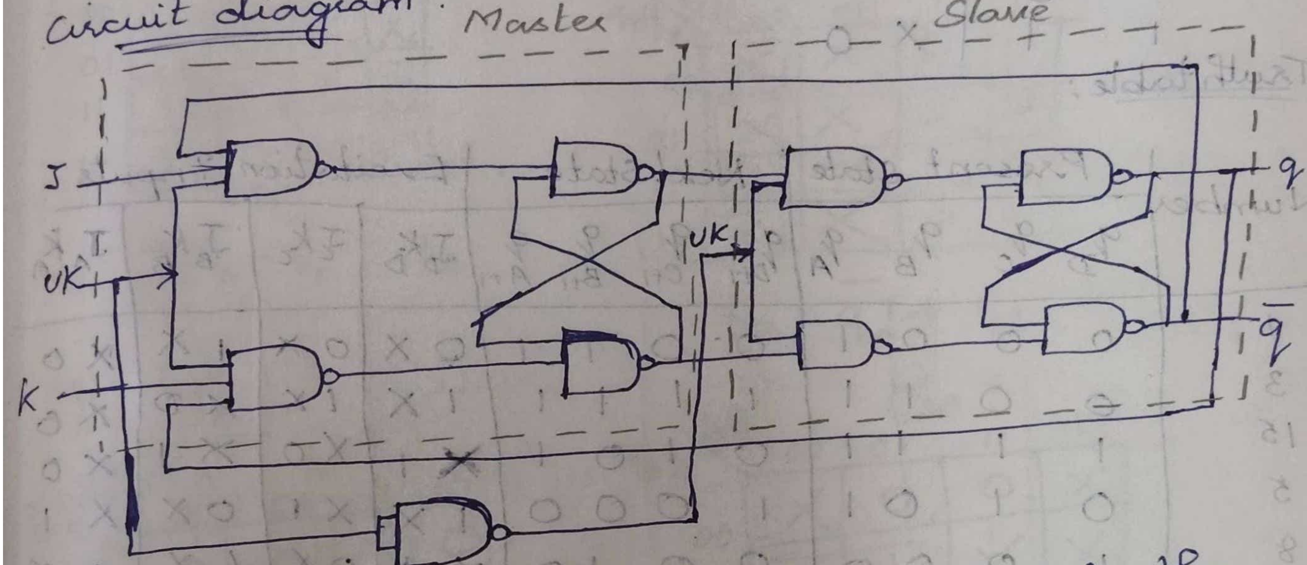
→ Before the development of edge triggered flip-flop the timing problem in level triggered flip-flop was often handled by Master Slave flip-flop.

→ At the end of the clock pulse the value of Q is unfound. This is called Race around condition. This can be avoided by Master Slave JK flip-flop.

Block diagram :



Circuit diagram :



- The clock signal is directly connected to the Master flip flop & is connected through inverter to the ~~s~~lave flip-flop.
- When clock ~~up~~ input has +ve edge, Master flip-flop acts according to the JK input but Slave will not respond.
- When clock input has -ve edge, Slave flip-flop will copy the Master output.
- Master does not respond to the feedback from q & $\bar{q}$ since it requires +ve edge, thus race around condition is avoided here.

[Write truth table, characteristic table, excitation table, to find q_{n+1}, state diagram from JK flip flop]