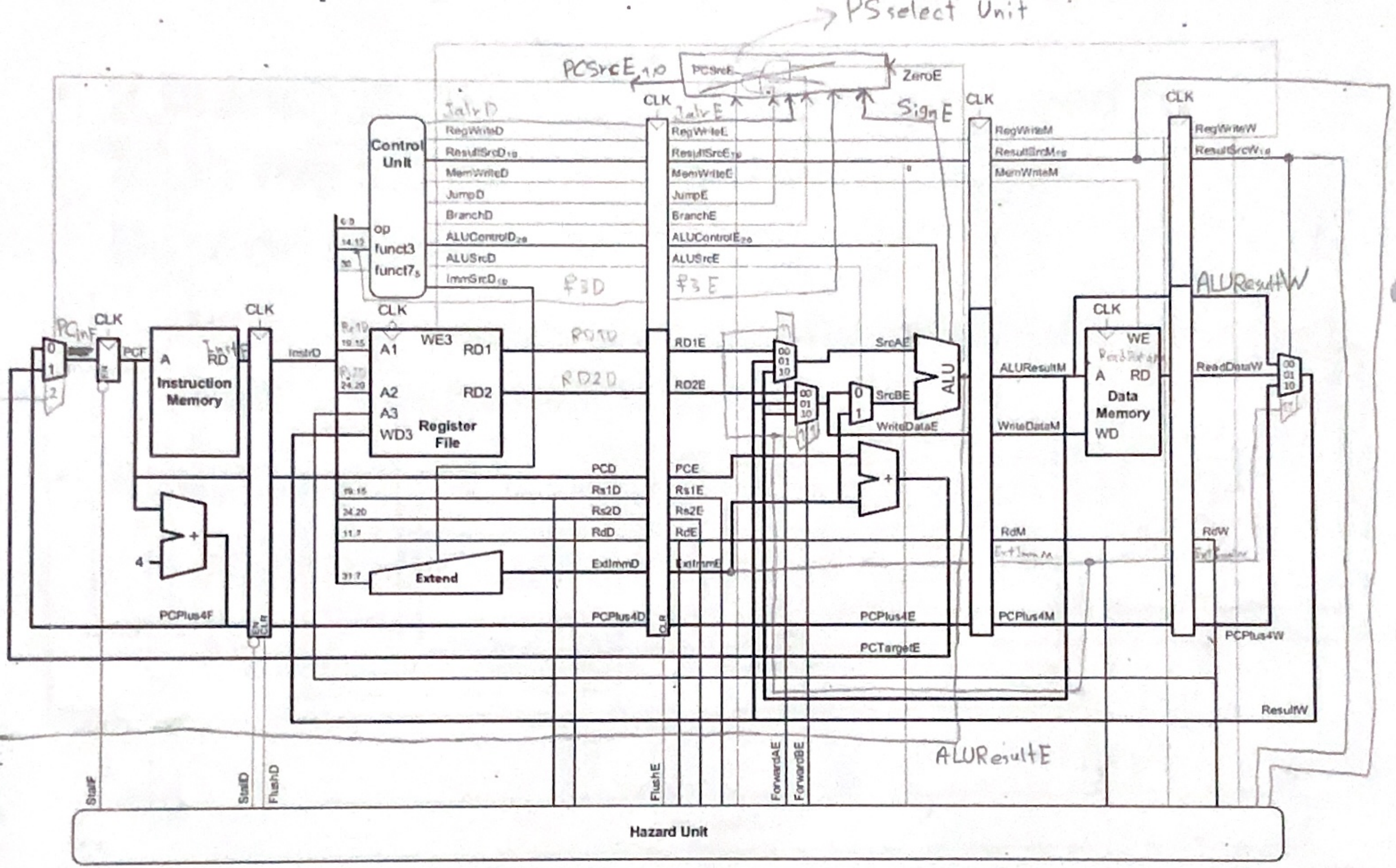
RISC-V Pipelined Processor with Hazard Unit



opc	Inst	RegwriteD	ImmSrcD	ALUSrcD	MemwriteD	ResultSrcD	ALUcontrolD	JalrD	JumpD	BranchD
3	lw	1	000	1	0	01	000	0	0	0
35	sw	0	001	1	1	xx	000	0	0	0
99	B-T	0	010	0	0	xx	001	0	0	1
51	R-T	1	xxx	0	0	00	add->000 or->011 sub->001 slt->101 and->010 sltu->110	0	0	0
19	I-T	1	000	1	0	00	addi->000 slti->101 xori->100 sltiu->110 ori->011	0	0	0
111	jal	1	011	x	0	10	xxx	0	1	0
55	lui	1	100	x	0	11	xxx	0	0	0
103	jalr	1	000	1	0	10	000	1	0	0

```
        lw   x8, 0(x0)
        addi x6, x0, 4
Loop:   sltiu x7, x6, 40
        beq  x7, x0, END_LOOP
        lw   x9, 0(x6)
IF:     slt  x1, x9, x8
        bne  x1, x0, END_IF
        add  x8, x0, x9
END_IF: addi x6, x6, 4
        j    Loop
END_LOOP:
```

x8 = جواب نهایی