LAB EXPERIMENTS USING NI ELVIS II AND NI MULTISIM

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Lab 6
Transient Responses of First-Order RC Circuits

Goals for Lab 6

- Learn about responses of first-order RC circuits to square-wave input signals of various frequencies
    - Exponential response, derived from first-order differential equations
    - Time constant τ is determined by the resistance and capacitance
    - DC steady-state is reached after $5 \cdot \tau$
    - Output waveforms depend on the ratio of period T to time constant τ
    - In the same series RC circuit, $V_C(t)$ is distinct from $V_R(t)$.

- In the pre-lab, simulate the responses $V_C(t)$ and $V_R(t)$ in a series RC circuit to the input square wave signals of various frequencies. In the in-lab, observe and measure these responses; in the post-lab compare the results of your simulations with your lab data.

- Explore, for extra credit, the effect of DC offset of the input square wave on the responses $V_C(t)$ and $V_R(t)$ in a series RC circuit.

- Learn about a first-order circuit with an op amp: in the pre-lab, simulate its responses to a square wave with 10% duty cycle; in the in-lab, observe and measure these responses; in the post-lab, compare the results of your simulations with your lab data and explain possible causes of their distinction.

- Explore, for extra credit, the ranges of frequencies where the output voltages in the op amp circuit reach the new DC steady state within 5% error.

Introduction

This lab introduces circuits that contain, besides resistors, sources and op amps, elements that you have not used in this course so far—capacitors (labeled C on the diagrams).

Circuits with capacitors behave differently from circuits that have only resistors, sources and op amps: their voltages and currents at the given moment depend not only on the input voltage at that moment but also on the history. In a certain sense, these circuits have memory: if a capacitor was charged to a certain voltage, it may still retain that charge or a part of it. The charge remaining on the capacitor influences voltages and currents in the circuit.

Interestingly enough, circuits without capacitors do not exist (outside theoretical calculations and textbooks), because—as you learned in physics—each conductor, even a piece of wire, has capacitance. In other words, besides capacitance of a component (called **capacitor**) that you get out of a bin, your circuit possesses unwanted capacitances, which may be called **effective** or **parasitic**.

In previous labs of this course, you neglected the effective capacitances of the circuits you built because you worked at low frequencies. In this lab, you will learn about the dramatic effects that the signal frequency has on the shape and magnitude of output signals, and observe that at high frequencies these effects may dominate, which is impossible to neglect.

In today's world, many electronic devices (including computers and cell phones) are built to operate at higher and higher frequencies thus it becomes extremely important to learn about their actual response to signals, which depends on the effective capacitances.

Mathematical description of circuits with resistors and capacitors and their response to varying input voltage involves differential equations. In the simplest case, a first-order differential equation is enough; therefore such circuits are called first-order circuits.

A simple circuit, for which the first-order differential equation is enough, includes one source, one resistor, and one capacitor, as shown in Figure 5-1.

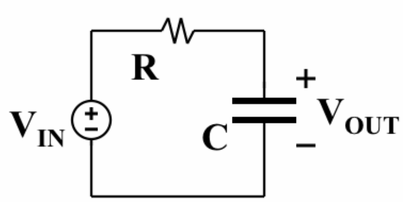


Figure 5-1. A simple first-order RC circuit.

Please note that the source and resistor in this simple circuit may represent the Thevenin equivalent parameters of a much more complicated device, as shown in Figure 5-2.

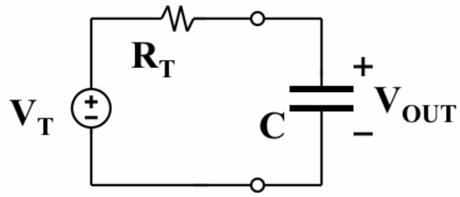


Figure 5-2. A simple first-order RC circuit can be Thevenin equivalent of a complicated device.

If the input signal (the source voltage) is a square wave, as shown in Figure 5-3, at a frequency, which is low enough (see details below), then the output signal measured across the capacitor looks like that sketched in Figure 5-4.

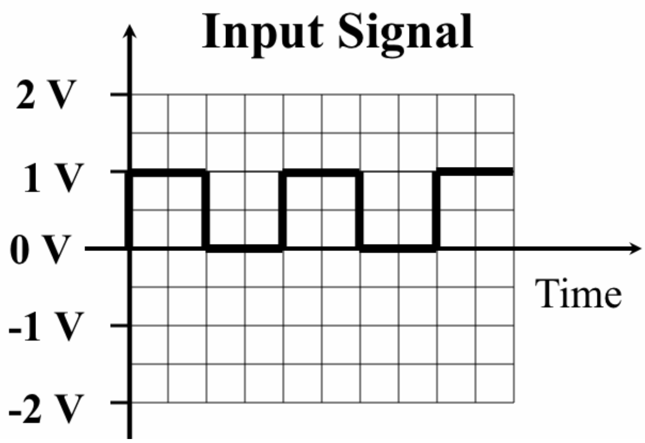


Figure 5-3. Input signal is a square wave with a positive DC offset.

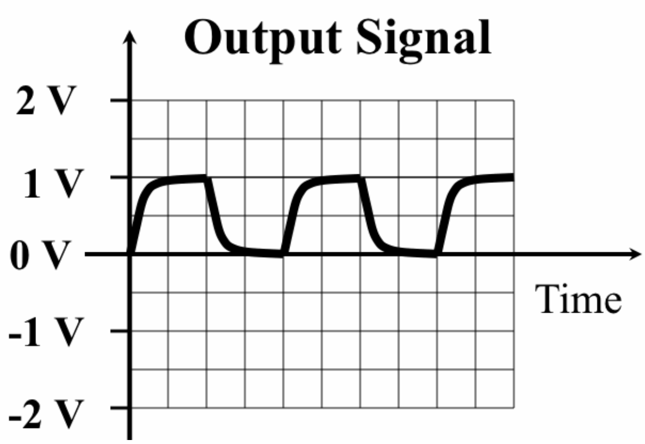


Figure 5-4. Output signal measured in the circuit of Figure 5-1 at a low frequency.

As shown in Figure 5-4, during the first half-period of the input square wave when the input voltage abruptly increased from 0 to 1 V and remained equal to 1 V, the capacitor, which was initially not charged, is gradually charging so that its voltage $V_C(t)$ asymptotically approaches the 1-V level. During the second half-period, after the input voltage abruptly dropped from 1 V to 0 V, the capacitor is gradually discharged thus its voltage $V_C(t)$ asymptotically approaches zero. Note that, in this example, the square wave voltage is high during 50% of the period and low during the rest 50%; this is called 50% duty cycle.

Gradual is the key word in the description of the capacitor discharge, because the capacitor voltage cannot change abruptly (the so-called continuity condition). Mathematically, the discharge of a capacitor is described with the exponential function

$$V_S(t) = V_0 \cdot e^{\left(-\frac{t}{\tau}\right)}$$

where V_0 is the initial voltage at time t = 0, and τ (Greek letter called **tau**) is the time constant, which for the circuit of Figure 5-1 equals the product of resistance and capacitance:

$$\tau = R \cdot C$$

This exponential function is used to describe many natural phenomena such as radioactive decay or bleaching of a dye. Figure 5-5 shows a plot of exponential decay normalized to 1, that is for $V_0 = 1$.

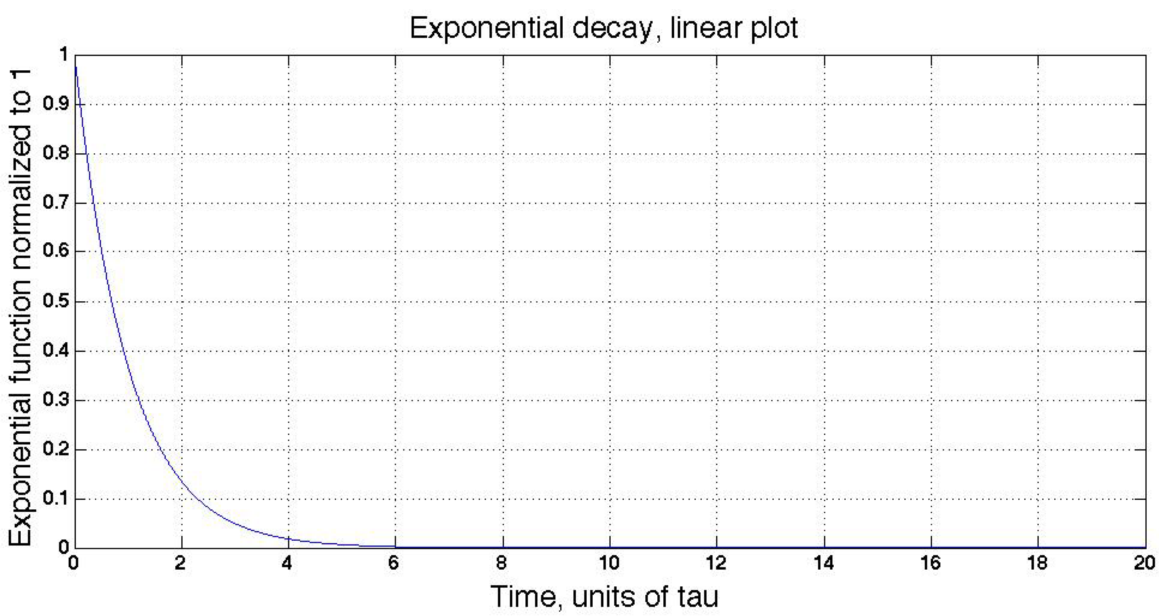


Figure 5-5. The exponential function $e^{\left(-\frac{t}{\tau}\right)}$ plotted versus time in units of τ (tau).

Note that by the time $t = 5 \cdot \tau$, the exponential function has decreased to less than 1% of its initial value at t = 0 ($e^{(-5)} = 0.0067$). Thus, in practice, you can safely assume that after $5 \cdot \tau$, a new DC steady state has been reached. (Refer to your textbook for the explanation of how τ is derived from circuit equations.)

The DC steady state can be defined as the condition at which all time derivatives $\frac{d}{dt}$ die out; on the plots and oscilloscope screen it corresponds to a flat horizontal part of the waveform (voltage or current as function of time).

Whether the DC steady-state condition is reached by the circuit during each half-period of the square wave, depends on the ratio r

$$r = \frac{\text{Period of square wave}}{\text{Characteristic time of the circuit}} = \frac{T}{\tau} = \frac{\text{Frequency } f_C = \frac{1}{\tau}}{\text{Frequency } f = \frac{1}{T}}$$

of the characteristic frequency of the circuit $f_C = \frac{1}{\tau}$ to the frequency f of the square wave. If this ratio is large (50 or more) the capacitor is given enough time to fully charge and fully discharge (or recharge to a different voltage) during each half-period of the square wave. If the ratio is small, the capacitor will only partly charge and discharge thus the peak-to-peak value of $V_C(t)$ will be smaller at the high frequency than at the low frequency.

For example, assume $\tau = RC$ with component values C = 1 μF and R = 200 Ω.

$$RC = \left(1 \cdot 10^{-6}\,F\right) \cdot \left(200\,\Omega\right) = 2 \cdot 10^{-4}\,\text{sec} = \tau = \frac{1}{f_C} = \frac{1}{5\,\text{kHz}}$$

If a square wave has 50% duty cycle, then each half-period should equal at least $5 \cdot \tau$

$$T = 10 \cdot \tau = 2 \cdot 10^{-3}\ \text{sec} \quad \text{Thus}\ \ f = \frac{1}{T} = \frac{1}{2 \cdot 10^{-3}} = 0.5\,\text{kHz} = 500\,\text{Hz}$$

$$\text{The ratio} = r = \frac{f_C}{f} = \frac{5\,\text{kHz}}{100\,\text{Hz}} = 50$$

At the square wave frequencies higher than 500 Hz, this circuit will not reach DC steady state during each half-period; in other words, the capacitor will not be given enough time to fully charge and discharge.

The most interesting part of exponential decay, between t = 0 and t = 5τ, is plotted in Figure 5-6.

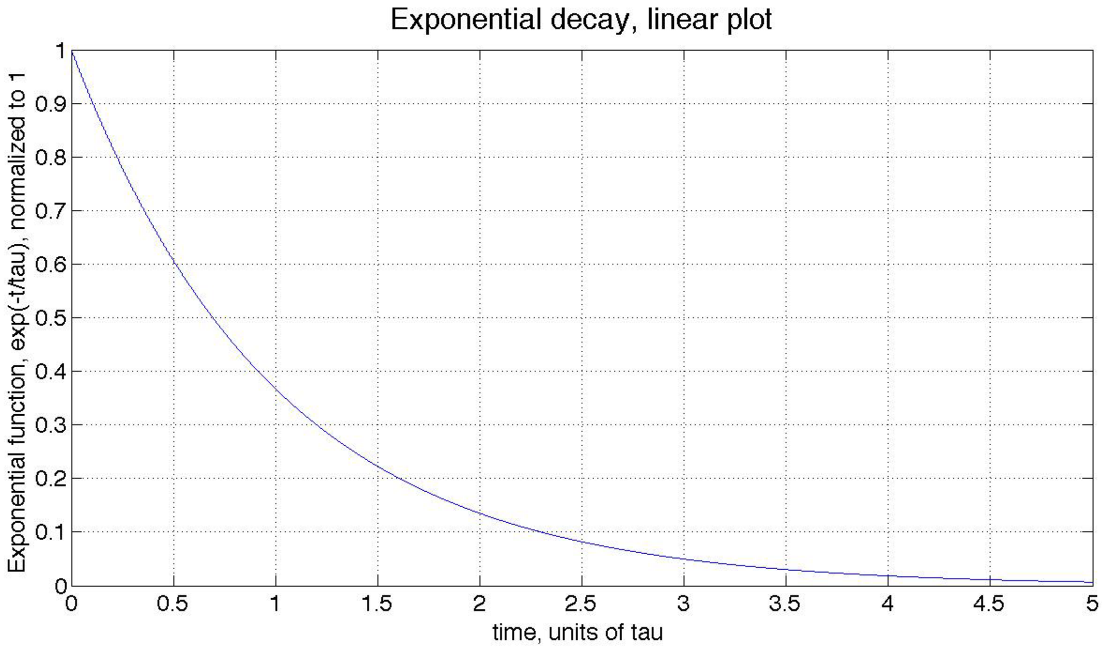


Figure 5-6. The exponential function $e^{\left(-\frac{t}{\tau}\right)}$ plotted versus time in units of τ over the interval from time t = 0 to t = 5τ.

For future reference, note that, by the time t = 3τ, the exponent decreases to below 5% of its initial value ($e^{(-3)} = 0.0498$).

From Figure 5-6, during time interval of 0.5 · τ, the capacitor voltage decreases only to 60% of its initial value. Thus, in response to a high-frequency square wave whose period T = τ, the output voltage in the circuit of Figure 5-1 will be much smaller than in response to a low-frequency square wave with T = 50 · τ.

You will clearly observe this distinction in your pre-lab simulation and in-lab experiments.

Another variant of the same circuit is shown in Figure 5-7: here the components are the same as in Figure 5-1 but the output voltage is measured across the resistor.

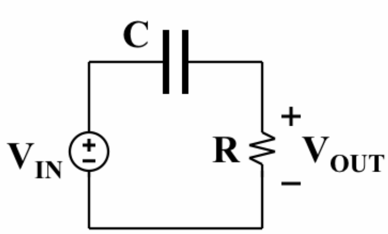


Figure 5-7. A first-order RC circuit with the output voltage measured across the resistor.

According to KVL, the sum of capacitor voltage and resistor voltage must equal the source voltage, or

$$-V_{IN} + V_C + V_R = 0$$

The source voltage V_{IN} changes abruptly (or very, very fast), the capacitor voltage V_C changes only gradually, with the time constant equal to $\tau = RC$, thus the resistor voltage V_R must change abruptly in order to satisfy KVL, as sketched in Figure 5-8.

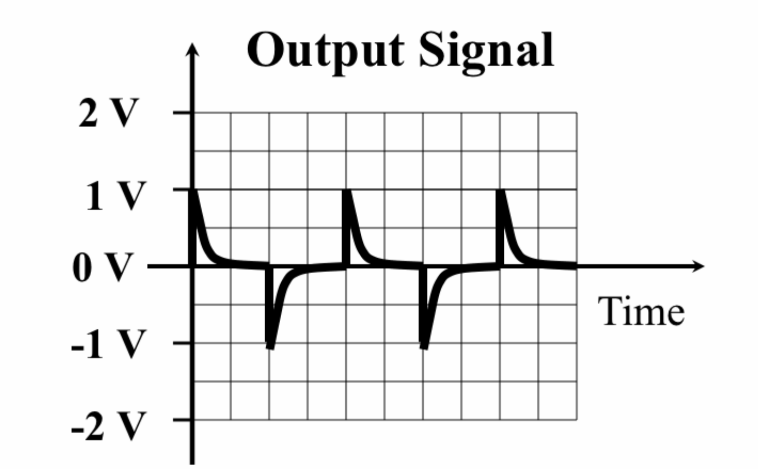


Figure 5-8. Output voltage measured across the resistor in the circuit of Figure 5-7, with the input signal of Figure 5-3.

Note that, under the DC steady state, the resistor voltage equals zero, because the capacitor acts like an open circuit and does not allow any current to flow through the resistor in the circuit of Figure 5-7.

In this lab we use the source voltages that abruptly change from one constant value V_1 to another constant value V_2. The sketch in Figure 5-3 shows a square wave with positive DC offset, for which these voltages are $V_1 = 0$ V and $V_2 = 1$ V; Figure 5-9 shows a square wave with zero DC offset, thus $V_1 = -0.5$ V and $V_2 = +0.5$ V.

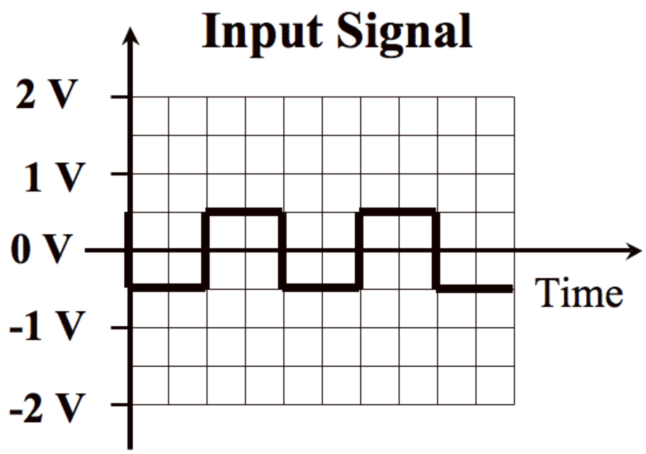


Figure 5-9. A square wave with zero DC offset.

In general, the current and voltages in the circuit of Figure 5-1 (or Figure 5-7) in response to input voltage that changes abruptly from V_1 to V_2 are mathematically described as

$$A \cdot e^{\left(-\frac{t}{\tau}\right)} + B$$

where A and B are constants, which should be found from the circuit equations (see your textbook).

For our introduction, it suffice to say that the output signals you will measure in RC circuits will strongly depend on the shape and frequency of input signal as well as its DC offset, and on whether you measure the output across the capacitor or across the resistor.

A significant part of this lab is based on the circuit taken from Example 5-15 in the textbook *Circuits* by Ulaby and Maharbiz (pages 223–225), shown in Figure 5-10 below. For the details of circuit analysis, please refer to the textbook.

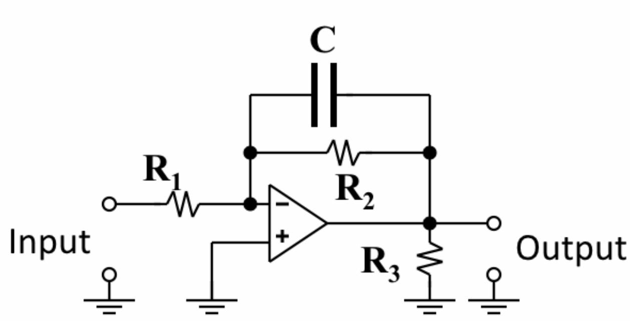


Figure 5-10. First-order op amp circuit.

An important variation of input signal waveform is shown in Figure 5-11.

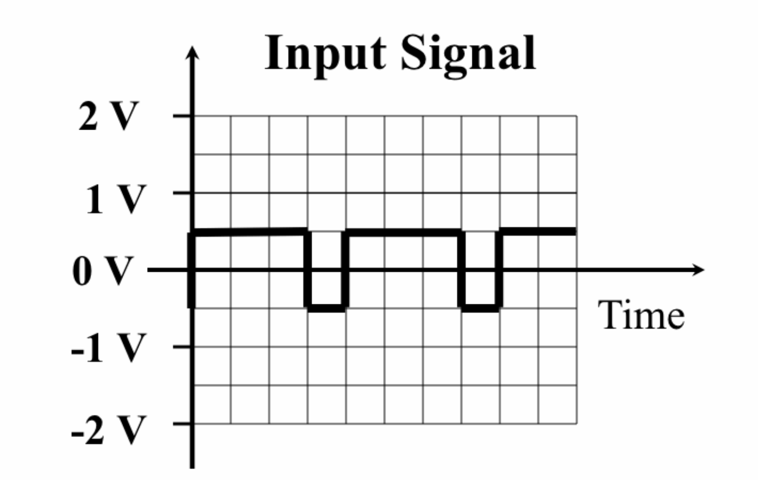


Figure 5-11. Square waveform with the duty cycle different from 50%.

Duty cycle of a square wave is defined as the percentage of each period, during which the signal is at its maximum. Thus Figure 5-11 shows a square wave with 75% duty cycle. The duration of the time interval when the signal is at its maximum can be found as the product $(\text{Duty cycle}) \cdot T$, where T is the period of the square wave. Recall that $T = \frac{1}{f}$, where period T is in seconds and frequency f is in hertz.

In the pre-lab you will simulate—and in the in-lab you will observe and measure—the responses of the circuit of Figure 5-10 to square waves with 90% duty cycle, at various frequencies. Under these conditions, the capacitor will be charged to a negative voltage during $0.9 \cdot T$ and recharged to the positive voltage during $0.1 \cdot T$. Three distinct responses are observed in the following ranges of frequencies:

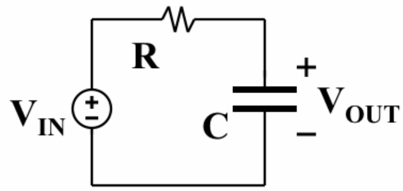
(1) At very low frequencies, when $0.1 \cdot T > 5 \cdot \tau$, the capacitor will be fully charged and fully recharged during each period; on the waveform $V_C(t)$ you will observe horizontal parts, which correspond to zero time derivatives (DC steady-state).
(2) At very high frequencies, when $T \sim \tau$ or $T < \tau$, the capacitor will never be fully charged thus on the waveform $V_C(t)$ you will not observe any horizontal parts.
(3) At intermediary frequencies, where $0.9 \cdot T > 5 \cdot \tau$ but $0.1 \cdot T < 5 \cdot \tau$, the capacitor will be fully charged to the negative voltage during $0.9 \cdot T$ but only partly recharged to the positive voltage during $0.1 \cdot T$.

Note that the time constant τ should be found from circuit analysis: in the circuit with 3 resistors (Figure 5-10) it is not evident what resistance enters the equation.

Pre-Lab:

1. Series RC circuit

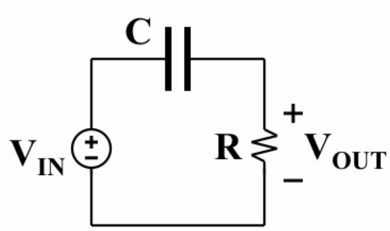
a. Calculate the time constant τ for the following circuit with R = 1 kΩ and C = 0.1 μF



b. Simulate the circuit's response to a 1 V_{PPK}, 500 Hz square wave. Provide a printout showing V_{IN} and V_C.

c. From the simulation results, determine $V_{C,\ PPK}$. Compare this value to $V_{IN,\ PPK}$.

d. From the simulation results, determine Δt, the time it takes for V_C to reach steady state. Compare this with the expected value of $5 \cdot \tau$.



Here, as before, R = 1 kΩ and C = 0.1 μF

e. Simulate the above circuit's response to a 1 V_{PPK}, 500 Hz square wave. Provide a printout showing V_{IN} and V_R.

f. From the simulation results, determine $V_{R,\ PPK}$.

g. Calculate the expected $V_{R,\ PPK}$ using circuit analysis.

h. Compare the simulated $V_{R,\ PPK}$ to the theoretical $V_{R,\ PPK}$.

i. From the simulation results, determine Δt, the time it takes for V_R to reach steady state. Compare this with the expected value of $5 \cdot \tau$.

j. Explain why V_C and V_R respond differently to the same input.

2. Exploration for Extra Credit: Nonzero DC Offset

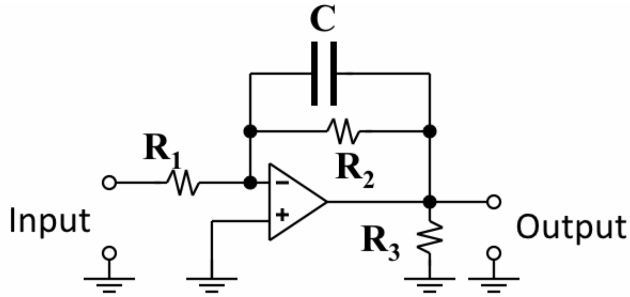
a. Repeat your simulation from Problem 1. This time use a 1 V_{PPK}, 500 Hz square wave with a +0.5 V DC offset. Provide two printouts, one showing V_{IN} and V_C and one showing V_{IN} and V_R.
b. Determine the effects the DC offset has on both V_C and V_R. Explain why V_C and V_R respond differently in the presence of the DC offset.
c. Verify the results of your simulation with calculations based on circuit analysis.

3. More on the Series RC Circuit

a. Repeat your simulation from Problem 1. This time use a 1 V_{PPK}, 2 kHz square wave with 0 V offset. Provide a printout showing V_{IN} and V_C.
b. From the simulated response, determine $V_{C,\,PPK}$.
c. Repeat the simulation again using a 10 kHz wave. Provide another printout showing V_{IN} and V_C for this frequency. Determine $V_{C,\,PPK}$.
d. Explain why the $V_{C,\,PPK}$ is smaller than $V_{IN,\,PPK}$ and why their ratio decreases as the frequency of the input signal increases.
e. Repeat Steps 2.a–2.c again, this time using V_R as the output voltage instead of V_C.
f. Explain the shape of V_R and its dependence on the frequency of the input signal.

4. First-Order Op Amp Circuit

a. Simulate the response the following circuit (with $R_1 = R_2 = R_3 = 1\ k\Omega$ and $C = 0.1\ \mu F$) in to a 1 V_{PPK}, 100 Hz square wave with a 15% duty cycle. Create a printout showing V_{IN} and V_{OUT}.



b. Repeat Problem 4.a for a 500 Hz wave.
c. Repeat Problem 4.a for a 10 kHz wave.
d. Explain why the signal sometimes reaches steady state, whereas in other cases it does not.

