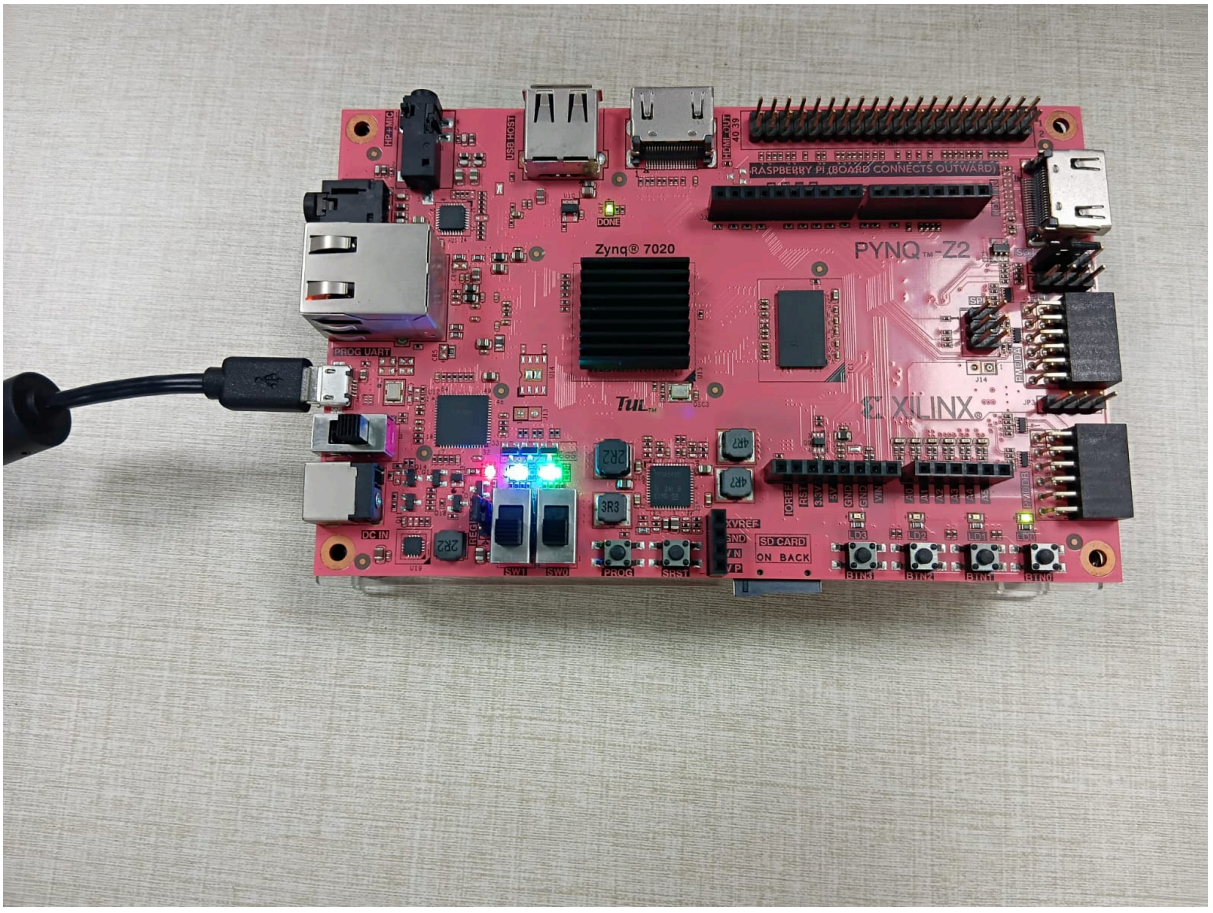
PROJECT WORK

‘TRAFFIC LIGHT CONTROLLER (12 I/O) - VERILOG PROJECT’



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VIVEKANANDA INSTITUTE OF PROFESSIONAL STUDIES

Acknowledgment

I would like to express my appreciation for the opportunity to work on this project titled **"Traffic Light Controller(12 I/O)- Verilog project"**.

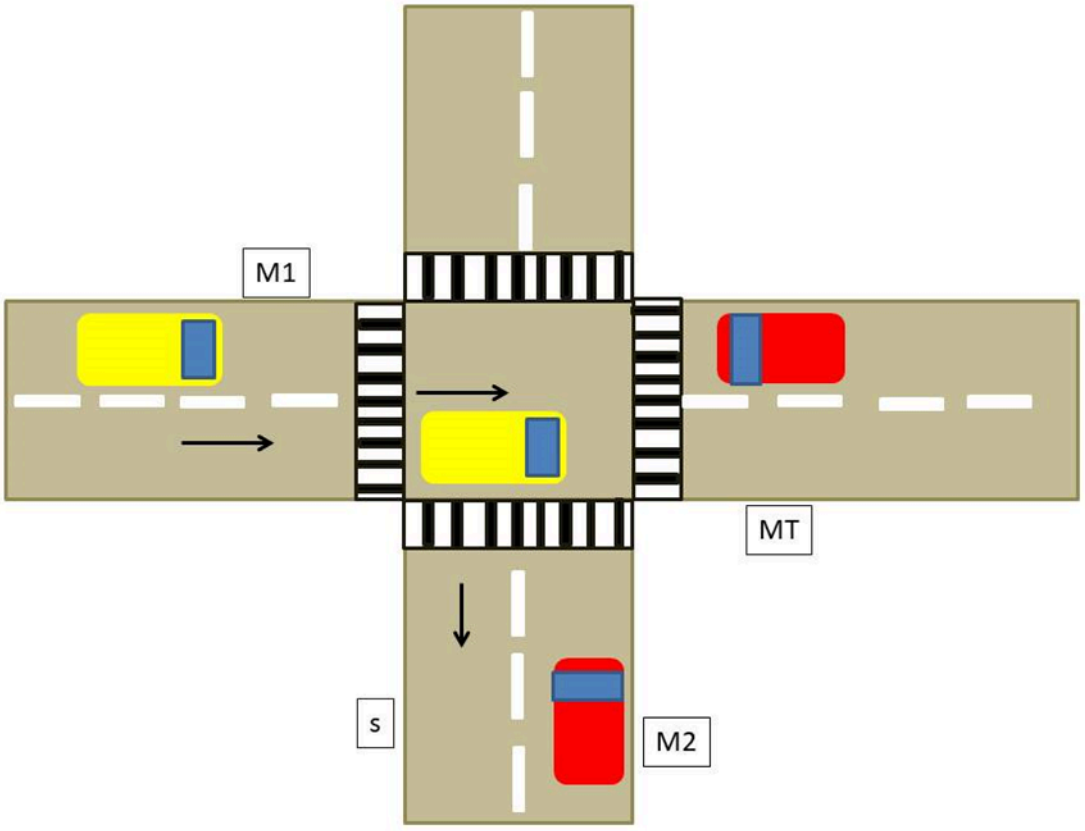
This project was completed entirely through self-directed research and learning, and it gave me a deeper understanding of digital logic design, state machines, and hardware simulation. Implementing and testing the design on the **PYNQ Z2 board** was a rewarding experience that enhanced my practical skills in Verilog and FPGA development.

I would also like to acknowledge the open-source tools, documentation, and community forums that were invaluable in resolving challenges during the development process.

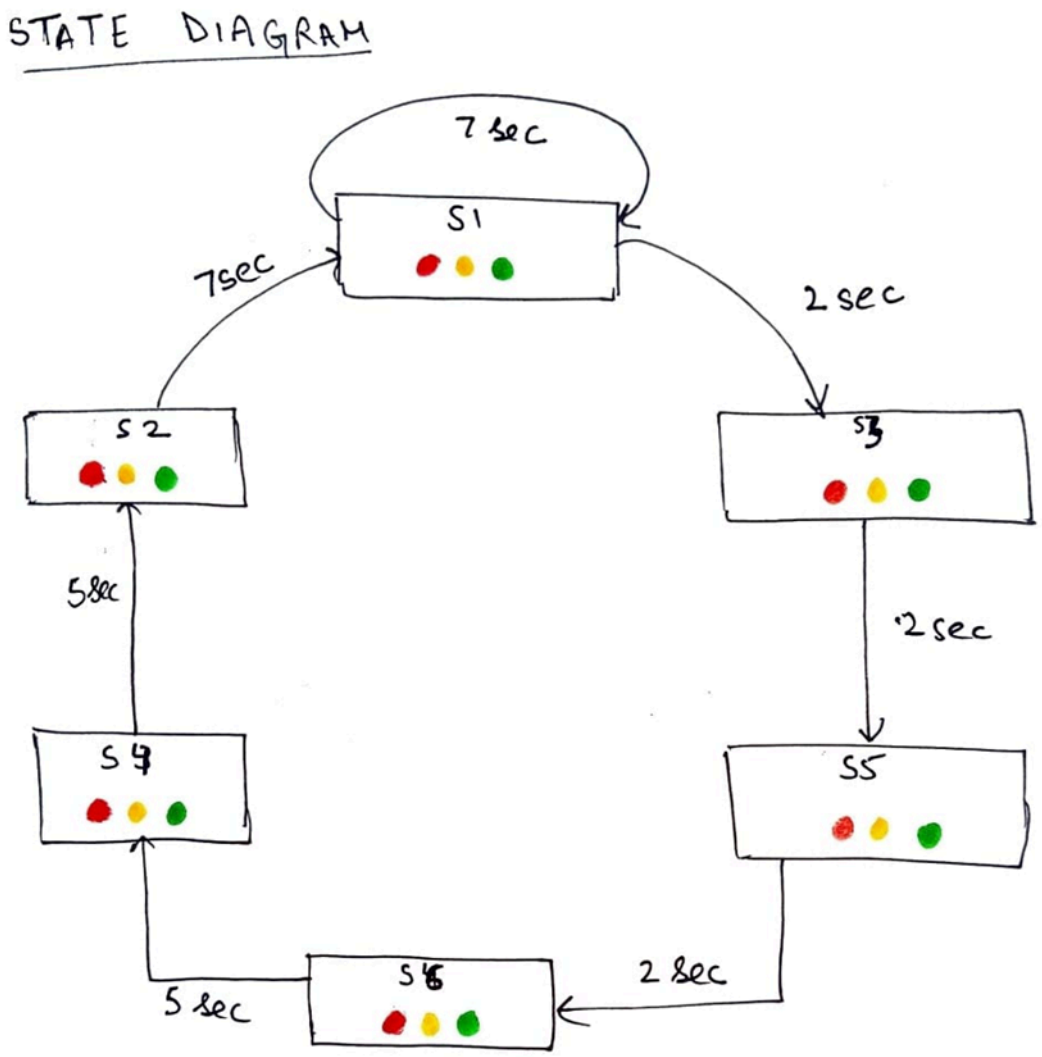
Lastly, I am grateful for the encouragement and support from my personal circle, which helped me stay motivated and focused throughout the project.

PROBLEM STATEMENT:

FPGA- Based traffic light controller with priority system



STATE DIAGRAM:



STATE TABLE:

STATE TABLE

PRESENT STATE	LIGHTS	NEXT STATE
S1	001	S1
S2	001	S2
S3	100	S4
S4	001	S5
S5	100	S6
S6	010	S6

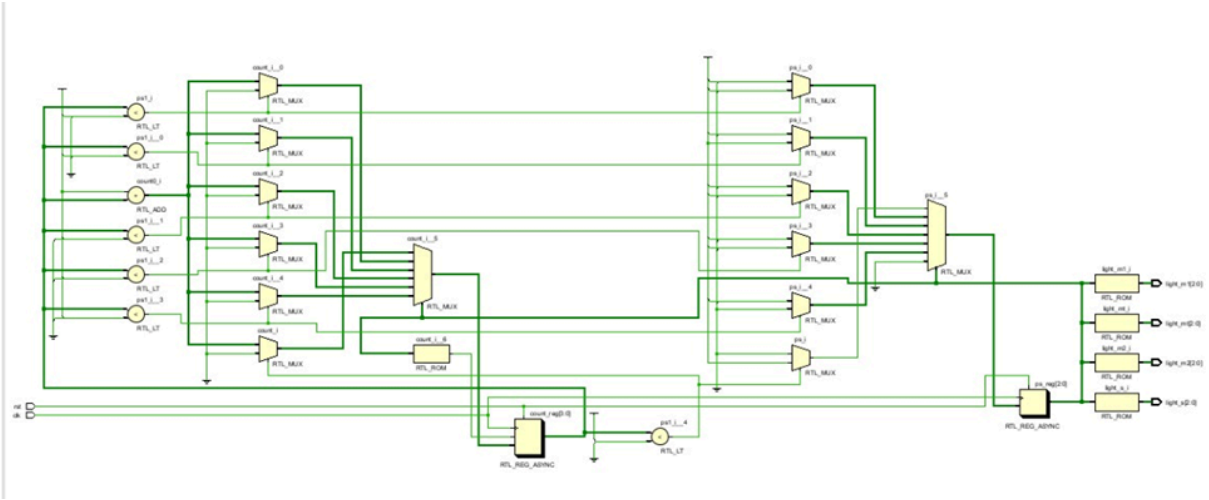
VERILOG CODE:

```
module ks_1(
    input clk,rst,
    output reg [2:0]light_m1,
    output reg [2:0]light_s,
    output reg [2:0]light_mt,
    output reg [2:0]light_m2
    );
    parameter s1=0, s2=1, s3=2, s4=3, s5=4, s6=5;
    reg[3:0]count;
    reg[2:0]ps;
    parameter sec7=7, sec9=9, sec13=13, sec2=2, sec1=1, sec3=3;

    always@(posedge clk or posedge rst)
    begin
    if(rst==1)
    begin
    ps<=s1;
    count<=0;
    end
    else

              case(ps)
              s1: if (count<sec7)
                        begin
                        ps<=s1;
                        count<=count+1;
                        end
                  else
                        begin
                        ps<=s2;
                        count<=0;
                        end
               s2: if (count<sec9)
                        begin
                        ps<=s2;
                        count<=count+1;
                        end
                  else
                        begin
                        ps<=s3;
                        count<=0;
```

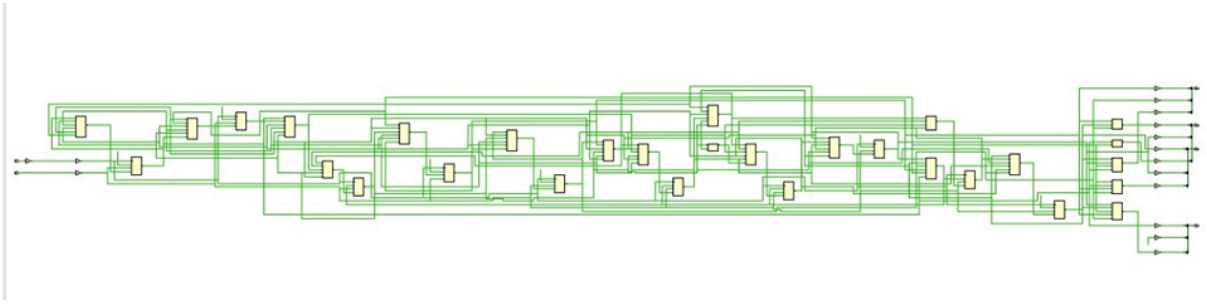
```
            endcase
    end

    always@(ps)
    begin
          case(ps)
               s1:
               begin
                    light_m1<=3'b001;
                    light_m2<=3'b001;
                    light_mt<=3'b100;
                    light_s<=3'b100;
                    end
               s2:
               begin
                    light_m1<=3'b001;
                    light_m2<=3'b010;
                    light_mt<=3'b100;
                    light_s<=3'b100;
                    end
               s3:
               begin
                    light_m1<=3'b001;
                    light_m2<=3'b100;
                    light_mt<=3'b001;
                    light_s<=3'b100;
                    end
               s4:
               begin
                    light_m1<=3'b010;
                    light_m2<=3'b100;
                    light_mt<=3'b010;
                    light_s<=3'b100;
                    end
               s5:
```

```
            s6:
            begin
                light_m1<=3'b100;
                light_m2<=3'b100;
                light_mt<=3'b100;
                light_s<=3'b100;
                end
            default:
            begin
                light_m1<=3'b000;
                light_m2<=3'b000;
                light_mt<=3'b000;
                light_s<=3'b000;
                end
                endcase
        end
endmodule
```

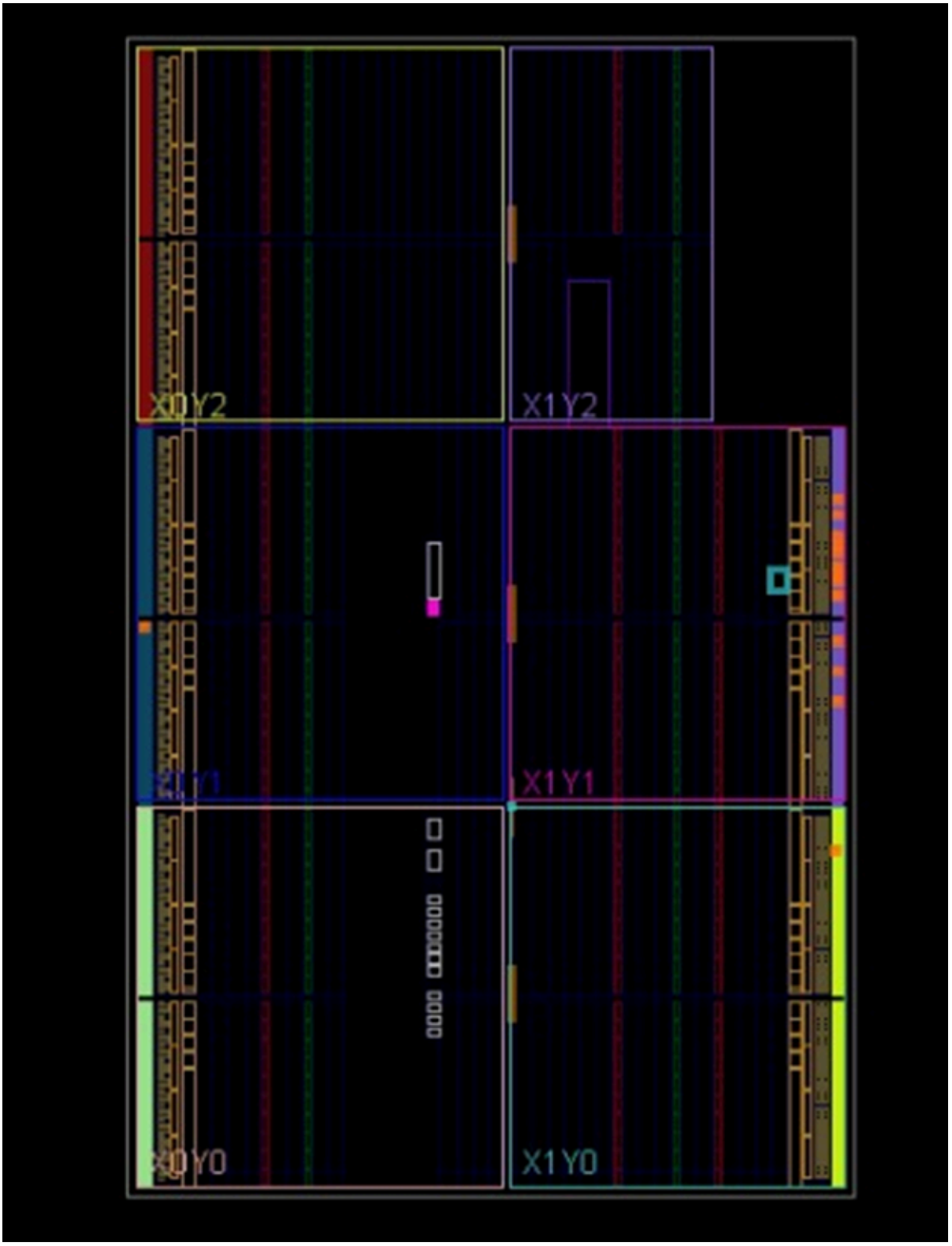
SCHEMATIC ELABORATED DESIGN:



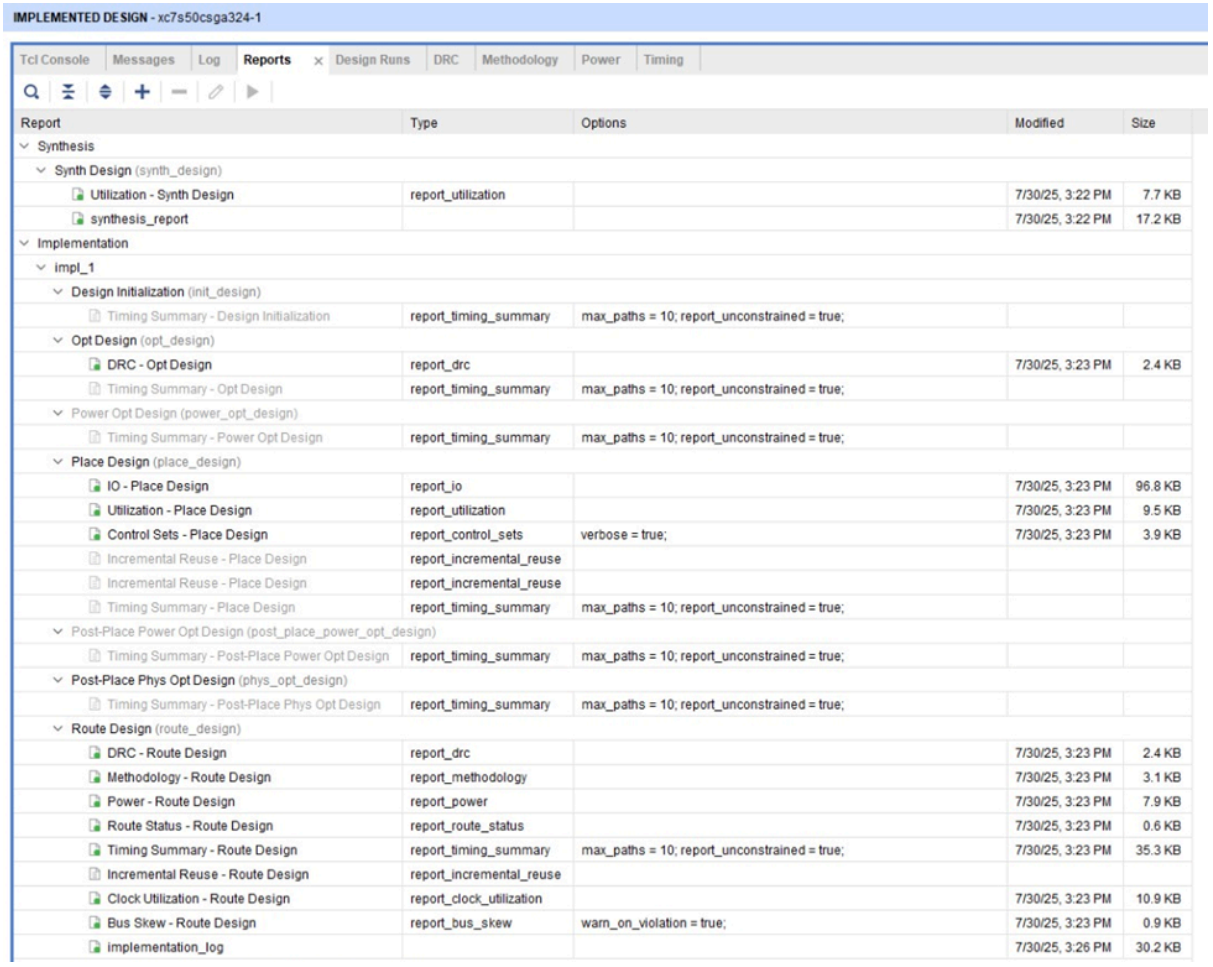
SYNTHESIZED SCHEMATIC DESIGN:



IMPLEMENTED DESIGN:



REPORTS OF IMPLEMENTED DESIGN:

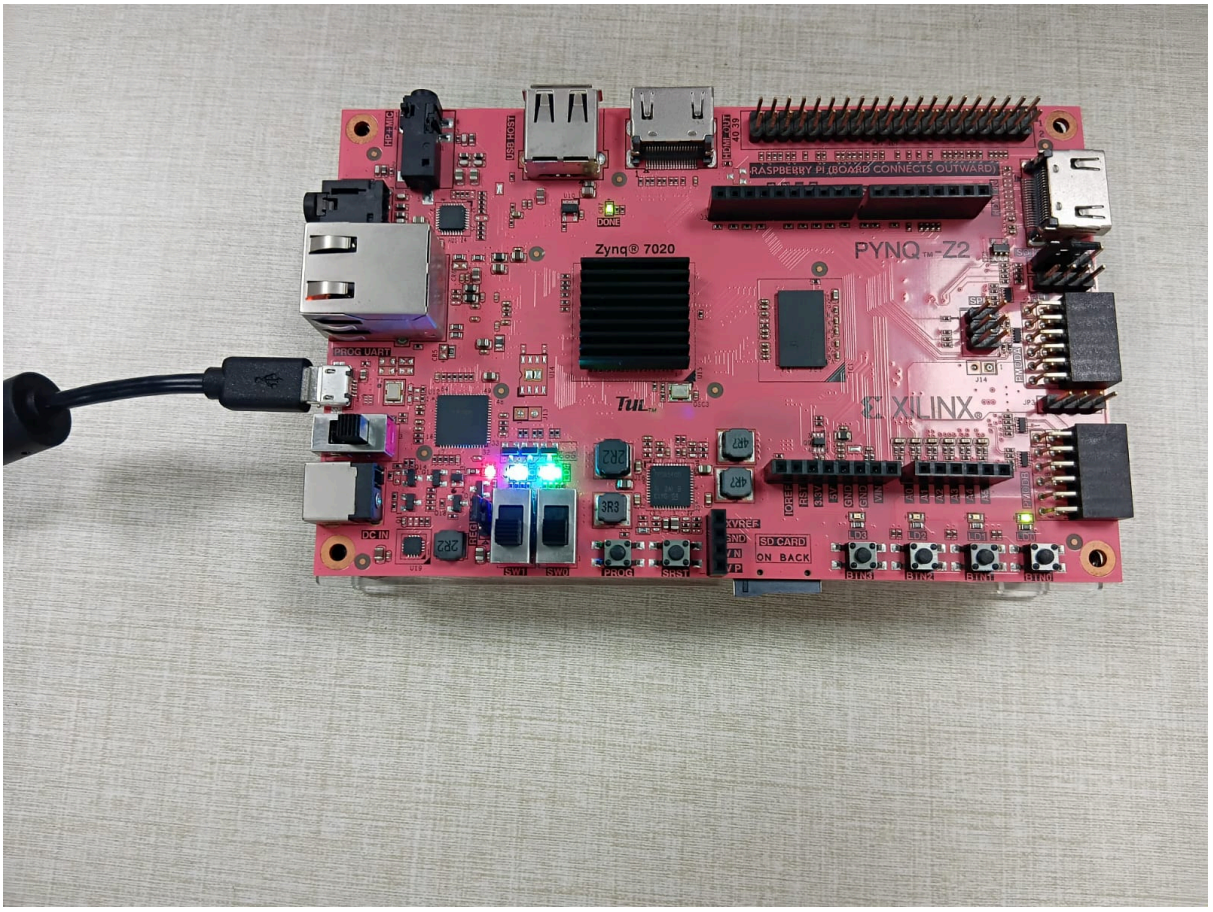


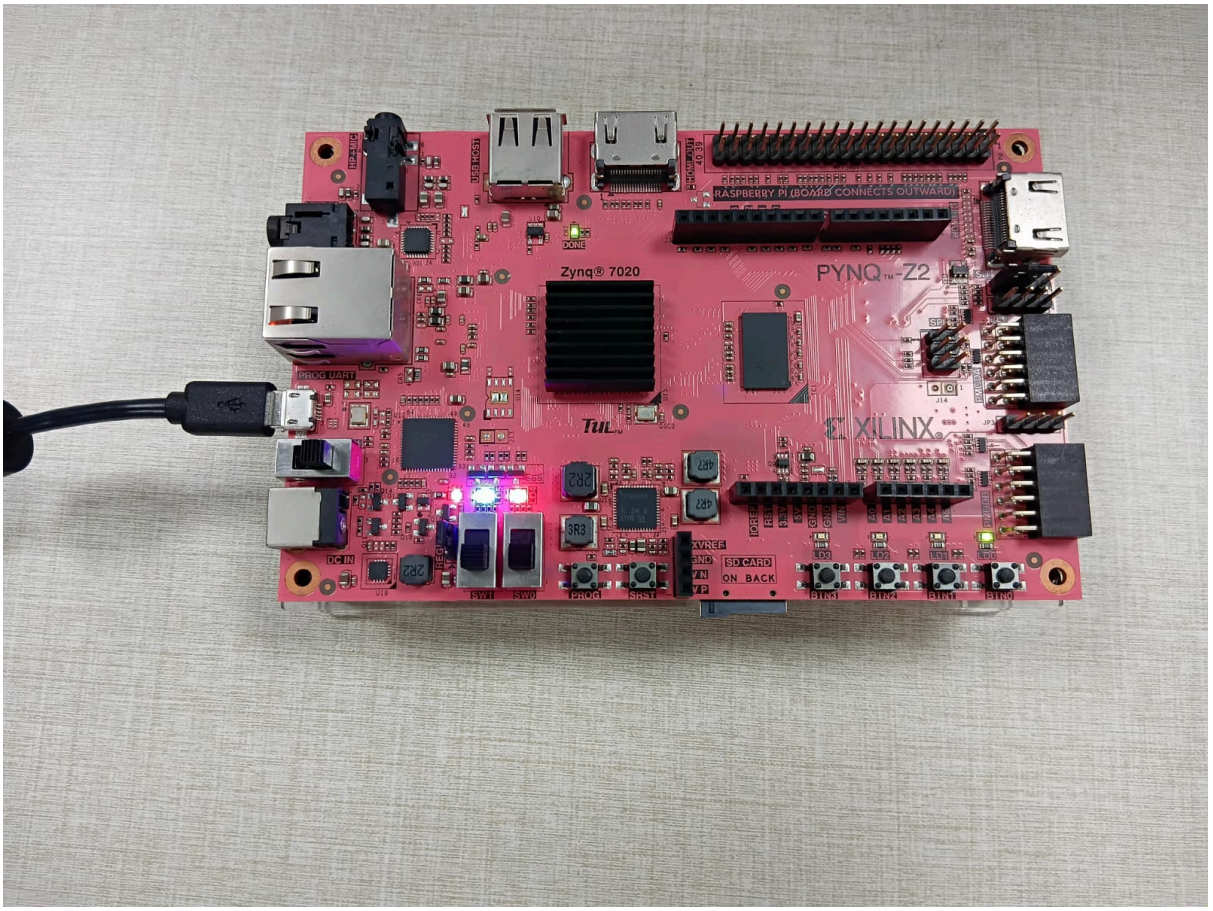
IMPLEMENTED DESIGN - xc7s50csga324-1

Tcl Console | Messages | Log | **Reports** | Design Runs | DRC | Methodology | Power | Timing

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		7/30/25, 3:22 PM	7.7 KB
synthesis_report			7/30/25, 3:22 PM	17.2 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc		7/30/25, 3:23 PM	2.4 KB
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io		7/30/25, 3:23 PM	96.8 KB
Utilization - Place Design	report_utilization		7/30/25, 3:23 PM	9.5 KB
Control Sets - Place Design	report_control_sets	verbose = true;	7/30/25, 3:23 PM	3.9 KB
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc		7/30/25, 3:23 PM	2.4 KB
Methodology - Route Design	report_methodology		7/30/25, 3:23 PM	3.1 KB
Power - Route Design	report_power		7/30/25, 3:23 PM	7.9 KB
Route Status - Route Design	report_route_status		7/30/25, 3:23 PM	0.6 KB
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;	7/30/25, 3:23 PM	35.3 KB
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization		7/30/25, 3:23 PM	10.9 KB
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;	7/30/25, 3:23 PM	0.9 KB
implementation_log			7/30/25, 3:26 PM	30.2 KB

FEW IMAGES OF THE FPGA BOARD:


RASPBERRY PI (BOARD CONNECTS OUTWARD)
Zynq® 7020
PYNQ™-Z2
XILINX
PROG UART
DC IN
SD CARD
ON BACK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