Design HW 1

Start Assignment

- Due Sep 20 by 10pm
- Points 30
- Submitting a file upload
- File Types sv and txt
- Available until Sep 20 at 10:05pm

Design a floating point multiplier. This are inspired by IEEE 754-2019 (See the SJSU library to download the specification)

The Floating point is 1 bit sign, 5 bits exponent biased at +16 (6'b10000), and 5 bits fraction (with a hidden 1, 6 effective bits) for 11 bits total

The multiplier and adder do not generate overflow or underflow, but "saturate" at +/- 8192.5

There is no need for NAN or infinities in the design due to the saturation applied at all steps.

A true Zero is represented by all zero bits in the exponent and fraction. Any other coding of the 11 bits represents a non zero value.

A true Zero is positive (sign bit is zero) when created by the multiplier. (-0 becomes 0)