San Jose State University

Department of Computer Engineering

CMPE 200 Report

Assignment 5 Report

Title Processor Design (1): Design Code Review and Functional Verification

Semester: Fall 2023 **Date:** 10/21/2023

by

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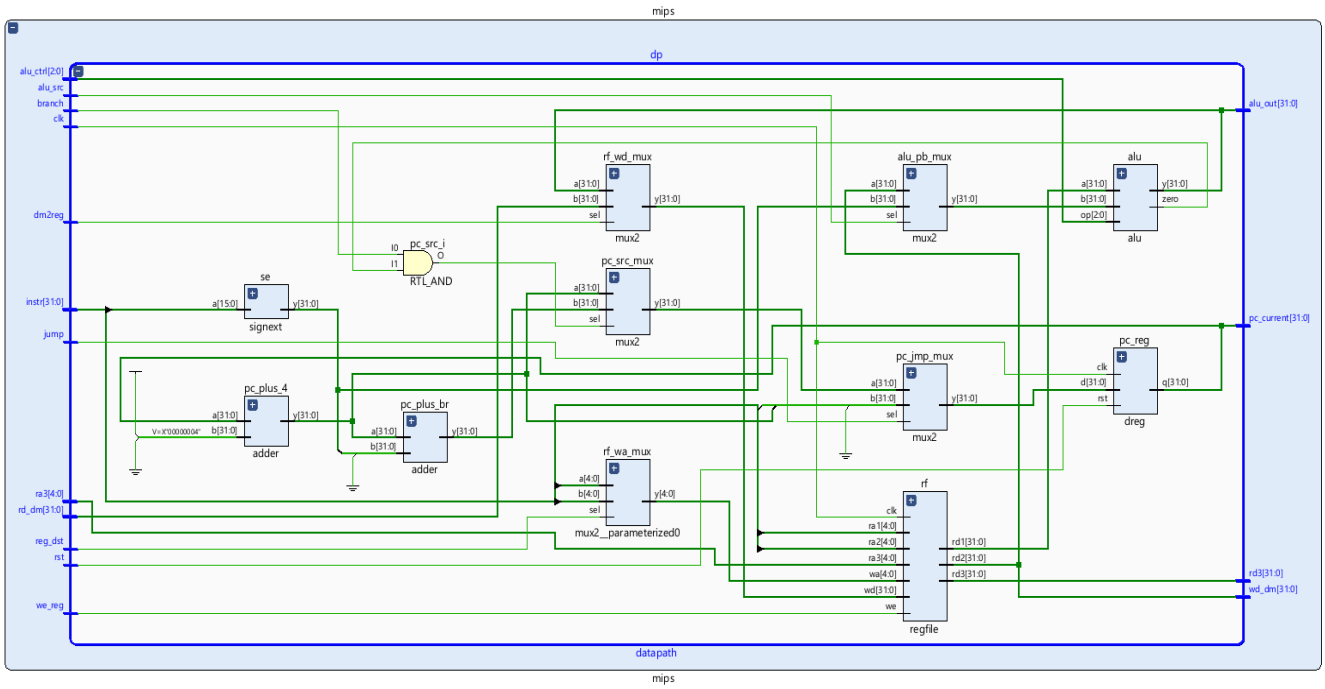
Goals of this lab assignment:

1. Review the RTL Verilog design code for the initial version of the single-cycle MIPS processor discussed in class to gain hands-on processor design experience.
2. Learn the basic technique for functionally verifying a processor.

Task 1: Block Diagrams for Initial Design of MIPS Processor

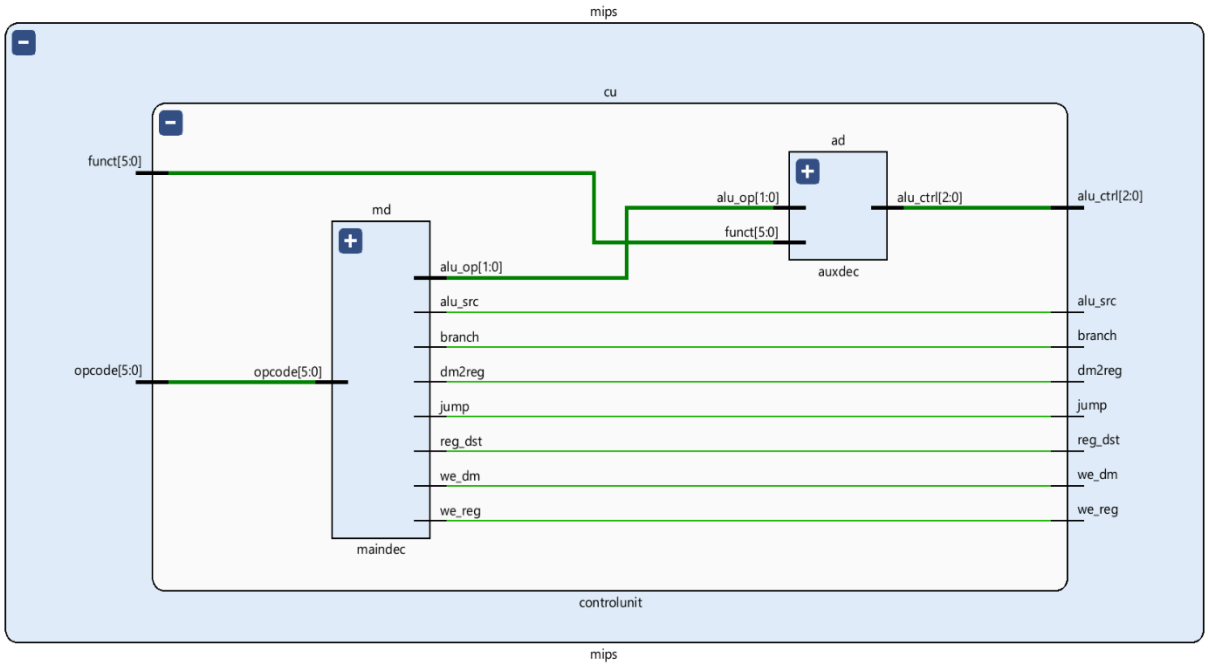
a) Datapath with Microarchitecture Details:

The Datapath block diagram illustrates the flow of data through the processor's various components. It includes the ALU, registers, multiplexers, and other essential components for data manipulation and processing. The microarchitecture details highlight the specific operations and data paths within the Datapath, excluding memory components.



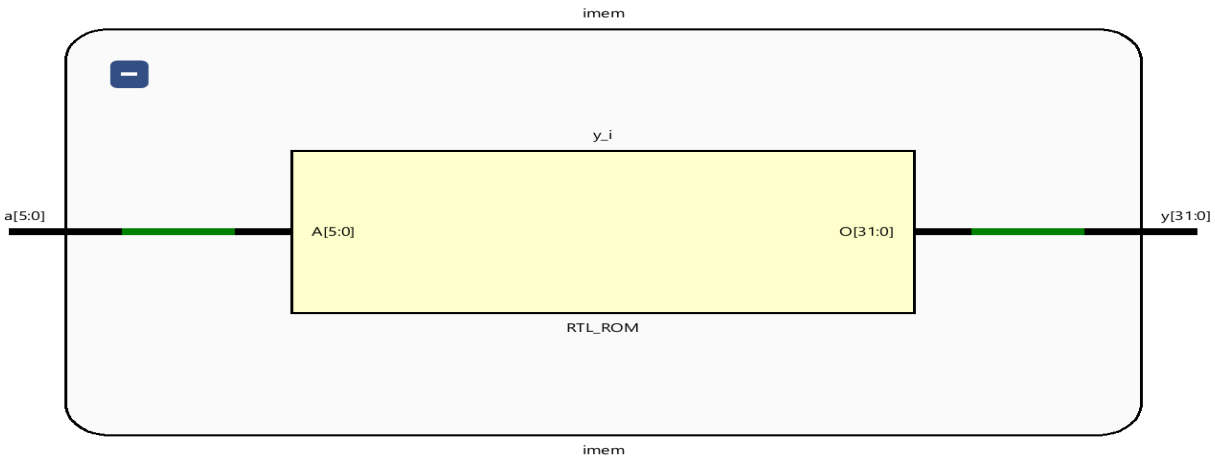
b) Control Unit with Microarchitecture Details:

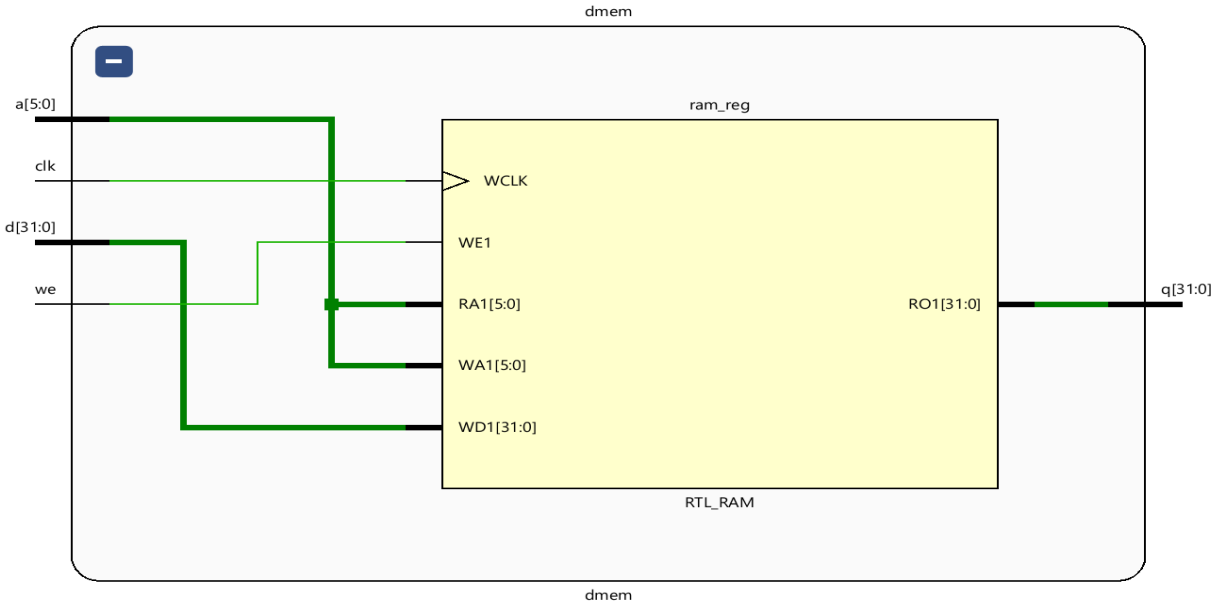
The control unit block diagram outlines the control signals and their generation, which manage the flow of data within the processor. It incorporates various control lines that dictate the behavior of the Datapath, including the selection of multiplexers, enabling of ALU operations, and the handling of instruction execution.



c) Instruction Memory and Data Memory:

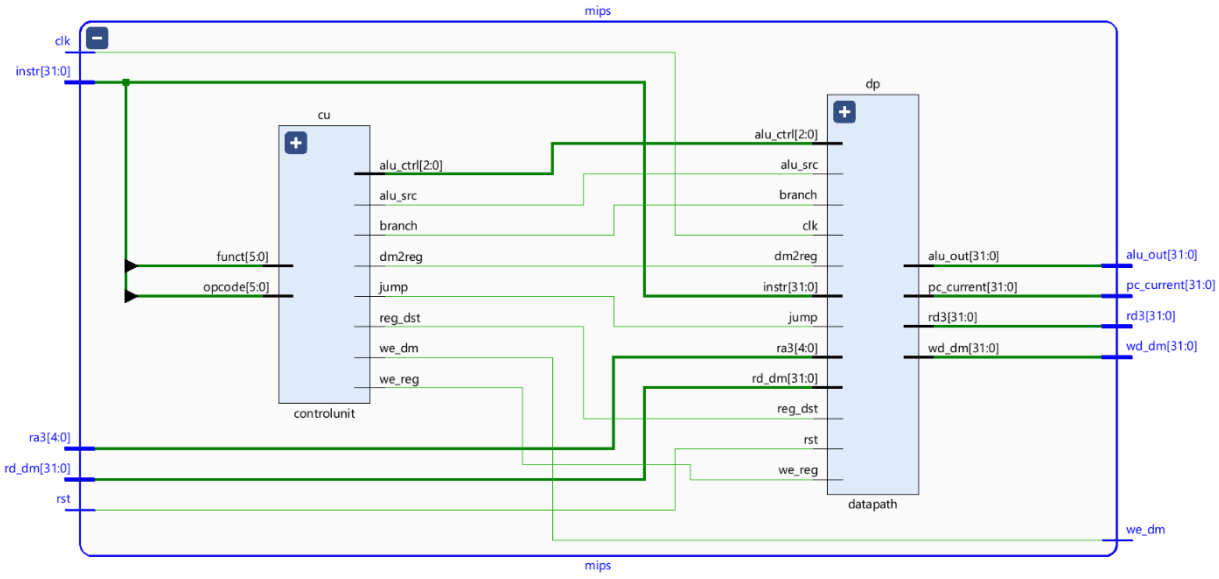
The instruction memory and data memory block diagrams exhibit the storage components within the processor. The instruction memory stores the program instructions, while the data memory stores data for processing. These components facilitate the reading and writing of instructions and data during program execution.





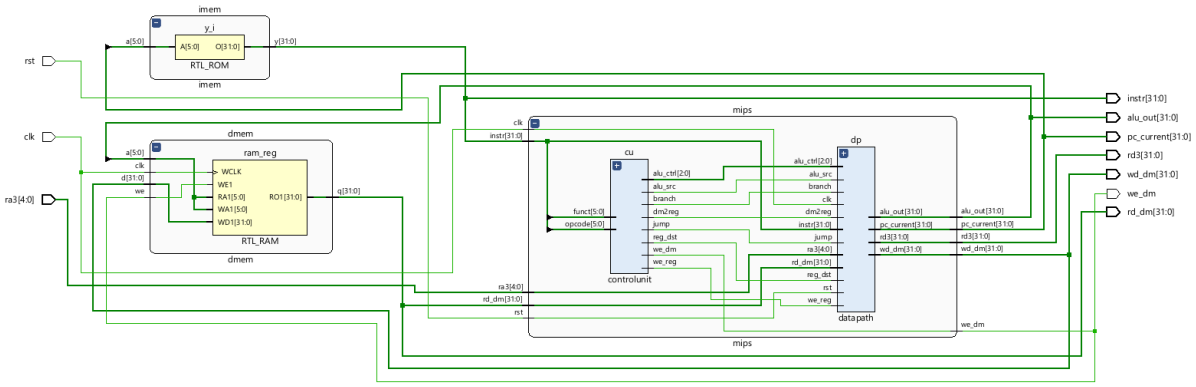
d) Processor Core:

The processor core diagram showcases the interconnection between the Datapath and its control unit, emphasizing how the control signals from the control unit affect the operations in the Datapath. It demonstrates the integration of the microarchitecture elements to form the core processing unit of the MIPS processor.



e) Complete Processor:

The complete processor block diagram illustrates the interconnections between the processor core and its memory components. It displays how the processor interacts with the instruction and data memory to execute programs and store data during runtime.

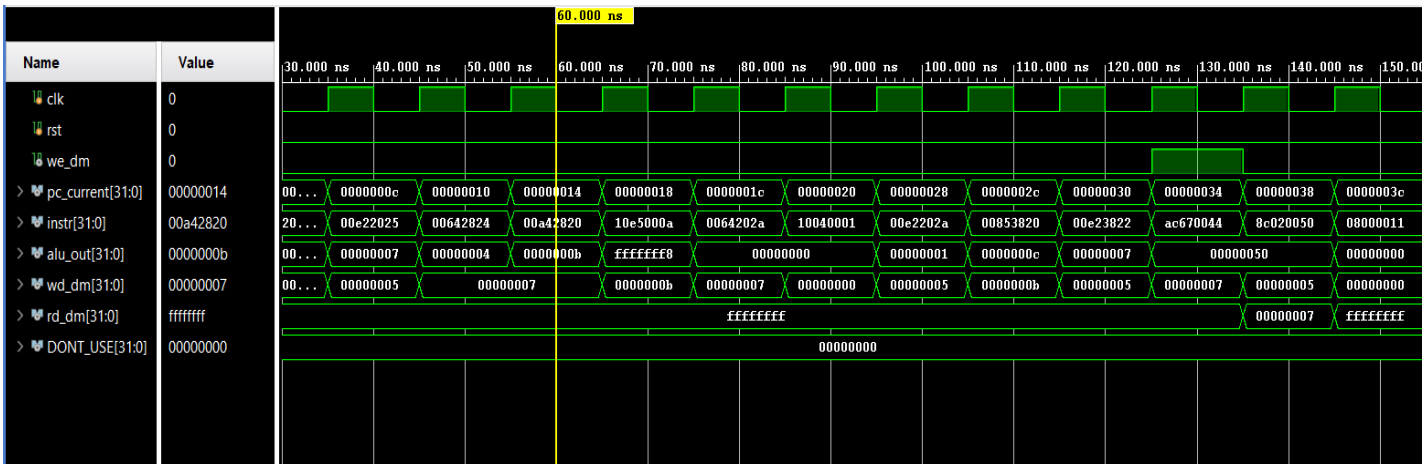


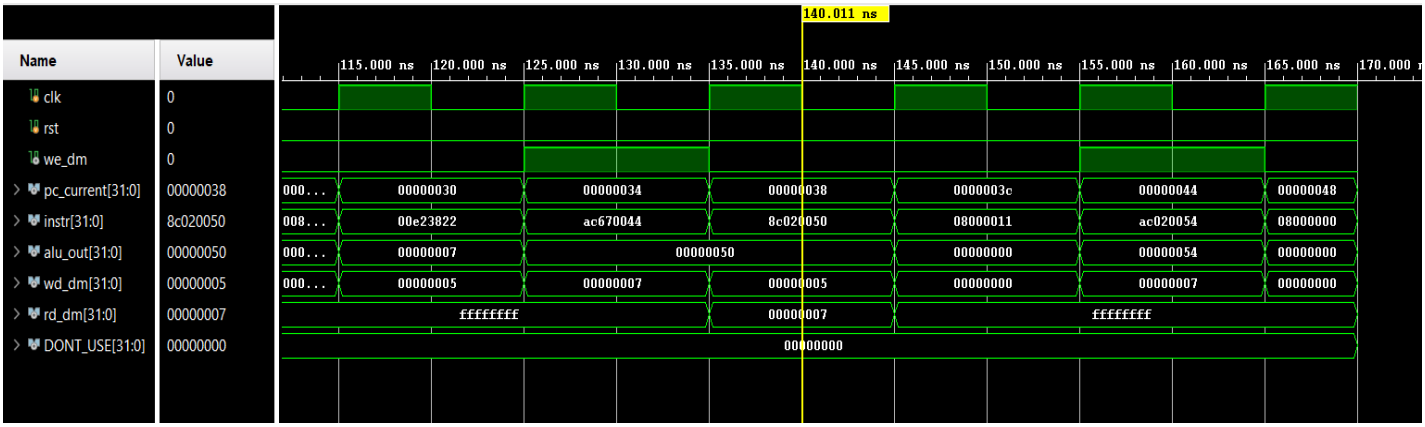
Task 2: Functional Verification of MIPS Processor

Using the provided resources in the archive, we built the initial design of the single-cycle MIPS processor and its accompanying test bench. We functionally verified the processor based on the sample program provided. The waveform monitoring involved the following signals:

- **clk:** Represents the clock signal for synchronization.
- **rst:** Indicates the reset signal for resetting the processor.
- **pc_current:** Displays the current program counter value.
- **instr:** Illustrates the current instruction being executed.
- **alu_out:** Represents the output of the Arithmetic Logic Unit (ALU).
- **we_dm:** Indicates the write enable signal for data memory.
- **wd_dm:** Represents the data to be written into data memory.
- **rd_dm:** Indicates the data read from the data memory.

The waveforms captured during the functional verification process are attached below with necessary comments and explanations for each signal's behavior and significance during the execution of the sample program.





Conclusion:

The successful functional verification of the MIPS processor, based on the provided sample program, indicates the initial design's operational accuracy and efficiency. The block diagrams and waveforms presented in this report provide a comprehensive understanding of the processor's architecture and functionality during program execution. Any further improvements or optimizations can be implemented based on the insights gained from this initial design and verification process.