EE275

San Jose State University Department of Electrical Engineering

Mini-Project I (Due Sep. 15)

Mini-project I is to be carried out <u>individually</u>. In this mini-project, you are to implement in Verilog or in C/C++/Matlab/Python a subset of the MIPS instruction set architecture (ISA) that can execute the dot product benchmark program as below:

You may use ModelSim, Altera Quartus, Xilinx Vivado, or any other equivalent CAD tool to design and show working simulations of your MIPS design for two vectors. Note that the instruction and data memory should be initialized with the program and data, respectively, in the test bench. The waveform from simulation should clearly show correct cycle-wise working of your design, as well as the correct dot product value at the end.

If using C/C++/Python/Matlab, timing diagrams are not required, but the "status" of the CPU, i.e., value of all relevant registers, for each clock cycle is to be shown. Thus, you are to design an emulator.

For demonstration purpose, the first vector should be 9 single digits taken from your 9-digit student ID and the second vector the first vector added digit-wise by 2. Note that 9 added by 2 is "wrapped around" to 1. For example, if your ID is 012345678, the first vector is (0,1,2,3,4,5,6,7,8) and the second vector (2,3,4,5,6,7,8,9,0), making dot product to $0\times2+1\times3+2\times4+3\times5+4\times6+5\times7+6\times8+7\times9+8\times0=3+8+15+24+35+48+63=196$. Working of your simulation for this demo case should be proven by the screen capture of the corresponding timing diagram or CPU status display.

You should submit the technical report on canvas, following the report writing guideline posted on canvas.