

CMPE 200 – Assignment 1

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System-Level Design Review

Purpose

Review system-level design by designing and functionally verifying a digital system for accelerating the factorial computation. The system should start execution upon receiving an external input “Go” and should output a “Done” signal when the execution is completed. In addition, an “Error” signal should be set when an input greater than 12 is entered.

Background

- 1) The algorithm for computing the factorial of n , i.e., $n! = 1 \times 2 \times \dots \times n$, is shown below:

```
INPUT  $n$ 
 $product = 1$ 
WHILE ( $n > 1$ ) {
     $product = product * n$ 
     $n = n - 1$ 
}
OUTPUT  $product$ 
```

Figure 1. The Factorial of n Algorithm

- 2) Functional building blocks to be used in building the datapath of the system is provided in Fig.2 below. CNT is a down counter with parallel load control and an enable signal; REG is a data register with a load control signal; CMP is a comparator with a GT (greater-than) output; MUL is a combinational multiplier for unsigned integers; MUX is a 2-to-1 multiplexer; BUF is a tri-state buffer for output control, but is recommended to use another 2-to-1 MUX for this purpose.

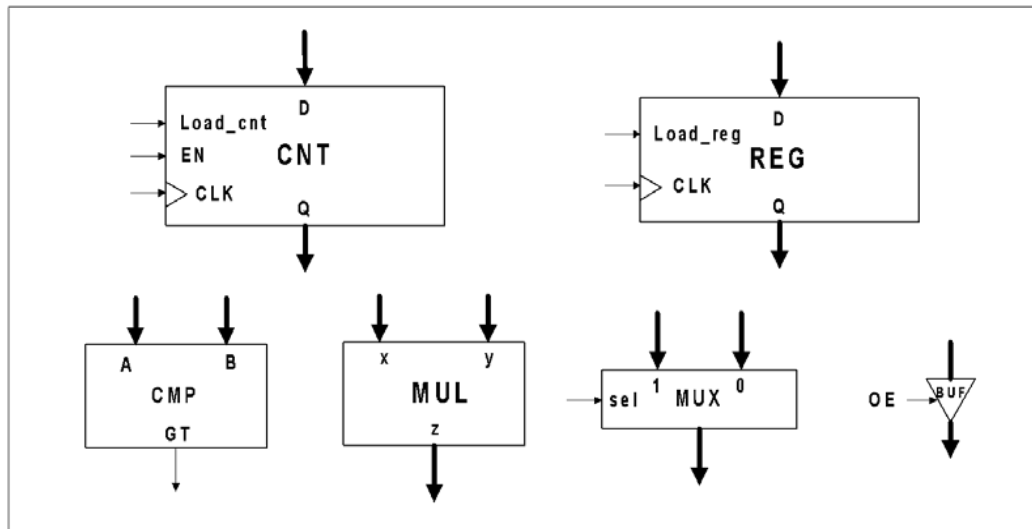


Figure 2. Functional Building Blocks of the Factorial Datapath Module

- 3) The factorial accelerator shall calculate and display results up to 12! (which is 0x1C8CFC00). Inputs for n should be unsigned. Use only one of each building block in Fig. 2 to build the accelerator's datapath (it is recommended to use a second 2-to-1 MUX to replace the output buffer BUF). In order to capture inputs that are greater than 12, an additional comparator (or some simple gate-level logic) will be needed. Except these, no other submodule should exist within the datapath. Parameterize the data path elements to make it easier for scaling the data width.

Tasks

- 1) Design the system's datapath using the given building blocks
- 2) Draw the two-piece (CU-DP) system block diagram that shows all relevant signals
- 3) Draw the ASM chart which describes the cycle-by-cycle operations of the datapath
- 4) Draw bubble diagram for the "next state logic" (NS) part of the control unit
- 5) Construct an output table for the "output logic" part of the control unit
- 6) Based on the above, write Verilog design code for the factorial accelerator, as well as testbench code to functionally verify your design
- 7) Write a report based on your work, with the following requirements (this is also the standard for future reports):
 - (1) Cover page (you can leave the Lab Checkup Record field blank)
 - (2) All requirements introduced in the Lab Report Requirements & Schematic Drawing Guidelines
 - (3) Appendices including the following:
 - (a) diagrams and table mentioned in Tasks 1 – 5, generated by Visio or other tools
 - (b) source code for both design and verification
 - (c) waveforms captured from your simulation results