EE287
Project S’23

FIR filter

You are to design a 29 tap FIR filter. The filter works on I Q signals (imaginary numbers where Q is the imaginary term) The filter is symmetrical. An FIR filter multiplies samples by a coefficient, and then adds the results together to give a result. The filter coefficients for the first and last 14 coefficients are the same. The center coefficient is applied to one sample.

The FIR filter contains the last 29 samples for processing. When a new sample is processed, the oldest contained sample is discarded. (Like a shift register)

Constraints:

- The clock frequency is 300MHz (Design will be synthesized to this clock rate)
- The design is limited to 5 complex multipliers. (4 multipliers per complex multiply) or 20 total multipliers.
- A filter operation must be performed in no more than 3 clock cycles. (100MHz sample rate)
- The design contains an input FIFO with a two flag push model of at least 4 samples. (Need to keep track of full and empty)
- Input data is fixed binary point 1.23 signed data The input ranges from -1<x<1
- The coefficients are 3.24 fixed signed binary. The filter coefficients range from -4<x<4
- Output data is fixed binary point 8.24
  - The filer can have a gain > 1
  - Higher precision is kept internally, and the results rounded towards zero. (Truncate positive values, increment negative values in position 8.25)
- All values reset to zero, including the FIFO

Bits:

Each complex multiply has one add, and then 29 values are added together. This implies keeping an additional 5 bits to the left and right of the binary point during the summation.
The data after a multiply of 3.24 and 1.23 is 4.47 format. Of these, only 8.24 will be in the final answer. Keeping an additional 5 bits above/below the binary precision requires the summation be 9.29 or 38 bits.

Note:

The design can be simplified if the first and last data are added, and then multiplied by the first coefficient. 28/2=>14 multiplies + 1 for center => 15 multiplies/5 multiplies/clock => 3 clocks/filter result. (The test bench only sends coefficient 0-14, 0 and 28 are the same value)

Interface:

The design will consist of a single module named fir29. This module may include other modules as desired. The DW02_mult modules will be included in the test bench.

Name	Width	Dir	Comment
Clk	1	In	Rising edge clock
Reset	1	In	Active high reset signal
PushIn	1	In	A sample push signal
StopIn	1	Out	The input cannot accept a sample
SampI	24	In	The real part of the sample in 1.23 format
SampQ	24	In	The imaginary part of the sample in 1.23 format
PushCoef	1	In	Indicates loading a coefficient
CoefAddr	5	In	The coefficient location 0-15 valid
CoefI	27	In	The coefficient Real part 3.24 format
CoefQ	27	In	The coefficient Imaginary part 3.24 format
PushOut	1	Out	Data out of the filter.
FI	32	Out	Real filtered output 8.24 format
FQ	32	Out	Imaginary filtered output 8.24 format