**LABORATORY-4**

1. **L-1 Cache Enabled and L-2 Cache Disabled**

A white background with black text

Description automatically generated

**Observation:** After executing the timing profiling p-chasing program, if we observe the time of access of each element of the array, we encounter one MISS after every seven HITS. That simply means every time we encounter a MISS, 32 Bytes (8 \* 4 Bytes) of data is fetched from the upper memory hierarchy. Thus, we can say that the **L1 cache line size is 32 Bytes.**

1. **L-1 Cache Disabled and L-2 Cache Enabled**

A screenshot of a computer

Description automatically generated

**Observation:** After executing the timing profiling p-chasing program, if we observe the time of access of each element of the array, we should be observing HIT and MISS sequence repeated similar to L1 enabled and L2 disabled case, but the second MISS couldn’t be observed, the reason for which is under investigation.