**2-bit comparator using Microwind tool**

Mini project-1 Report

*Submitted in Partial Fulfillment of the Requirements for the Degree*

Of

**Bachelor of Technology**

In

**Electronics & Communication Engineering**

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1. **Introduction:**

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number [1]. So, comparator is used for this purpose. Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes (Fig.1). The outcome of comparison is specified by three binary variables that indicate whether A>B, A=B, or A<B. [1]

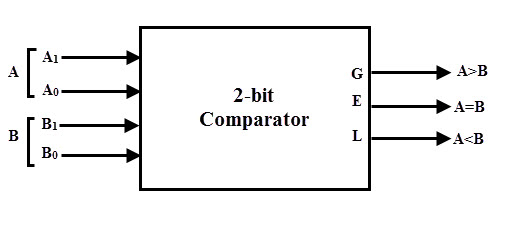


Fig 1: 2-bit comparator diagram

The circuit, for comparing two n-Bit numbers, has 2n inputs & 22n entries in the truth table, for 2-Bit numbers, 4-inputs & 16-rows in the truth table, similarly, for 3-Bit numbers 6-inputs & 64-rows in the truth table. For example, the two 2-bit number are A = A1A0 and B=B1B0. If A1 is not equal to B1, then it is clear that A is greater than B for A1 =1 & B1= 0 or else A is less than B for A0= 0 & B0 =1. At this stage the process of comparison ceases. If the MSBs are equal, i.e., A1=B1 only then we need to compare the next significant bits A0 and B0 and decide whether the number is greater than, less than or equal. So, the comparator produces three outputs as L, E and G corresponds to less than, equal and greater than comparisons. [2]

1. **Truth Table:**

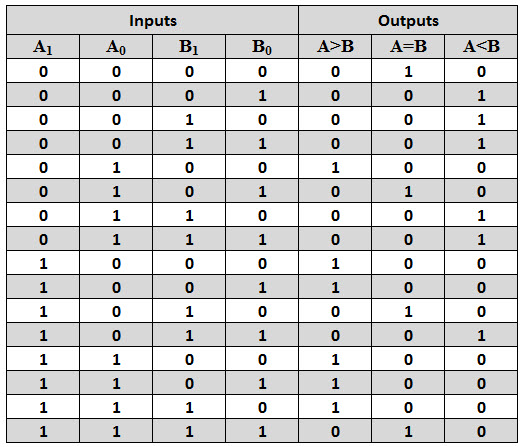


Fig 2: Truth table of 2-bit comparator [3]

1. **Boolean equation & Karnaugh Mapping**

A>B: = A1B1’ + A0B0’A1’B1’ + A0B0’A1B1

= A1B1’ + A0B0’ (A1’B1’ + A1B1)

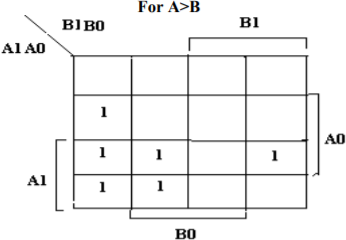


Fig 3: A>B [3]

A=B: =A1‟A0‟B1‟B0‟+A1‟A0B1‟B0+A1A0‟B1B0‟+A1A0B1B0

= (A1‟B1‟+A1B1) (A0‟B0‟+A0B0)

= (A1ʘB1)(A0ʘB0)

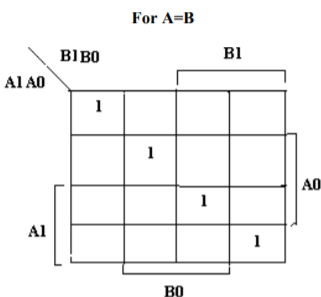


Fig 4: A=B [3]

A<B: = A1‟B1+A0‟B0A1‟B1‟+A0‟B0A1B1

= A1‟B1+A0‟B0(A1‟B1‟+A1B1)

= A1‟B1+A0‟B0 X1

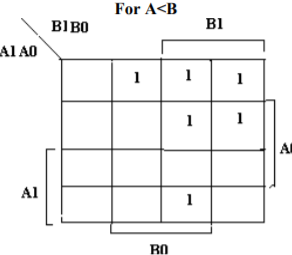


Fig 5: A<B [3]

1. **Gate level circuit diagram**

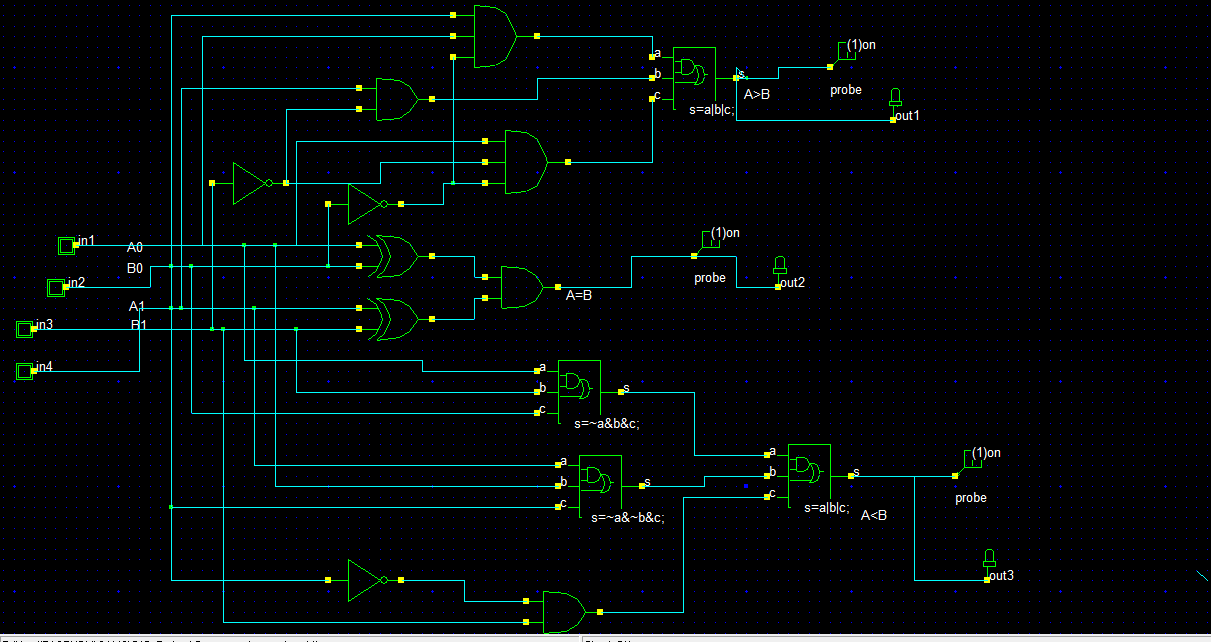
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Fig 6: Gate-level diagram [3]

1. **CMOS implementation:**

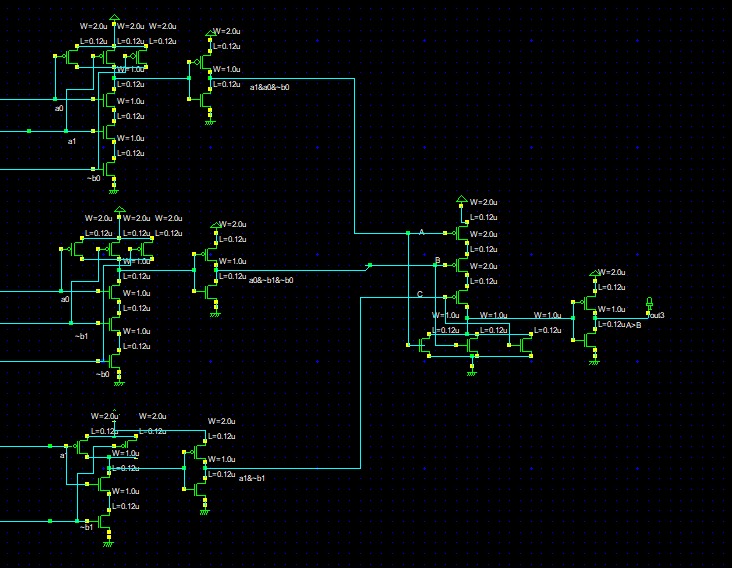
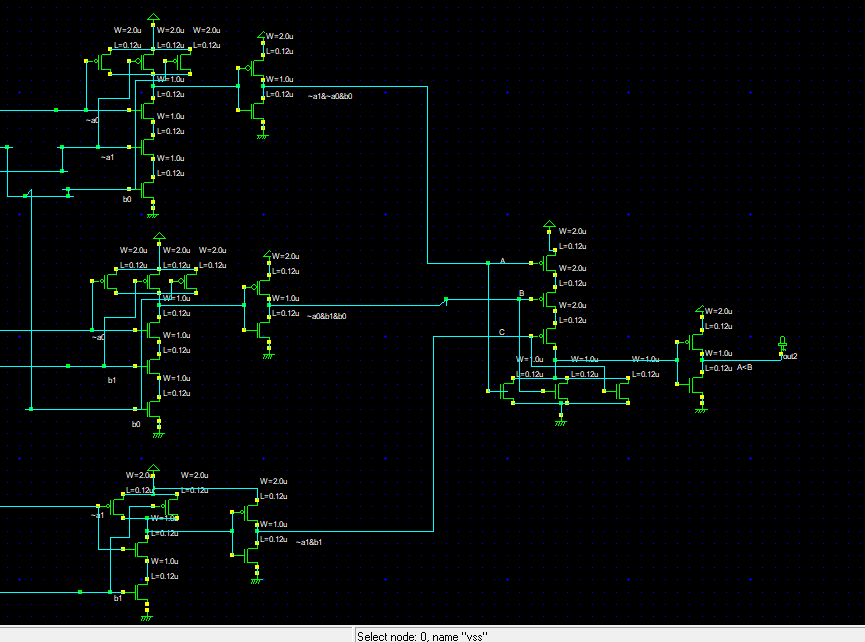


Fig 7: Circuit layout for A>B in Microwind Tool

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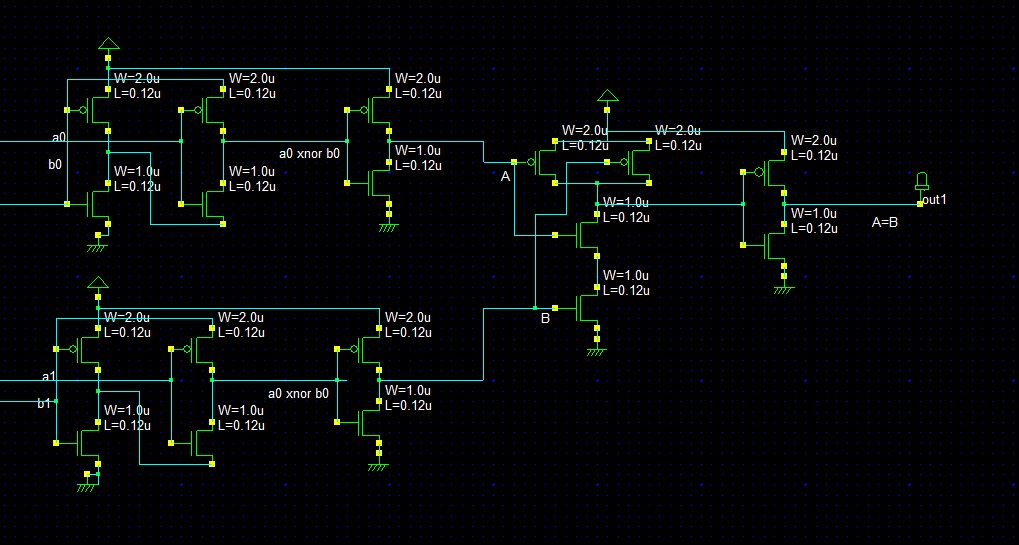
Fig 8: Circuit layout for A<B in Microwind Tool

Fig 9: Circuit layout in Microwind Tool

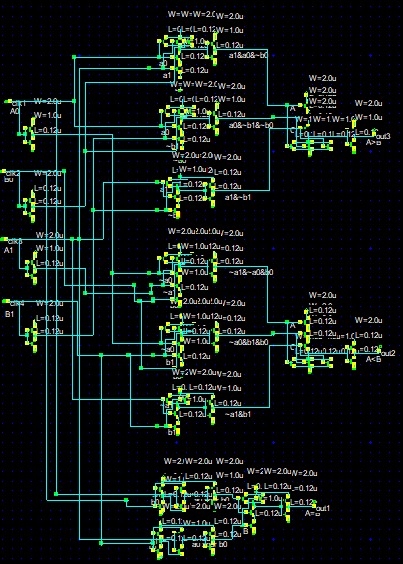


Fig 11: TTL view

**Equivalent Inverter circuit**

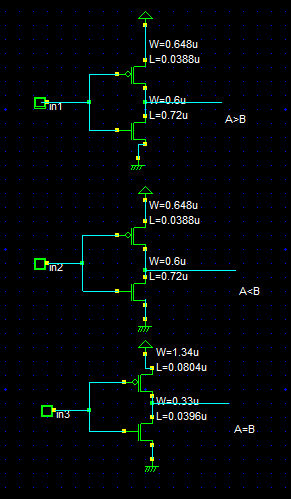


Fig 11: Equivalent Inverter circuit

1. **State the various level of VOL corresponding to various transistor statuses**.

|  |  |  |  |
| --- | --- | --- | --- |
| Output voltage level | | | |
| Output | A=B | A>B | A<B |
| Voh | 1.058 | 1.06 | 1.065 |
| Vol | -0.01 | -0.018 | -0.013 |

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1. **For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?**

Ans: Here, there will be common output resistance because the input value is fixed (A=B) = 1, (A>B) = 1, (A<B) = 1).

1. **For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?**

Ans: For output to be low, we have 4 patterns for each, but since each pattern is making the same effect on both the transistor output resistance will be same for all.

1. **Synthesis Results:**

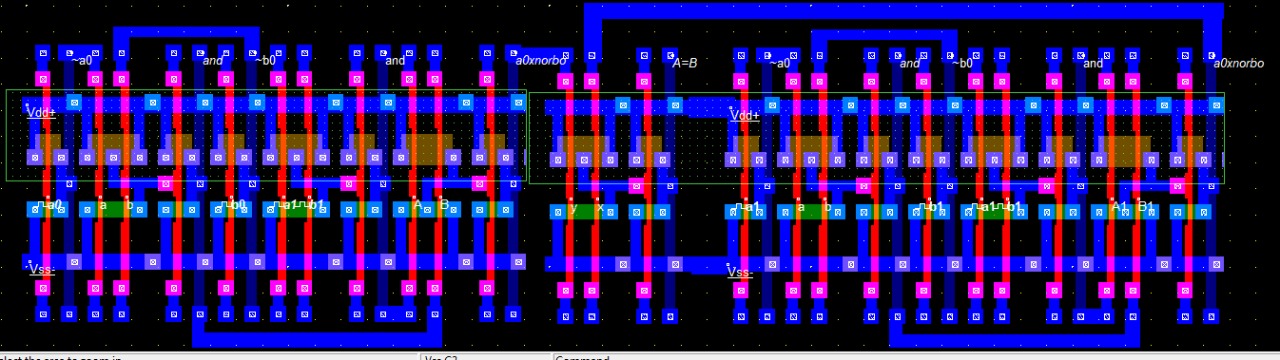


Fig 12: Synthesis of A=B in Microwind

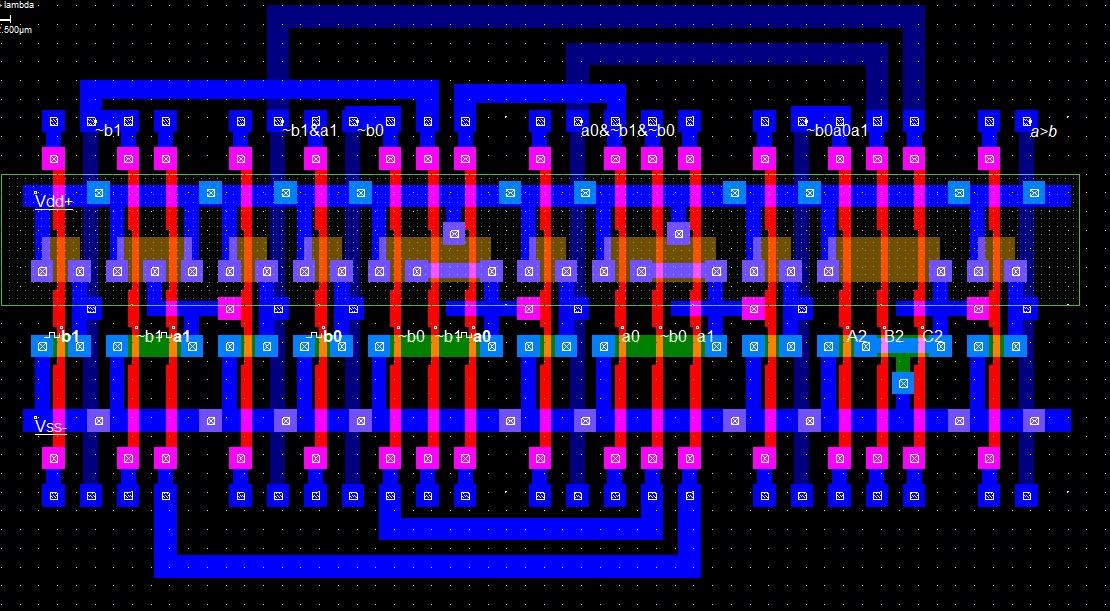


Fig 13: Synthesis of A>B in Microwind

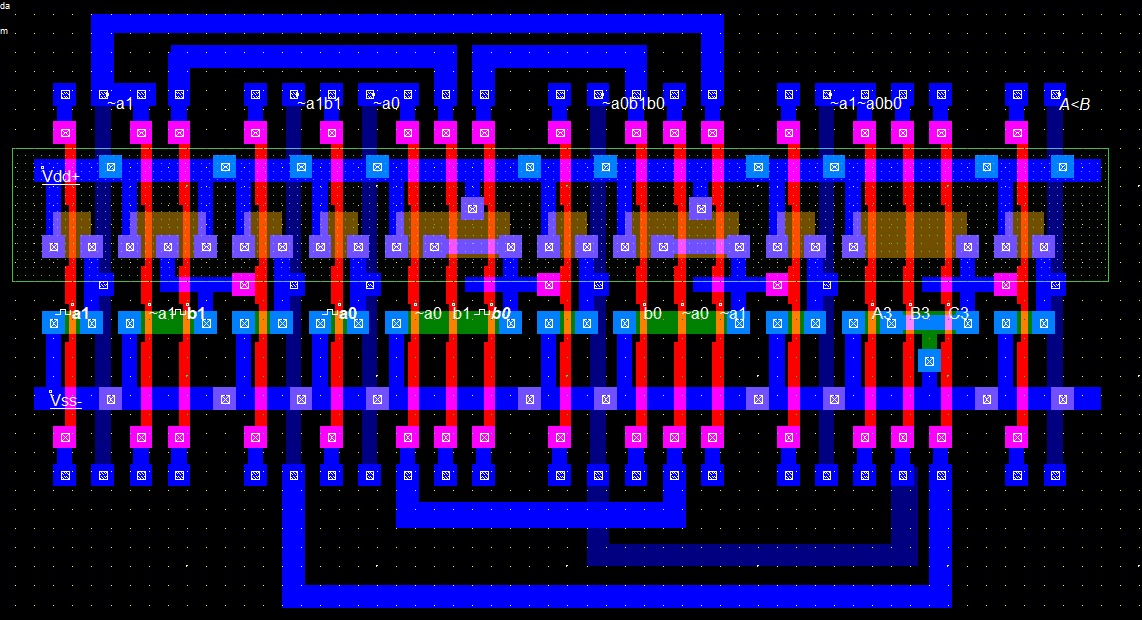


Fig 14: Synthesis of A<B in Microwind

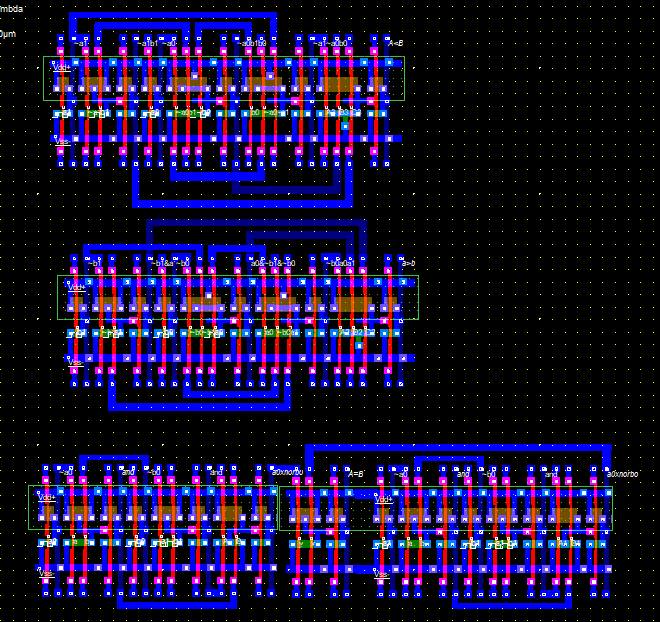


Fig 15: Synthesis in Microwind 2-bit comparator

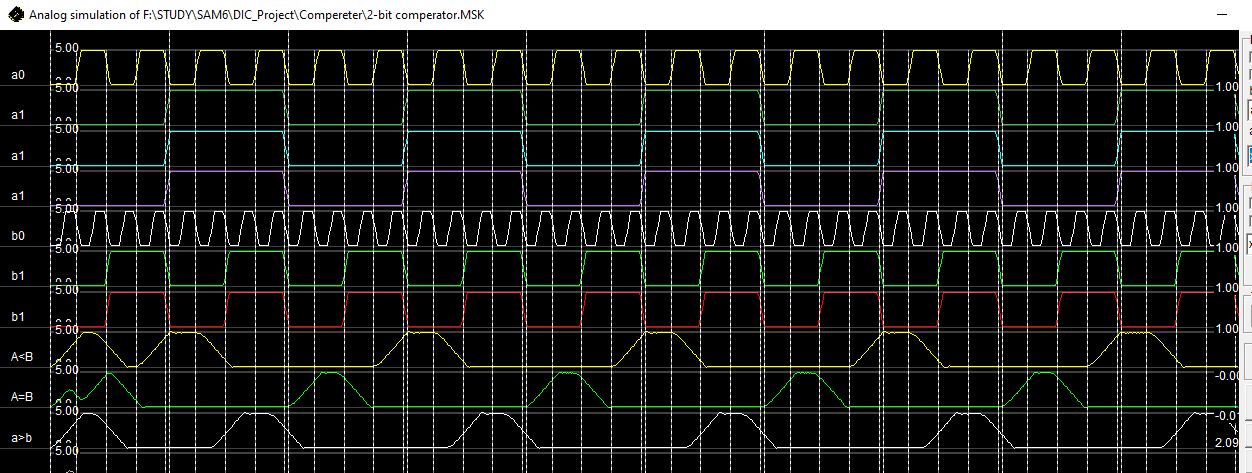


Fig 16: output of 2bit comparator

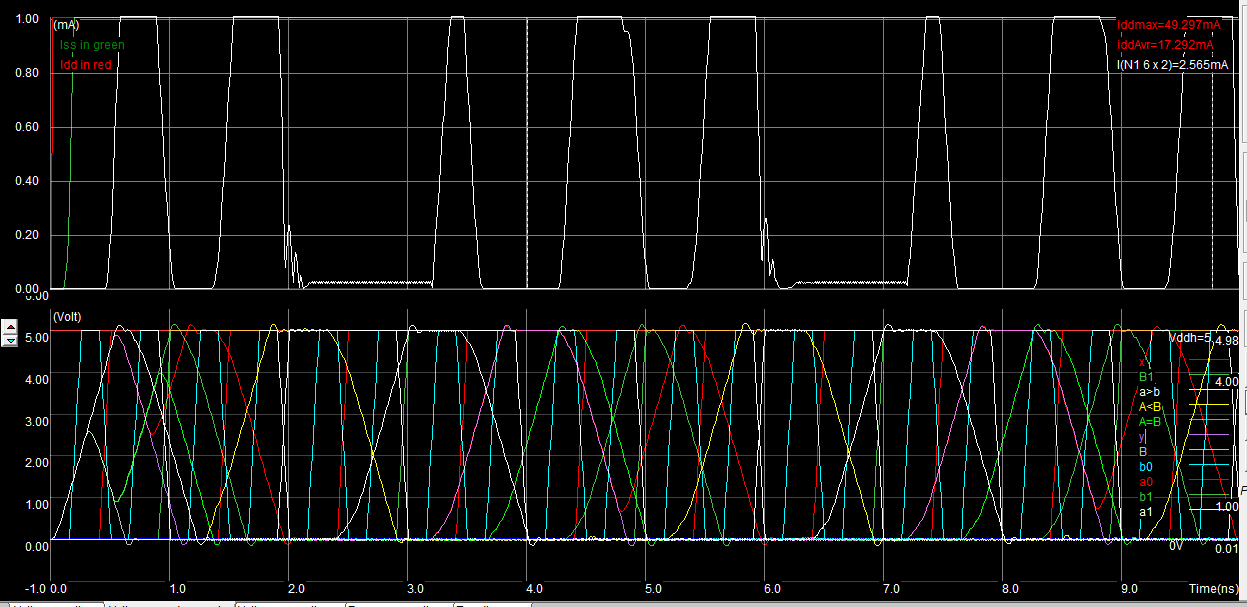


Fig 17: Voltage vs. Current

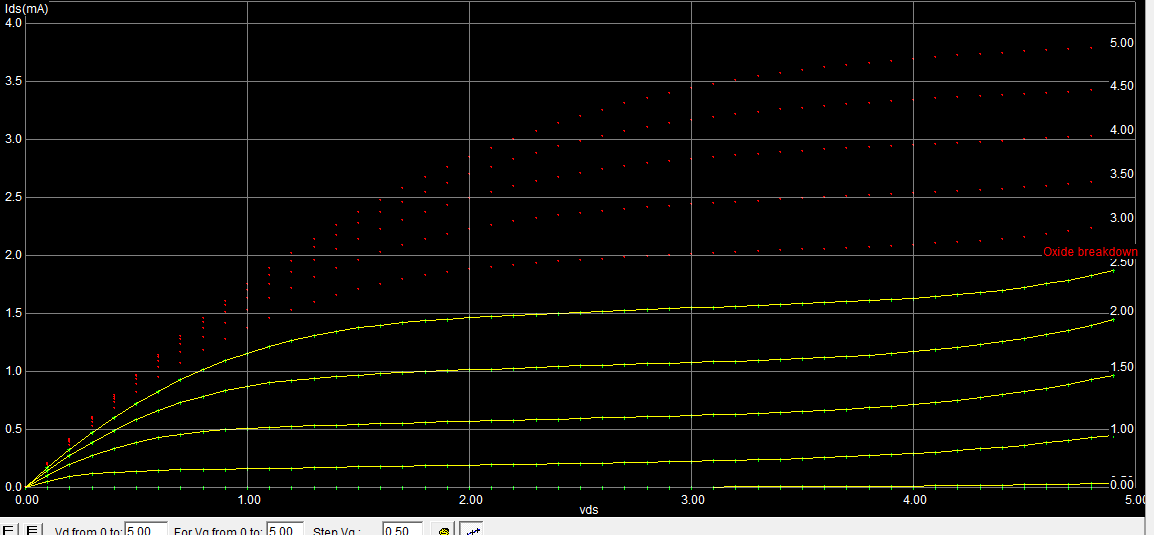


Fig 18: Id vs. Vd

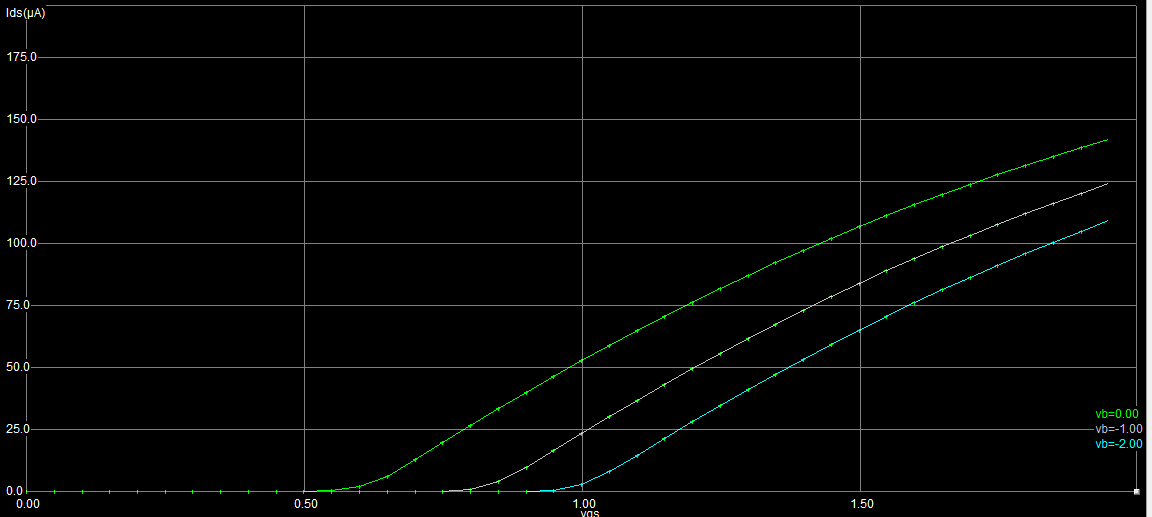


Fig 19: Id vs. Vg

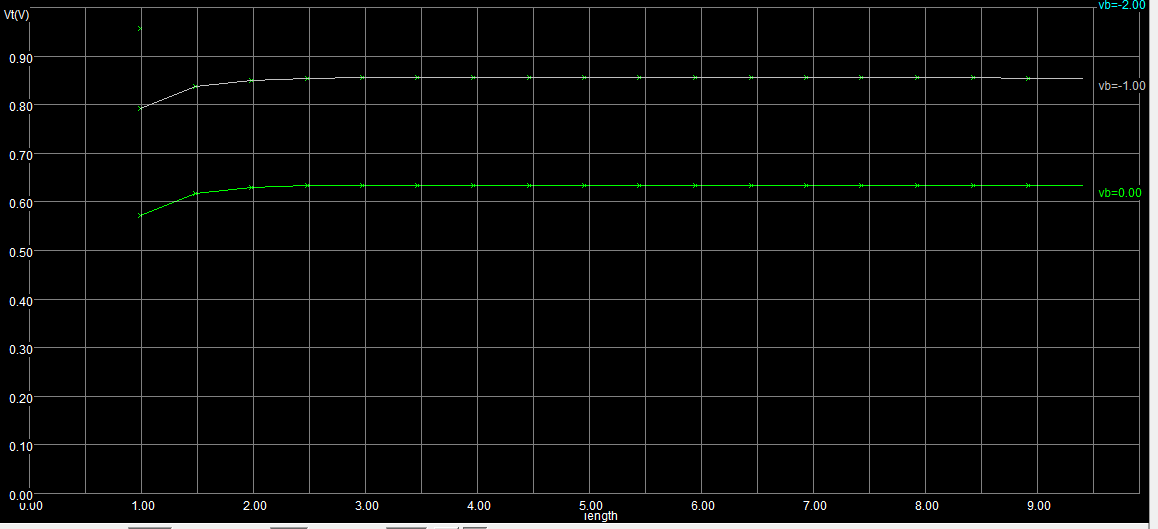


Fig 20: Threshold Voltage

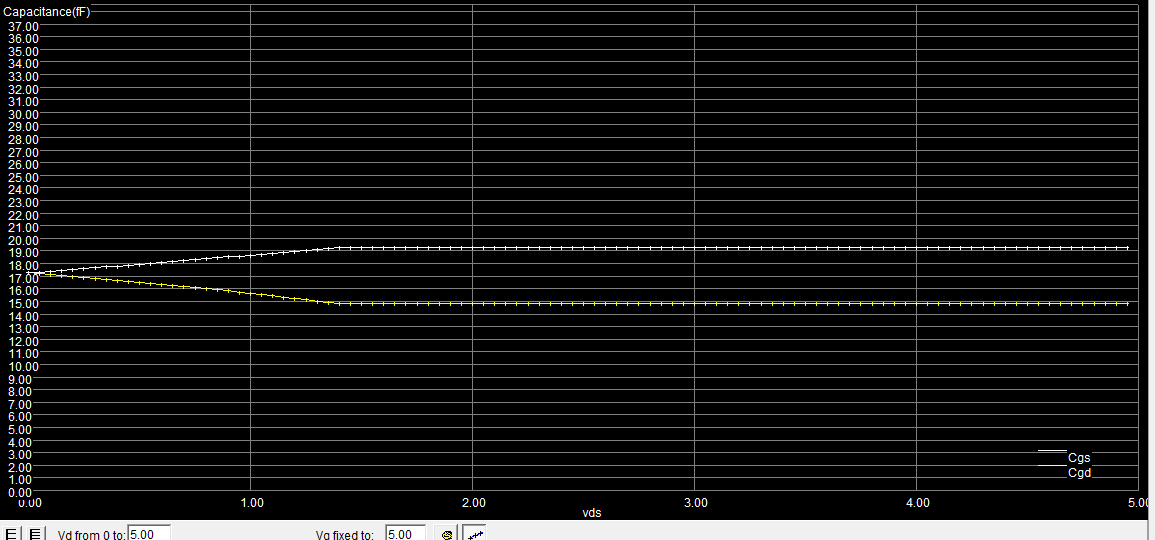


Fig 21: Capacitance

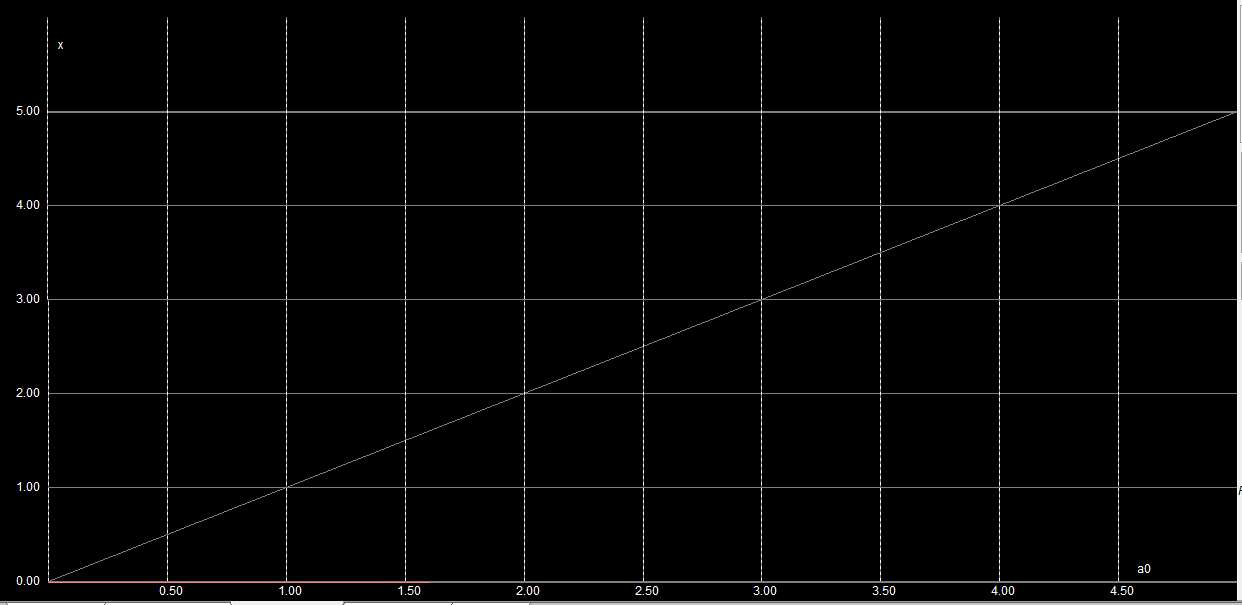


Fig 22: voltage to voltage

|  |  |  |  |
| --- | --- | --- | --- |
| **Output** | **Rise time**  **(ns)** | **Fall time**  **(ns)** | **Propagation delay(ns)** |
| A=B | 0.340 | 0.387 | 0.727 |
| A>B | 0.362 | 0.345 | 0.707 |
| A<B | 0.370 | 0.321 | 0.691 |

Table1: Timing analyses for output

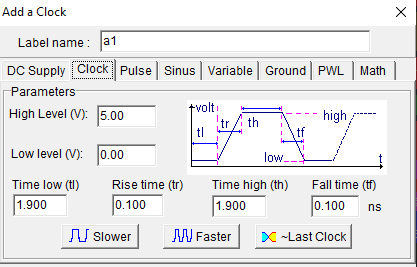


Fig 23: Timing analyses of input signal

1. **Conclusion:**

Microwind tool widely used in Industry for fabrication and testing of CMOS. It is offer other many tools like DSCH to help to simulating circuit and create a transistor level simulation. Design of the 2-bit comparator is easy in microwind once the gate specification and gate level model is ready. It is very helpful to know for individual transistor characteristic and also make particular W/L transistor. It was also providing different kind of output graph at different point. So that we can use this different functionality of the microwind and make 2-bit comparator.

# **9.References:**

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| --- | --- |
| [1] | S. A. Anjuli, "2-Bit Magnitude Comparator Design Using Different Logic Styles," *International Journal of Engineering Science Invention,* p. 24, 2013. |
| [2] | 4 4 2020. [Online]. Available: https://www.electronicshub.org/digital-comparator-and-magnitude-comparator/. |
| [3] | GeeksforGeeks, 4 4 2020. [Online]. Available: https://www.geeksforgeeks.org/magnitude-comparator-in-digital-logic/. |