

1. Specifications

In this project we have designed an LDO subject to different conditions. For this design we are designing the LDO for both externally and internally compensated LDO. We have considered different technology nodes for the same. For the below figure we are considering 45nm technology node. The technology node file is attached here. Our aim is to design the LDO for a max and a min load condition.

For externally Compensated we have the following specifications:-

Table 1: Specifications Table

Parameter	Value	Comments
V_{in}	1.4 V	-
V_{out}	1 V	Relaxed
PSRR	60 dB	Aggressive
$I_{load, \text{max}}$	2 mA	Moderate
C_{load}	1 F	Aggressive
$I_{quiescent}$	50 A	Moderate

For internally compensated we have the following specifications:-

Table 2: Specifications Table

Parameter	Value	Units	Comments
V_{in}	1.4	V	-
V_{out}	1	V	Relaxed
PSRR	50	dB	Aggressive
$I_{load\text{--}min}$	2	mA	-
$I_{load\text{--}max}$	10	mA	Moderate
C_{load}	2	nF	Aggressive
Load Slew Rate	50	mA/s	Aggressive
Transient Spread	15	% of V_{out} peak-to-peak	Relaxed
$I_{quiescent}$	50	A	Moderate
Transient Duration	1	s	Moderate

2. Purpose of an LDO

An LDO is a type of linear regulator, which can regulate output voltages to values very close to the supplied input voltage. The input to output differential voltage, at which the LDO fails to regulate the output is defined as the dropout voltage. The structure of a generic LDO is provided in the block diagram shown in Figure 1. An LDO consists of an error amplifier (EA), an NMOS or PMOS pass transistor (PT) and a resistor divider forming a negative feedback loop. The EA is fed with a constant reference voltage (V_{ref}) by a bandgap circuit and in turn controls the PT through the feedback loop and the resistor divider circuit. The EA tracks the error between the output and V_{ref} and accordingly regulates the gate voltage of PT. The PT acts as a variable resistor and adjusts the output current to further control the output voltage at the desired level.

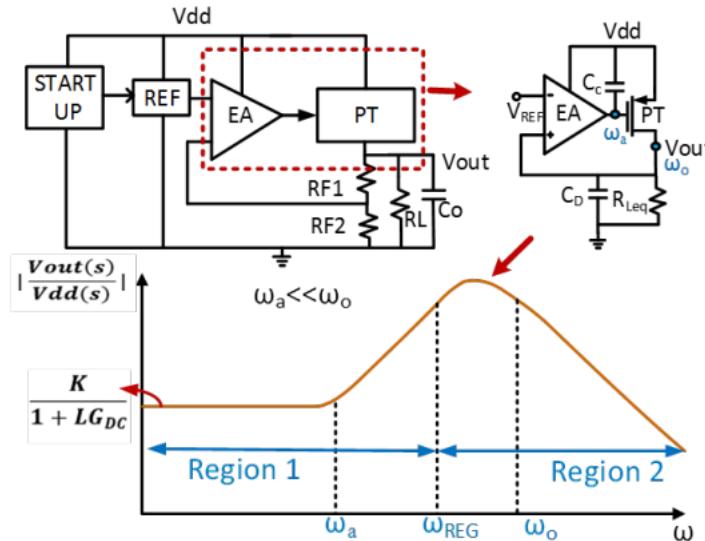


Figure 1: : Block diagram of a low drop-out (LDO) regulator and its associated PSRR curve (linear scale)

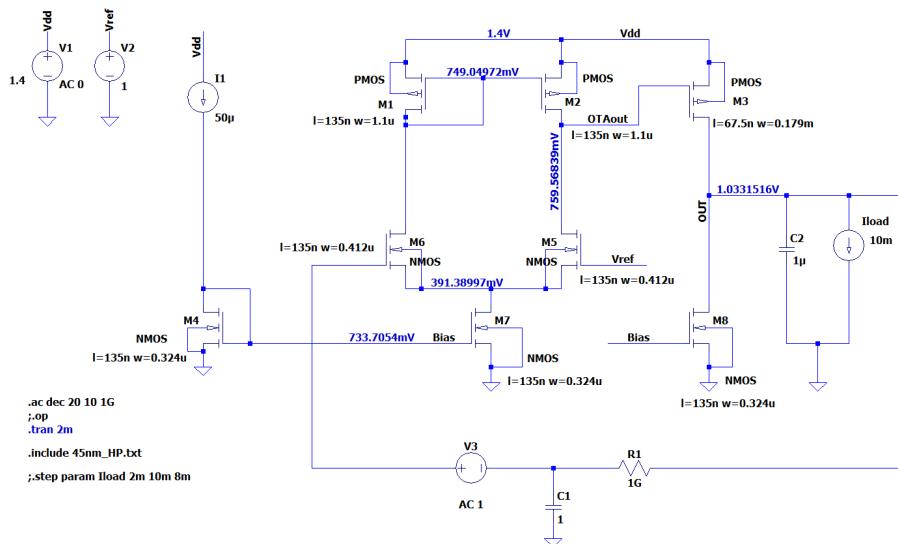


Figure 2: Our LDO schematic

3. Relevance of Techplots

We include all techplots generated after Python postprocessing. There are 5 takeaways, and we share a schematic of how these techplots were obtained.

Why do we prefer using techplots over the square law when sizing transistors?

- **Techplots** (or I-V characteristic curves) are often preferred over the **square law** because they provide a more accurate depiction of how transistors behave under different conditions.
- The **square law** offers a simplified model that assumes constant values for parameters like k and V_{th} . However, in reality, these values can vary due to factors such as the transistor's physical dimensions, doping levels, and manufacturing process.
- **Techplots** show how transistors perform across all their operational regions (cut-off, linear, and saturation), which is crucial for precise sizing and performance predictions.
- The **square law** can oversimplify the behavior of transistors in the saturation region, potentially leading to incorrect sizing and suboptimal performance.
- **Techplots** take into account process variations and environmental factors like temperature and voltage, which can significantly affect transistor behavior. The square law does not capture these dependencies.
- Overall, using **techplots** provides a more comprehensive view of transistor characteristics, helping designers make better choices that optimize performance, such as switching speed, power efficiency, and gain.

- **Github Link:** <https://github.com/Omkar-Vijay-Gavandi/Analog-CMOS-project/tree/main>
Technology node : 45 nm
- f_T improves with shorter channel lengths, making circuits faster with scaling.
- Comparison of different FOMs at different lengths

Length (nm)	gmro	Id/w	ft (GHz)
45	7	170	180
67.5	30	120	100
225	135	40	10

Table 3: Comparison of different FOM at different lengths for NMOS

- We chose the Vds to be 0.4 mV, and we expect that to result in some error because the Vds across every MOSFET might not be the same after sizing the circuit under a particular load. It is very possible that the Vds across the MOSFETs can change under different values of load current. The above phenomenon can be understood from the output log files mentioned below.

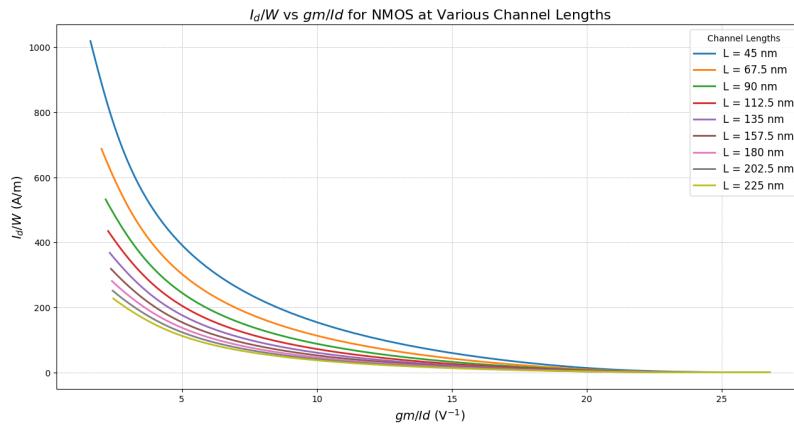


Figure 3: NMOS Techplots after Python postprocessing - Id/W

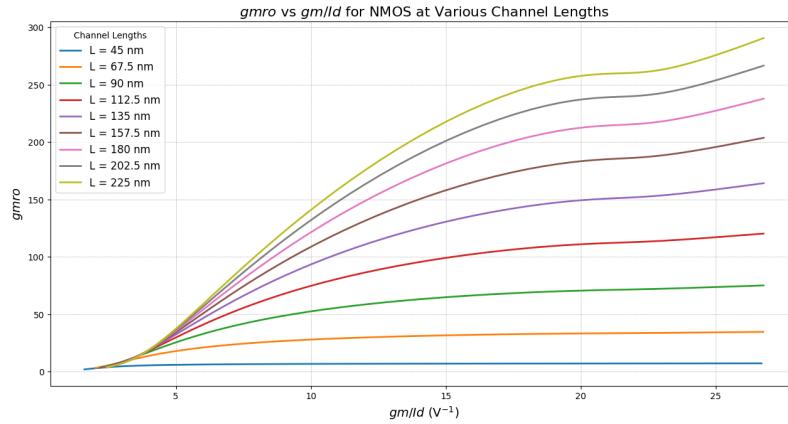


Figure 4: NMOS Techplots after Python postprocessing - $gmro$

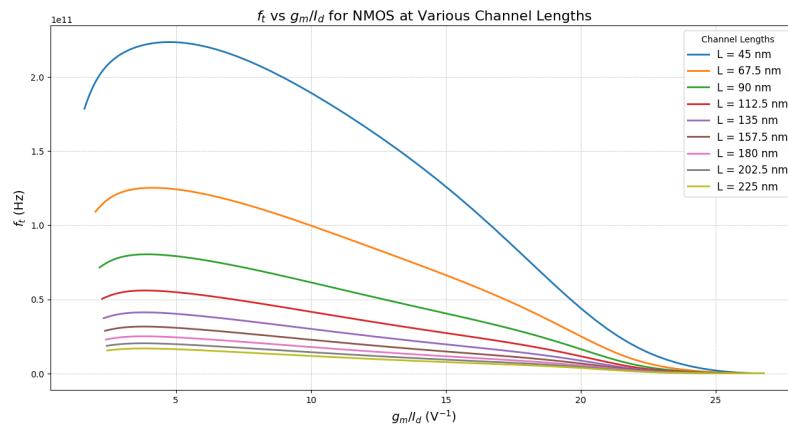


Figure 5: NMOS Techplots after Python postprocessing - f_T

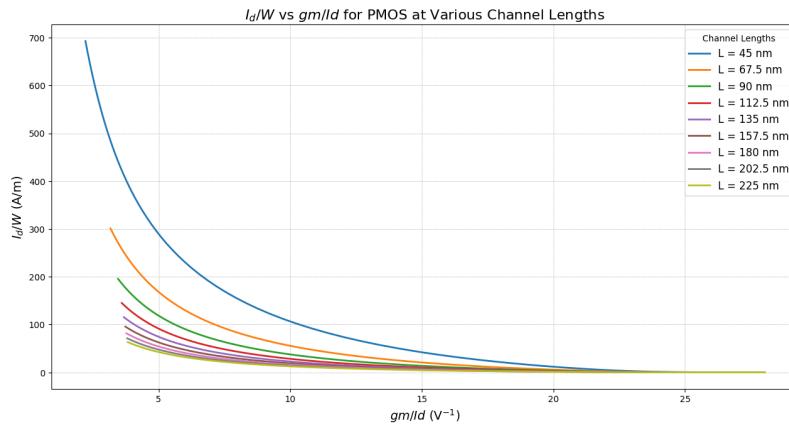
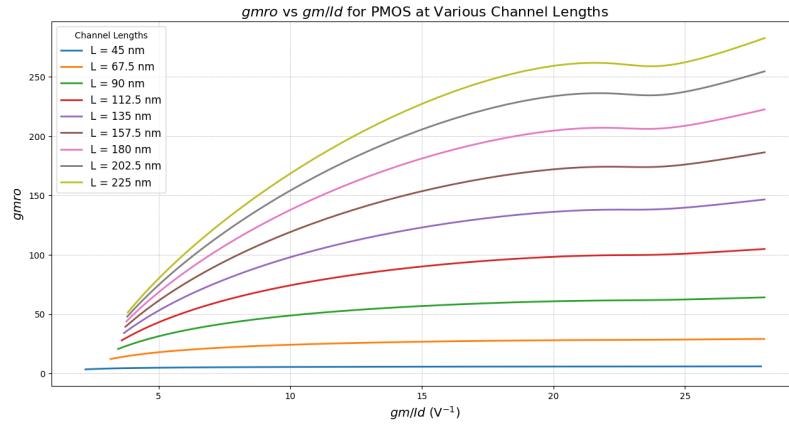
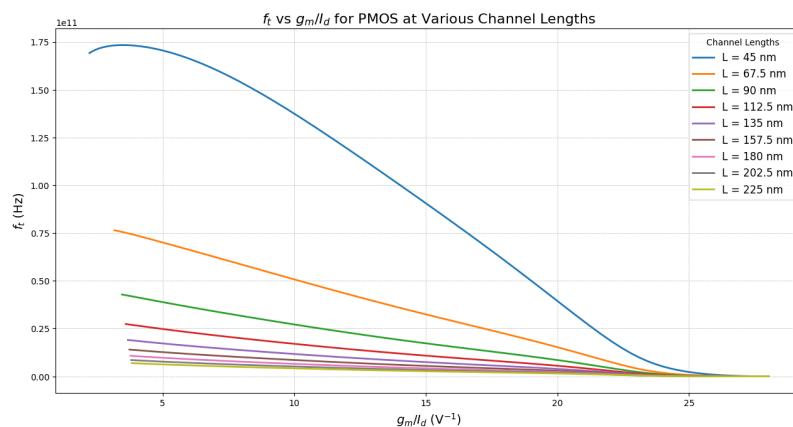
Figure 6: PMOS Techplots after Python postprocessing - Id/W Figure 7: PMOS Techplots after Python postprocessing - $gmro$ Figure 8: PMOS Techplots after Python postprocessing - fT

Table 4: Key Differences Between 180nm and 45nm Technology Nodes for NMOS

Parameter	180nm Technology Node	45nm Technology Node
gmro	20	6.721
Id/W ($\mu\text{A}/\mu\text{m}$)	28	154.324
fT (Hz)	1.6×10^{10}	18.93×10^{10}

Table 5: Observations on Technology Scaling Effects

Parameter	Observation
gmro	As the channel length decreases, the output resistance (r_o) decreases significantly, which dominates the intrinsic gain ($gmro$). As a result, the overall value of $gmro$ decreases.
Id/W	With reduced channel length, the drain current (I_d) increases due to higher mobility and lower channel resistance. Consequently, I_d/W increases, which is evident from the data.
fT	A decrease in channel length increases the transconductance (g_m), which directly leads to an increase in the unity-gain cutoff frequency (f_T). This trend is observed in the values.

4. FET Sizes

we Provide the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

Table 6: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	0.179m/67.5n	10	24.18	55.62	50.76 GHz
Diff-Amp pmos	1.1u/135n	10	97.93	22.71	11.71 GHz
Diff-Amp nmos	0.412u/135n	10	93.43	60.51	30 GHz
Current Mirror nmos	0.324u/135n	10	155	154.1	30 GHz

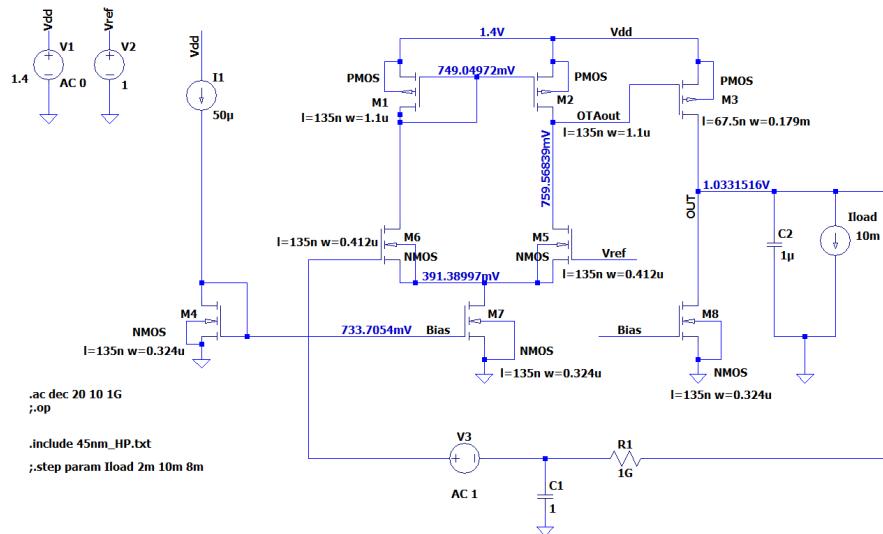


Figure 9: FET sizes and characteristics.

5. Stability Analysis

For Heavy load we get the following curve:

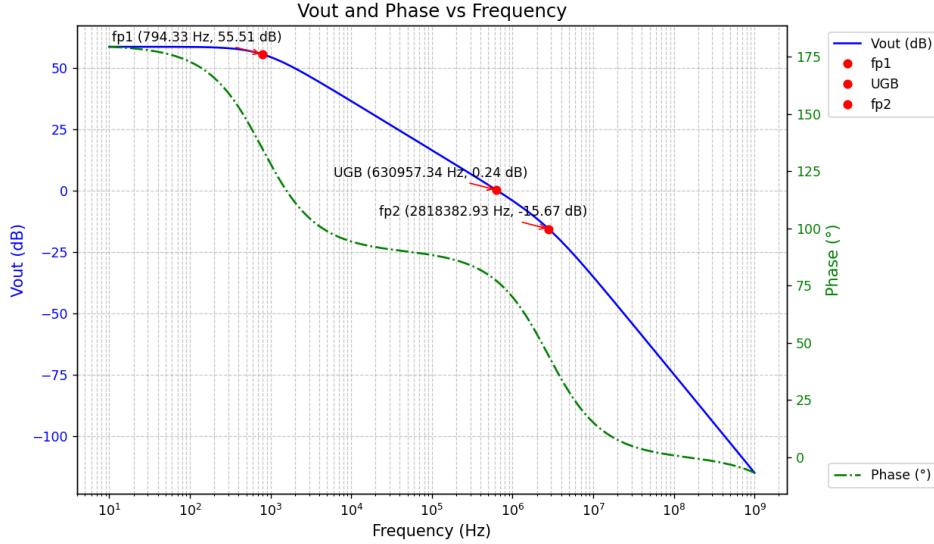


Figure 10: Vout and phase vs Frequency

For Light load we get the following curve

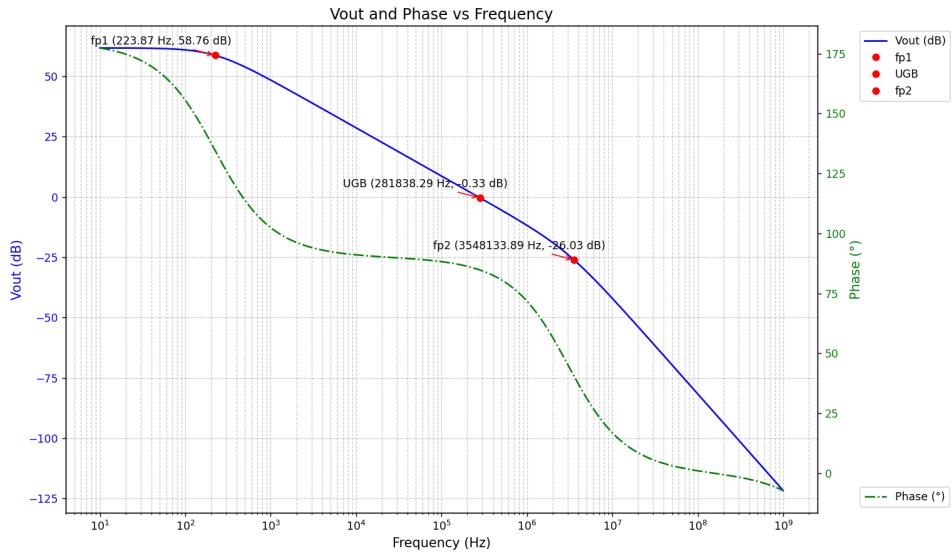


Figure 11: Vout and phase vs Frequency

From the above analysis, we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. We can also observe a lesser phase margin of 76 degrees for the heavy load case than that of the light load case. From this analysis, we can say that when we apply light load, we get a more stable system.

Table 7: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	58.5	61.02
Unity Gain Bandwidth (kHz)	647.855	271.274
Phase Margin (degrees)	77.43	85.29
Pole 1 (Hz)	784.097	220.521
Pole 2 (MHz)	2.74	3.035

6. PSRR Explanation

LDOs are essential components in the power supply of most ICs. They provide a ripple-free, stable fixed output voltage; isolating it from the input noise. An LDO has several important performance specifications and the power supply rejection ratio (PSRR) is one of them. PSRR is a quantitative measure of the attenuation of input ripples by the LDO at its output. These ripples can originate from various parts of the circuit, like DC/DC converters or shared power supplies of other circuit blocks. PSRR is expressed as $\text{PSRR} = 20\log(v_{\text{out}}/v_{\text{in}})$, where v_{out} and v_{in} refer to magnitudes of input and output ripples. In Figure 12, the PSRR of LDO is divided into two distinct regions (region 1 and region 2). Region 1 covers the low and mid frequency range till the regulator bandwidth frequency (ω_{REG}), where PSRR primarily depends on the loop gain (LG) of the regulator. Region 2 starts after ω_{REG} , where PSRR is independent of LG and is dominated by output parasitics, PCB impedance, etc.

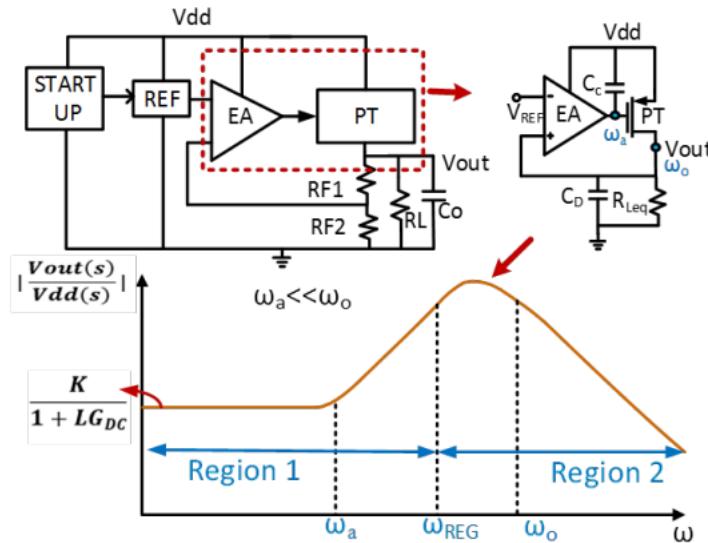


Figure 12: : Block diagram of a low drop-out (LDO) regulator and its associated PSRR curve (linear scale)

7. PSRR Simulation Results

we have made three schematics in LTSpice to calculate the three conditions. We have made a simulation artifact for the same.

Case 1 : Loop Gain Analysis

Case 2 : Open Loop PSRR Calculation

Case 3 : Closed Loop PSRR Calculation

Heavy Load (10mA)

Schematic

Case 1:- Loop gain analysis:-

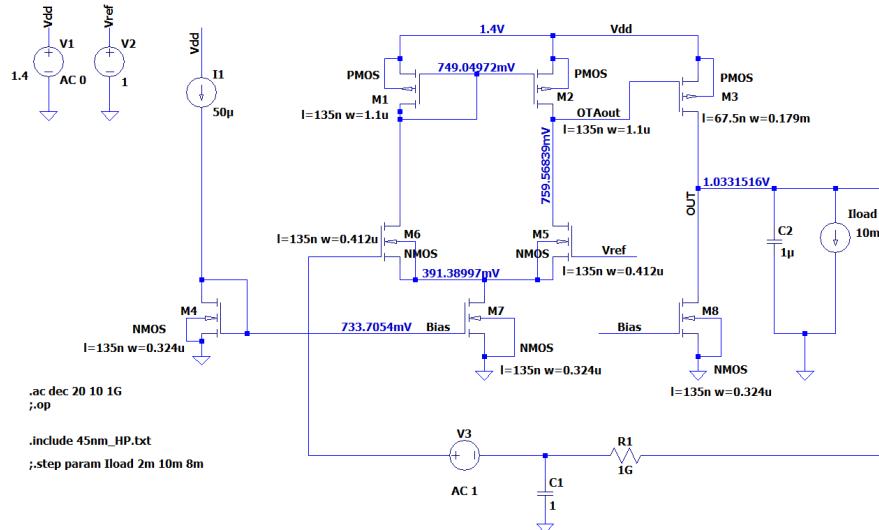


Figure 13: Schematic

Explanation of the artifact used:-

In order to calculate the loop gain we have given a RC circuit in the feedback loop alongwith a AC source with amplitude 1 (as we want to maintain an AC voltage of 1V) at the output. At the same time we also need to bias the circuit and provide a dc voltage to the gate of the nmos in the differential amplifier and for this we are giving the RC circuit which will prevent the flow of dc current to ground but will send any AC signal at the output to ground at high frequency. Also the drop across the resistor will be very less as we have given a very high resistance with very negligible current (since current going into the gate of the mosfet is zero). Thus we will bias the circuit and also calculate the loop gain.

Output Log File:-

```

SPICE Output Log: D:\Desktop\ACMOS_project\Cat 1\VL502_1st_LDO\502_try1.log
LTspice 24.0.12 for Windows
Circuit: * D:\Desktop\ACMOS_project\Cat 1\VL502_1st_LDO\502_try1.asc
Start Time: Sat Nov 30 16:49:50 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:      m1      m2      m3      m4      m5
Model:     pmos    pmos    pmos    nmos    nmos
Id:   -2.43e-05 -2.42e-05 -1.01e-02 5.00e-05 2.43e-05
Vgs:   -6.51e-01 -6.51e-01 -6.40e-01 7.34e-01 6.09e-01
Vds:   -6.51e-01 -6.40e-01 -3.67e-01 7.34e-01 3.68e-01
Vbs:    0.00e+00  0.00e+00  0.00e+00 0.00e+00 0.00e+00
Vth:    4.89e-01 -4.89e-01 -4.81e-01 4.67e-01 4.68e-01
Vdsat: -1.78e-01 -1.78e-01 -1.73e-01 2.41e-01 1.51e-01
Gm:    2.45e-04  2.45e-04  9.78e-02 2.79e-04 2.43e-04
Gds:    2.42e-06  2.43e-06  4.82e-03 3.31e-06 2.83e-06
Gmb:    5.18e-05  5.18e-05  2.07e-02 7.01e-05 5.65e-05
Cbd:   4.66e-16  4.67e-16  8.07e-14 1.35e-16 1.86e-16
Cbs:   8.80e-16  8.80e-16  1.43e-13 2.59e-16 3.30e-16

Name:      m6      m7      m8
Model:     nmos    nmos    nmos
Id:   2.43e-05  4.85e-05  5.09e-05
Vgs:   6.09e-01  7.34e-01  7.34e-01
Vds:   3.58e-01  3.91e-01  1.03e+00
Vbs:    0.00e+00  0.00e+00  0.00e+00
Vth:    4.68e-01  4.68e-01  4.66e-01
Vdsat:  1.51e-01  2.40e-01  2.41e-01
Gm:    2.43e-04  2.69e-04  2.83e-04
Gds:    2.93e-06  7.07e-06  3.17e-06
Gmb:    5.65e-05  6.77e-05  7.12e-05
Cbd:   1.86e-16  1.45e-16  1.28e-16
Cbs:   3.30e-16  2.59e-16  2.59e-16

Total elapsed time: 0.144 seconds.

```

Figure 14: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.651	0.651	0.489	0.162	Saturation
M2	PMOS	0.64	0.651	0.489	0.162	Saturation
M3	PMOS	0.367	0.64	0.481	0.159	Saturation
M4	NMOS	0.734	0.734	0.4	0.334	Saturation
M5	NMOS	0.368	0.609	0.468	0.141	Saturation
M6	NMOS	0.358	0.609	0.468	0.141	Saturation
M7	NMOS	0.391	0.734	0.468	0.266	Saturation
M8	NMOS	1.03	0.734	0.466	0.268	Saturation

Table 8: Transistor Parameters and Operating Regions

Output on Python:-

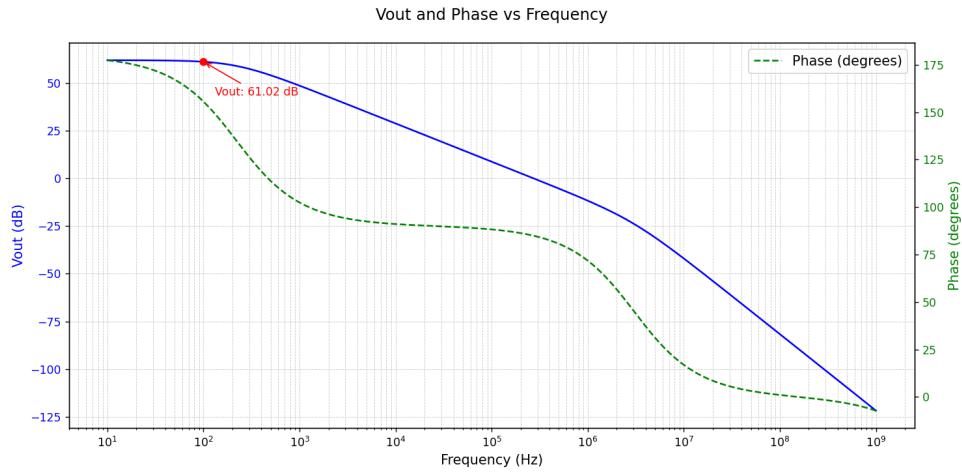


Figure 15: Vout and phase vs Frequency for heavy load

Phase margin

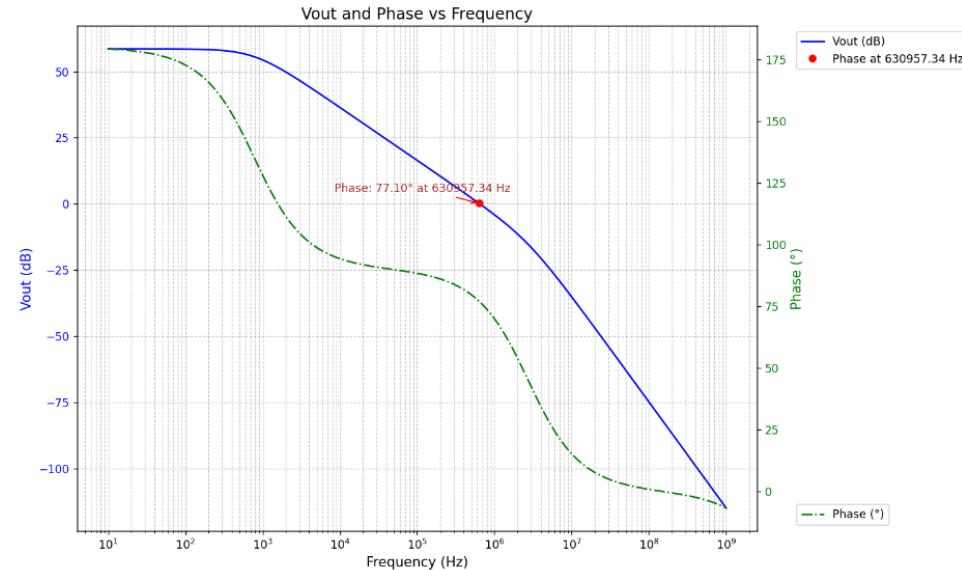


Figure 16: Phase margin

The phase margin is 77.10

The output voltage (Loop gain) comes out to be close to 58.3db . The formula for loop gain is $A_{diff} A_{pass}$ where A_{diff} is differential amplifier gain and A_{pass} is the passfet gain.

Case 2:- Open Loop PSRR calculation

Schematic

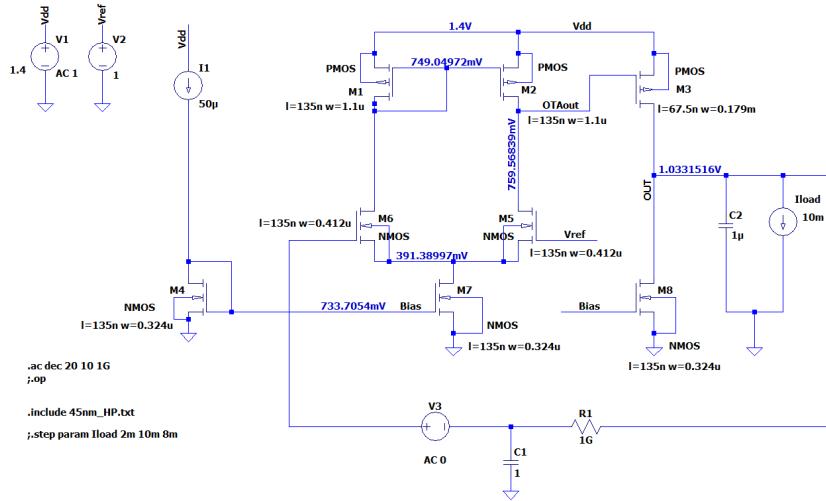


Figure 17: Schematic

Explanation of the artifact used:-

In order to calculate the open loop PSRR we need to send an AC signal from the source which in our case is VDD. Here we are giving an AC 1 signal in the source. This signal is given to the source of the passfet and the source of pmos in the diffamp. We will ideally want very bad PSRR in the diffamp as we want the OTA output to have all the AC noise such that V_{sg} of pmos = 0 (small signal analysis). Thus all the noise will get rejected and we will get a noise free dc voltage at the output of the LDO. Here in order to calculate the open loop PSRR we have a RC circuit to bias the differential amplifier. You can see AC 0 in the circuit indicating that there is an open loop in the circuit . From here we have calculated the open loop PSRR in the circuit. Since there is no feedback in the circuit we can thus say that there will be noise at the output and thus the rejection will be very poor.

Output on Python:-

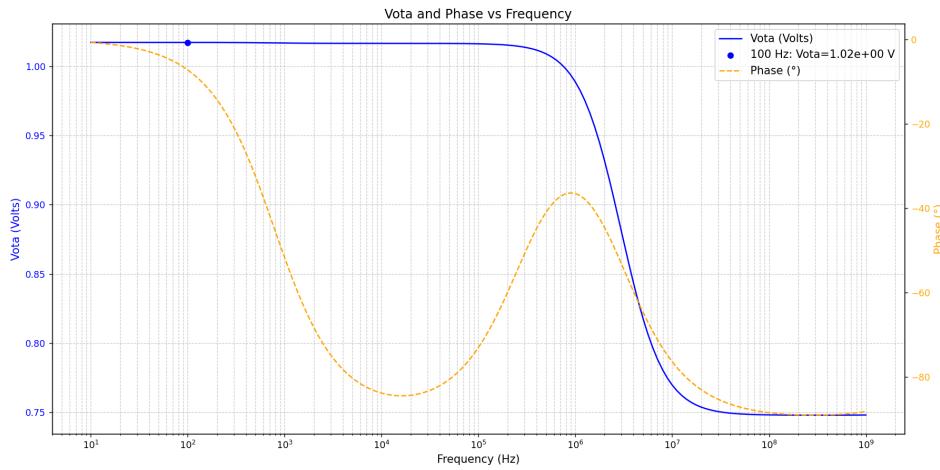


Figure 18: Vota and phase vs Frequency for heavy load

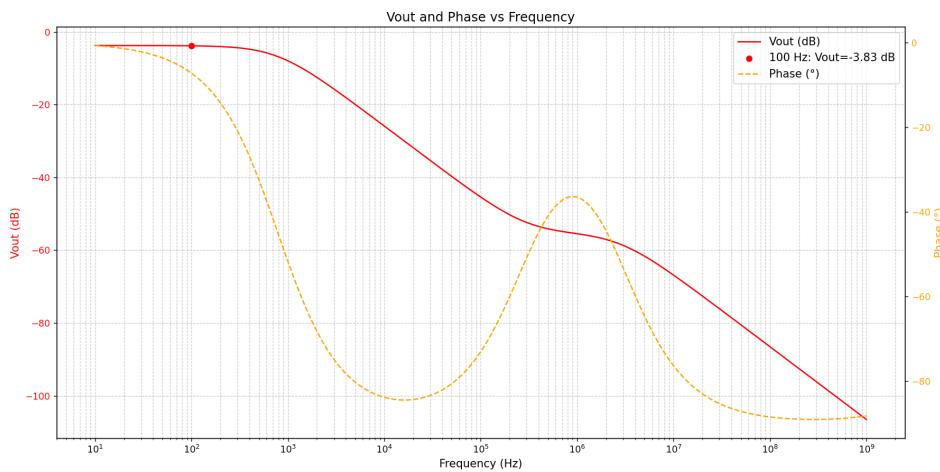


Figure 19: Vout and phase vs Frequency for heavy load

Note:- Always observe the Vota output in volts because it will give you the insight into what AC voltage is coming into the gate of the passfet. It should be close to VDD. The closer it is to 1v the better it is for a very bad PSRR at the output as the Vsg value will be close to 0.

Case 3:- Closed Loop PSRR Calculation

Schematic

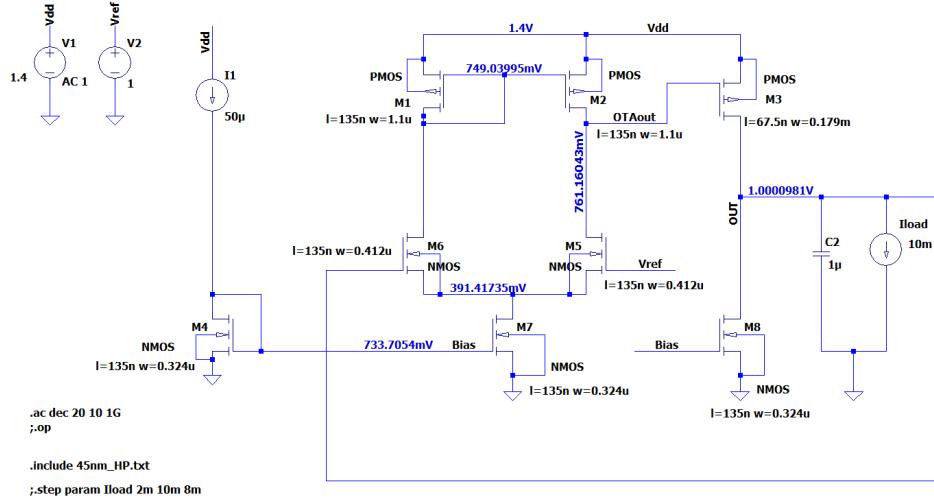


Figure 20: Schematic

Explanation of the artifact used:-

In this case we can see that we have given a AC source in the voltage source VDD. We want to see the negative feedback in the circuit due to which we will get the output voltage cancelled out (small signal analysis). Here we should observe a high PSRR according to our specifications (60db) which tells us that our sizing is perfect. For this circuit we have given a feedback from the output terminal to the input of the diffamp which indicates the feedback path.

Output on Python:-

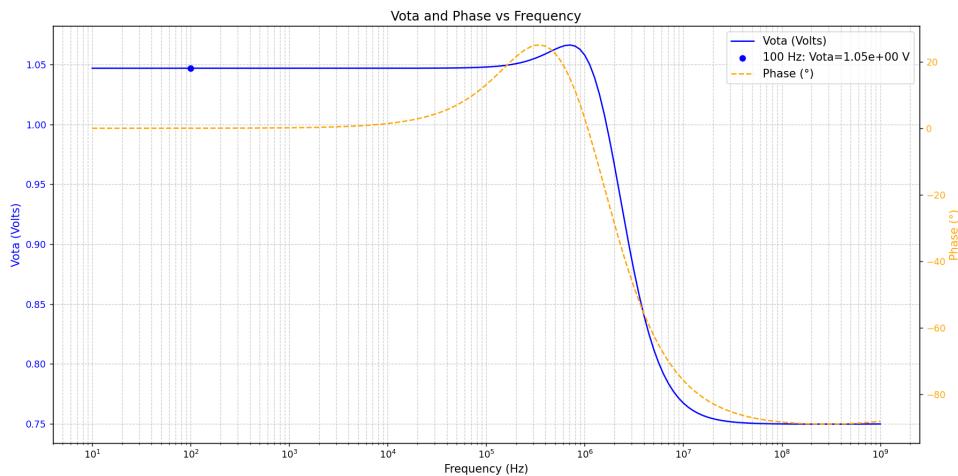


Figure 21: Vota and phase vs Frequency for heavy load



Figure 22: Vout and phase vs Frequency for heavy load

Light Load (2mA)

Case 1:- Loop gain analysis

Schematic

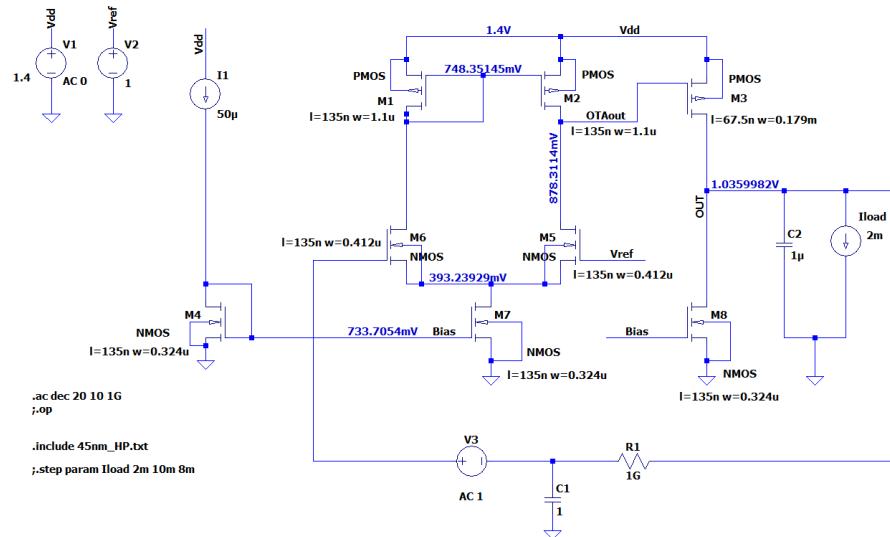
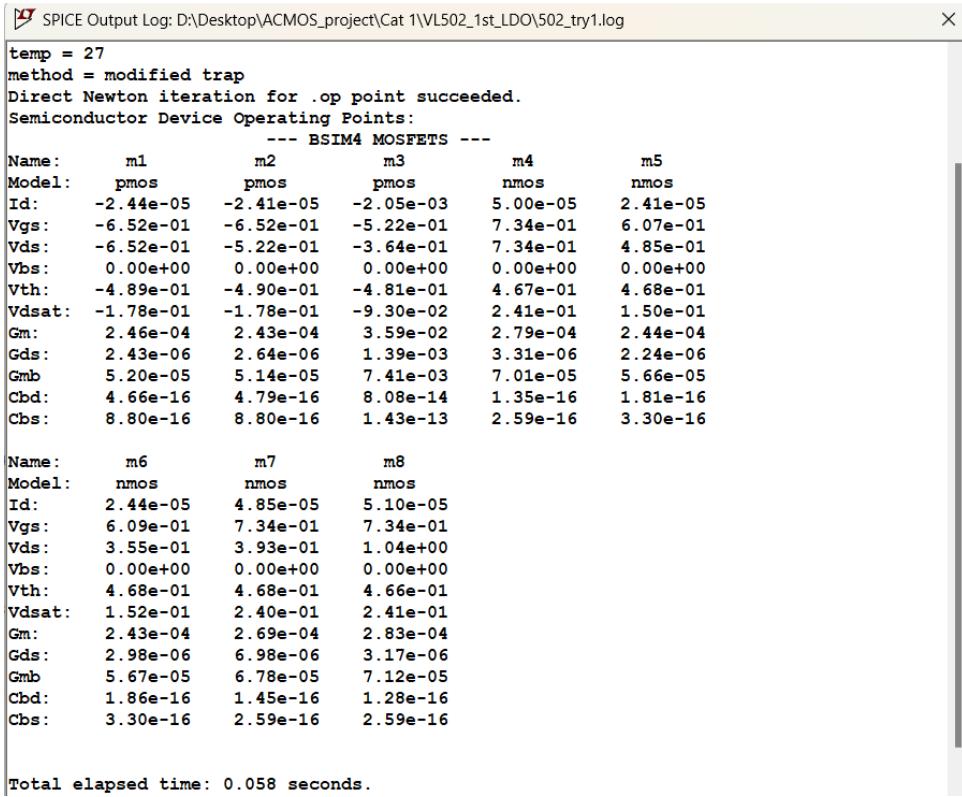


Figure 23: Schematic

Output Log File:-



```

SPICE Output Log: D:\Desktop\ACMOS_project\Cat 1\VL502_1st_LDO\502_try1.log

temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
--- BSIM4 MOSFETS ---
Name: m1 m2 m3 m4 m5
Model: pmos pmos pmos nmos nmos
Id: -2.44e-05 -2.41e-05 -2.05e-03 5.00e-05 2.41e-05
Vgs: -6.52e-01 -6.52e-01 -5.22e-01 7.34e-01 6.07e-01
Vds: -6.52e-01 -5.22e-01 -3.64e-01 7.34e-01 4.85e-01
Vbs: 0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00
Vth: -4.89e-01 -4.90e-01 -4.81e-01 4.67e-01 4.68e-01
Vdsat: -1.78e-01 -1.78e-01 -9.30e-02 2.41e-01 1.50e-01
Gm: 2.46e-04 2.43e-04 3.59e-02 2.79e-04 2.44e-04
Gds: 2.43e-06 2.64e-06 1.39e-03 3.31e-06 2.24e-06
Gmb: 5.20e-05 5.14e-05 7.41e-03 7.01e-05 5.66e-05
Cbd: 4.66e-16 4.79e-16 8.08e-14 1.35e-16 1.81e-16
Cbs: 8.80e-16 8.80e-16 1.43e-13 2.59e-16 3.30e-16

Name: m6 m7 m8
Model: nmos nmos nmos
Id: 2.44e-05 4.85e-05 5.10e-05
Vgs: 6.09e-01 7.34e-01 7.34e-01
Vds: 3.55e-01 3.93e-01 1.04e+00
Vbs: 0.00e+00 0.00e+00 0.00e+00
Vth: 4.68e-01 4.68e-01 4.66e-01
Vdsat: 1.52e-01 2.40e-01 2.41e-01
Gm: 2.43e-04 2.69e-04 2.83e-04
Gds: 2.98e-06 6.98e-06 3.17e-06
Gmb: 5.67e-05 6.78e-05 7.12e-05
Cbd: 1.86e-16 1.45e-16 1.28e-16
Cbs: 3.30e-16 2.59e-16 2.59e-16

Total elapsed time: 0.058 seconds.

```

Figure 24: Output Log Details

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.652	0.652	0.489	0.163	Saturation
M2	PMOS	0.522	0.652	0.490	0.162	Saturation
M3	PMOS	0.364	0.522	0.481	0.041	Saturation
M4	NMOS	0.734	0.734	0.467	0.267	Saturation
M5	NMOS	0.485	0.607	0.468	0.139	Saturation
M6	NMOS	0.355	0.609	0.468	0.141	Saturation
M7	NMOS	0.393	0.734	0.468	0.266	Saturation
M8	NMOS	1.04	0.734	0.466	0.268	Saturation

Table 9: Transistor Data Table

Output on Python:-

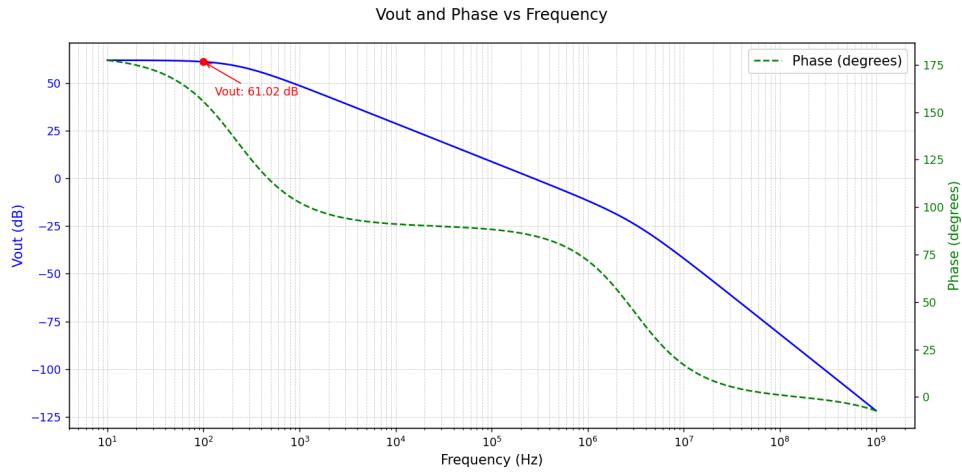


Figure 25: Vout and phase vs Frequency for light load

Phase Margin

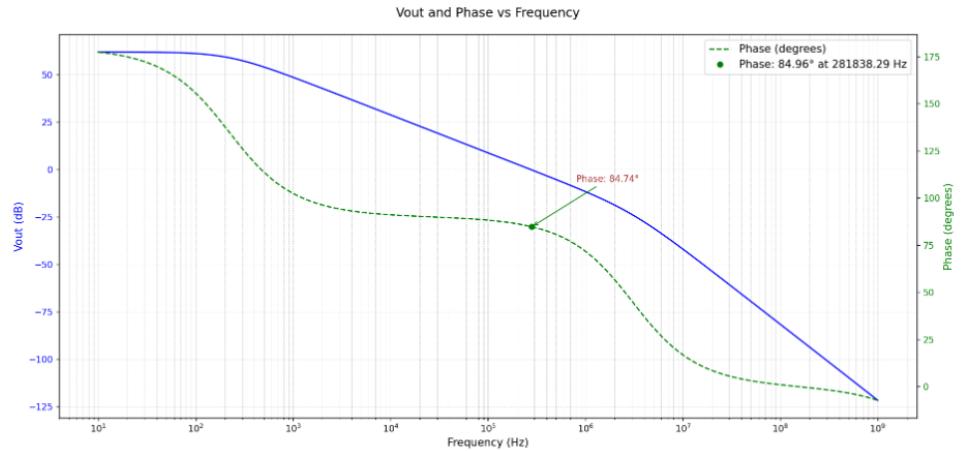


Figure 26: Phase Margin

Observations: The phase margin obtained is 84.74 degrees. This value is higher compared to that obtained for a heavy load. In the case of externally compensated LDOs, we know that the second pole is independent of changes in load current, but both the unity gain bandwidth frequency and the first pole increase with an increase in the load current. Thus, under light load conditions, the unity gain bandwidth frequency is further apart from the second pole compared to the heavy load conditions. These results indicate a better phase margin for light load conditions.

Case 2:- Open Loop PSRR calculation

Schematic

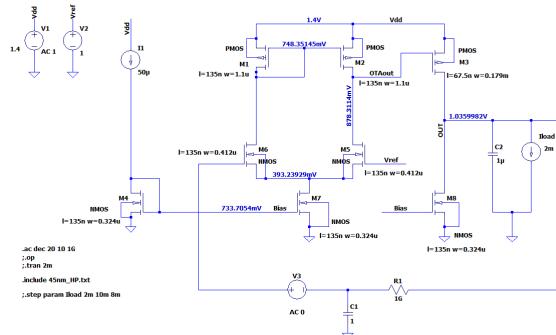


Figure 27: Schematic

Output on Python:-

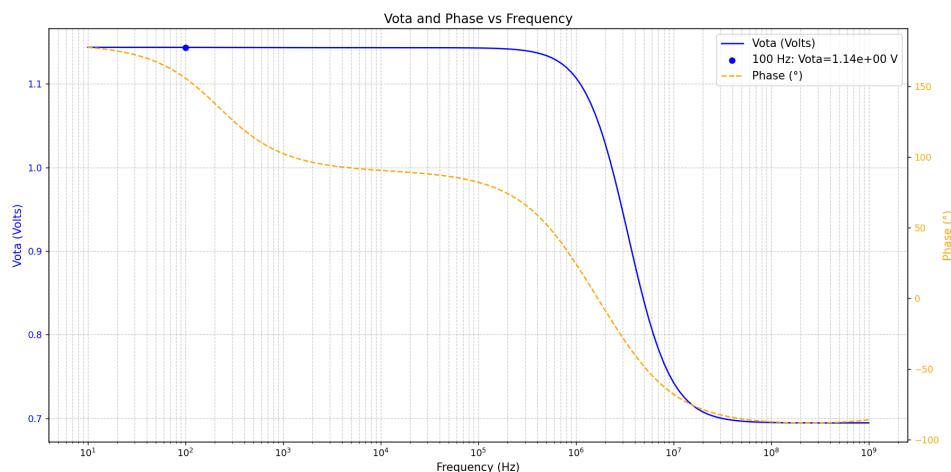


Figure 28: Vota and phase vs Frequency for light load

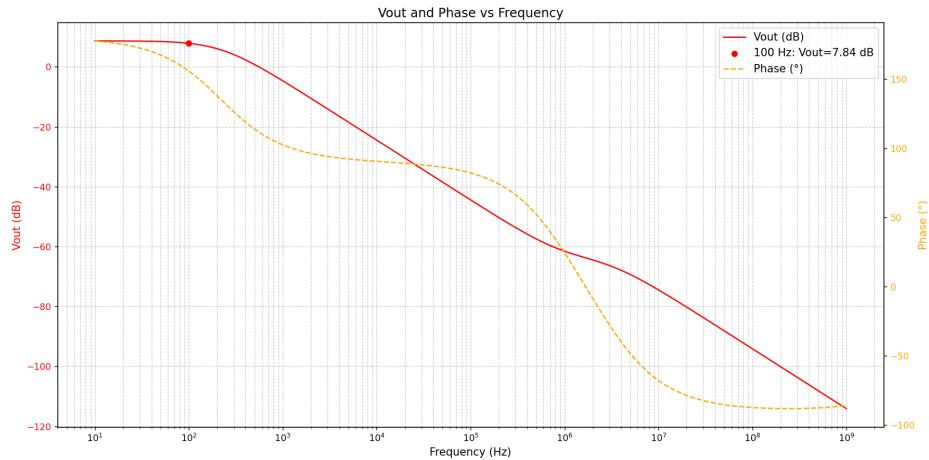


Figure 29: Vout and phase vs Frequency for light load

Case 3:- Closed loop PSRR calculation

Schematic

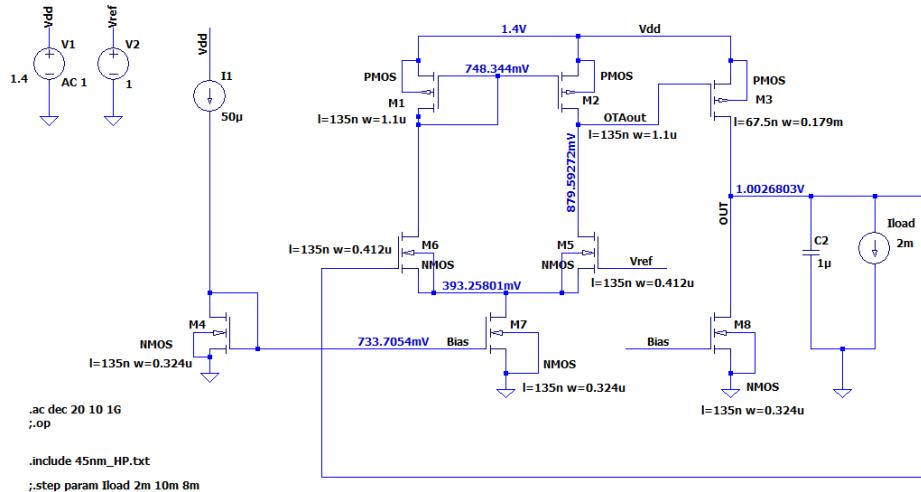


Figure 30: Schematic

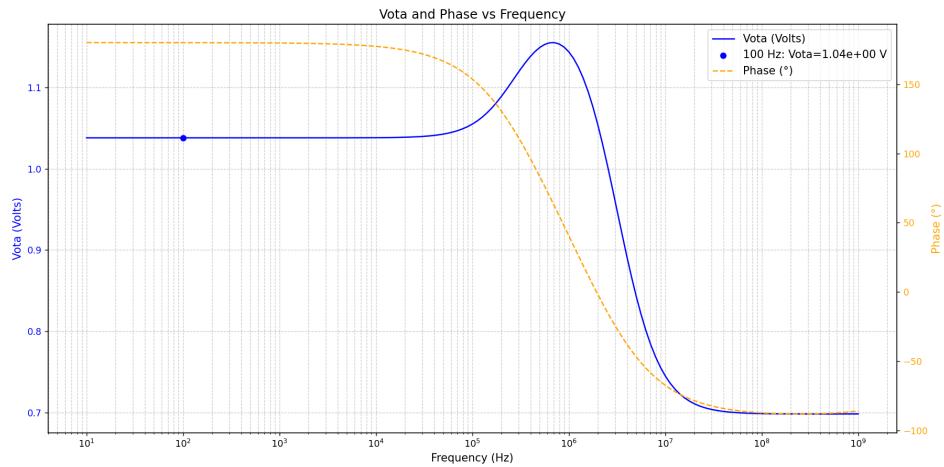
Output on Python:-

Figure 31: Vota and phase vs Frequency for light load

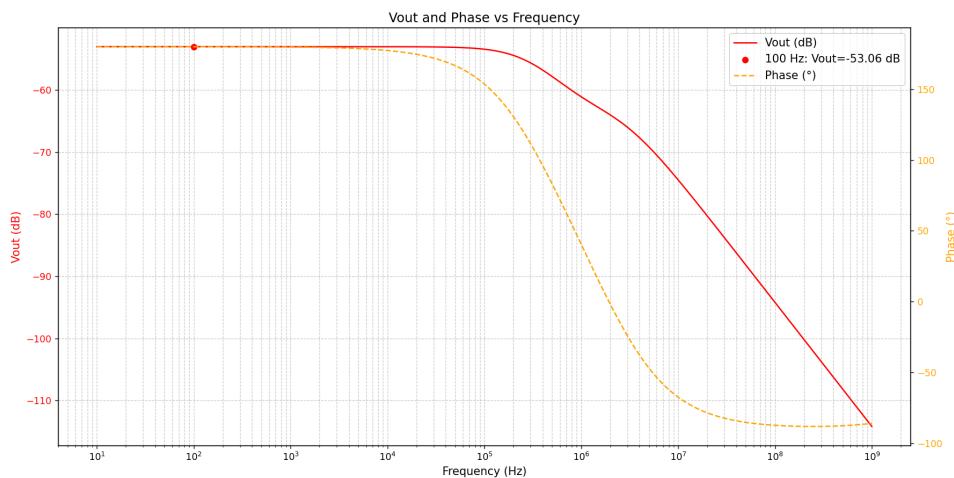


Figure 32: Vout and phase vs Frequency for light load

8. Transient Simulation Results

We have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a 50% duty cycle. From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

Schematic:-

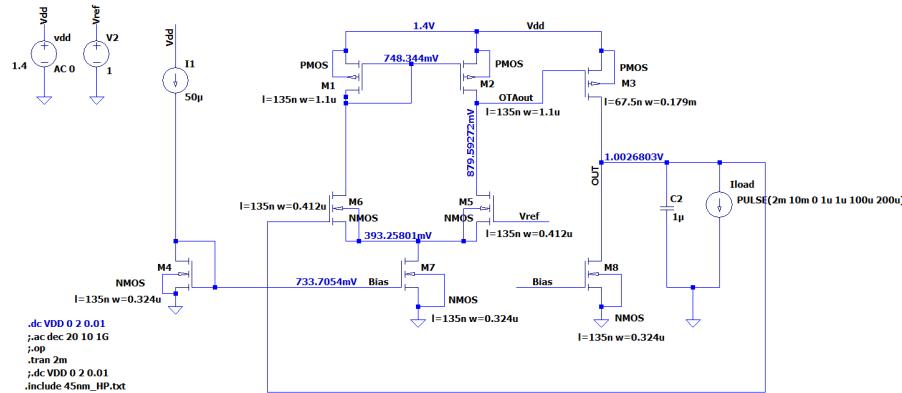


Figure 33: Schematic to do transient analysis

Output on Python:-

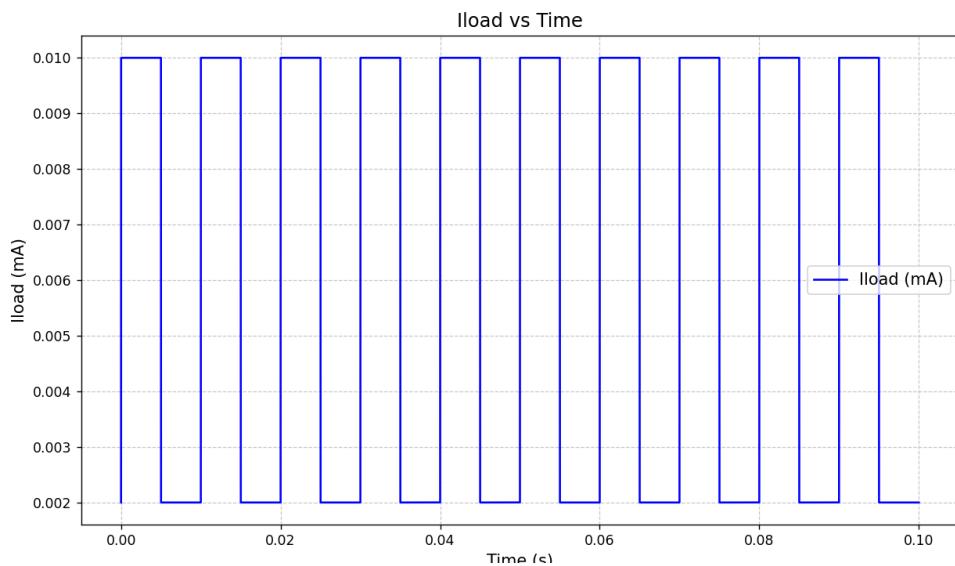


Figure 34: Iload vs Time

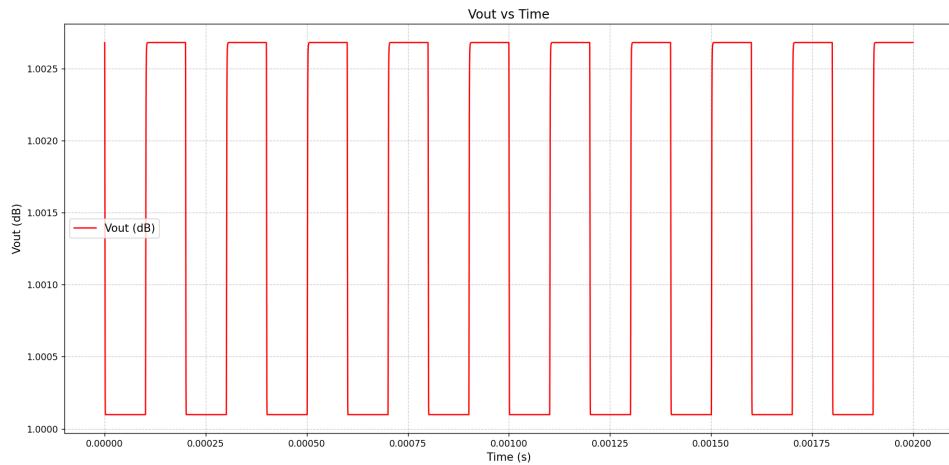


Figure 35: Vout vs Time

9. Simulation vs. Hand Calculations

For Passfet

Hand Calculation

- $r_o = 242 \Omega$
- $g_m = 0.1 \text{ A/V}$
- W_{p1} (first pole location) = 4.14k
- $g_m r_o = 24.18$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 207.42 \Omega$
- $g_m = 0.0978 \text{ A/V}$
- W_{p1} (first pole location) = 4.132k
- $g_m r_o = 20.289$

Table 10: Simulation vs. Hand Calculations with Percentage Error

Parameter	Simulation	Hand-Calculation	% Error
ro ()	207.42	242.00	14.32%
gm (A/V)	0.0978	0.1000	2.20%
Wp1 (Hz)	4.132k	4.14k	0.19%
gmro	20.289	24.18	16.08%

10. Effect of VDD on the output voltage

Schematic

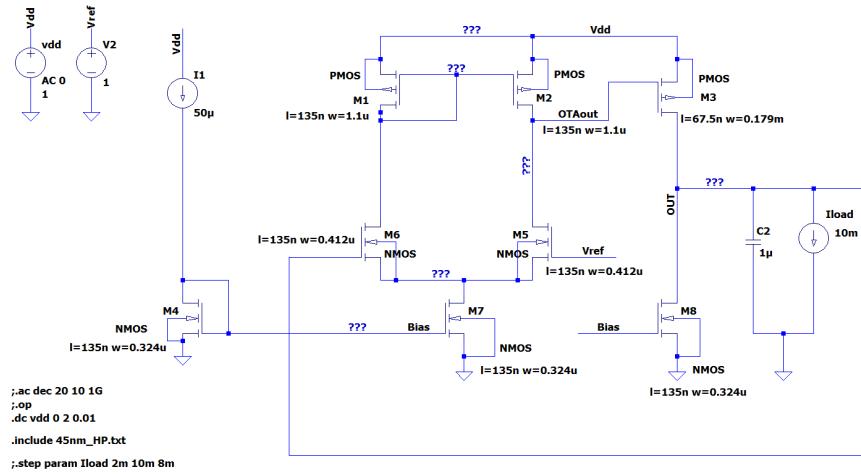


Figure 36: Schematic

Output plots

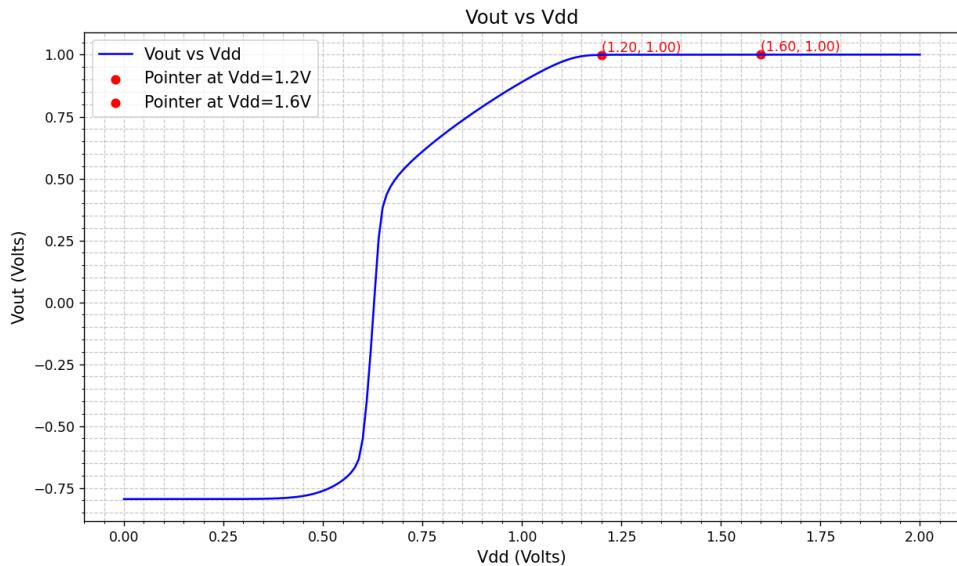


Figure 37: Vout vs Vdd for heavy load

From the plots we can see that we are getting regulation after 1.2 till 1.4v. After this voltage we are still getting 1v output but we can't comment on the circuit since the device has a nominal voltage of 1v and the vds across the mosfets might go above 1v so the device can breakdown.

Area vs gm/Id plot

This document summarizes the area calculations for different gm/Id values. The table below lists the areas of individual transistors (passfet, PMOS diffamp FET, NMOS diffamp

FET, and current mirror FET) as well as the overall area for each gm/Id value.

0.1 Transistor Calculations for Different g_m/I_D Ratios

gm/Id	Passfet Area	P Area	N Area	C M FET Area	Overall Area (μm^2)
10	12.08	0.297	0.1124	0.9085	13.3979
12	17.82	0.445	0.1156	1.36	19.781
15	32.46	0.544	0.215	2.55	35.769

Table 11: Table of FET Areas vs gm/Id

For $g_m/I_D = 15$

- Area of passfet: $32.46 \mu\text{m}^2$
- Area of PMOS diffamp FET: $0.544 \mu\text{m}^2$
- Area of NMOS diffamp FET: $0.215 \mu\text{m}^2$
- Area of Current mirror FET: $2.55 \mu\text{m}^2$
- **Overall area:** $35.769 \mu\text{m}^2$

For $g_m/I_D = 12$

- Area of passfet: $17.82 \mu\text{m}^2$
- Area of PMOS diffamp FET: $0.445 \mu\text{m}^2$
- Area of NMOS diffamp FET: $0.1156 \mu\text{m}^2$
- Area of Current mirror FET: $1.36 \mu\text{m}^2$
- **Overall area:** $19.781 \mu\text{m}^2$

For $g_m/I_D = 10$

- Area of passfet: $12.08 \mu\text{m}^2$
- Area of PMOS diffamp FET: $0.297 \mu\text{m}^2$
- Area of NMOS diffamp FET: $0.1124 \mu\text{m}^2$
- Area of Current mirror FET: $0.9085 \mu\text{m}^2$
- **Overall area:** $13.3979 \mu\text{m}^2$

Overall Area Vs GM/Id

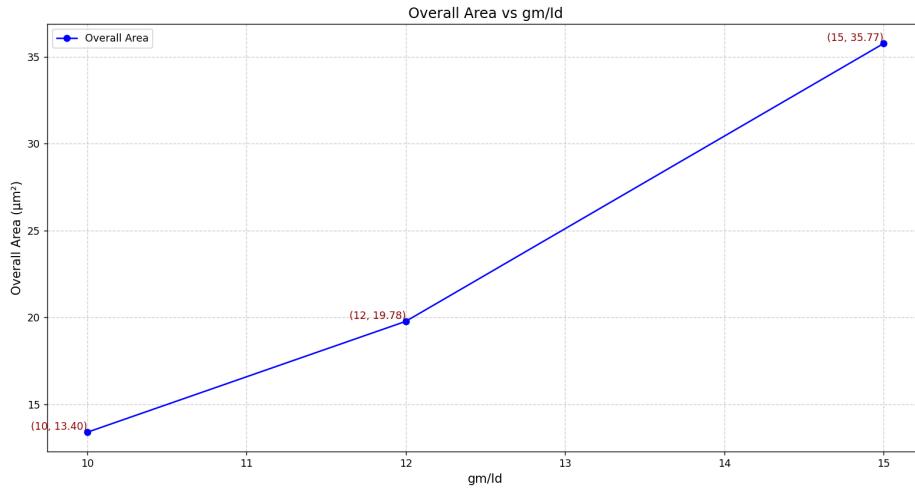


Figure 38: Overall Area Vs GM/Id

We can observe that the area increases but the device is going in the subthreshold region as the overdrive voltage decreases. The V_{gs} is also decreasing assuming that the threshold voltage remains the same. Based on this we can say that the source voltage required to drive the LDO will decrease and also the bias currents required to bias the mosfets will reduce and thus we require less power to drive the entire circuit.

2. Internally Compensated LDO

PSRR Simulation Results

we have made three schematics in LTSpice to calculate the three conditions. We have made a simulation artifact for the same.

Case 1 : Loop Gain Analysis

Case 2 : Open Loop PSRR Calculation

Case 3 : Closed Loop PSRR Calculation

Light Load (2mA)

Schematic

Case 1:- Loop gain analysis:-

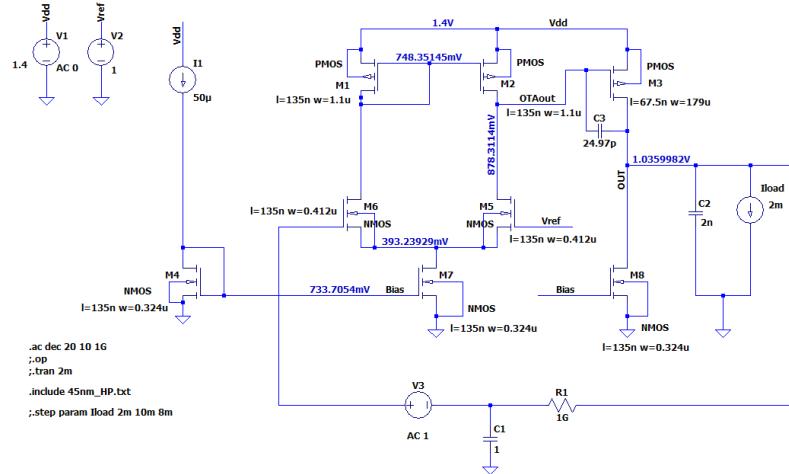


Figure 39: Schematic

Output Log File:-

```

LTspice 24.0.12 for Windows
Circuit: * C:\Users\usman\Downloads\502_try1.asc
Start Time: Tue Dec 3 22:05:11 2024
solver = Normal
Maximum thread count: 12
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:      m1        m2        m3        m4        m5
Model:     pmos      pmos      pmos      nmos      nmos
Id:       -2.44e-05  -2.41e-05  -2.05e-03  5.00e-05  2.41e-05
Vgs:      -6.52e-01  -6.52e-01  -5.22e-01  7.34e-01  6.07e-01
Vds:      -6.52e-01  -5.22e-01  -3.64e-01  7.34e-01  4.85e-01
Vbs:       0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.00e+00
Vth:      -4.89e-01  -4.90e-01  -4.81e-01  4.67e-01  4.68e-01
Vdsat:    -1.78e-01  -1.78e-01  -9.30e-02  2.41e-01  1.50e-01
Gm:       2.46e-04   2.43e-04   3.59e-02  2.79e-04  2.44e-04
Gds:      2.43e-06   2.64e-06   1.39e-03  3.31e-06  2.24e-06
Gmb:      5.20e-05   5.14e-05   7.41e-03  7.01e-05  5.66e-05
Cbd:      4.66e-16   4.79e-16   8.08e-14  1.35e-16  1.81e-16
Cbs:      8.80e-16   8.80e-16   1.43e-13  2.59e-16  3.30e-16

Name:      m6        m7        m8
Model:     nmos      nmos      nmos
Id:       2.44e-05  4.85e-05  5.10e-05
Vgs:      6.09e-01  7.34e-01  7.34e-01
Vds:      3.55e-01  3.93e-01  1.04e+00
Vbs:       0.00e+00   0.00e+00   0.00e+00
Vth:      4.68e-01  4.68e-01  4.66e-01
Vdsat:    1.52e-01  2.40e-01  2.41e-01
Gm:       2.43e-04  2.69e-04  2.83e-04
Gds:      2.98e-06  6.98e-06  3.17e-06
Gmb:      5.67e-05  6.78e-05  7.12e-05
Cbd:      1.86e-16  1.45e-16  1.28e-16
Cbs:      3.30e-16  2.59e-16  2.59e-16

Total elapsed time: 0.122 seconds.

```

Figure 40: Output Log Details

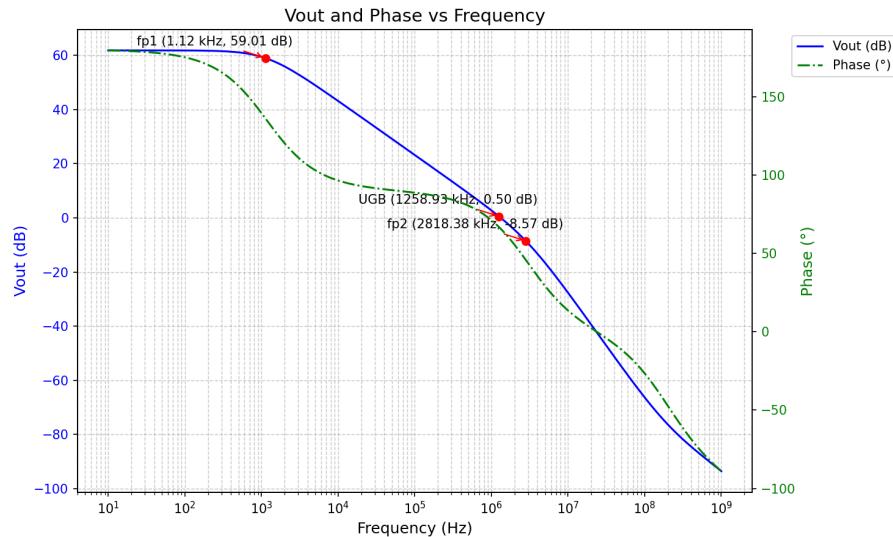
From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.652	0.652	0.489	0.163	Saturation
M2	PMOS	0.522	0.652	0.490	0.162	Saturation
M3	PMOS	0.364	0.522	0.481	0.041	Saturation
M4	NMOS	0.734	0.734	0.467	0.267	Saturation
M5	NMOS	0.485	0.607	0.468	0.139	Saturation
M6	NMOS	0.355	0.609	0.468	0.141	Saturation
M7	NMOS	0.393	0.734	0.468	0.266	Saturation
M8	NMOS	1.04	0.734	0.466	0.268	Saturation

Table 12: Transistor Parameters and Operating Regions

Output on Python:-Figure 41: V_{out} and phase vs Frequency for light load

Phase margin

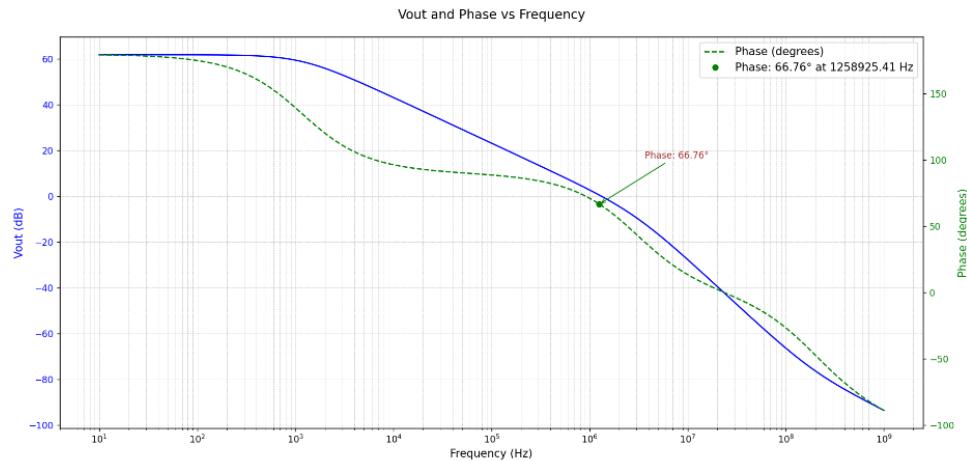


Figure 42: Phase margin

Case 2:- Open Loop PSRR calculation

Schematic

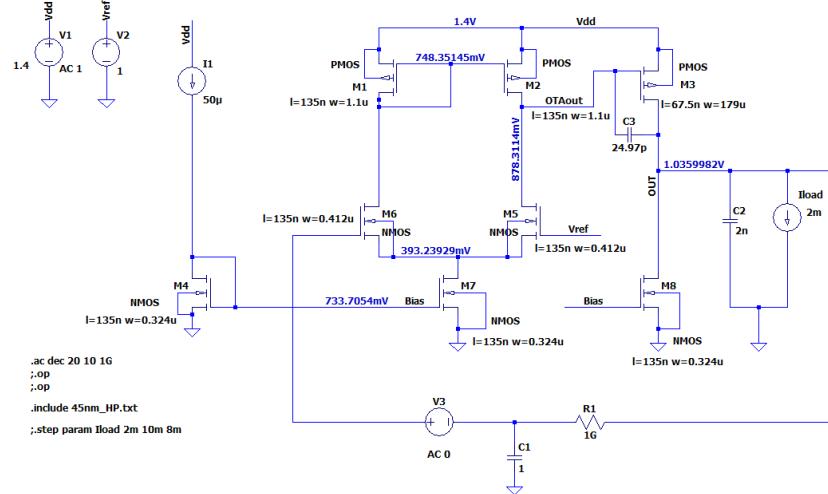


Figure 43: Schematic

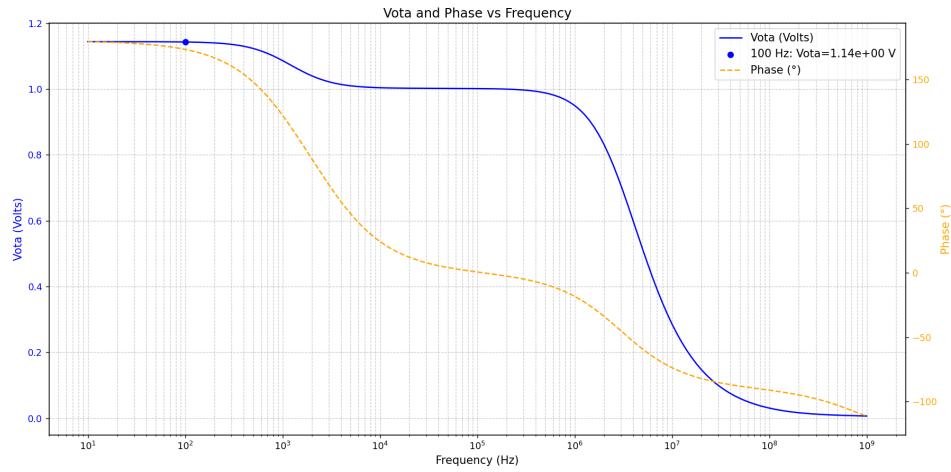
Output on Python:-

Figure 44: Vota and phase vs Frequency for light load

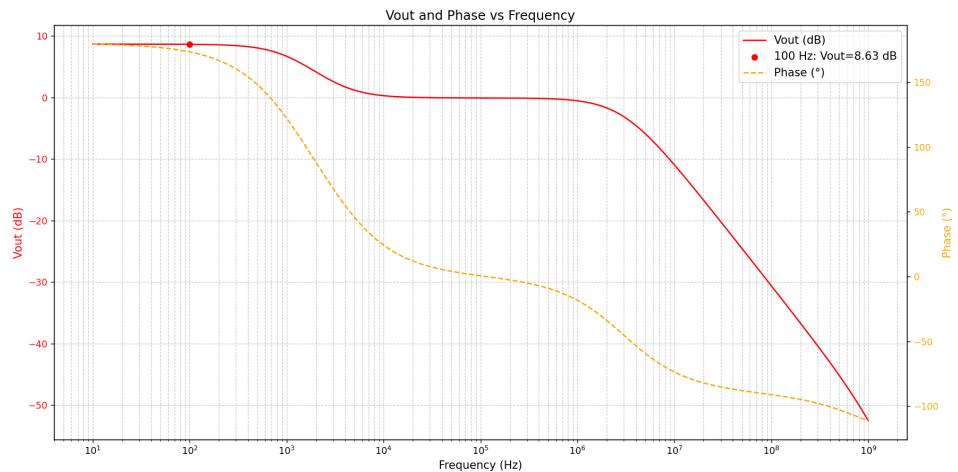


Figure 45: Vout and phase vs Frequency for light load

Case 3:- Closed loop PSRR calculation

Schematic

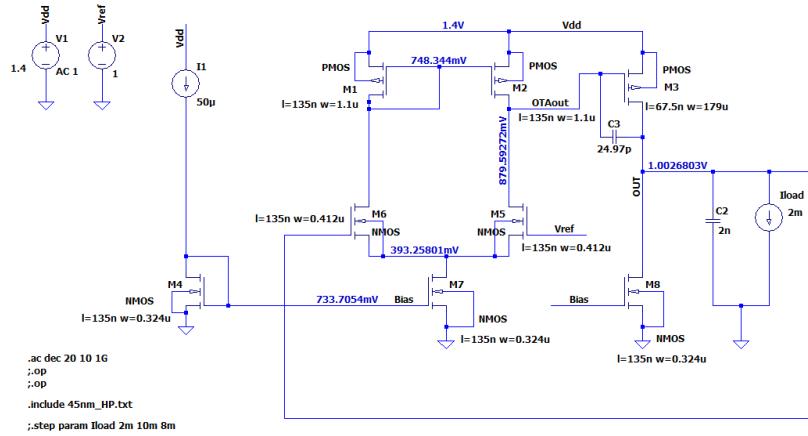


Figure 46: Schematic

Output on Python:-

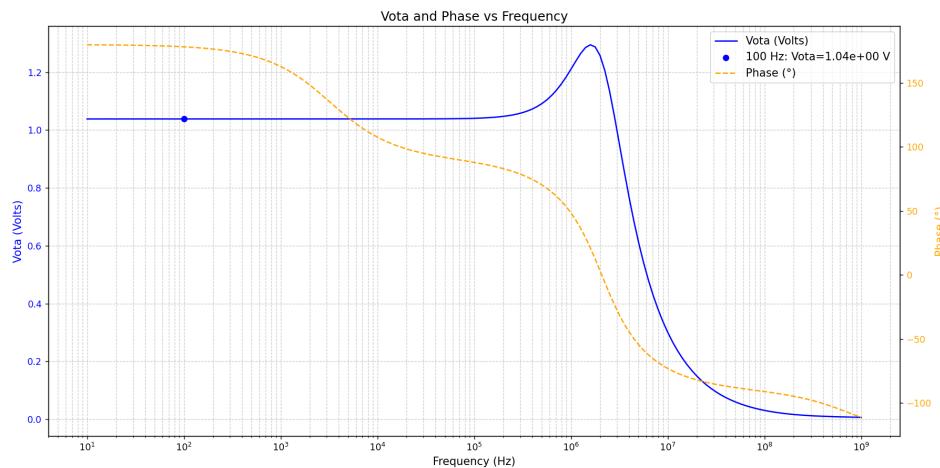


Figure 47: Vota and phase vs Frequency for light load

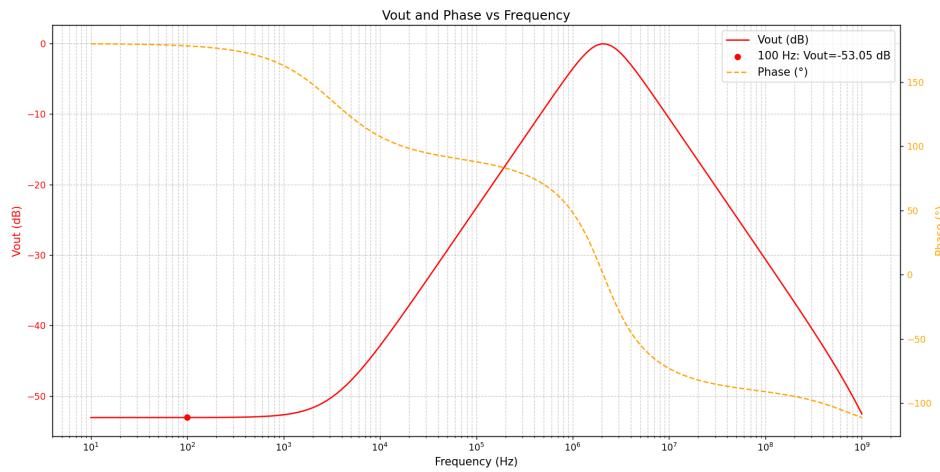


Figure 48: Vout and phase vs Frequency for light load

Heavy Load (10mA)

Schematic

Case 1:- Loop gain analysis:-

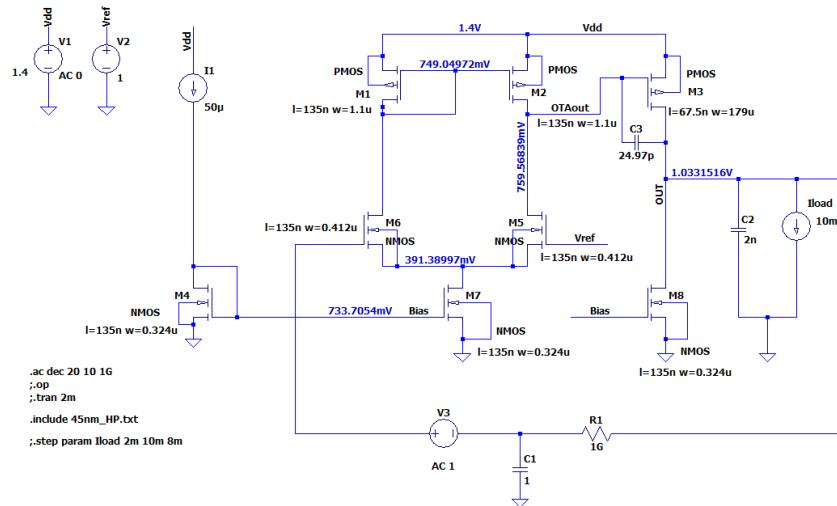


Figure 49: Schematic

Output Log File:-

```

SPICE Output Log: C:\Users\usman\Downloads\502_try1.log
LTspice 24.0.12 for Windows
Circuit: * C:\Users\usman\Downloads\502_try1.asc
Start Time: Tue Dec 3 22:07:31 2024
solver = Normal
Maximum thread count: 12
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:     m1      m2      m3      m4      m5
Model:   pmos    pmos    pmos    nmos    nmos
Id:    -2.43e-05  -2.42e-05  -1.01e-02  5.00e-05  2.43e-05
Vgs:   -6.51e-01  -6.51e-01  -6.40e-01  7.34e-01  6.09e-01
Vds:   -6.51e-01  -6.40e-01  -3.67e-01  7.34e-01  3.68e-01
Vbs:    0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
Vth:   -4.89e-01  -4.89e-01  -4.81e-01  4.67e-01  4.68e-01
Vdsat: -1.78e-01  -1.78e-01  -1.73e-01  2.41e-01  1.51e-01
Gm:    2.45e-04  2.45e-04  9.78e-02  2.79e-04  2.43e-04
Gds:   2.42e-06  2.43e-06  4.82e-03  3.31e-06  2.83e-06
Gmb:   5.18e-05  5.18e-05  2.07e-02  7.01e-05  5.65e-05
Cbd:   4.66e-16  4.67e-16  8.07e-14  1.35e-16  1.86e-16
Cbs:   8.80e-16  8.80e-16  1.43e-13  2.59e-16  3.30e-16

Name:     m6      m7      m8
Model:   nmos    nmos    nmos
Id:    2.43e-05  4.85e-05  5.09e-05
Vgs:   6.09e-01  7.34e-01  7.34e-01
Vds:   3.58e-01  3.91e-01  1.03e+00
Vbs:    0.00e+00  0.00e+00  0.00e+00
Vth:   4.68e-01  4.68e-01  4.66e-01
Vdsat: 1.51e-01  2.40e-01  2.41e-01
Gm:    2.43e-04  2.69e-04  2.83e-04
Gds:   2.93e-06  7.07e-06  3.17e-06
Gmb:   5.65e-05  6.77e-05  7.12e-05
Cbd:   1.86e-16  1.45e-16  1.28e-16
Cbs:   3.30e-16  2.59e-16  2.59e-16

```

Figure 50: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	PMOS	0.651	0.651	0.489	0.162	Saturation
M2	PMOS	0.640	0.651	0.489	0.162	Saturation
M3	PMOS	0.367	0.640	0.481	0.159	Saturation
M4	NMOS	0.734	0.734	0.467	0.267	Saturation
M5	NMOS	0.368	0.609	0.468	0.141	Saturation
M6	NMOS	0.358	0.609	0.468	0.141	Saturation
M7	NMOS	0.391	0.734	0.468	0.266	Saturation
M8	NMOS	1.03	0.734	0.466	0.268	Saturation

Table 13: Updated Transistor Parameters and Operating Regions

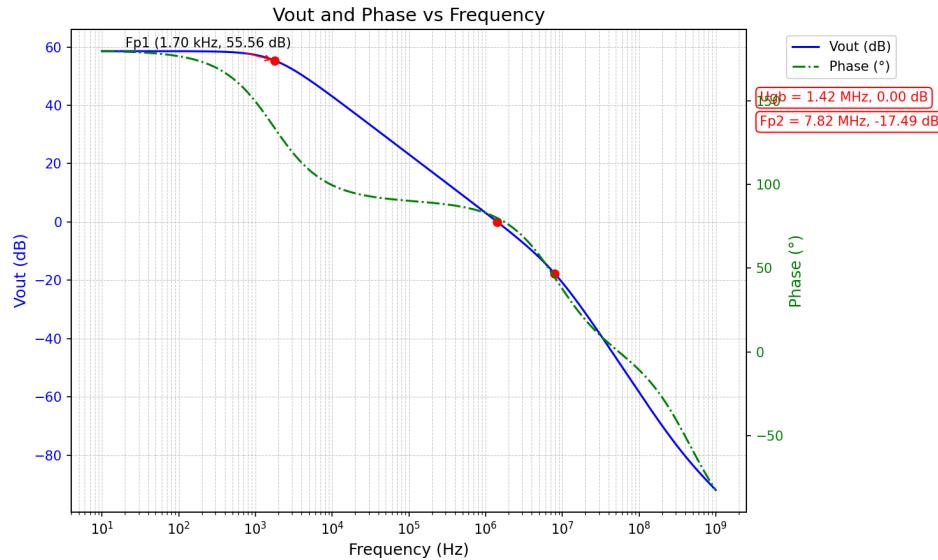
Output on Python:-

Figure 51: Vout and phase vs Frequency for high load

Phase Margin

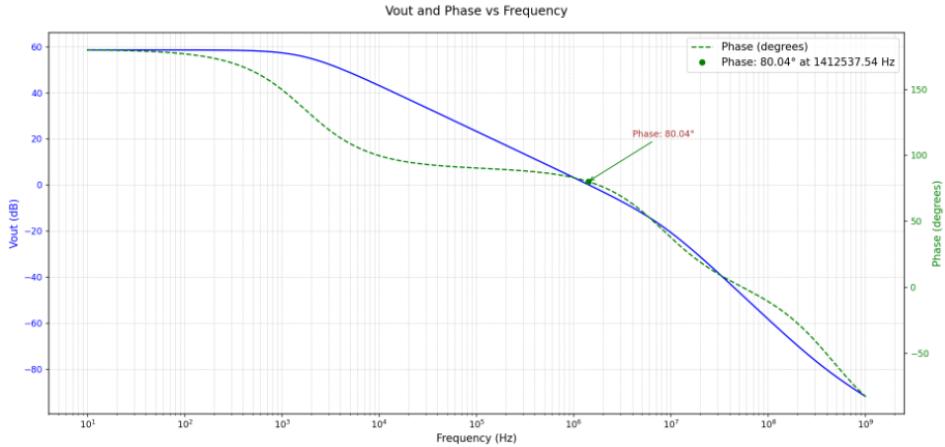


Figure 52: Phase Margin

Observations: The phase margin obtained is 80.04 degrees. This value is higher compared to that obtained for a light load. This is because, in internally compensated LDOs, the first and second poles move away from the origin as the load current increases, but the unity gain bandwidth remains constant irrespective of the load current change. Due to this, the second pole in light load conditions is closer to the unity gain bandwidth frequency than in heavy load conditions. Consequently, we observe a higher phase margin for the heavy load condition compared to the light load.

Case 2:- Open Loop PSRR calculation

Schematic

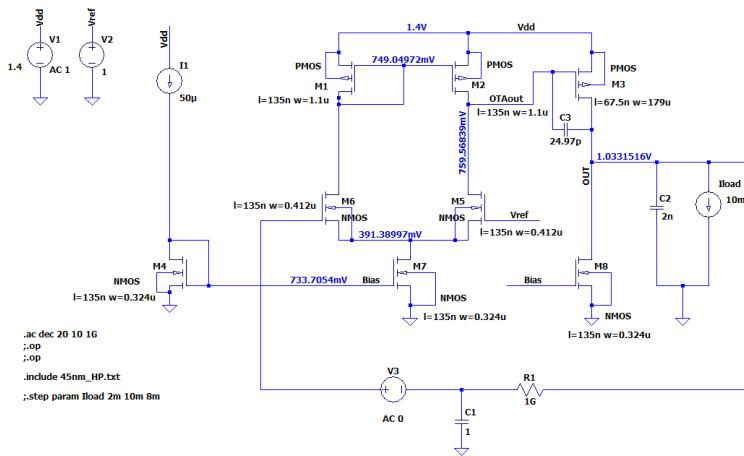


Figure 53: Schematic

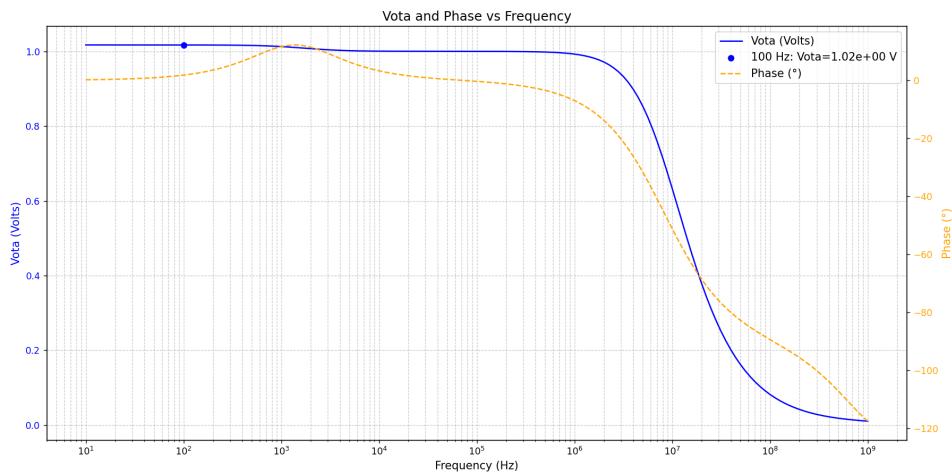
Output on Python:-

Figure 54: Vota and phase vs Frequency for high load

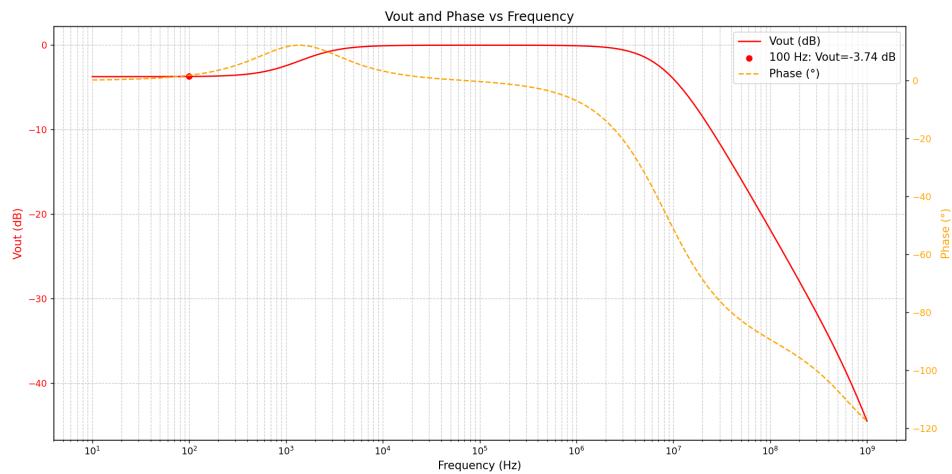


Figure 55: Vout and phase vs Frequency for high load

Case 3:- Closed loop PSRR calculation

Schematic

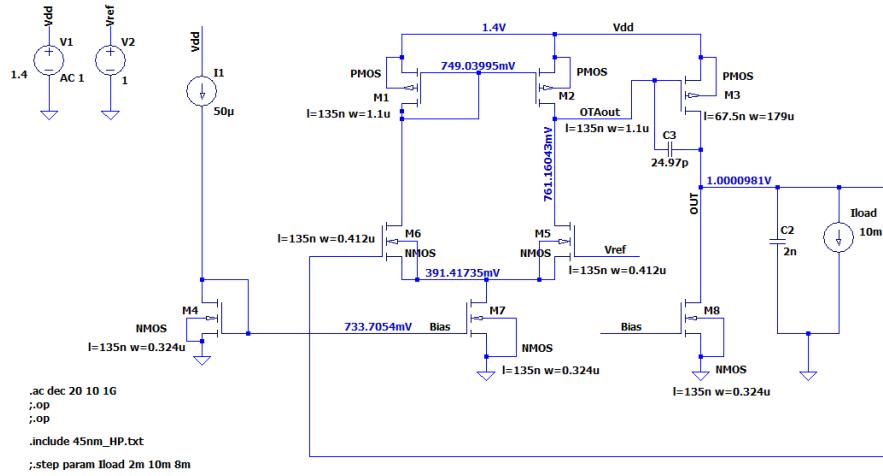


Figure 56: Schematic

Output on Python:-

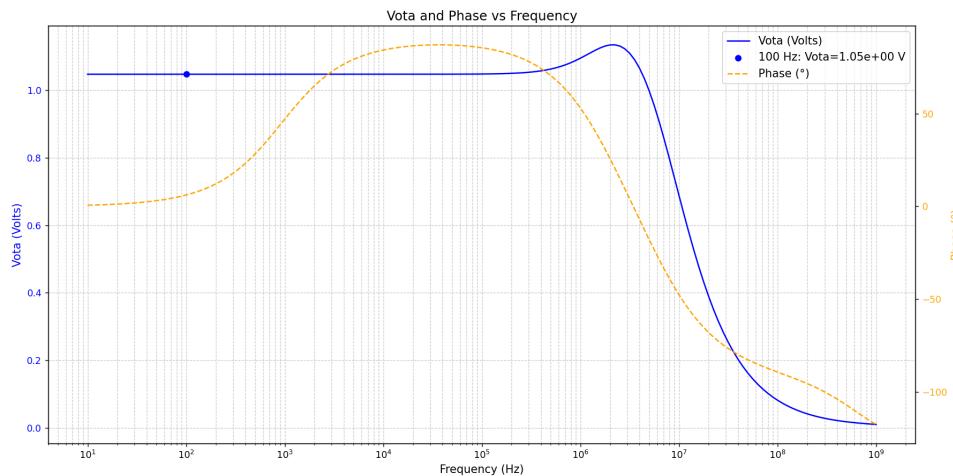


Figure 57: Vota and phase vs Frequency for high load

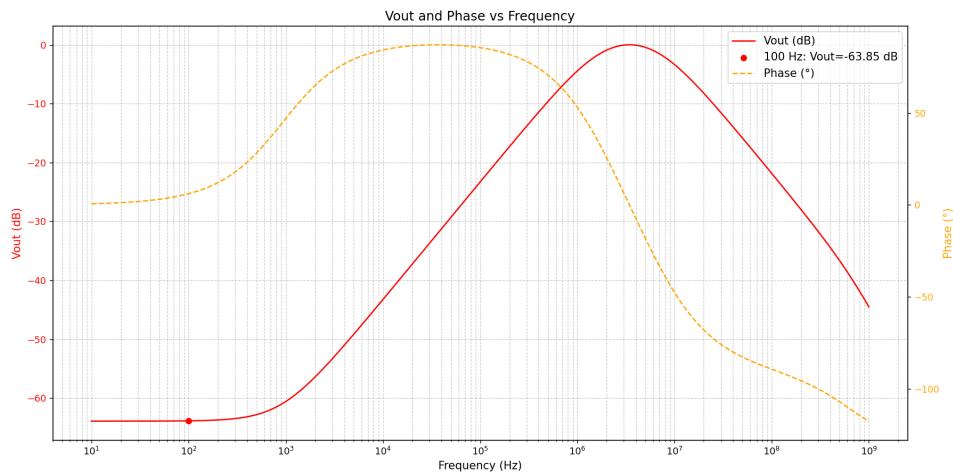


Figure 58: Vout and phase vs Frequency for high load

Transient Analysis

Schematic

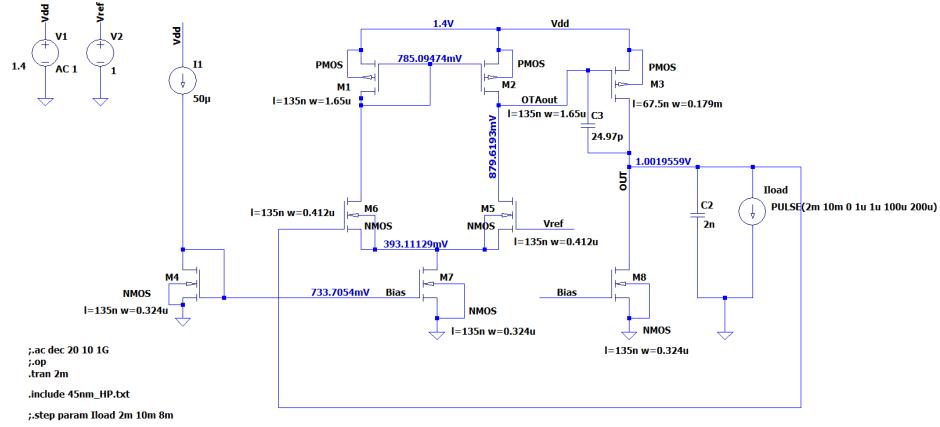


Figure 59: Schematic

Iload Vs Time

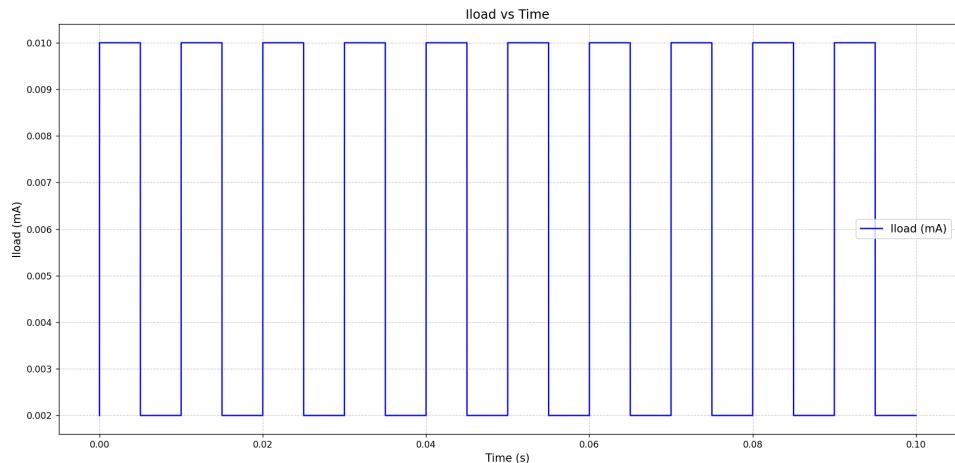


Figure 60: Iload Vs Time

Vout vs Time

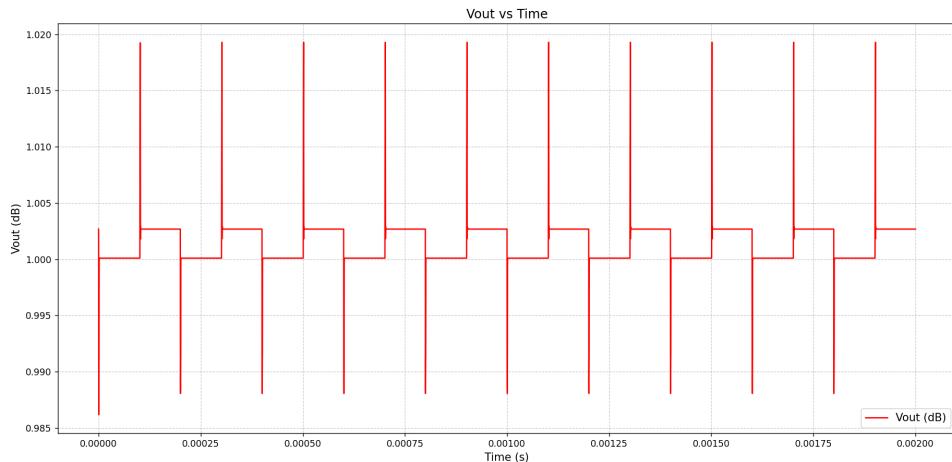


Figure 61: Vout vs Time

Observations:

- In the above figure, we observe that when the output load current transitions from 2 mA to 10 mA (from best-case to worst-case condition in terms of stability), there is a larger peak during this transition compared to the transition from 10 mA to 2 mA. This is because 10 mA represents the worst-case condition, leading to more deviation in the peak.
- Additionally, there were no overshoots or undershoots observed during the externally compensated transient analysis. This behavior is attributed to the 1 μ F capacitor attached at the load, which effectively manages the overshoots and undershoots.

FET Sizes

In the below table we have mentioned the sizing of the entire LDO including the sizing of the passfet, differential- amplifier , pmos load and the current mirror circuit.

Table 14: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	0.179m/67.5n	10	24.18	55.62	50.76 GHz
Diff-Amp pmos	1.1u/135n	10	97.93	22.71	11.71 GHz
Diff-Amp nmos	0.412u/135n	10	93.43	60.51	30 GHz
Current Mirror nmos	0.324u/135n	10	155	154.1	30 GHz

The value of the capacitance for the internal capacitor is 24.97pf

Stability Analysis

For Heavy load we get the following curve:

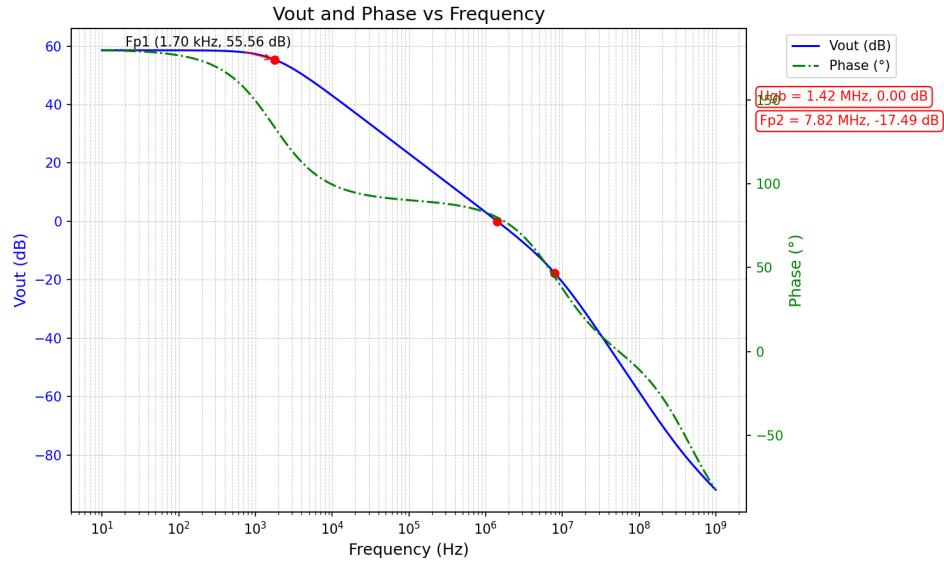


Figure 62: Vout and phase vs Frequency for high load

For Light load we get the following curve

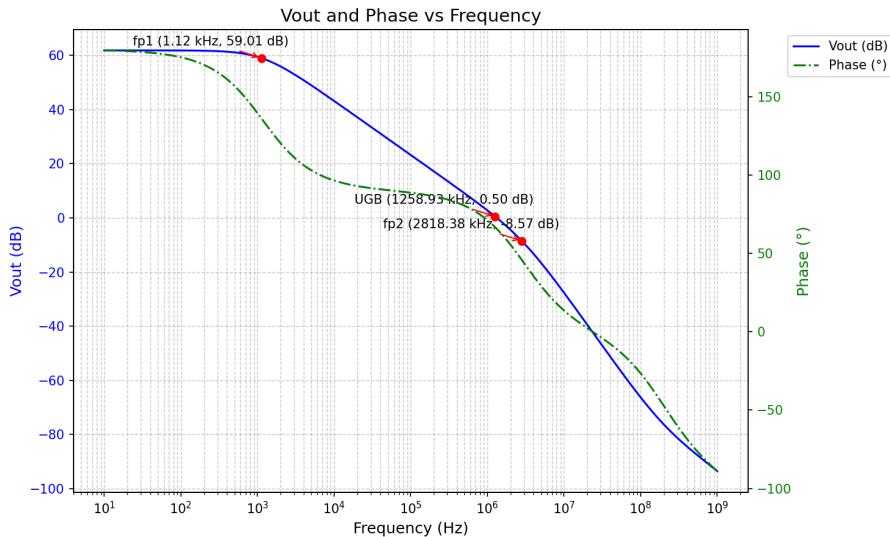


Figure 63: Vout and phase vs Frequency for light load

From the above analysis we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. From the phase margin also we can observe that we observe a lesser phase margin of 76 degrees for the heavy load case than that of the light load case. From this analysis, we can say that we get a more stable system when we apply light load.