DEPARTMENT OF ELECTRONICS ANDCOMMUNICATION ENGINEERING

PDPM-IIITDM JABALPUR, MADHYA PARDESH - 482005

Cadence Lab File

IT 3E01: -

(Cadence),2022-23

Submitted to

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Submitted by:

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Experiment1: Design and analysis of transfer and output characteristics of NMOS circuit using cadence.

Procedure:

1. Go to work

2. Open terminal there

3. type commands:

* csh

* Source cshrc_new12 or cshrc_new1 or cshrc_new based on the cshrc file present in the work folder

* virtuoso

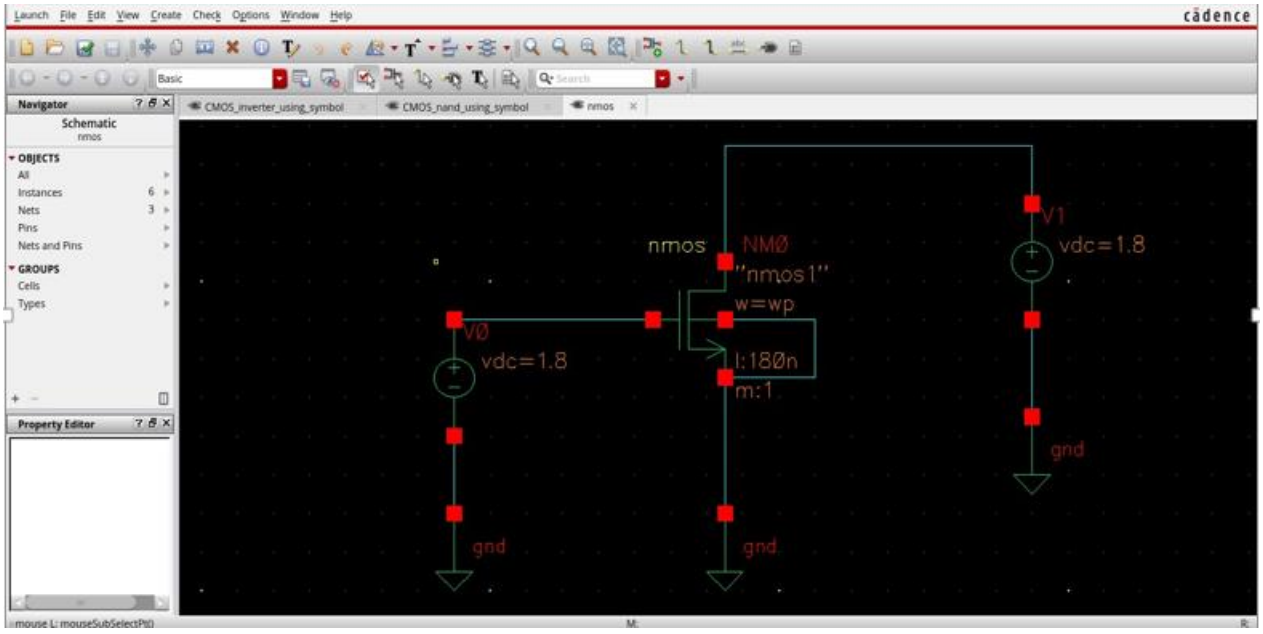
4. After Virtuoso is launched , select file -> new -> create new library -> type name(your name for example) and select “Attach to an existing technology library option and press ok.

In the “Attach Design Library to Technology File” form, select gpdk180 from the cyclic field and click OK.

A new folder with your name is created successfully.

5. Now again Select File->New->cellview->select the library name which you created above(with your name)->give it a name(ex. Cmos inverter)->click ok.

6. Create **NMOS Diagram**



- Click instance  (or press I) -> select library(gpdk180 for nmos and pmos, analog lib for normal circuit components like battery, resistance etc) -> choose the required component ->close->hide -> paste the component.
- The components can be joined using wires , wires are selected by clicking wires icon  or pressing shortcut ‘w’ , wires are drawn by pressing and holding the mouse button
- Nmos and pmos can be acquired from gpdk_new library and voltage ,pulse ground and resistance can be obtained in analogLib library

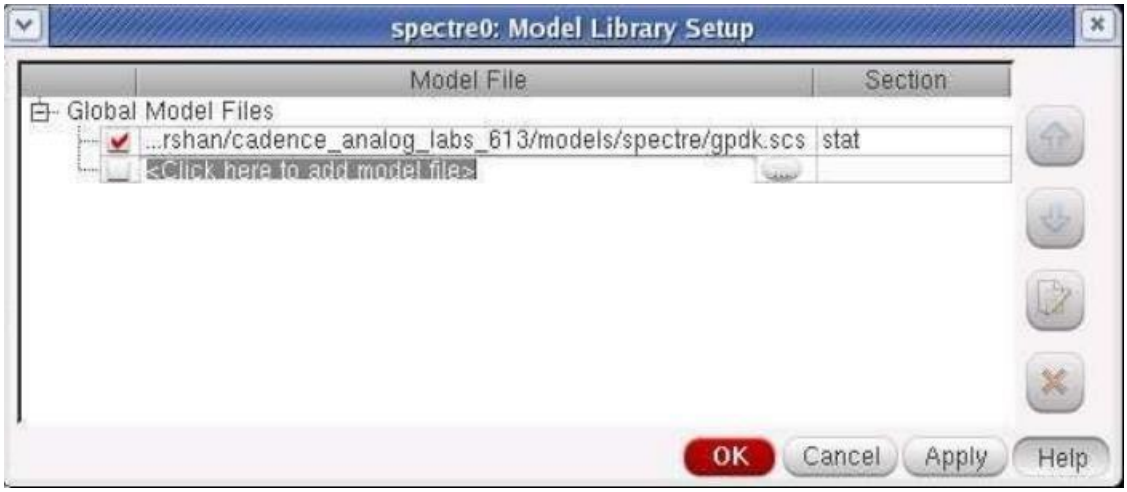
7.Check for errors using key ‘x’ or by clicking the check and save option next to the save file button. After successful compilation now do the simulation.

8.Launch ADEL

- Click Launch ADEL from the top left corner.

- Setup the working environment model libraries using following process:

  Setup->model libraries->path of file if already not present:
  /TOOLS/PDK/180_new/models/spectre/gpdk.scs->Choose stat



Input Characteristics :

9.Within ADEL click on output menu

- Output->select from Design
- Select Vgs (click on wire for voltage) and Id(click on node)
- Click ok

10.Click Analysis

- Choose dc analysis
- Component sweep parameter
- Component Name, from schematic choose Vgs->dv voltage
- Start : 0 , Stop : 1.8
- Click ok

11. Plotting

- Run using Green play button located on right side

12.Results are obtained on a graph plot

Output characteristics :

13. Within ADEL click on output menu

- Output->select from Design
- Select Vds (click on wire for voltage) and Id(click on node)
- Click ok

14.Click Analysis

- Choose dc analysis
- Component sweep parameter
- Component Name, from schematic select choose Vds->dc voltage
- Start : 0 , Stop : 1.8
- Click ok

15. Plotting

- Run using Green play button located on right side

Parametric analysis

16.In the schematic select nmos->press ‘q’ button->give nmos Total width as variable (w)

17.Launch ADEL and setup environment as given in step number 8-15 for different parametric analysis on input and output characteristics.

18.Go to outputs and select Vgs and Id

19.Click on ‘Variables’ menu and select ‘copy from cellview’ option until you see w as the parameter on the left side.

20. Once variable is visible in left side of window , intialize the variable with some value(say 2u)

21. Click Tools->parametric analysis

- GIve following values:
- Add variable->w
- Range ->from/to
- From: 2u
- To :10u
- Step mode: linear steps
- Step size: 2u

22.Select dc analysis as given in previous steps and vary Vgs

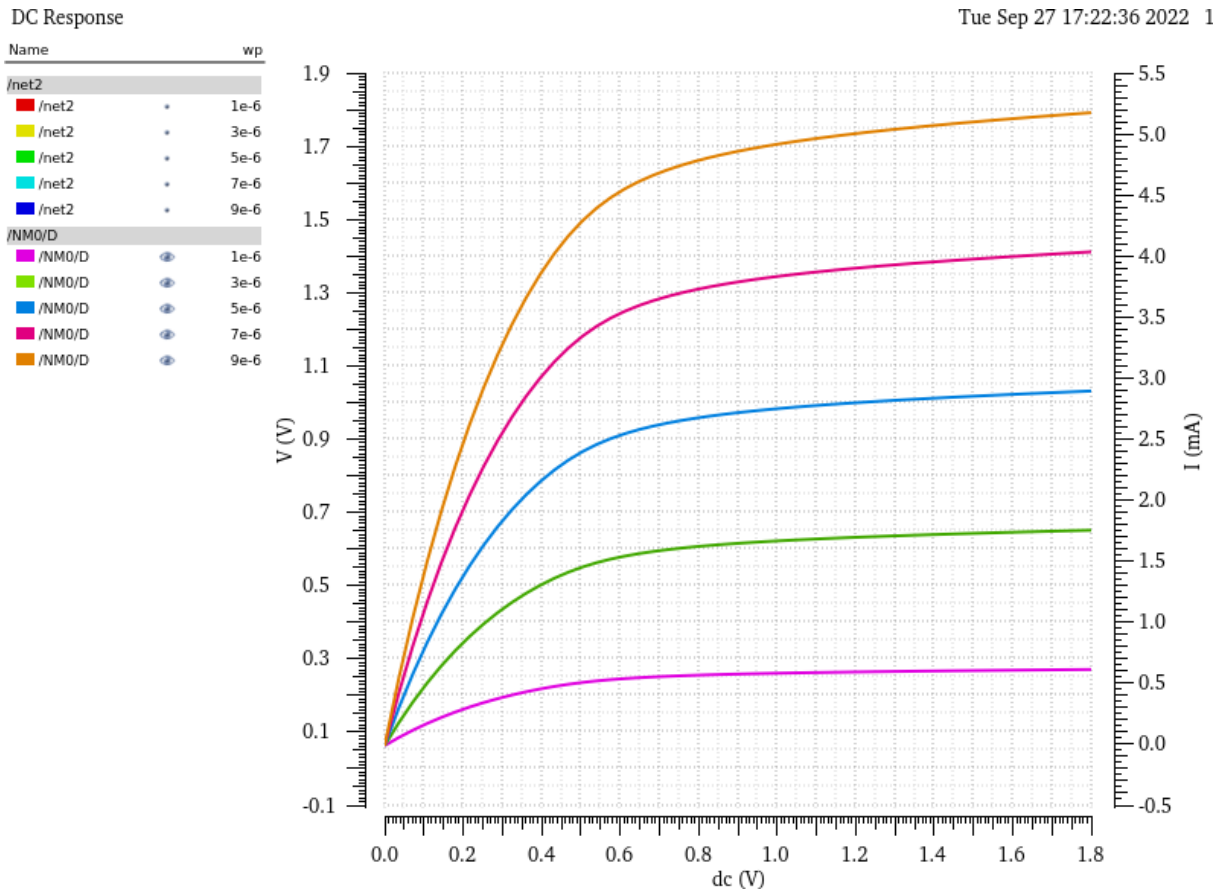
23.Run using Green play button In parametric analysis screen.

24. For output parametric analysis select Vds in place of Vgs and follow the same procedure.

25.Results are obtained in a graph

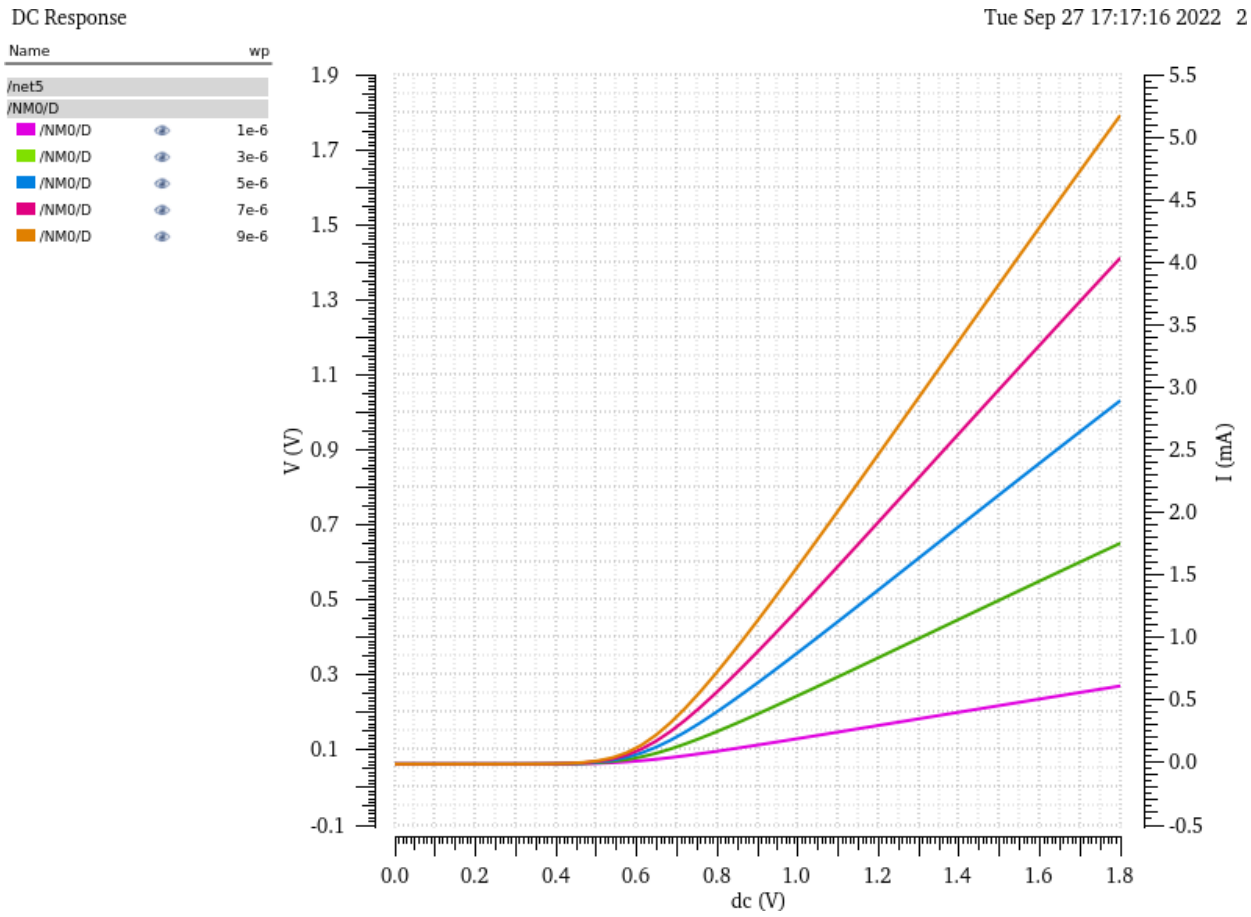
Results:

1. We can see that the saturation current increases with increase in the value of width of nmos(wp).



Id vs Vds curve with varying width

2. The value of transconductance(Id/Vgs) increases with increase in the value of wp.



Id vs Vgs curve with varying width

Experiment 2: Design resistive load inverter in cadence

Procedure:

1. Go to work

2. Open terminal there

3. type commands:

    * csh

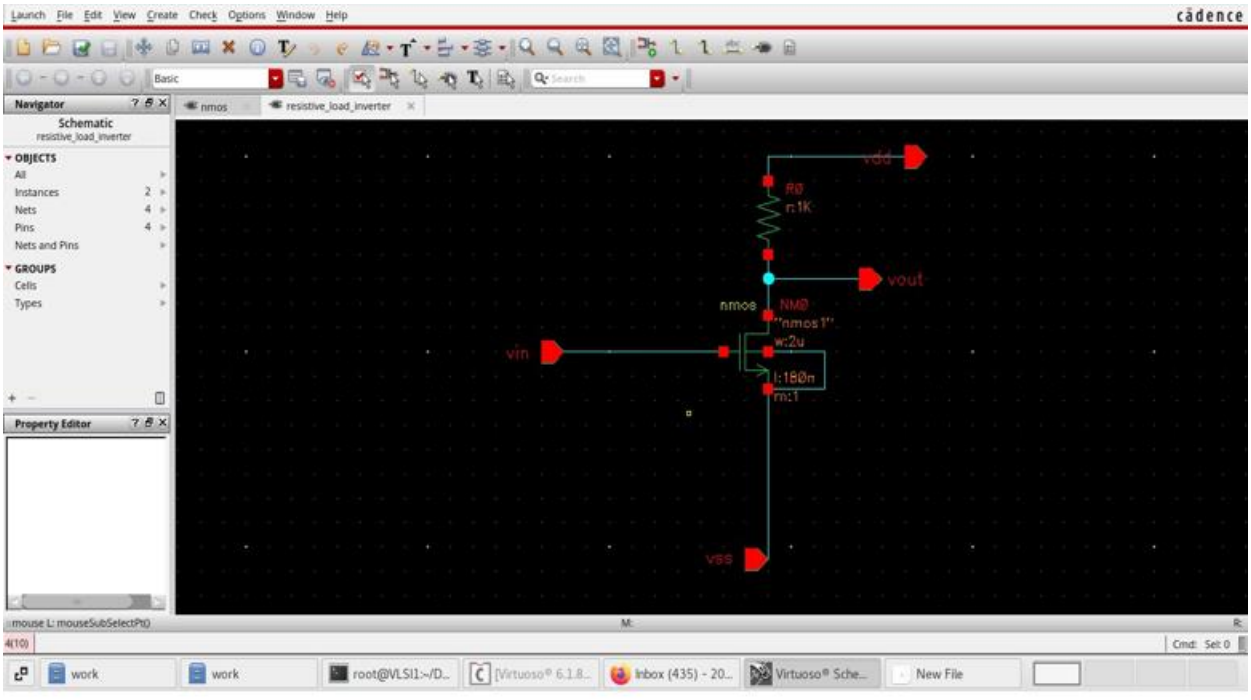
    * Source cshrc_new12 or cshrc_new1 or cshrc_new based on the cshrc file present in the work folder

    * virtuoso

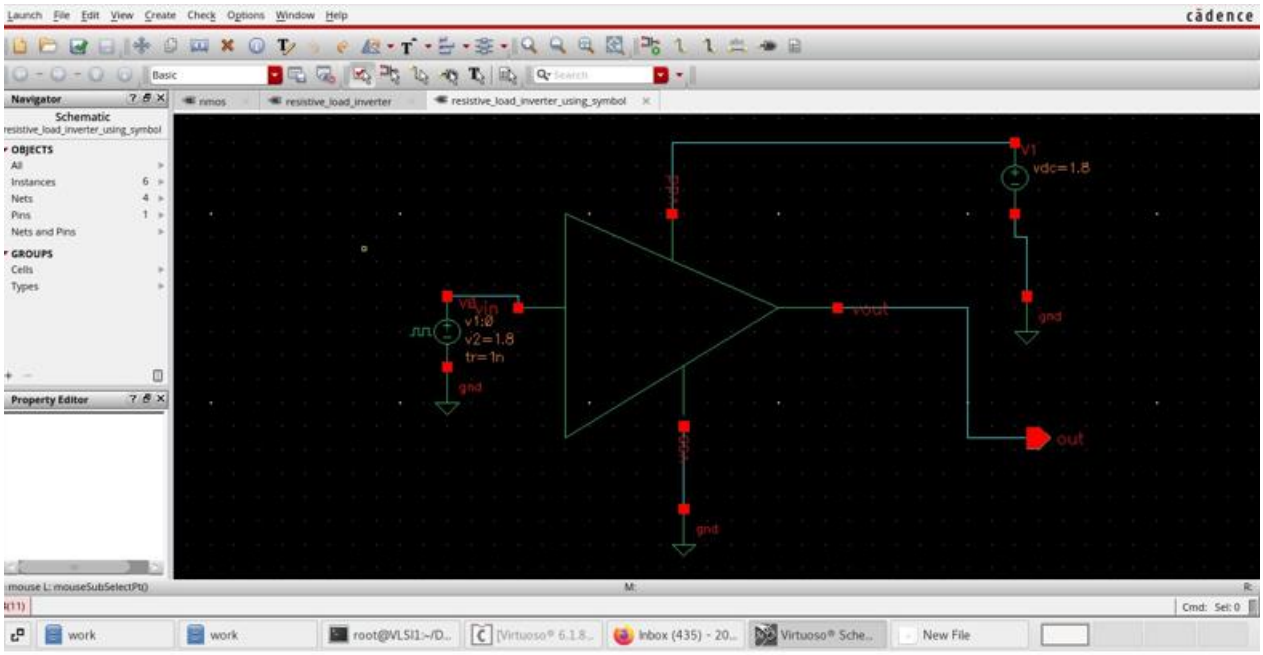
4. After Virtuoso is launched , select file -> new -> create new library -> type name(your name for example) and select “Attach to an existing technology library” option and press ok.

5. Now again Select File->New->cellview->select the library name which you created above(with your name)->give it a name(Resistive Load inverter)->click ok.

6. Create **Resistive Load Inverter Diagram**

7. 

Using Symbol View



- Click instance  (or press I) -> select library(gpdk180 for nmos and pmos, analog lib for normal circuit components like battery, resistance etc) -> choose the required component ->close->hide -> paste the component.
- The components can be joined using wires , wires are selected by clicking wires icon  or pressing shortcut ‘w’ , wires are drawn by pressing and holding the mouse button
- Nmos and pmos can be acquired from gpdk_new library and voltage ,pulse ground and resistance can be obtained in analogLib library.
- Add the necessary input and output pins at the input and output side as shown in the diagram.
- After successful save and check option create its symbol view.
- Create-> Cellview -> from CellView and press ok.

8.After Successful creating symbol, now use that symbol and create the schematic as shown below. After successful save and check we can now proceed to simulation.

9.Launch ADEL

- Click Launch ADEL from the top left corner.

- Setup the working environment model libraries using following process:
    - Setup->model libraries->path of file is not already present:
    - /TOOLS/PDK/180_new/models/spectre/gpdk.scs->Choose stat
- Now click the analysis optioin in the ADL window.
- Select ->dc -> save DC point -> select component -> select vgs-> dc voltage -> set range from 0 to 1.8 V -> click ok.
- Select outputs -> to be plotted -> select on screen->
    - Select vgs and vds by clicking on their wires.
- Click the green button to start the simulation.

9.Output graph is shown below.

10.We can make the graph more accurate by changing the value of Resistance.

11.Now for the parametric analysis we change the nmos width to some variable w.

12.In the ADL window repeat previous steps to set dc analysis along with the

input. Analysis-> transient -> Stop time=200n -> Moderate -> ok for transient

analysis.

12.Click on 'Variables' menu and select 'copy from cellview' option until you see w as the parameter on the left side.

14. Once variable is visible in left side of window , initialize the variable with some value(say 2u)

15. Click Tools->parametric analysis

- GIve following values:
- Add variable->w
- Range ->from/to
- From: 2u
- To :10u
- Step mode: linear steps
- Step size: 2u

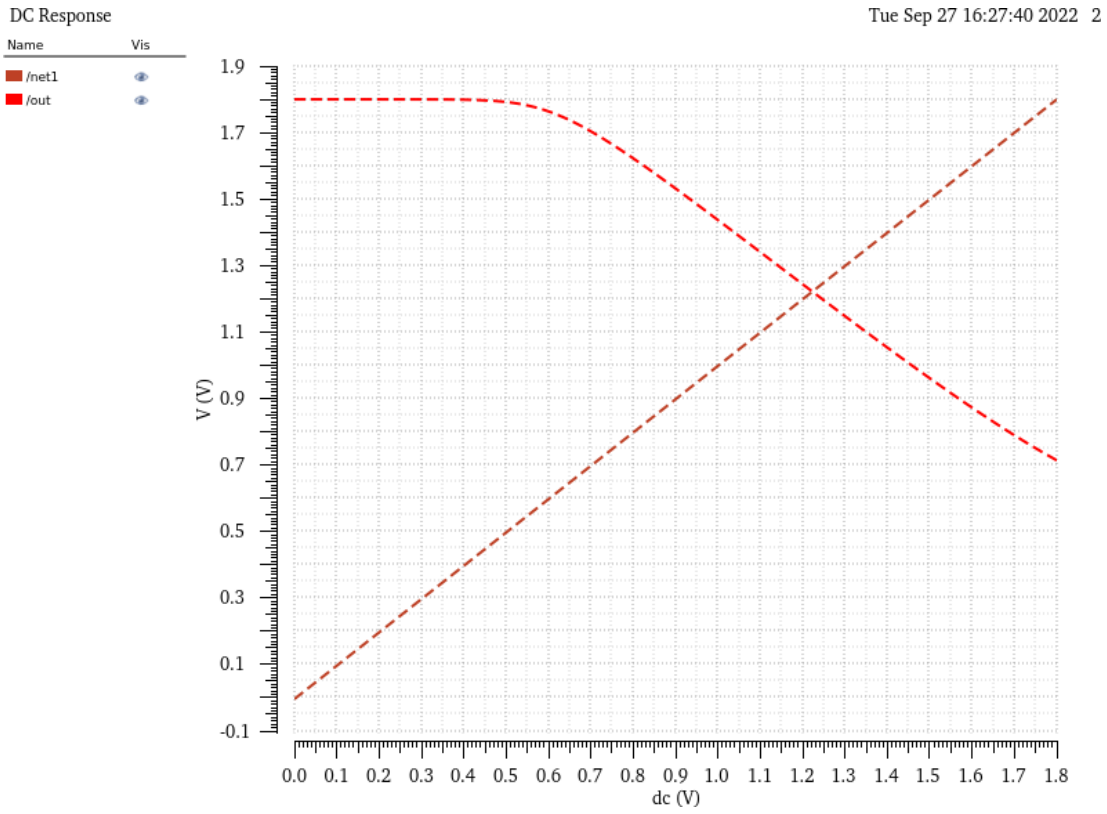
16.Run using Green play button In parametric analysis screen.

17.For output parametric analysis select Vds in place of Vgs and follow the same procedure.

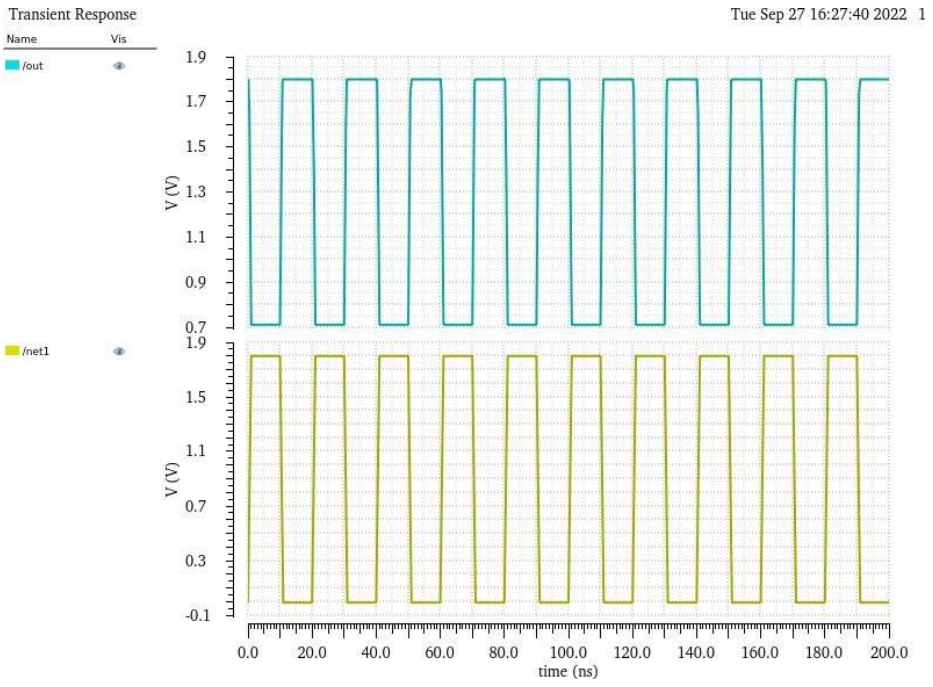
18.Results are obtained in a graph

Results:

1. By varying value the value of R we obtain a graph significantly close to the ideal inerter in transient response and a sharp drop is obtained in dc analysis.



DC ANALYSIS



Transient Analysis

Experiment 3: Design CMOS Inverter using Cadence

Procedure:

1. Go to work

2. Open terminal there

3. type commands:

   * csh

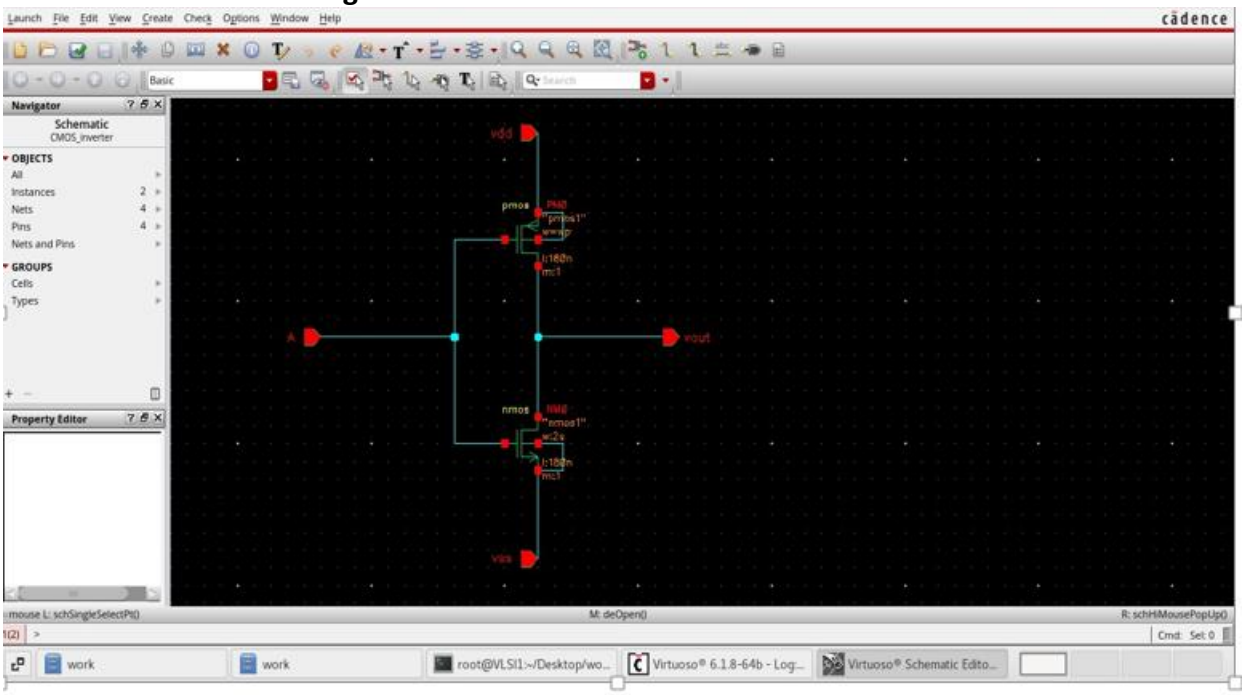
   * Source cshrc_new12 or cshrc_new1 or cshrc_new based on the cshrc file present in the work folder

   * virtuoso

4. After Virtuoso is launched , select file -> new -> create new library -> type name(your name for example) and select “Attach to an existing technology library” option and press ok.

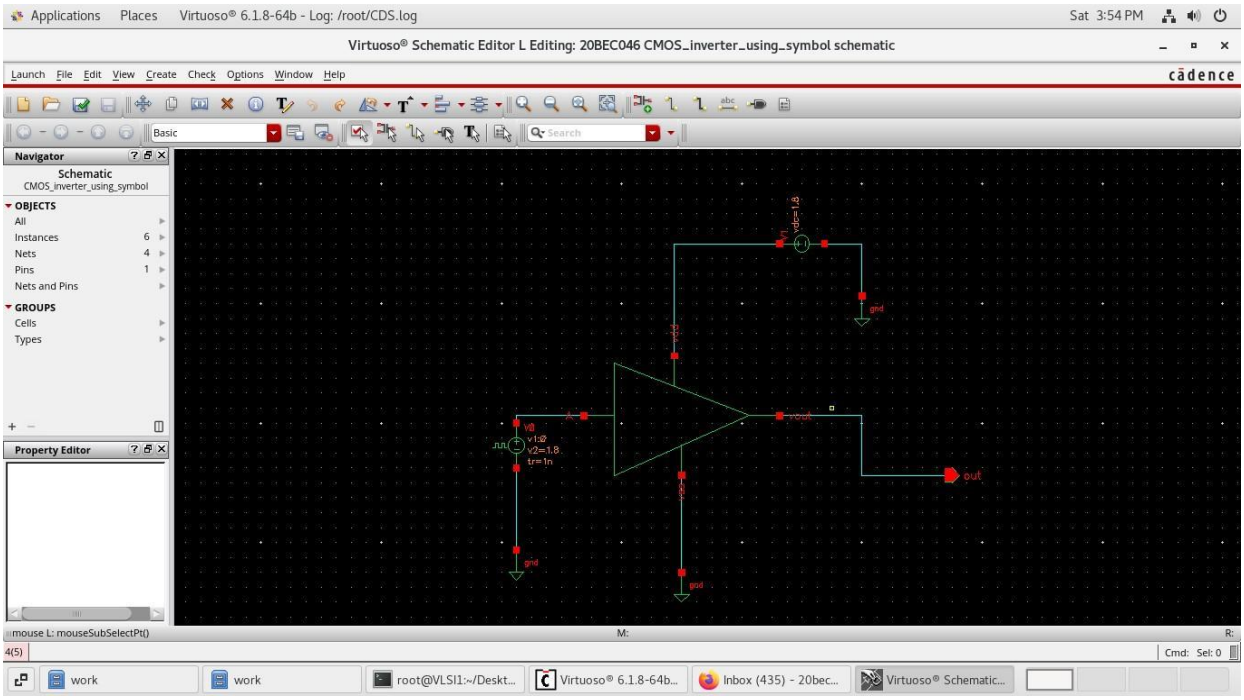
5. Now again Select File->New->cellview->select the library name which you created above(with your name)->give it a name(Resistive Load inverter)->click ok.

6. Create **CMOS Inverter Diagram**



7.

Symbol View



- Click instance (or press I) -> select library(gpdk180 for nmos and pmos, analog lib for normal circuit components like battery, resistance etc) -> choose the required component ->close->hide -> paste the component.
- The components can be joined using wires , wires are selected by clicking wires icon  or pressing shortcut ‘w’ , wires are drawn by pressing and holding the mouse button
- Nmos and pmos can be acquired from gpdk_new library and voltage ,pulse ground and resistance can be obtained in analogLib library.
- Add the necessary input and output pins at the input and output side as shown in the diagram.
- After successful save and check option create its symbol view.
- Create-> Cellview -> from CellView and press ok.

8.After Successful creating symbol, now use that symbol and create the schematic as shown below. After successful save and check we can now proceed to simulation.

9.Launch ADEL

- Click Launch ADEL from the top left corner.

- Setup the working environment model libraries using following process:
  - Setup->model libraries->path of file is not already present:
  - /TOOLS/PDK/180_new/models/spectre/gpdk.scs->Choose stat
- Now click the analysis optioin in the ADL window.
- Select ->dc -> save DC point -> select component -> select vin-> dc voltage -> set range from 0 to 1.8 V -> click ok.
- Select outputs -> to be plotted -> select on screen->
  - Select vin and vout by clicking on their wires.
- Click the green button to start the simulation.

9.Output graph is shown below.

10.Now for the parametric analysis we change the nmos width to some variable w.

11.In the ADL window repeat previous steps to set dc analysis along with the input.

12. Click on 'Variables' menu and select 'copy from cellview' option until you see wn as the parameter on the left side.

13. Once variable is visible in left side of window , initialize the variable with some value(say 2u)

14. Click Tools->parametric analysis

- GIve following values:
- Add variable->wn
- Range ->from/to
- From: 2u
- To :10u
- Step mode: linear steps
- Step size: 2u

15. Run using Green play button In parametric analysis screen.

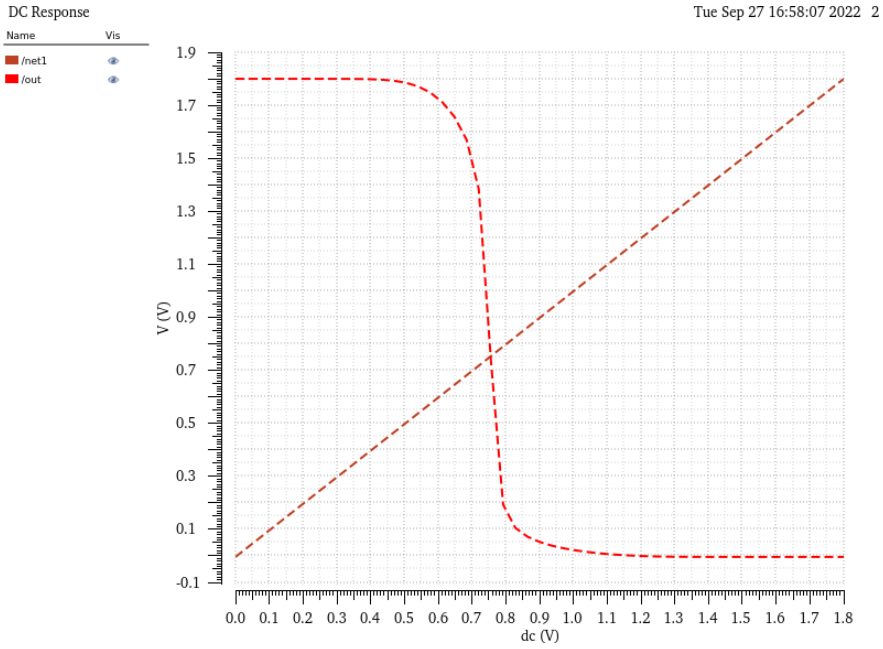
16. For output parametric analysis select Vds in place of Vgs and follow the same procedure.

17.Results are obtained in a graph

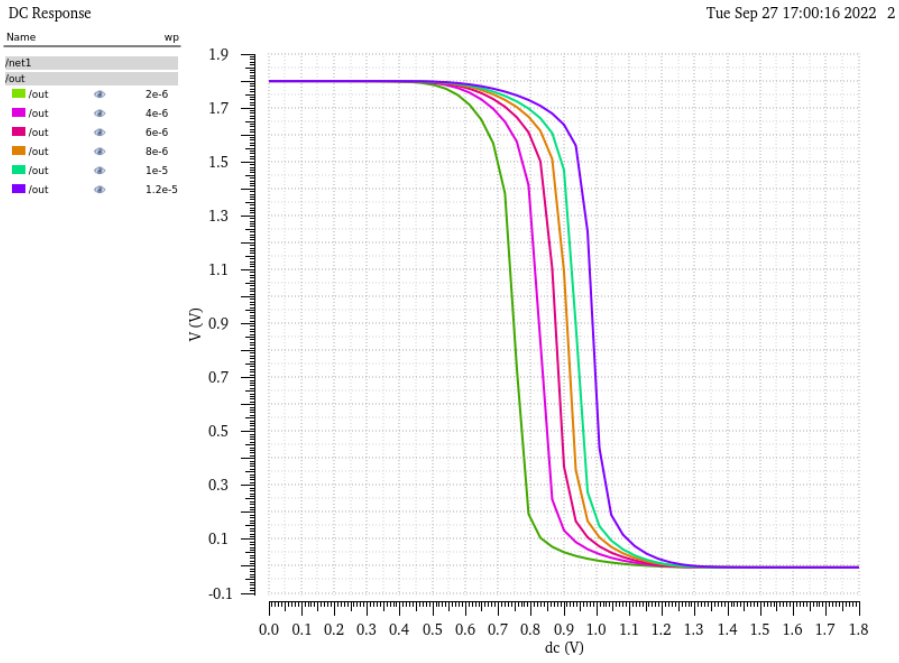
18. Same thing can be done by varying the width of pmos.

Results:

1. Dc analysis for wn=2u of nmos.



2. Parametric analysis for width of nmos. We here observe that the graph falls more rapidly and early with decrease in width of nmos.



Experiment 4: Design and analysis of NAND and NOR circuit using COMS technology.

Procedure: NAND Gate

1. Go to work

2. Open terminal there

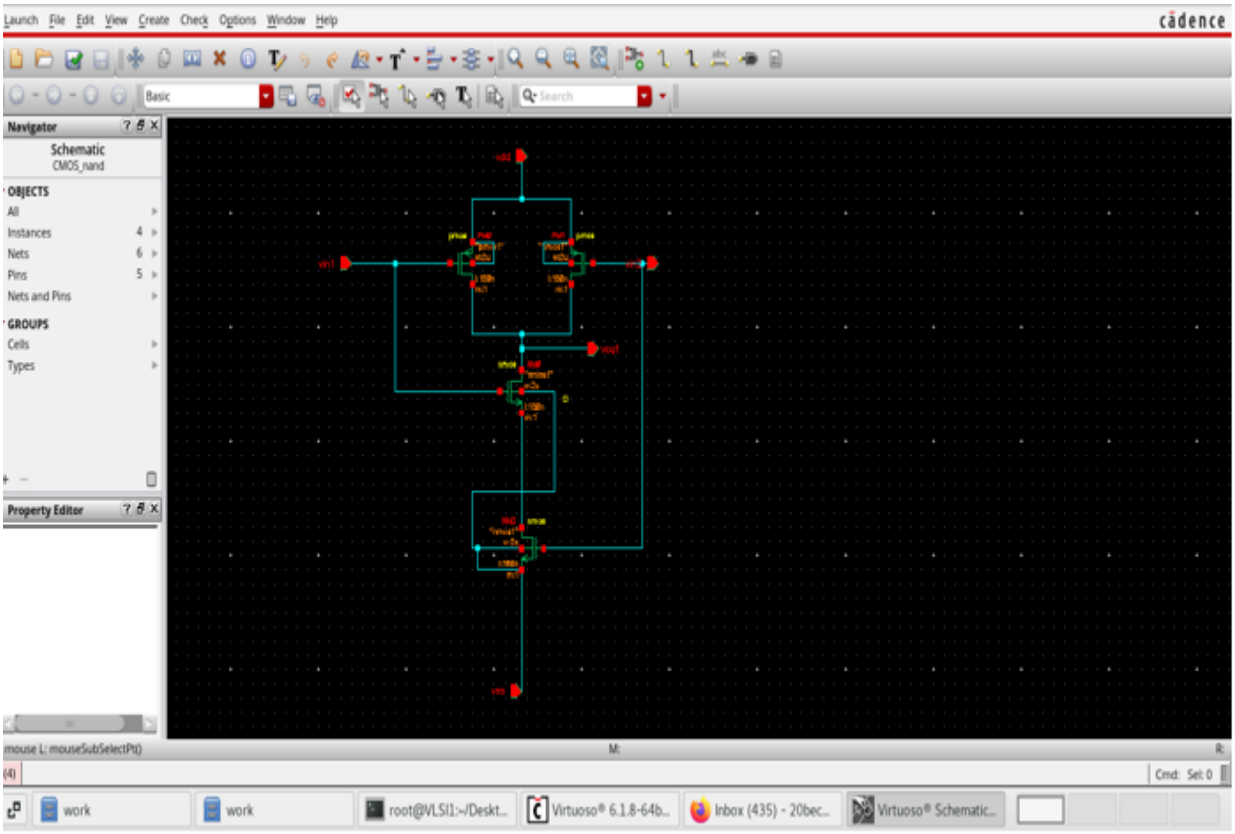
3. type commands:

    * csh
    * Source cshrc_new12 or cshrc_new1 or cshrc_new based on the cshrc file present in the work folder
    * virtuoso

4. After Virtuoso is launched , select file -> new -> create new library -> type name(your name for example) and select “Attach to an existing technology library” option and press ok.

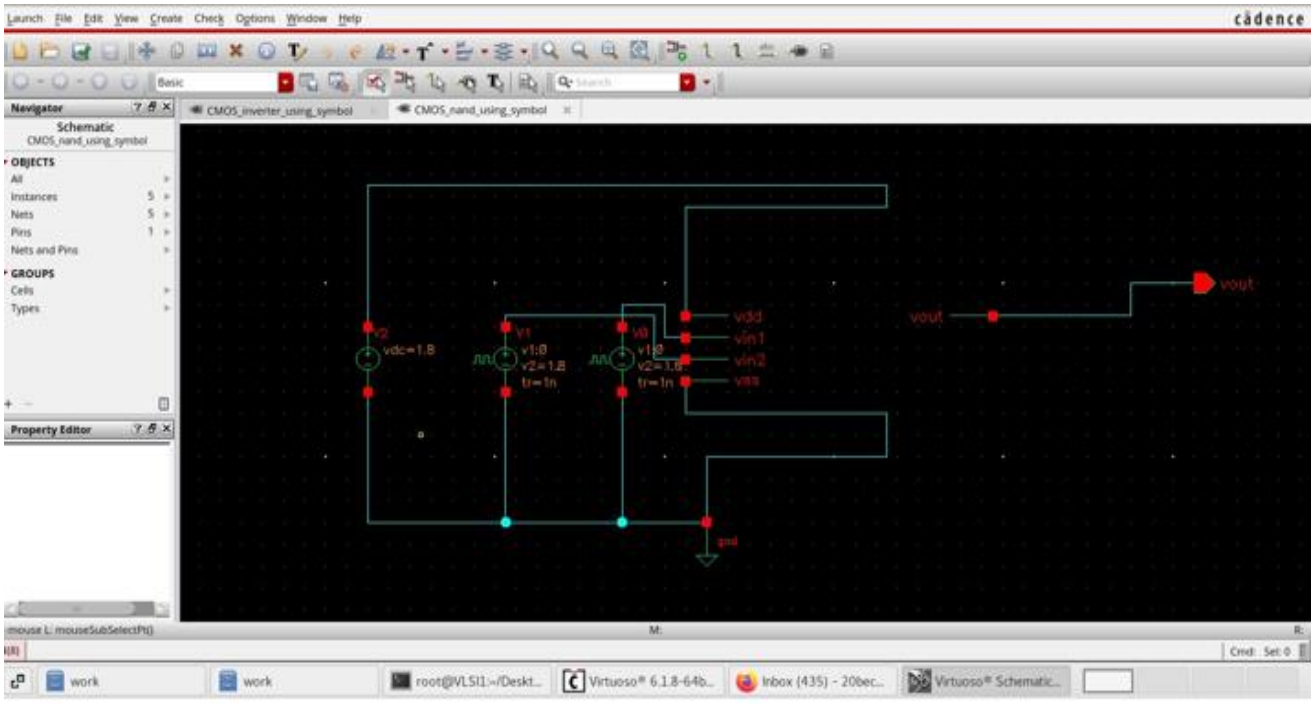
5. Now again Select File->New->cellview->select the library name which you created above(with your name)->give it a name(Resistive Load inverter)->click ok.

6. Create **NAND Diagram**



7.

Symbol view



- Click instance  (or press I) -> select library(gpdk180 for nmos and pmos, analog lib for normal circuit components like battery, resistance etc) -> choose the required component ->close->hide -> paste the component.
- The components can be joined using wires , wires are selected by clicking wires icon  or pressing shortcut ‘w’ , wires are drawn by pressing and holding the mouse button
- Nmos and pmos can be acquired from gpdk_new library and voltage ,pulse ground and resistance can be obtained in analogLib library.
- Add the necessary input and output pins at the input and output side as shown in the diagram.
- After successful save and check option create its symbol view.
- Create-> Cellview -> from CellView and press ok.

8.After Successful creating symbol, now use that symbol and create the schematic as shown below. After successful save and check we can now proceed to simulation.

9.Within the schematic pulse is used in both inputs which can be set up as follows:

- Select pulse component and press ‘q’
- Give following values

- V1:0
- V2:1.8
- Period:10n and 20n seconds respectively.
- Rise and fall time as 1n seconds each.
- Dealy time as 0 seconds.

10. Check for errors using key ‘x’ and save and check the file for

errors. 10.Lauch and set ADEL

11. Setup the model libraries and choose the analysis type as follows->

Analysis-> transient -> Stop time=200n -> Moderate -> ok

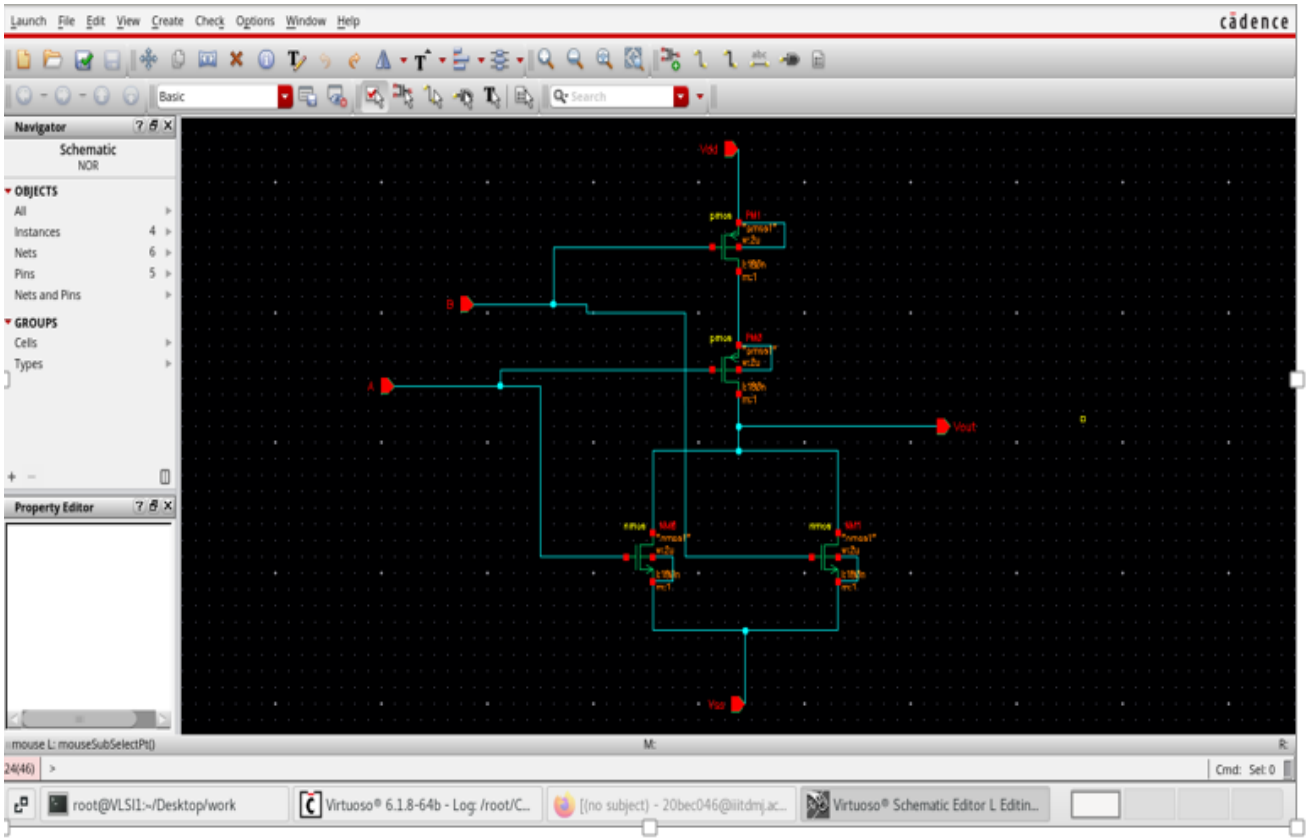
12.Click on output menu and select vout pin and both inputs pins as output and click

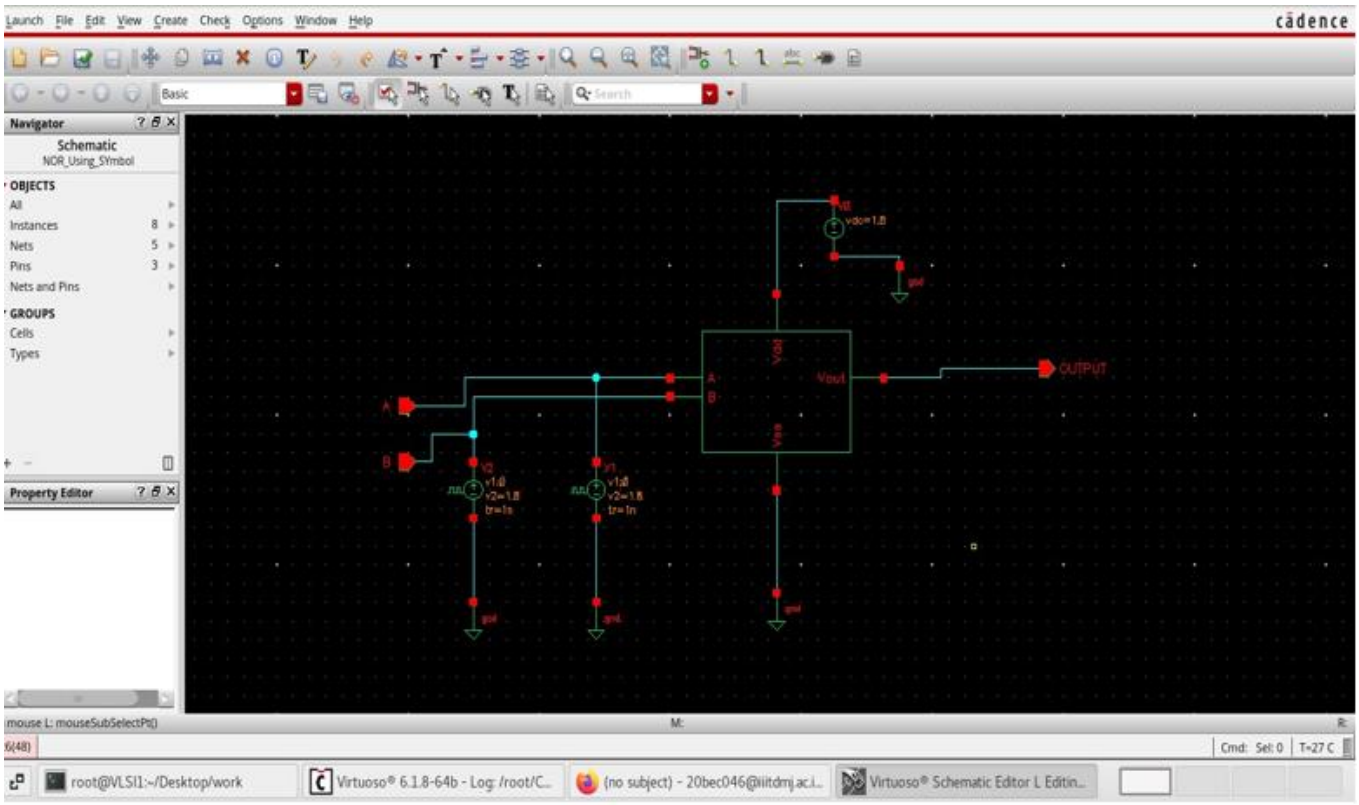
ok 13.Run the stimulation

14. Result is obtained in plot

NOR Gate

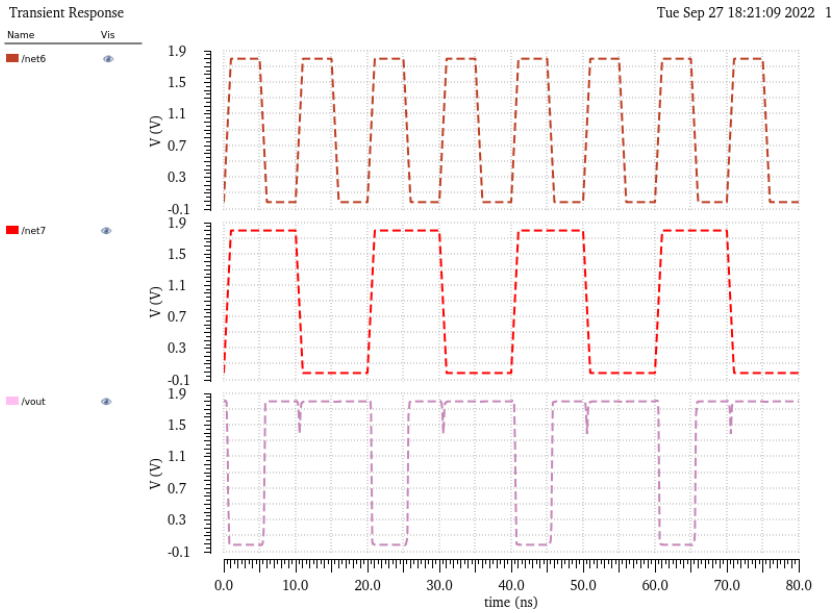
The same procedure needs to be followed using the below schematic for the NOR gate.



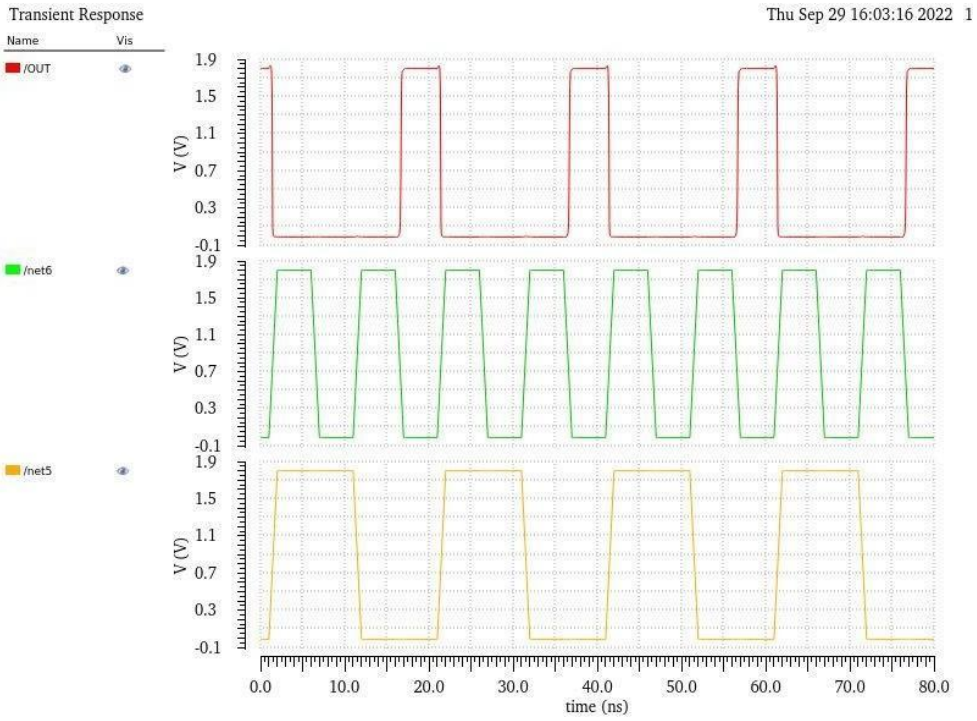


Result:

1. Transient response can be seen from the figure. The NAND(AB)' output shows 0 when both inputs are 1, else the output is always 1.



2. Transient response can be seen from the figure. The NOR(A+B)' output shows 1 when both inputs are 0, else the output is always 0.



Experiment 5: Design and analysis of XOR and XNOR circuit using CMOS technology.

Procedure: XOR Gate

1. Go to work

2. Open terminal there

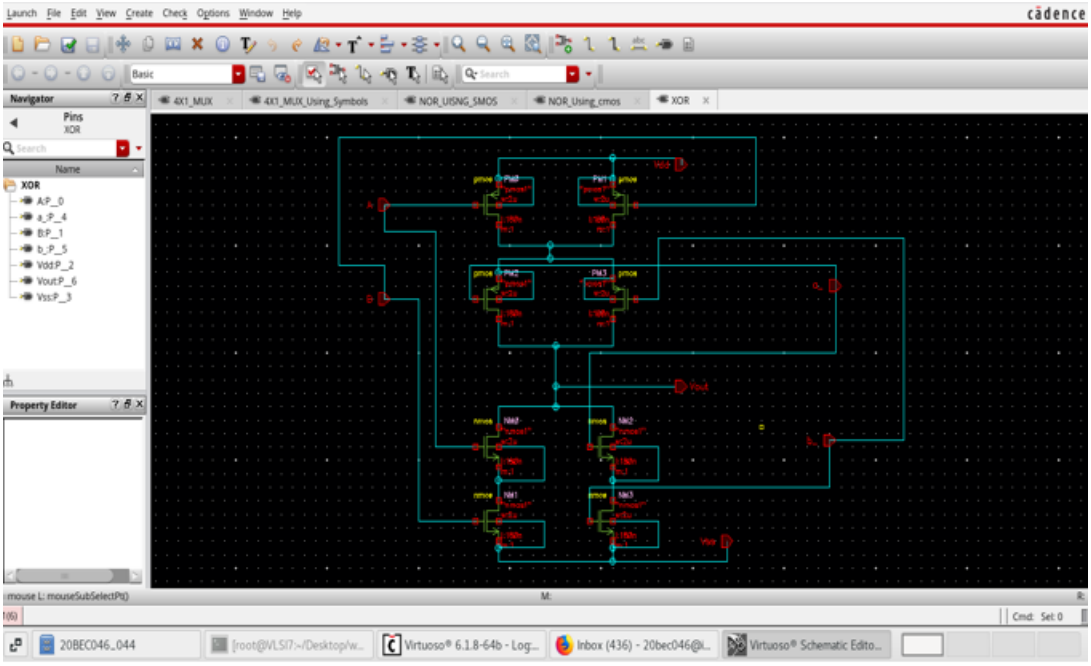
3. type commands:

    * csh
    * Source cshrc_new12 or cshrc_new1 or cshrc_new based on the cshrc file present in the work folder
    * virtuoso

4. After Virtuoso is launched , select file -> new -> create new library -> type name(your name for example) and select “Attach to an existing technology library” option and press ok.

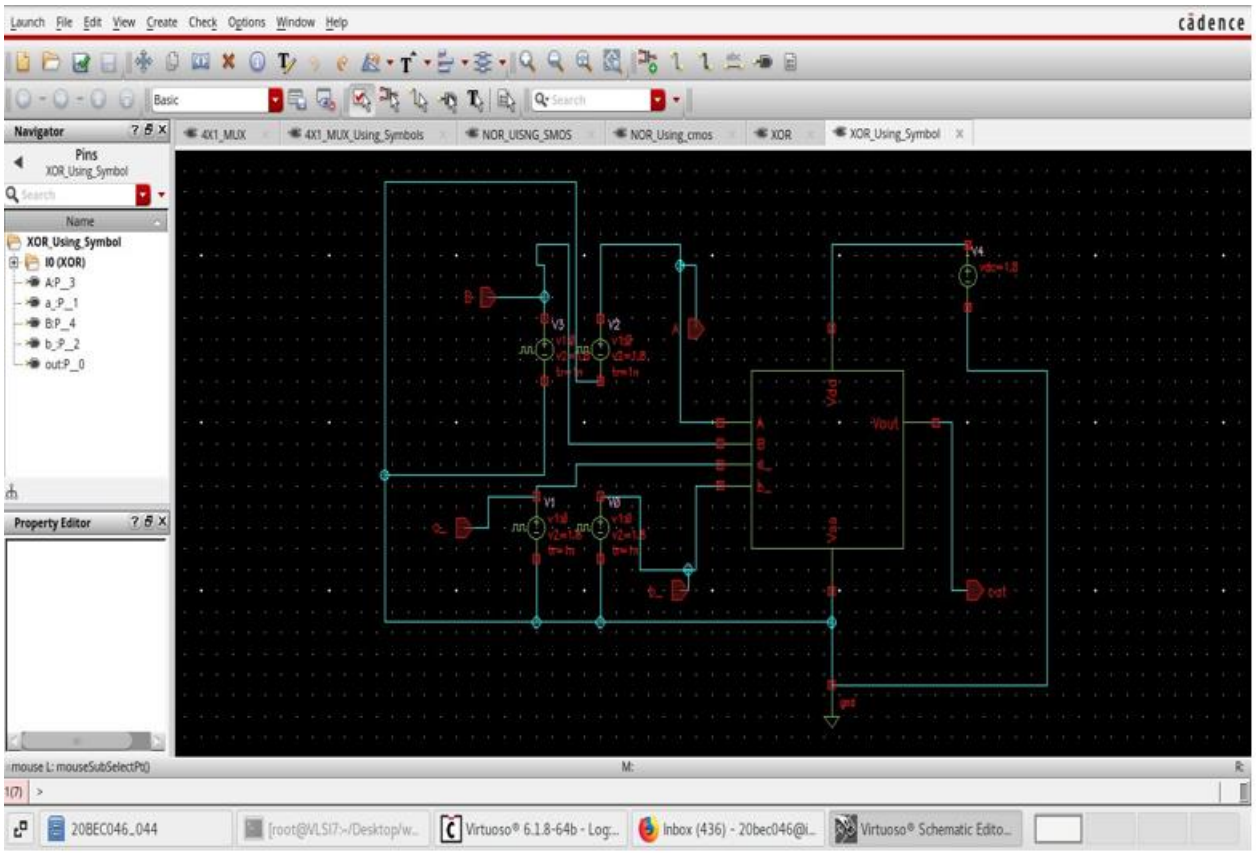
5. Now again Select File->New->cellview->select the library name which you created above(with your name)->give it a name(Resistive Load inverter)->click ok.

6. Create **XOR Diagram**



7.

Symbol view of XOR



- Click instance  (or press I) -> select library(gpdk180 for nmos and pmos, analog lib for normal circuit components like battery, resistance etc) -> choose the required component ->close->hide -> paste the component.
- The components can be joined using wires , wires are selected by clicking wires icon  or pressing shortcut ‘w’ , wires are drawn by pressing and holding the mouse button
- Nmos and pmos can be acquired from gpdk_new library and voltage ,pulse ground and resistance can be obtained in analogLib library.
- Add the necessary input and output pins at the input and output side as shown in the diagram.
- After successful save and check option create its symbol view.
- Create-> Cellview -> from CellView and press ok.

8.After Successful creating symbol, now use that symbol and create the schematic as shown below. After successful save and check we can now proceed to simulation.

9.Within the schematic pulse is used in both inputs which can be set up as follows:

- Select pulse component and press ‘q’
- Give following values
- V1:0 for every A,B,A-,B-
- V2:1.8 for every A,B,A-,B-.
- Period:10n , 20n , 10n, 20n seconds for A,B,A-,B- respectively.
- Rise and fall time as 1n seconds each.
- Dealy time as 0 ,0,10n,20n seconds for A,B,A-,B- respectively.

9.Check for errors using key ‘x’ and save and check the file for errors.

10.Lauch and set ADEL

11. Setup the model libraries and choose the analysis type as follows->

Analysis-> transient -> Stop time=200n -> Moderate -> ok

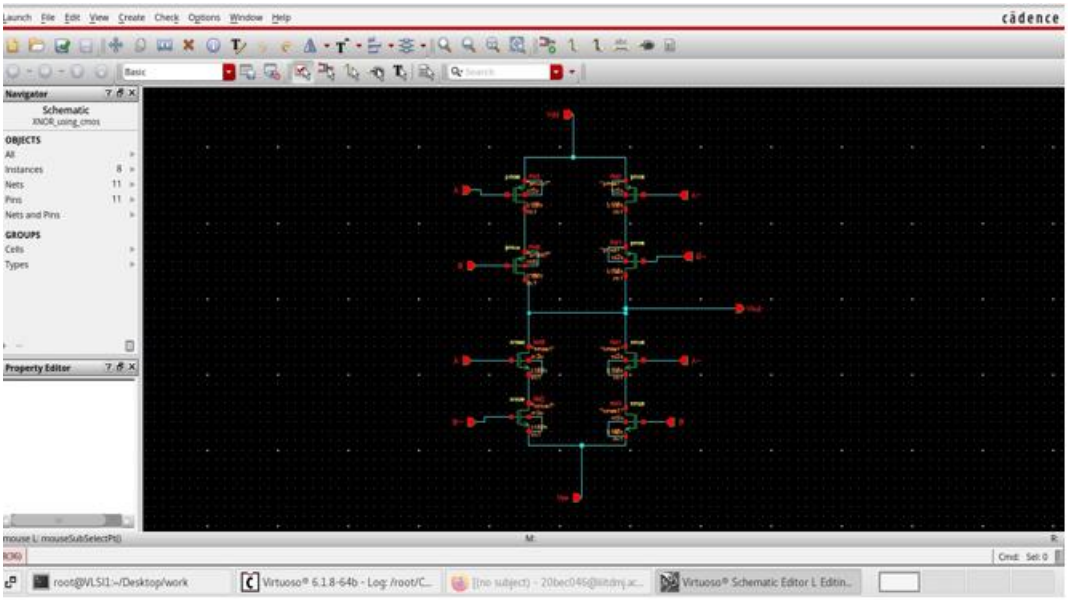
12.Click on output menu and select vout pin and both inputs pins as output and click

ok 13.Run the stimulation

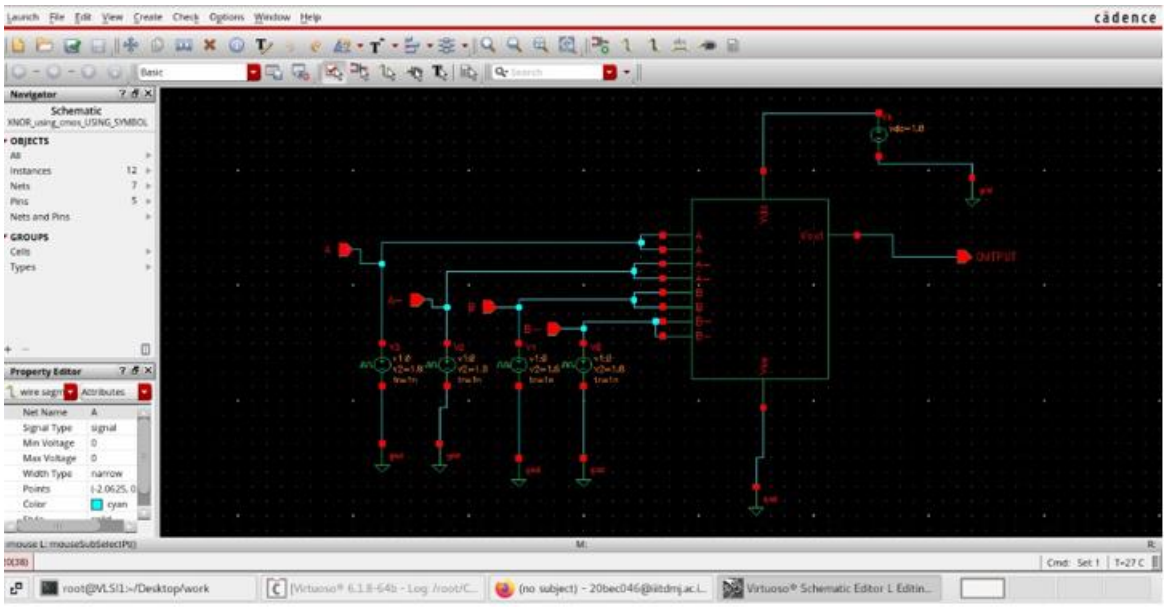
14. Result is obtained in plot

XNOR Gate

The same procedure needs to be followed using the below schematic for the XOR gate.

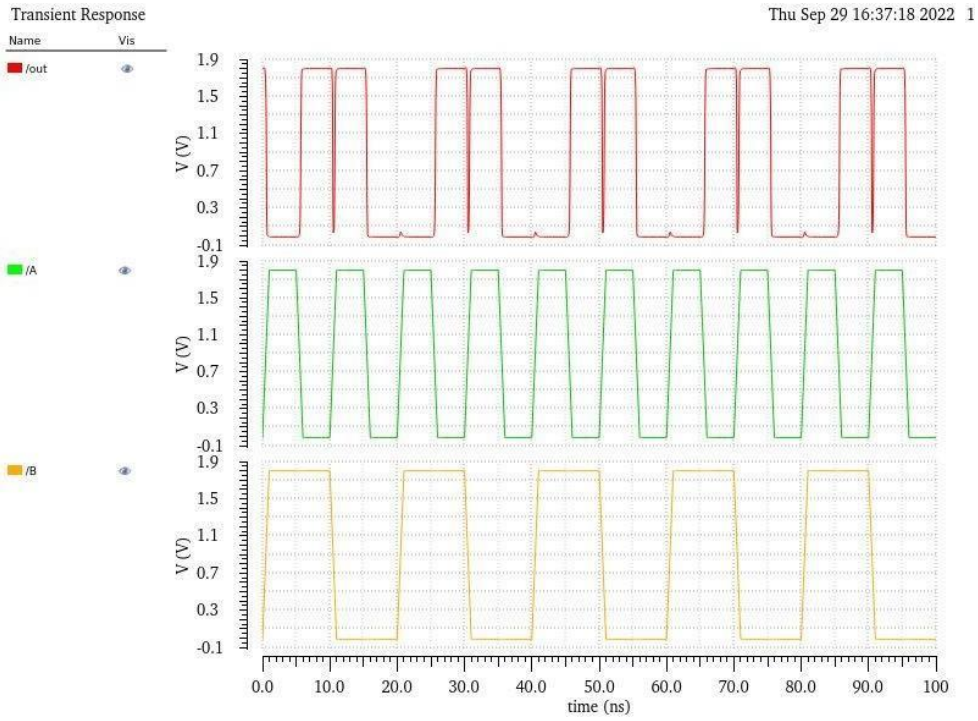


Symbol View for XOR

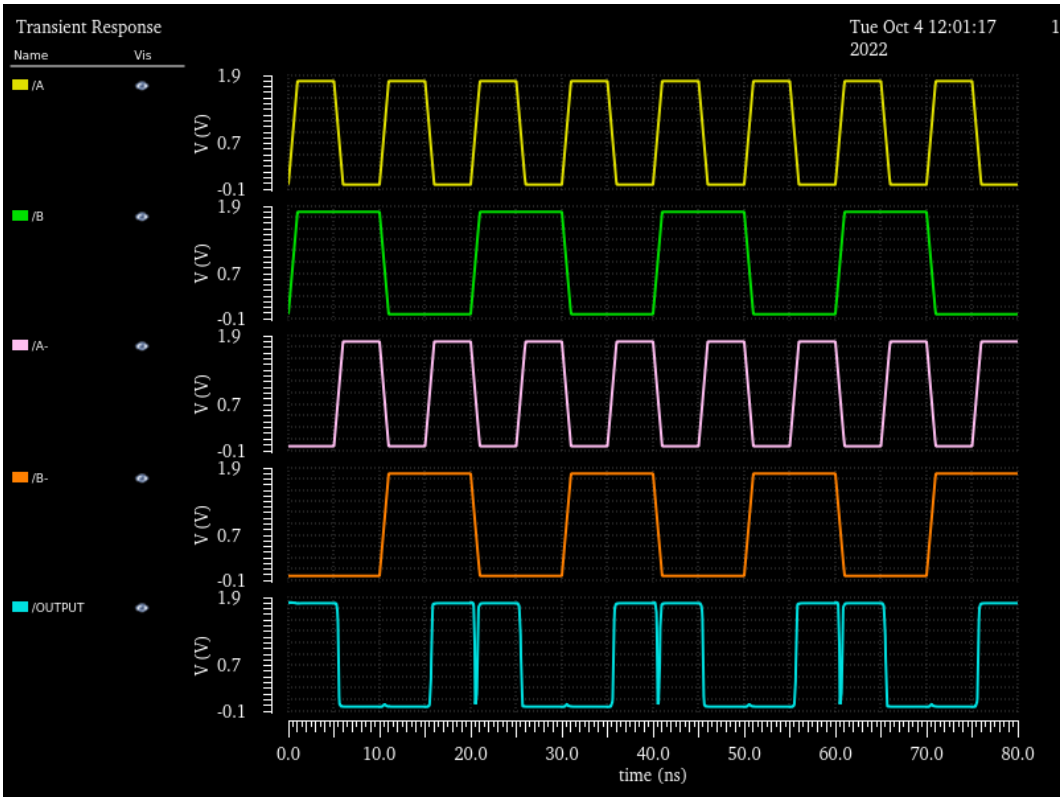


Results:

1. Transient response can be seen from the figure. The XOR(AB'+A'B) output shows 1 when both inputs are opposite(01,10), else the output is always 0.



2. Transient response can be seen from the figure. The XOR((AB)'+ AB) output shows 1 when both inputs are 1or 0, else the output is always 0.



Experiment 6: Design 4X1 MUX using COMS technology.

Procedure:

1. Go to work

2. Open terminal there

3. type commands:

    * csh

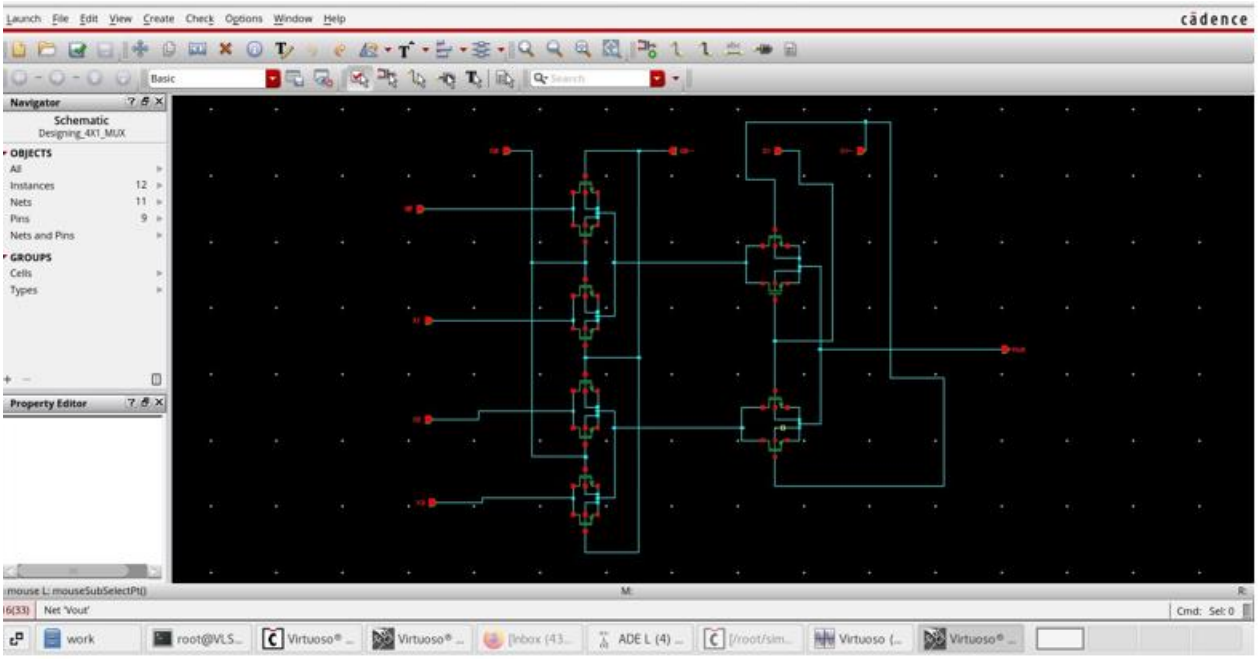
    * Source cshrc_new12 or cshrc_new1 or cshrc_new based on the cshrc file present in the work folder

    * virtuoso

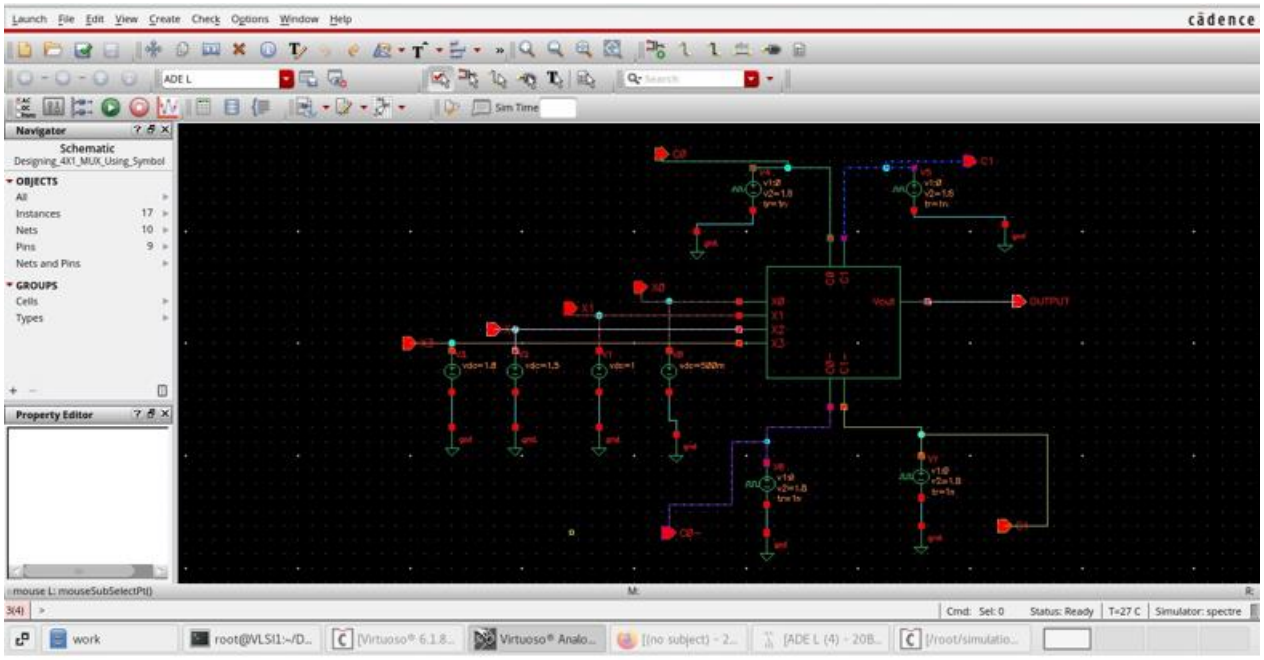
4. After Virtuoso is launched , select file -> new -> create new library -> type name(your name for example) and select “Attach to an existing technology library” option and press ok.

5. Now again Select File->New->cellview->select the library name which you created above(with your name)->give it a name(Resistive Load inverter)->click ok.

6. Create **4X1 MUX Diagram** as shown

7. 

Using Symbol View



- Click instance (or press I) -> select library(gpdk180 for nmos and pmos, analog lib for normal circuit components like battery, resistance etc) -> choose the required component ->close->hide -> paste the component.
- The components can be joined using wires , wires are selected by clicking wires icon  or pressing shortcut ‘w’ , wires are drawn by pressing and holding the mouse button
- Nmos and pmos can be acquired from gpdk_new library and voltage ,pulse ground and resistance can be obtained in analogLib library.
- Add the necessary input and output pins at the input and output side as shown in the diagram.
- After successful save and check option create its symbol view.
- Create-> Cellview -> from CellView and press ok.

8.After Successful creating symbol, now use that symbol and create the schematic as shown below. After successful save and check we can now proceed to simulation.

9.Within the schematic pulse is used in inputs which can be set up as follows:

- Select pulse component and press ‘q’

- Give following values
- V1:0 for every C0,C1
- V2:1.8 for every C0,C1
- Period:20n ,40n , 20n, 40n seconds for C0,C1,C0-,C1- respectively.
- Rise and fall time as 1n seconds each.
- Dealy time as 0 ,0,20n,40n seconds for C0,C1,C0-,C1- respectively.
- X0,X1,X2,X3 as constant dc voltages of 0.5V,1V,1.4V,1.8V respectively.

9.Check for errors using key ‘x’ and save and check the file for errors.

10. Lauch and set ADEL

11. Setup the model libraries and choose the analysis type as follows->

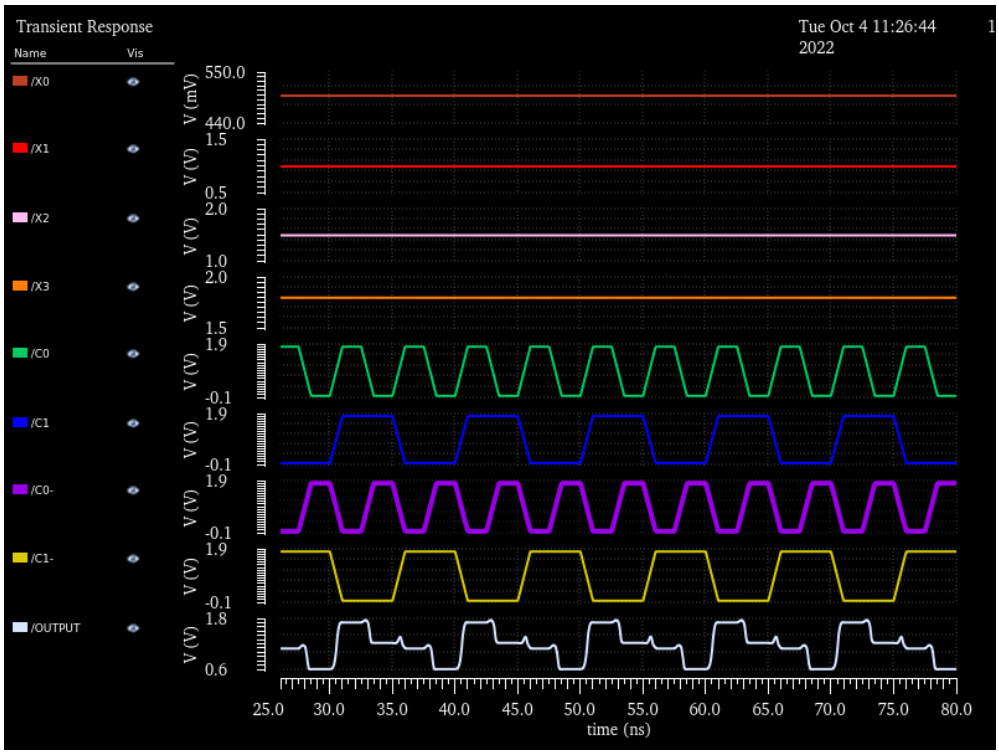
Analysis-> transient -> Stop time=200n -> Moderate -> ok

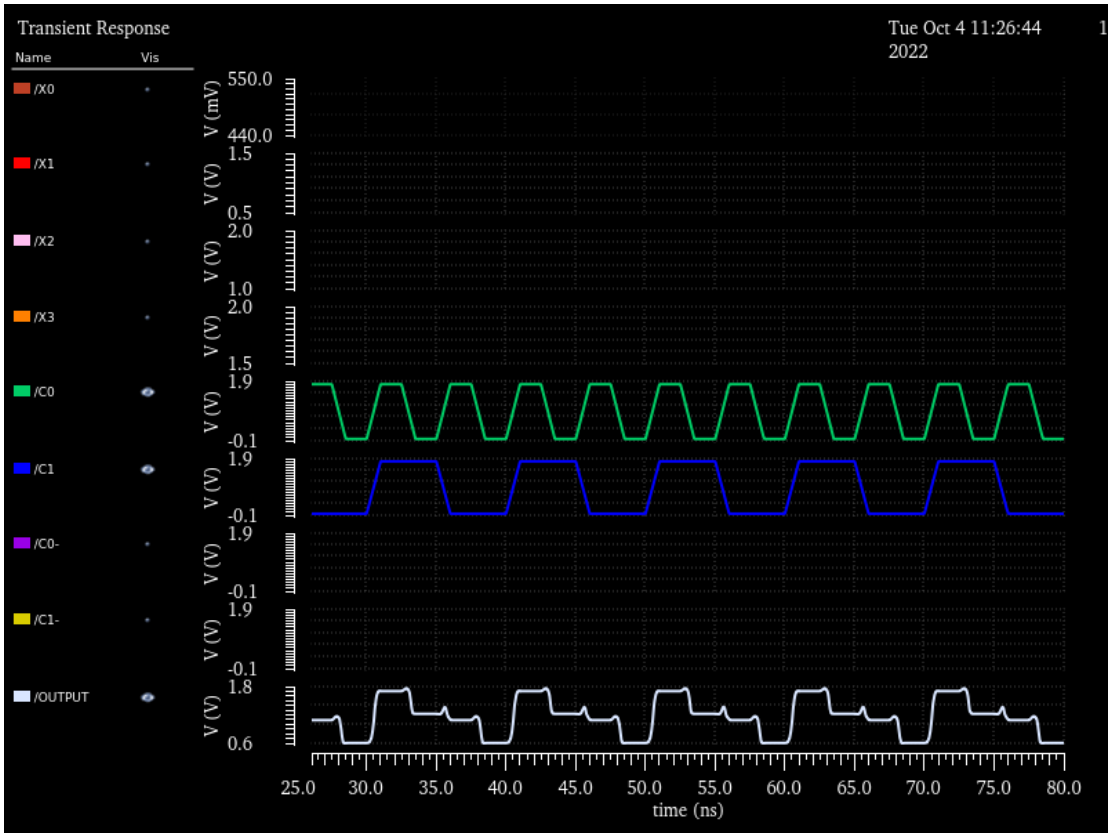
12. Click on output menu and select vout pin and all inputs pins as output and click

ok 13.Run the stimulation

Result:

1. Based on different combinations of C0 and C1 we can see that different inputs(X0,X1,X2,X3) are observed at the output side.




Transient Response
Tue Oct 4 11:26:44 2022
Name
Vis
/X0
/X1
/X2
/X3
/C0
/C1
/C0-
/C1-
/OUTPUT
V (mV)
550.0
440.0
V (V)
1.5
0.5
2.0
1.0
2.0
1.5
1.9
-0.1
1.9
-0.1
1.9
-0.1
1.9
-0.1
1.8
0.6
25.0
30.0
35.0
40.0
45.0
50.0
55.0
60.0
65.0
70.0
75.0
80.0
time (ns)

PDPM
INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, DESIGN & MANUFACTURING.

Experiment 7: Design a logic function f=A'B+CD+(ABC)'

Procedure:

1. Go to work

2. Open terminal there

3. type commands:

   * csh

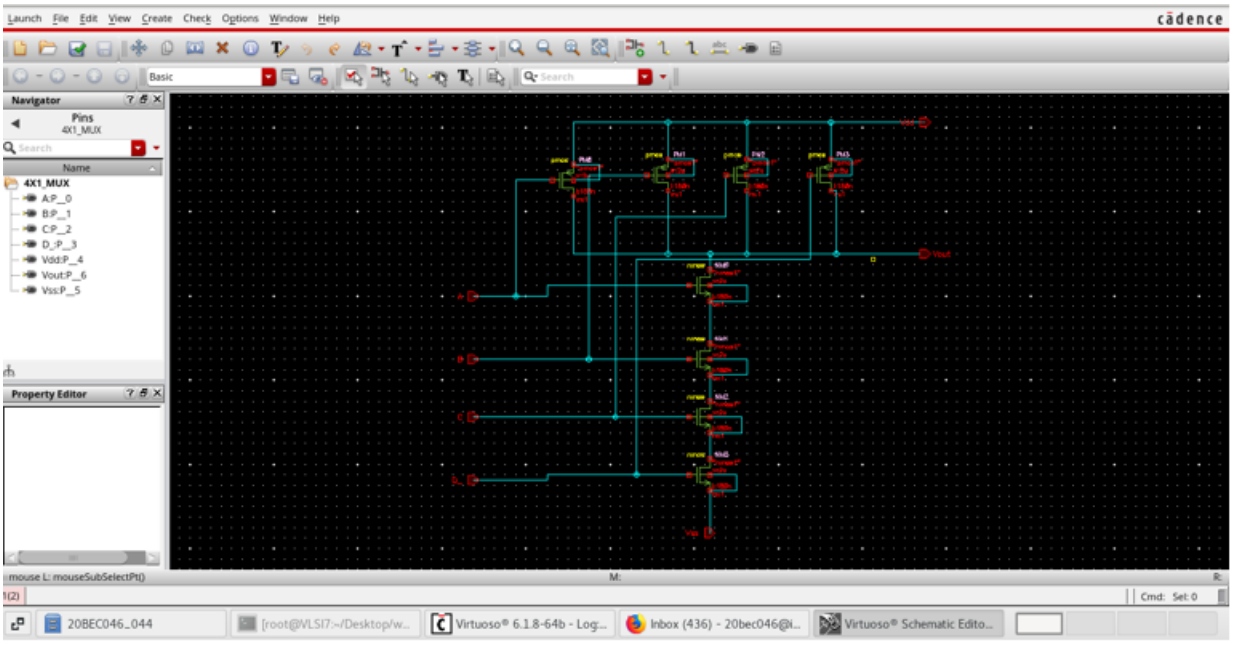
   * Source cshrc_new12 or cshrc_new1 or cshrc_new based on the cshrc file present in the work folder

   * virtuoso

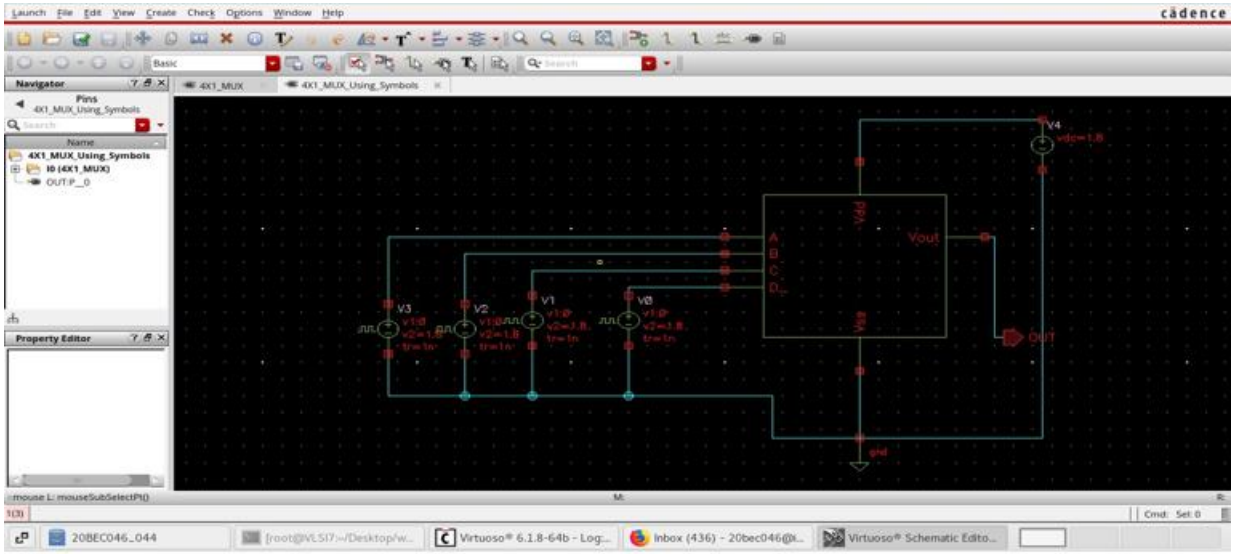
4. After Virtuoso is launched , select file -> new -> create new library -> type name(your name for example) and select "Attach to an existing technology library" option and press ok.

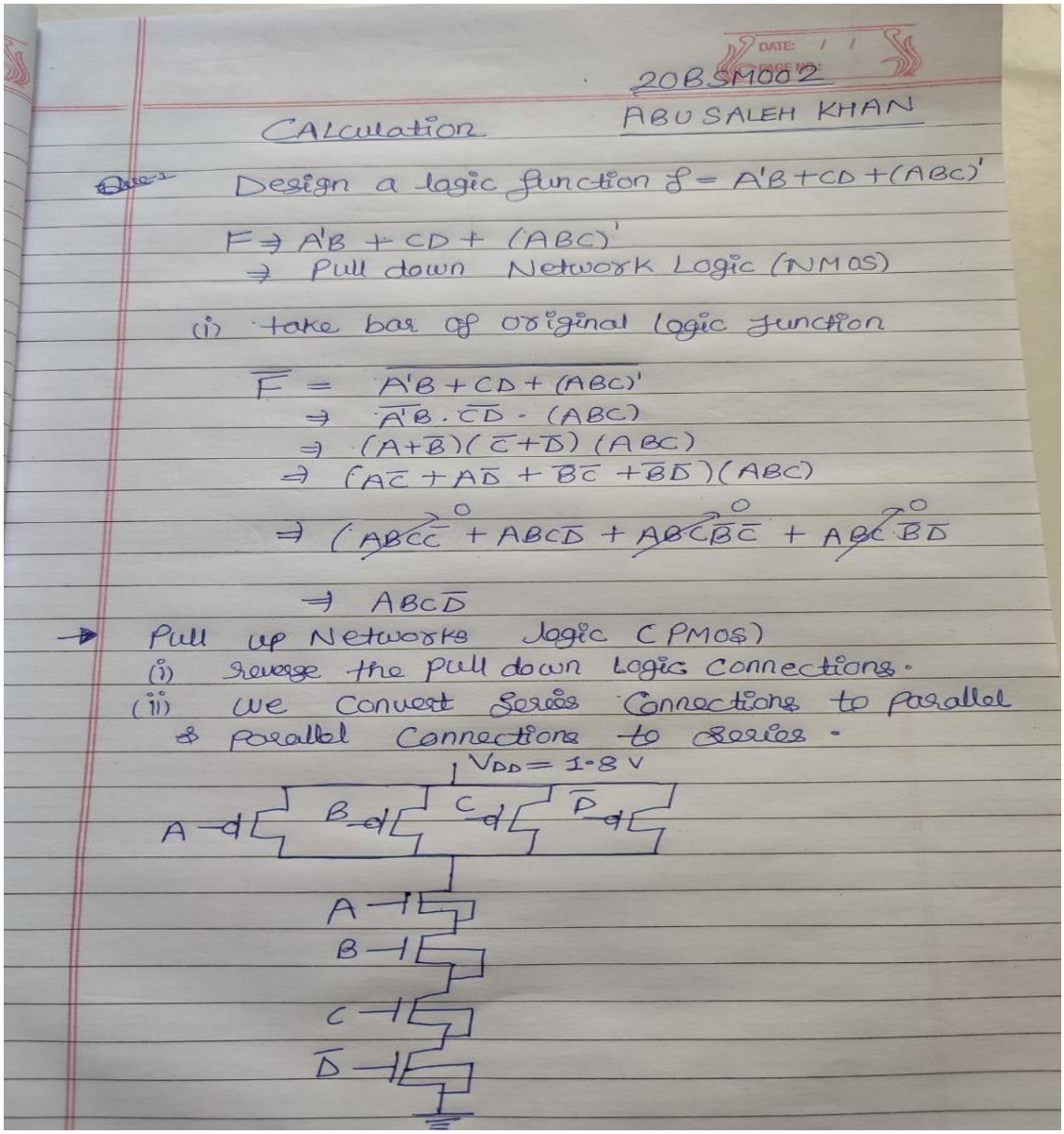
5. Now again Select File->New->cellview->select the library name which you created above(with your name)->give it a name(Resistive Load inverter)->click ok.

6. Create the **Project function schematic** as shown

7. 

Using Symbol View





- Click instance  (or press I) -> select library(gpdk180 for nmos and pmos, analog lib for normal circuit components like battery, resistance etc) -> choose the required component ->close->hide -> paste the component.
- The components can be joined using wires , wires are selected by clicking wires icon  or pressing shortcut ‘w’ , wires are drawn by pressing and holding the mouse button
- Nmos and pmos can be acquired from gpdk_new library and voltage ,pulse ground and resistance can be obtained in analogLib library.
- Add the necessary input and output pins at the input and output side as shown in the diagram.
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8.After Successful creating symbol, now use that symbol and create the schematic as shown below. After successful save and check we can now proceed to simulation.

9.Within the schematic pulse is used in inputs which can be set up as follows:

- Select pulse component and press ‘q’
- Give following values
- V1:0 for every A,B,C,D
- V2:1.8 for every A,B,C,D
- Period:5n ,10n , 20n, 40n seconds for A,B,C,D respectively.
- Rise and fall time as 1n seconds each.
- Dealy time as 0 seconds for all A,B,C,D respectively..

9.Check for errors using key ‘x’ and save and check the file for errors.

10.Lauch and set ADEL

11. Setup the model libraries and choose the analysis type as follows->

Analysis-> transient -> Stop time=200n -> Moderate -> ok

12.Click on output menu and select vout pin and all inputs pins as output and click

ok 13.Run the stimulation

14. Result is obtained in plot

Result:

1. Transient response can be easily seen for the function F= A'B+CD+(ABC)'

2. Output Table:

	A	B	C	D	OUT
i.	0	0	0	0	1
ii.	0	0	0	1	1
iii.	0	0	1	0	1
iv.	0	0	1	1	1
v.	0	1	0	0	1
vi.	0	1	0	1	1
vii.	0	1	1	0	1
viii.	0	1	1	1	1
ix.	1	0	0	0	1
x.	1	0	0	1	1
xi.	1	0	1	0	1
xii.	1	0	1	1	1
xiii.	1	1	0	0	1
xiv.	1	1	0	1	1
xv.	1	1	1	0	0
xvi.	1	1	1	1	1