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INDIAN INSTITUTE OF INFORMATION TECHNOLOGY,
DESIGN AND MANUFACTURING, JABALPUR (MP)

IT3E01: IT Workshop (Sentaurus)

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EXPERIMENT : Design, simulate and Analyze Silicon on Insulator (SOI) FinFet using Sentaurus TCAD Software.

THEORY:

Sentaurus TCAD (Technology Computer-Aided Design) is a software suite developed by Synopsys for simulating and analyzing semiconductor devices and processes. It is a simulation software for semiconductor design based on fundamental principles of physics, offering advanced capabilities for coupled multiphysics simulations and user-friendly visualization tools.

FinFET:

1) It stands as a Fin Field effect transistor.
2) Traditionally used transistors like MOSFET have a planar structure where the gate is on top of the channel and controls the current flow from a single direction.
3) FinFET has a three-dimensional silicon channel or the fin with the gate wrapped around it. In such a structure the gate channel interface is large and the gate controls the current flow from three directions hence improving the overall control.
4) The FinFET with gate on three sides of the channel is also called trigate or triple-gate SOI FinFET. SOI stands for Silicon on oxide where the fin is built on an oxide layer that is deposited on the substrate to provide insulation and reduce leakage current.

Difference Between Finfet and mosfet:

MOSFET	FinFET
It is metal oxide semiconductor field effect transistor that is a planar device	It is a fin field effect transistor and the fin is a three dimensional structure.
As there is no insulation between gate and substrate leakage current is present.	The gate is insulated from the substrate using oxide resulting in reduced leakage current.
The gate controls the channel only from the top.	The channel is controlled by gates from multiple directions due to the 3d fin.
Short channel effects are significant in smaller mosfet	Due the presence of fin and better gate control the short channel behavior is better even in smaller finfets.
Voltage gain is lower.	Finfets offer higher voltage gain when compared to mosfets.
The power consumption is higher.	The power consumption is low as compared to mosfet.
It is simple to Fabricate if compared to FinFET	It is very complex to fabricate as design have many complications

Given Structure Dimensions and Doping

Dimensions				
Region	**Material**	**Thickness (nm)**	**Height (nm)**	**Length (nm)**
Substrate	Silicon	20	15	66
SOI Box	SiO2	20	8	66
Fin	Silicon	8	42	36
Channel / Gate	Silicon	20	48	20
Metal Thickness	TiN	2	NA	NA

Doping			
Region	**Type**	**Material**	**Concentration (per cm3)**
Substrate	P-type	Boron	1.00E+15
Source	N-type	Arsenic	2.00E+20
Drain	N-type	Arsenic	2.00E+20
Extension Region	N-type	Arsenic	2.00E+18
Channel / Gate	P-type	Boron	2.00E+16

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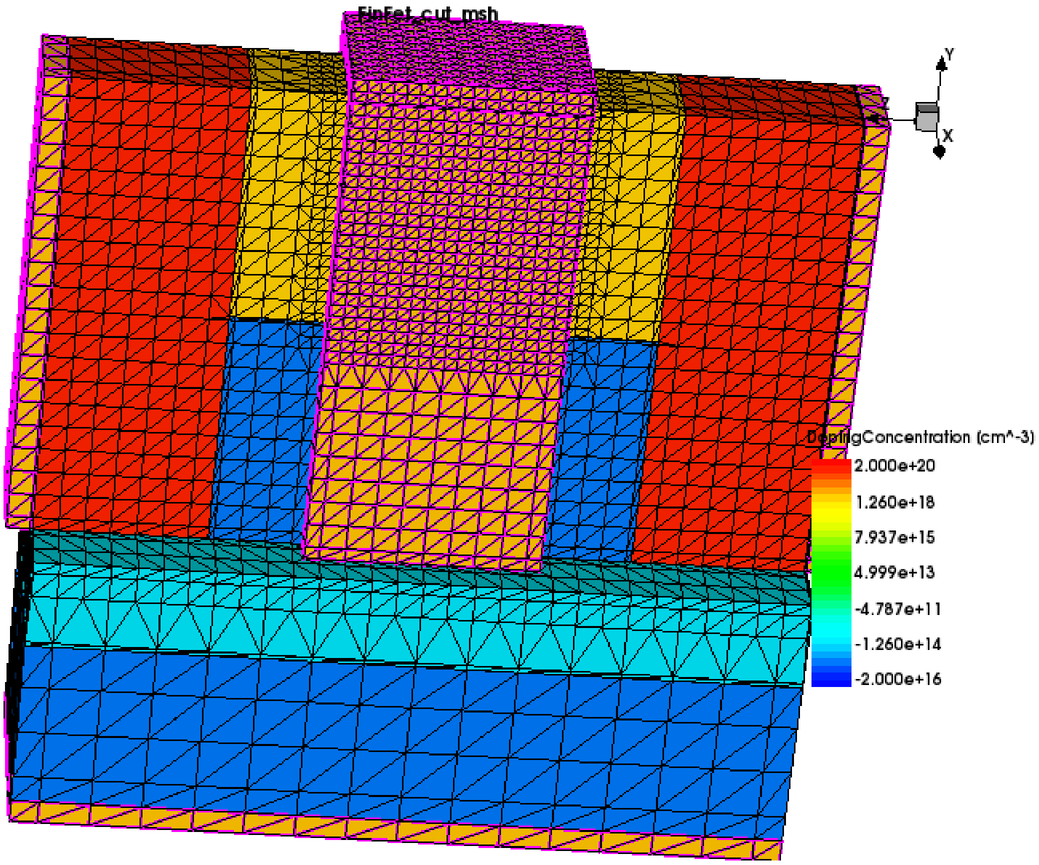
STRUCTURE AND DOPING PROFILE:



INPUT PARAMETERS-

Vg: Voltage applied at the gate terminal
Vd: Voltage applied at the drain terminal
Drain Resistance(R): Resistance offered by the drain.
Work function(Φ): the minimum quantity of energy which is required to remove an electron to infinity from the surface of a given solid, usually a metal.

PARAMETERS TO BE CALCULATED -

ON current (ID on): It is the current flowing through the FinFET when the value of Vg and Vd is high (0.7V).

OFF Current (ID off): It is the current flowing through the FinFET when the value of Vg is 1e^(-7) that is low and the value of Vd is high(0.7V).

Threshold Voltage (Vth): It is the minimum gate voltage required for the current to start flowing through the FinFET.

ON OFF Ratio: The ratio between on current and off current.

Subthreshold slope:

It is the slope of the Id vs Vg graph for the values of Vg below the threshold voltage Vth and the y-axis is taken as log(Id). It gives the initial rise in the current where ideally the current should have been zero.
It can be calculated using following steps,
Plot the IdVg graph using svisual
Get the value of Vg1 at Id1=1e^(-7)A
Get the value of Vg2 at Id2=1e^(-8)A
Get the value of Vg3 at Id3=1e^(-9)A
Slope is given by formula: **S=(y2-y1)/(x2-x1)**
S=(Id3-Id1)/(Vg3-Vg1)
Where S obtained is the sub-threshold slope

DIBL Factor: DIBL stands for drain induced barrier lowering. It is the phenomenon due to which the threshold voltage decreases due to the high voltage provided at the drain terminal.
Its factor can be calculated as follows ,
Get value of Vth for Vd=0.7 and Vg=0.7 called as saturation threshold voltage(Vtsat)
Get the value of Vth for lower value of Vd let Vd=0.05 and Vg=0.7 called as linear threshold voltage (Vtlin) which will be higher than Vtsat as the value of Vd has been reduced.
The dibble factor is calculated as
N=del (Vth)/del (Vd)

N=(Vtlin-Vtsat)/ (0.7-0.05)
N=(Vtlin-Vtsat)/0.65
NDR effect: Negative Differential resistance occurs when the drain current drops with a negative slope with increase in Vd voltage.

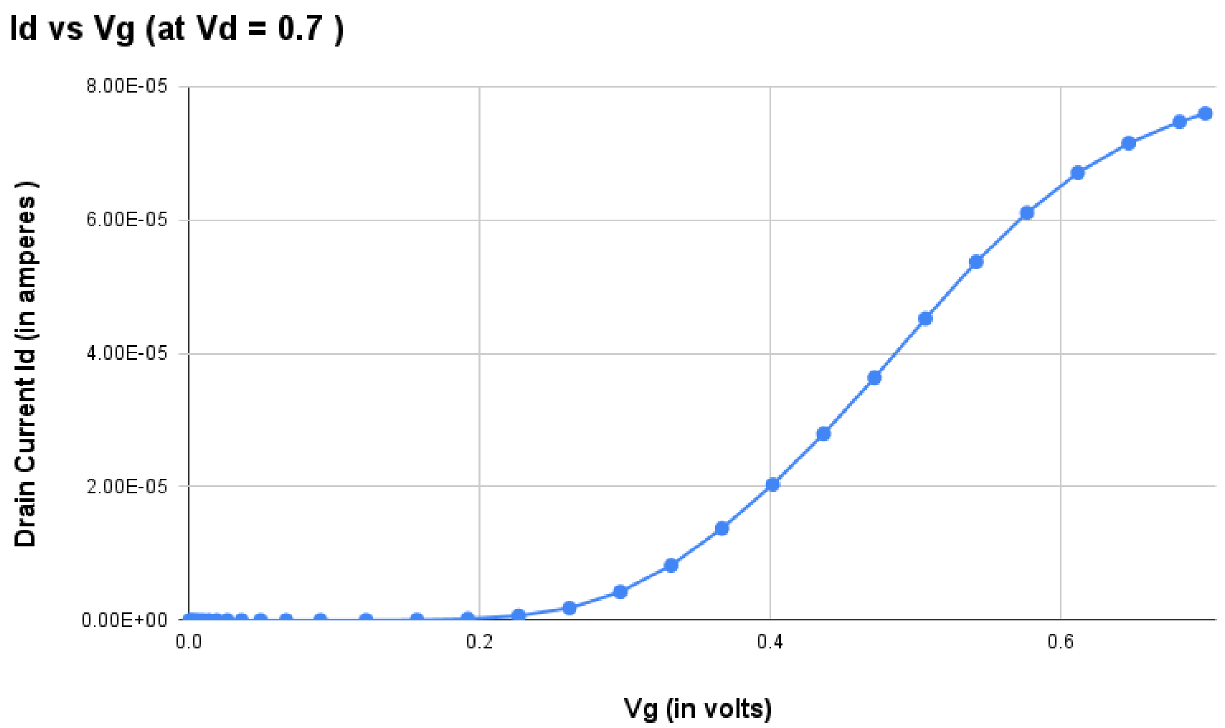
CALCULATION OF Id:

1) It is obtained by sweeping Vd form 0 to 0.7 and Vg form 0 to 0.7 at constant Vd

Following are the recorded Values of ID-on and ID-off varying with work function and resistance

The value of ID on and ID off can be varied by changing the work function and resistance
According to the recorded variations the value of "ID on" is mostly dependent on Value of Resistance and it is inversely proportional
The value of "ID off" varies mostly due to work function and increases with the decrease in the work function.

RESULT AND DISCUSSION :
ID-Vg Graph
For Vd=0.7V:



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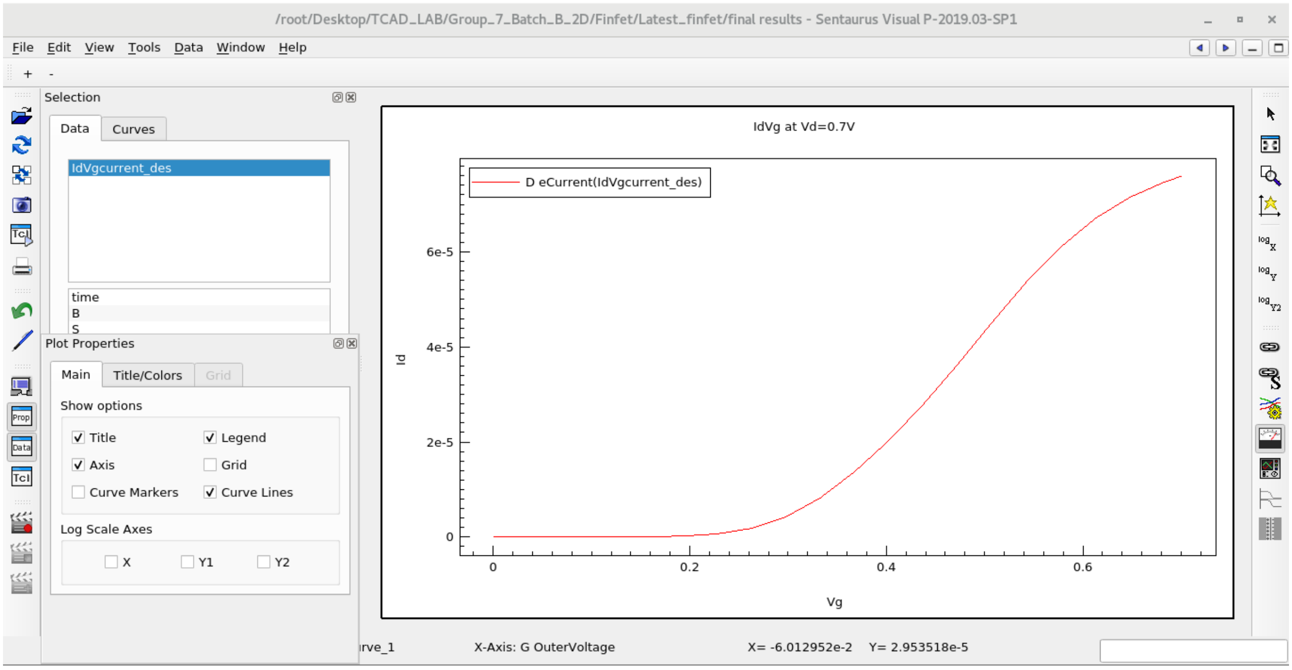
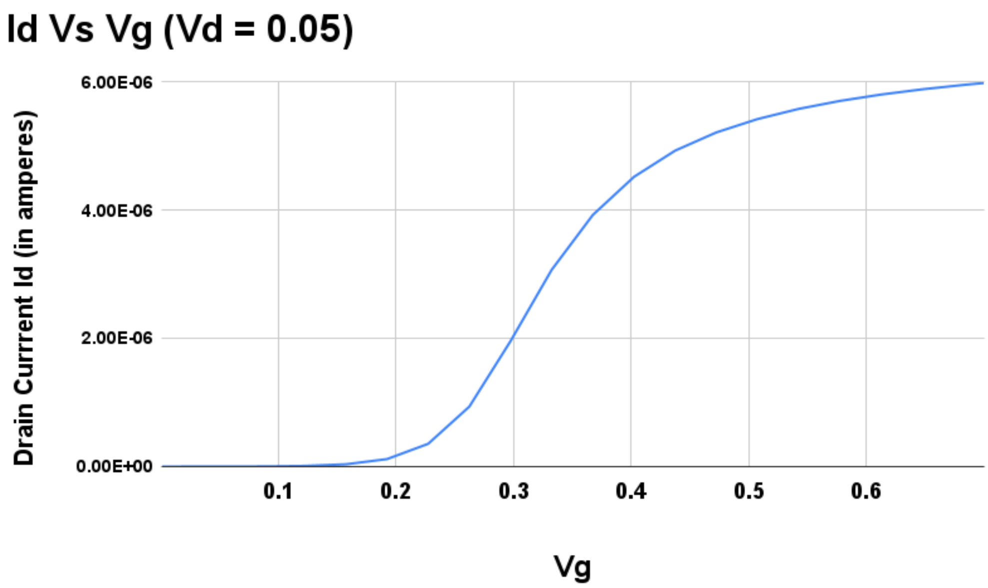
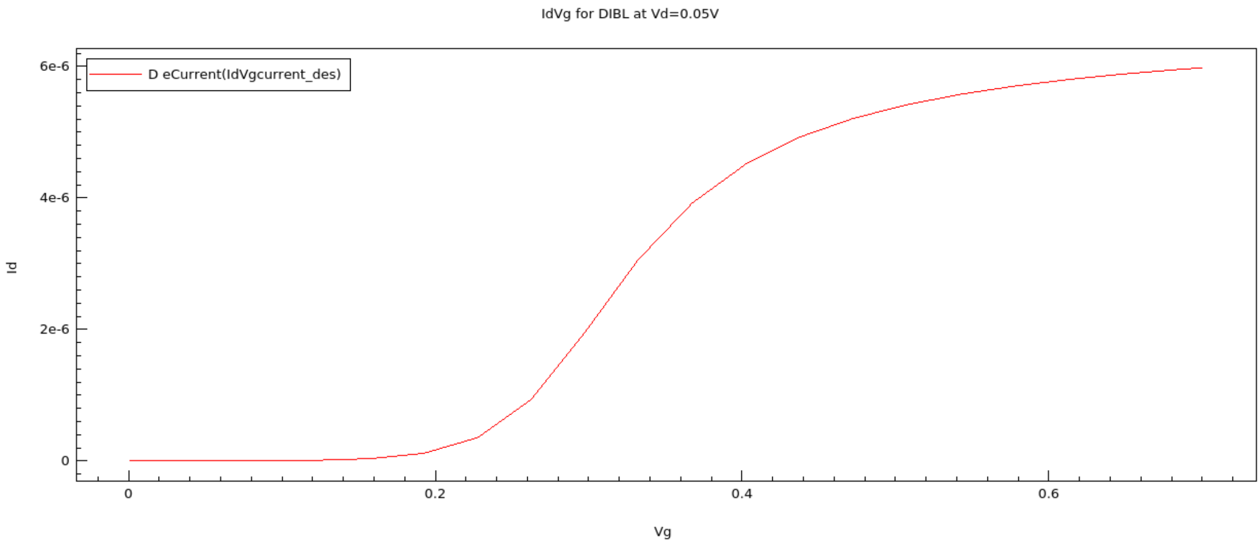
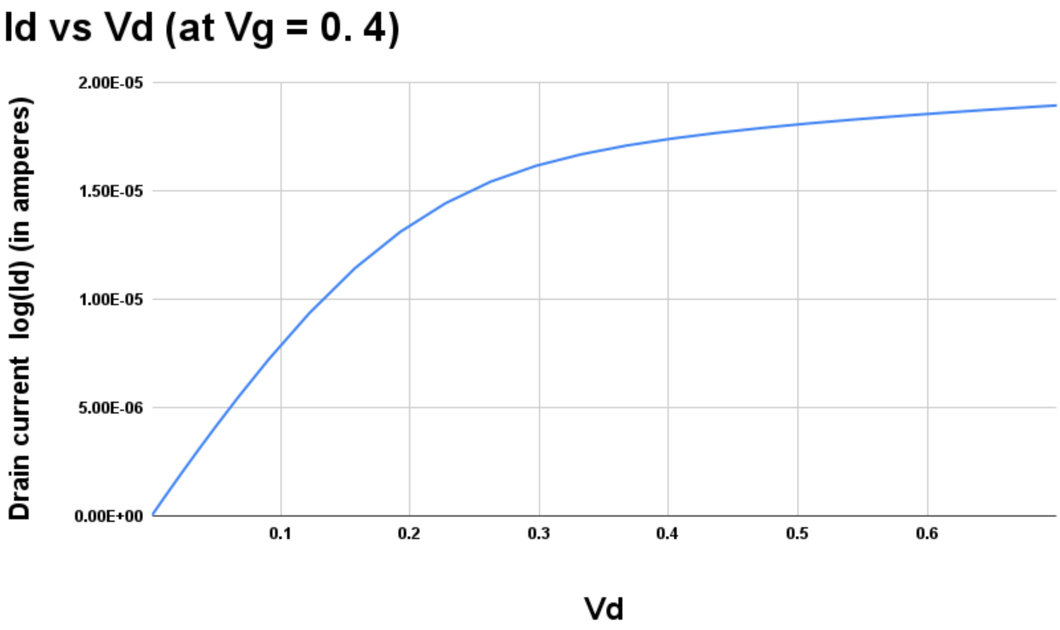


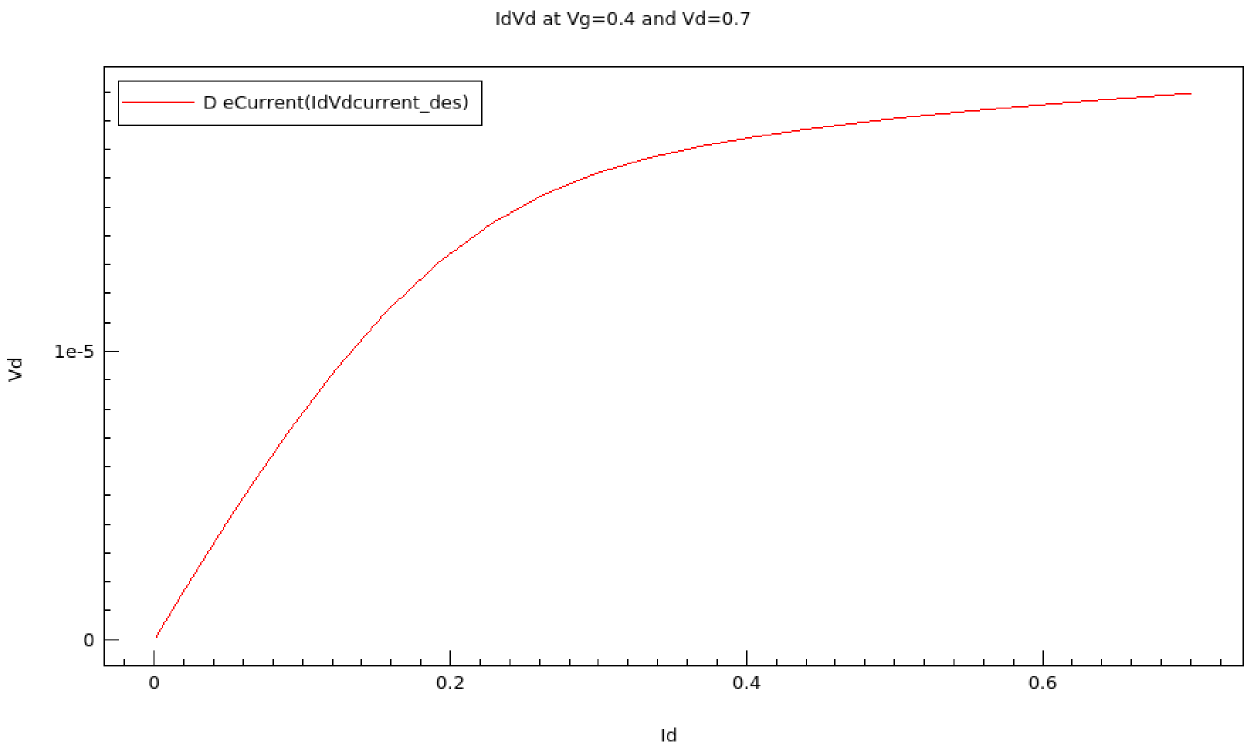
For Vd=0.05V


Id Vs Vg (Vd = 0.05)
Drain Currrent Id (in amperes)
6.00E-06
4.00E-06
2.00E-06
0.00E+00
0.1
0.2
0.3
0.4
0.5
0.6
Vg


IdVg for DIBL at Vd=0.05V
D eCurrent(IdVgcurrent_des)
6e-6
4e-6
2e-6
0
Id
0
0.2
0.4
0.6
Vg

ID-Vd Graph:





RESULT AFTER SIMULATION:

ID-off = 251.58 x 10^(-12)A
ID-on = 75.934 x 10^(-6)A = 75.9 uA
ID-on/ID-off Ratio = 3.0182 x 10^(5)
Threshold Voltage (Vt) = 0.1648 V
Resistance Used = 4600 ohm
Work Function = 4.4095 V
DIBL factor: 0.031076
Vg at ID 1e-8= 99.28mV
Vg at ID 1e-9=38.609mV

Calculation Of ID:

ID on is calculated at Vg=0.7 V and Id off is calculated at Vg=0.001 or 1e-3 V.

Calculation of Threshold voltage (Vt):

It is calculated by plotting the Id-Vg graph and obtaining the value of Vg when ID is 1e^(-7)
Vth= 0.1648

Calculation of subthreshold slope:

The Required values obtained are as follows

For ID=1e^ (-7)
    Vg=0.1648V
For ID=1e^ (-8)
    Vg=0.09928V
For ID=1e^ (-9)
    Vg=0.038609V

Slope is calculated as:
S=(1e^(-7)-1e^(-9))/(0.1648-0.038609)
=0.006218235(A/V)

CALCULATION OF DIBL FACTOR:

The Required values obtained are as follows:
For Vg from 0 to 0.7 and Vd from 0 to 0.05

Vt=0.185V

For Vg from 0 to 0.7 and Vd from 0 to 0.7

Vtsat=0.1648V

It is observed that by increasing the Drain voltage value there is a decrease in the threshold observed hence DIBL effect is verified.

DIBL Factor is calculated as:

N=(Vtlin-Vtsat)/(0.7-0.05)

N=(0.185-0.1648)/(0.65)

N=0.031076

NDR effect:

The given structure has no NDR effect associated with it as shown from Id Vd graph shown above.

Comparison Table: Comparison between Predicted and Actual Value

Parameter	Predicted Value	Actual Value	Deviation
Idon	7.60E-05	7.59E-05	0.01E-05
Idoff	2.50E-10	2.51E-10	-0.01E-10
Vth	2.00E-01	1.65E-01	-0.35E-01
Idon/Idoff	3.04E+05	3.02E+05	0.04E+05

OTHER SIMULATED VALUES

S.NO	Work function	Resistance (ohm)	Ion(uA)	Ioff(pA)	Vth (volt)
1.	4.40893	4700	75.29	256.85	0.1643
2.	4.41	4600	75.29	247.05	0.165
3.	4.4099	4600	75.9	247.95	0.165129
4.	4.408	5000	73.34	265.67	0.163