# YMG8K16F18L5BR1

8Kx16 bits Embedded MTP

## Common Specification

### Whole Macro

| | | |
|---|---|---|
| **Process** | | 0.18um 3.3V/(5V)6Vdual-gate MCU Technology Process |
| **Read Current @ 5.0V** | **16 MHz** | $I_{DR}$ ≈ 6.5 mA (typ.) [High speed mode] |
| | **4 MHz** | $I_{DR}$ ≈ 3.5 mA (typ.) [High speed mode] |
| | **2 MHz** | $I_{DR}$ ≈ 1.3 mA (typ.) [Low power mode] |
| | **1 MHz** | $I_{DR}$ ≈ 0.8 mA (typ.) [Low power mode] |
| | **500 KHz** | $I_{DR}$ ≈ 0.5 mA (typ.) [Power saving mode] |
| | **32 KHz** | $I_{DR}$ ≈ 30 uA (typ.) [Power saving mode] |
| **Write Current** | | $I_{DW}$ ≈ 30 mA (typ.) |
| **Standby Current** | | $I_{SB}$ ≈ 1 uA (typ.) |
| **Operating Temperature** | | Tj = -40°C to 85°C |
| **IP layout (Non-Isolated)** | | 1P3M (Metal 3 layer follow the top metal thickness: 11 KÅ) |
| **Device Information** | | nmos_5p0, pmos_5p0, ppolyf_u, VPNP_10X10 |

Note: The IP requires an extra mask for cell implant.

### MTP and Information blocks

| | | |
|---|---|---|
| **Read Voltage** | | VDD : 1.8V~5.5V |
| **Read Cycle Time** | **High speed** | 60 ns (min.) @ 4.5V≤VDD≤5.5V<br>300 ns (min.) @ 1.8V≤VDD<4.5V |
| | **Low power** | 500 ns (min.) @ 4.5V≤VDD≤5.5V<br>1 us (min.) @ 1.8V≤VDD<4.5V |
| | **Power saving** | 2 us (min.) @ 1.8V≤VDD≤5.5V |
| **Write Voltage** | | VDD : 4.5V~5.5V |
| **Write Time** | | 16-bit Write Time (changed code) : 0.3 ms (typ.) |
| | | 16-bit Write Time (non-changed code) : 20 us (min.) |
| **Data Retention** | | 10 Years under 85°C (Pre-condition: VDD=5.0V/1,000T Cycles) |
| **Endurance** | **MTP block** | 1,000 Cycles (16-bit Write) |
| | **Information block** | 1,000 Cycles (16-bit Write) |

EEPROM block

| | | |
|---|---|---|
| **Read Voltage** | | VDD : 1.8V~5.5V |
| **Read Cycle Time** | **High speed** | 300 ns (min.) @ 1.8V≤VDD≤5.5V |
| | **Power saving** | 2 us (min.) @ 1.8V≤VDD≤5.5V |
| **Write Voltage** | | VDD : 2.6V~5.5V |
| **Write Time** | | Byte Write Time (changed code) : 0.7 ms (typ.) |
| | | Byte Write Time (non-changed code) : 80 us (min.) |
| **Data Retention** | | 10 Years under 85°C (Pre-condition: VDD=5.0V/10,000T Cycles) |
| **Endurance (Byte Write)** | | 10,000 Cycles |

## Features

- Memory Organization :
  - MTP block: 8K x 16 bits
  - Information block: 32 x 16 bits
  - EEPROM block: 128 x 8 bits
- I/O Configuration :
  - MTP block: x16 separate DIN [15:0] / DOUT [15:0] Bus
  - Information block: x16 separate DIN [15:0] / DOUT [15:0] Bus
  - EEPROM block: x8 separate DIN [7:0] / DOUT [7:0] Bus
- Read / Write Operation
  - MTP block: 16-bit Read / 16-bit Write Operation
  - Information block: 16-bit Read / 16-bit Write Operation
  - EEPROM block: Byte Read / Byte Write Operation
- Write time is not a fixed value
- BUSY signal provides a hardware method of detecting write operation completion
- Built-in charge pump

## General Description

YMG8K16F18L5BR1 is an embedded MTP IP macro fabricated in the 0.18um 3.3V/(5V)6Vdual-gate MCU Technology Process. The memory arrays are partitioned into three memory blocks each. One is the MTP block (8K x 16 bits); one is the Information block (32 x 16 bits); the other is the EEPROM block (128 x 8 bits). The YMG8K16F18L5BR1 supports two operating modes: User mode and Test mode. User mode provides five memory operations: standby (STANDBY) / static (STATIC) / non-static (NON-STATIC) / read (READ) / write with internal high voltage (INTHV WRITE). Test mode provides three memory operations: measure memory cell current (CLEN) / read for data retention test (MRGN READ) / write with internal high voltage for data retention test (MRGN INTHV WRITE).

## Pin Description[1]

| Pin Name | Direction | Signal Level | Description |
|---|---|---|---|
| ADR[12:0] | I | VDD | Address input pin. |
| DIN[15:0] | I | VDD | Data input pin. |
| DOUT[15:0] | O | VDD | Data output pin. |
| CS | I | VDD | IP macro selective input, active HIGH. |
| READ | I | VDD | Read operation enable input, active HIGH. |
| WR | I | VDD | Write operation enable input, active HIGH. |
| CLEN | I | VDD | Define test mode of cell current measurement. |
| IFREN | I | VDD | IFREN = “H” to select the Information block. |
| EEPROM | I | VDD | EEPROM = “H” to select the EEPROM block. |
| SRL[2] | I | VDD | Select default or shadow cell in MRGN READ / CLEN operation. |
| MRGN | I | VDD | MRGN = “H” to select MRGN READ / MRGN INTHV WRITE operation for data retention test when select the EEPROM block. |
| CLKIN | I | VDD | Define User-Supplied clock cycle under 12.5us (typ.).<br>CLKIN must be stable before asserting WR. |
| ISAVB | I | VDD | Option setting for Read operation :<br>ISAVB = “H” to select the high speed mode.<br>ISAVB = “L” to select the low power or power saving mode. |
| STATICEN | I | VDD | STATICEN = “H”, STATIC mode ($I_{DS}$ <500uA).<br>STATICEN = “L”, NON-STATIC mode ($I_{NDS}$ <10uA). |
| BUSY | O | VDD | Flag indicating that write operation is complete or not. |
| VDD | I | - | Power supply |
| VSS | I | - | Ground |

Notes:

1. We suggest multiplexing all control, address and data signals to package pins to facilitate direct memory test.
2. There are two memory cells per bit, one is default memory cell, and the other is shadow memory cell.

## Recommended DC Operating Conditions (Tj = specified, Cload=1pF)

### Whole Macro

| Operation Mode | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply | $VDD_{min}$ | 1.8 | - | - | V |
| Ground | VSS | 0 | 0 | 0 | V |

### MTP and Information blocks

| Operation Mode | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| READ | VDD | 1.8 | 5.0 | 5.5 | V |
| INTHV WRITE | VDD | 4.5 | 5.0 | 5.5 | V |
| CLEN | VDD | - | 5.0 | - | V |
| | DIN | 1.0 | | | |

### EEPROM block

| Operation Mode | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| READ / MRGN READ | VDD | 1.8 | 5.0 | 5.5 | V |
| INTHV WRITE / MRGN INTHV WRITE | VDD | 2.6 | 5.0 | 5.5 | V |
| CLEN | VDD | - | 5.0 | - | V |
| | DIN | 1.0 | | | |

## DC Electrical Characteristics (Tj = specified, VDD = specified, VSS =0V, Cload=1pF)

| Operation Mode | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| READ / MRGN READ (VDD Current @ 5V) [High speed mode] | $I_{DR}$ (@ 16 MHz) | - | 6.5 | - | mA |
| | $I_{DR}$ (@ 4 MHz) | - | 3.5 | - | |
| READ (VDD Current @ 5V) [Low power mode] | $I_{DR}$ (@ 2 MHz) | - | 1.3 | - | mA |
| | $I_{DR}$ (@ 1 MHz) | - | 0.8 | - | |
| READ / MRGN READ (VDD Current @ 5V) [Power saving mode] | $I_{DR}$ (@ 500 KHz) | - | 0.5 | - | mA |
| | $I_{DR}$ (@ 32 KHz) | - | 30 | - | uA |
| INTHV WRITE / MRGN INTHV WRITE (VDD Current) | $I_{DW}$ | - | 30 | - | mA |
| STATIC (VDD Current) | $I_{DS}$ | - | - | 500 | uA |
| NON-STATIC (VDD Current) | $I_{NDS}$ | - | - | 10 | uA |
| STANDBY (VDD Current) | $I_{SB}$ | - | 1 | 10 | uA |

## READ (MRGN READ) Peak Current

| Parameter | Symbol | Slow (VDD = 1.8V@ 85℃) | Typical (VDD = 5.0V@ 25℃) | Fast (VDD = 5.5V@ -40℃) | Unit |
|---|---|---|---|---|---|
| Read in Peak Current (VDD Current) | $I_{DRP}$ | TBD | TBD | TBD | mA |
| | | TBD | TBD | TBD | ns |

## INTHV WRITE (MRGN INTHV WRITE) Peak Current

| Parameter | Symbol | Slow (VDD = 2.6V@ 85℃) | Typical (VDD = 5.0V@ 25℃) | Fast (VDD = 5.5V@ -40℃) | Unit |
|---|---|---|---|---|---|
| Write in Peak Current (VDD Current) | $I_{DWP}$ | TBD | TBD | TBD | mA |
| | | TBD | TBD | TBD | ns |

## Operating Mode Selection[1]

### User Mode

| Pin Name | STANDBY | STATIC | NON-STATIC | READ[2] | | INTHV WRITE | |
|---|---|---|---|---|---|---|---|
| CS | L | H | H | H | | H | |
| READ | L or H | L | L | H | | L | |
| WR | L or H | L | L | L | | H | |
| CLEN | L or H | L | L | L | | L | |
| IFREN | L or H | L or H | L or H | L or H | L | L or H | L |
| EEPROM | L or H | L or H | L or H | L | H | L | H |
| SRL | L or H | L | L | L | | L | |
| MRGN | L or H | L | L | L | | L | |
| CLKIN | L or H | L or H | L or H | L or H | | L / H toggle | |
| ISAVB | L or H | L or H | L or H | *2 | | L or H | |
| STATICEN | L or H | H | L | | | L or H | |

### Test Mode

| Pin Name | CLEN | | MRGN READ[2] | MRGN INTHV WRITE |
|---|---|---|---|---|
| CS | H | | H | H |
| READ | L | | H | L |
| WR | L | | L | H |
| CLEN | H | | L | L |
| IFREN | L or H | L | L | L |
| EEPROM | L | H | H | H |
| SRL | L | L or H | L or H | L |
| MRGN | L | | H | H |
| CLKIN | L or H | | L or H | L / H toggle |
| ISAVB | L or H | | *2 | L or H |
| STATICEN | L or H | | | L or H |

Notes:

1. Please refer to user and test mode waveform.

2. Option setting for Read operation:

| IFREN | EEPROM | ISAVB | STATICEN | Remark |
|---|---|---|---|---|
| L or H | L | H | H | High speed mode (16 MHz, 4 MHz operation) |
| L | H | | | |
| L or H | L | L | H | Low power mode (2 MHz, 1 MHz operation) |
| L or H | L | L | L | Power saving mode (500 KHz & 32 KHz operation) |
| L | H | | | |

We propose to select high speed mode when the operation is more than 4 MHz, select low power mode should follow the operating voltage, at less than or equal to 500 KHz operation, select the power saving mode. To change the option setting for read operation, the READ signal must be low, and the next READ signal can be pulled “H” after 100 ns.

## SRL Function Table

| Mode | SRL=L | SRL=H |
|---|---|---|
| **CLEN** | Measure Cell Current<br>in default cell per bit | Measure Cell Current<br>in shadow cell per bit |
| **MRGN READ** | Read Data in default cell | Read Data in shadow cell |

## MRGN Function Table

| Mode | MRGN = L or H | Note |
|---|---|---|
| **READ** | MRGN = L | Normal read operation.<br>(Default or shadow cell code could not be read out alone.) |
| **INTHV WRITE** | MRGN = L | Default and shadow cells will be written into the inverse code. |
| **CLEN** | MRGN = L | Default or shadow cell could be measure current alone.<br>User could use SRL pin to select default or shadow cell. |
| **MRGN READ** | MRGN = H | Default and shadow cells code could be read out.<br>User could use SRL pin to select default or shadow cell. |
| **MRGN INTHV WRITE** | MRGN = H | Default and shadow cells will be written into the same code. |

## Capacitance

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Address/Control Input Pin Capacitance | $C_{IN}$ | - | 0.2 | pF |
| Data Input Pin Capacitance | $C_{DIN}$ | - | 0.2 | pF |
| Data Output Pin Capacitance | $C_{DOUT}$ | - | 0.1 | pF |

## MTP, Information and EEPROM blocks Selection

| EEPROM Pin | IFREN Pin | Used Address Pin | Selected Block | Selected Address |
|---|---|---|---|---|
| L | L | ADR[12:0] | MTP | 0000H ~ 1FFFH |
| L | H | ADR[4:0] | Information[1] | 0000H ~ 001FH |
| H | L | ADR[6:0] | EEPROM[2] | 0000H ~ 007FH |

Notes:

1. Information block: ADR [12:5] should remain logic “L” state.
2. EEPROM block: ADR [12:7] should remain logic “L” state.
   I/O Configuration: x8 separate DIN [7:0] / DOUT [7:0] Bus.
   Write mode: DIN [15:8] should remain logic “H” or “L” state.

## Timing Parameters (Tj = specified, VDD = specified, VSS =0V, Cload=1pF)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Setup Time between VDD and CS | Tpwcss | 1.8V≤VDD≤5.5V | 1 | - | - | us |
| Hold Time between VDD and CS | Tpwcsh | 1.8V≤VDD≤5.5V | 0 | - | - | ns |
| CS to READ / WR Setup time | Tcsctrls | 1.8V≤VDD≤5.5V | 100 | - | - | ns |
| Address/Data Setup Time | Tads | 1.8V≤VDD≤5.5V | 15 | - | - | ns |
| DOUT Hold Time | Tdoh | 1.8V≤VDD≤5.5V | 0 | - | - | ns |
| Address Hold Time for Read | Tadhr | 1.8V≤VDD≤5.5V | 5 | - | - | ns |
| Clock Cycle | Tclk | 2.6V≤VDD≤5.5V | 10 | 12.5 | 15 | us |
| WR Pulse Width | Twpw | 2.6V≤VDD≤5.5V | 100 | - | - | ns |
| BUSY Access Time to WR | Tbas | 2.6V≤VDD≤5.5V | - | - | 100 | ns |
| Write Recovery Time | Twrc | 2.6V≤VDD≤5.5V | 1 | - | - | us |
| Measurement Current Wait Time | Tmcw | VDD=5.0V | 100 | - | - | ns |
| Address Hold Time for CLEN | Tadhc | VDD=5.0V | 0 | - | - | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| Write Time (changed code) @ MTP / Information | Twr | 4.5V≤VDD≤5.5V | - | 0.3 | - | ms |
| Write Time (changed code) @ EEPROM | | 2.6V≤VDD≤5.5V | - | 0.7 | - | ms |
| Write Time: (non-changed code) @ MTP / Information | | 4.5V≤VDD≤5.5V | 20 | - | - | us |
| Write Time: (non-changed code) @ EEPROM | | 2.6V≤VDD≤5.5V | 80 | - | - | us |

## Read Operation: High speed mode

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| READ Cycle Time @ MTP / Information | Trc | 4.5V≤VDD≤5.5V | 60 | - | - | ns |
| | | 1.8V≤VDD<4.5V | 300 | - | - | ns |
| READ Cycle Time @ EEPROM | | 1.8V≤VDD≤5.5V | 300 | - | - | ns |
| READ Access Time @ MTP / Information | Trac | 4.5V≤VDD≤5.5V | - | - | 60 | ns |
| | | 1.8V≤VDD<4.5V | - | - | 300 | ns |
| READ Access Time @ EEPROM | | 1.8V≤VDD≤5.5V | - | - | 300 | ns |

## Read Operations: Low power mode

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| READ Cycle Time @ MTP / Information | Trc | 4.5V≤VDD≤5.5V | 500 | - | - | ns |
| | | 1.8V≤VDD<4.5V | 1 | - | - | us |
| READ Access Time @ MTP / Information | Trac | 4.5V≤VDD≤5.5V | - | - | 500 | ns |
| | | 1.8V≤VDD<4.5V | - | - | 1 | us |

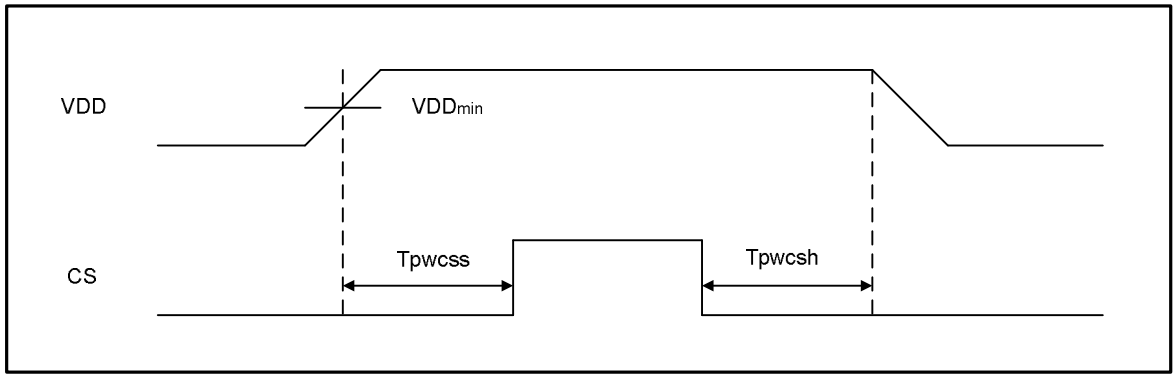
## Read Operations: Power saving mode

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| READ Cycle Time | Trc | 1.8V≤VDD≤5.5V | 2 | - | - | us |
| READ Access Time | Trac | 1.8V≤VDD≤5.5V | - | - | 2 | us |

## Operation Sequence and Timing

## User Mode

1. Power on and Power down Timing



# 2. READ Operation (ADR toggle type)

## 2.1. READ Operation Sequence

I. READ operation is controlled by “ADR” signal. When "ADR" changing, the data of corresponding ADDRESS can be read-out through “DOUT” pin after the read access time.

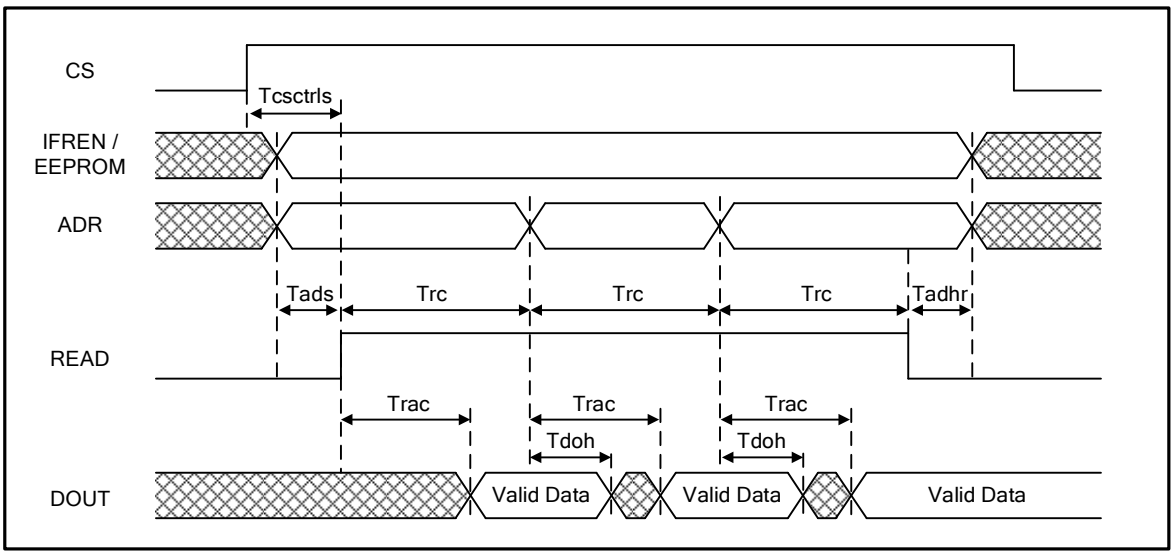
## 2.2. Sequence for READ

I. Set “CS” as “H”.

II. Set the target address, and then set "READ" to "H".

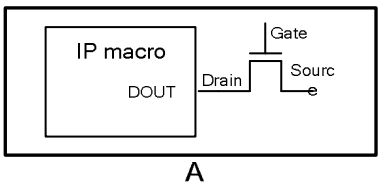
III. Valid data is accessible by through “DOUT” pin after specified “access time.”

## 2.3. READ Operation Timing

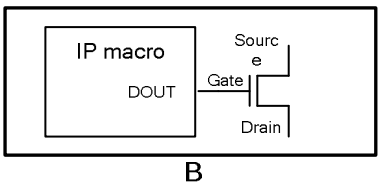



DOUT Pin Connection Requirement

1. It is NOT allowed to connect DOUT to the drain nor source of NMOS / PMOS. (Refer to figure A as below.)
2. Strongly recommend user connecting DOUT to the gate of NMOS / PMOS. (Refer to figure B as below.)




A




B

# 3. INTHV WRITE Operation

## 3.1. INTHV WRITE Operation Sequence

I. INTHV WRITE means to execute WRITE operation by internal charge pump of IP macro itself.

II. The data in DIN will be written into the corresponding ADDRESS after “WR” signal rising.

III. “BUSY” signal is necessary to be detected during WRITE operation to judge whether WRITE operation is completed.

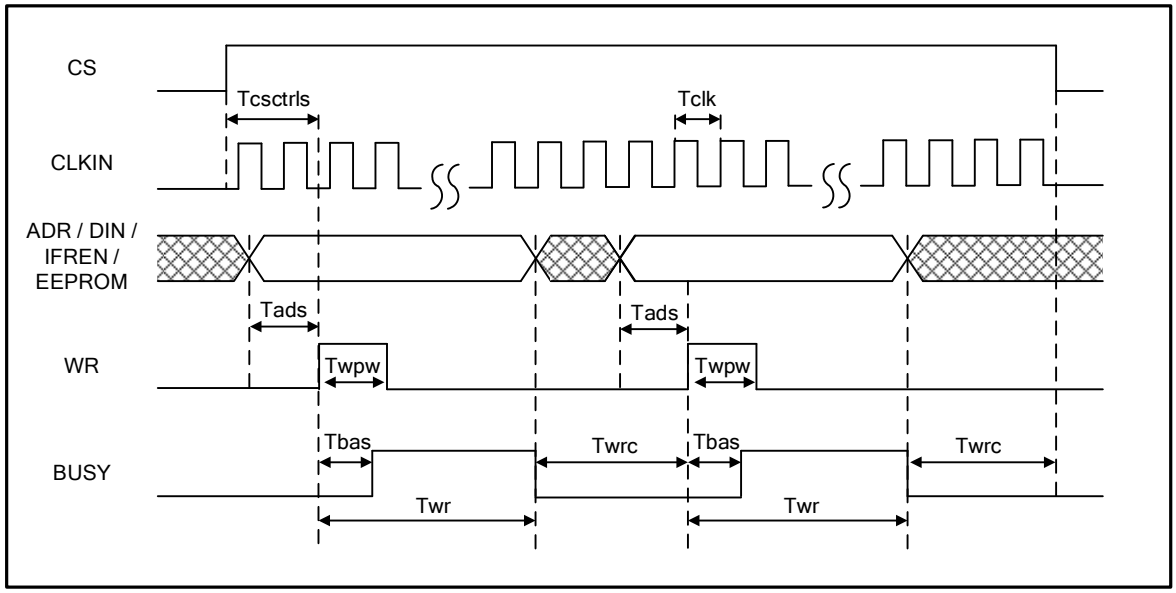
## 3.2. Sequence for INTHV WRITE

I. Set “CS” as “H”. Set “CLKIN” as “L” / “H” toggle.

II. Set the Data and corresponding ADDRESS, and then execute a WR Pulse.

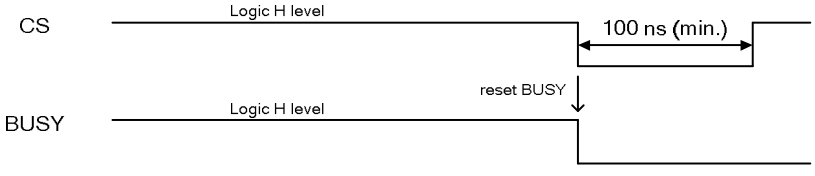
III. Detect “BUSY” signal for judging whether WRITE operation is completed.

## 3.3. INTHV WRITE Operation Timing




Notes:

1. The time period for a data written-in is not fixed. User is NOT allowed to finish the writing operation by waiting a fixed time period.
2. Data access operation is allowable in 1us later after “BUSY” is pulled to “L”. Otherwise incorrect Data may be read-out.
3. CLKIN duty cycle: 50%/50%
4. An unexpected write cycling number over the endurance specification may make BUSY signal keep at logic H level. Please pull-down CS signal to reset BUSY signal and the next CS signal can be pulled “H” after 100 ns.



# Test Mode

## 1. CLEN Operation

### 1.1. CLEN Operation Sequence

I. "CLEN" operation is used for the measurement of memory cell current by through DIN pin. This function provides great help for the analysis if there is any failure event and issue. User is recommended strongly to set this function up.

### 1.2. Sequence for CLEN

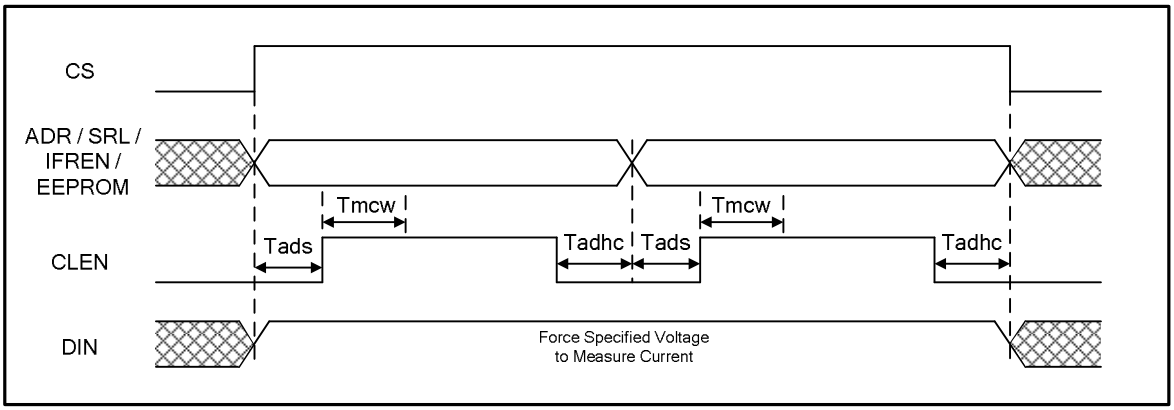
I. Set "CS" as "H".

II. Set the target ADDRESS.

III. Set "CLEN" as "H" and to keep it.

IV. Force bias on DIN pin to measure the bit cell current.

### 1.3. CLEN Operation Timing




Notes:

1. DIN pin should be tied to IO pad and forced the bias which is mentioned in the "Recommended DC Operating Conditions table."
2. After the target ADDRESS is set, the bit cell current can be measured by through the specific IO pad.
3. IFREN and EEPROM can't be high at the same time.
4. SRL = L, measured default memory cell; SRL = H, measured shadow memory cell.

# 2. MRGN READ Operation (ADR toggle type)

## 2.1. MRGN READ Operation Sequence

I. MRGN READ operation is a test mode for data retention test. Default or shadow cell code could be read out alone.

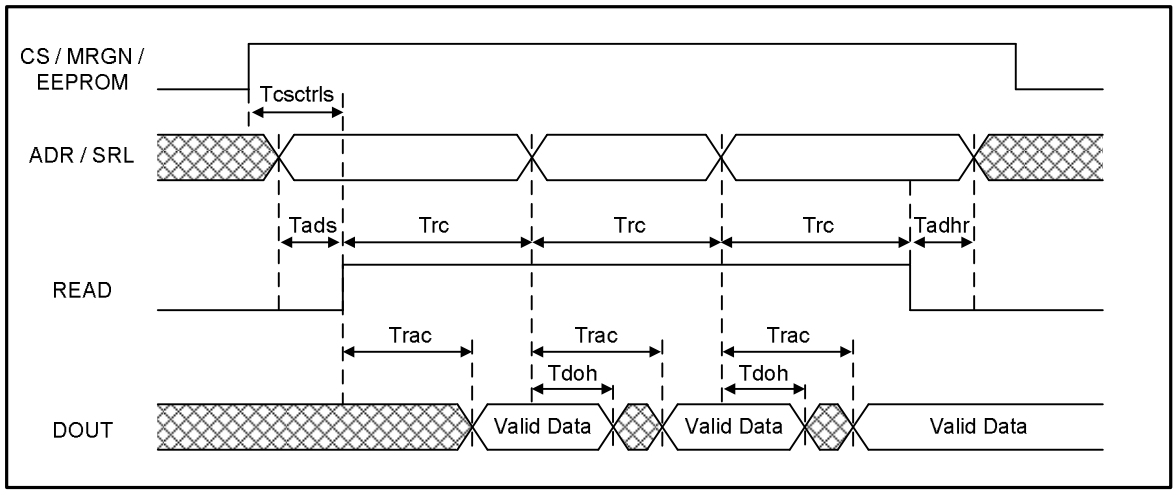
## 2.2. Sequence for MRGN READ

I. Set “CS” as “H”. Set “EEPROM” as “H”. Set “MRGN” as “H”.

II. Set the target address, and then set "READ" to "H".

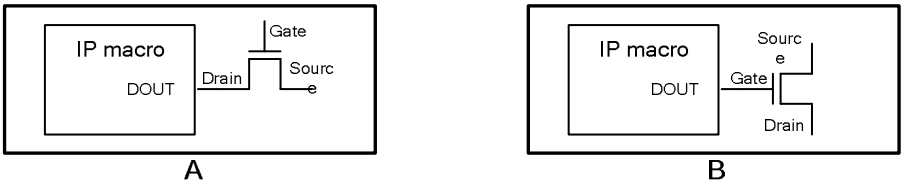
III. Valid data is accessible by through “DOUT” pin after specified “access time.”

## 2.3. MRGN READ Operation Timing




DOUT Pin Connection Requirement

1. It is NOT allowed to connect DOUT to the drain nor source of NMOS / PMOS. (Refer to figure A as below.)
2. Strongly recommend user connecting DOUT to the gate of NMOS / PMOS. (Refer to figure B as below.)



# 3. MRGN INTHV WRITE Operation

## 3.1. MRGN INTHV WRITE Operation Sequence

I. MRGN INTHV WRITE means to execute WRITE operation by internal charge pump of IP macro itself.

II. The data in DIN will be written into the corresponding ADDRESS after “WR” signal rising.

III. “BUSY” signal is necessary to be detected during WRITE operation in order to judge whether WRITE operation is completed.

## 3.2. Sequence for MRGN INTHV WRITE

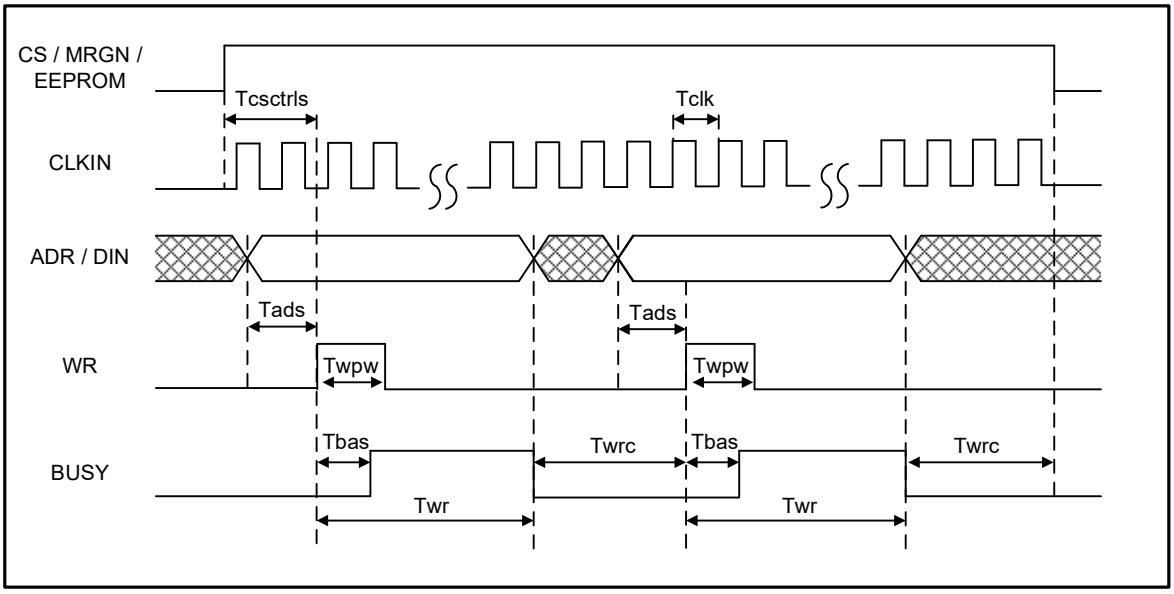
I. Set “CS” as “H”. Set “EEPROM” as “H”. Set “MRGN” as “H”.

II. Set “CLKIN” as “L” / “H” toggle.

III. Set the Data and corresponding ADDRESS, and then execute a WR Pulse.

IV. Detect “BUSY” signal for judging whether WRITE operation is completed.

## 3.3. MRGN INTHV WRITE Operation Timing




Notes:

1. The time period for a data written-in is not fixed. User is NOT allowed to finish the writing operation by waiting a fixed time period.
2. Data access operation is allowable in 1us later after “BUSY” is pulled to “L”. Otherwise incorrect Data may be read-out.
3. CLKIN duty cycle : 50%/50%

## Update history:

| Date | Rev | | What | Who |
|---|---|---|---|---|
| 2022/04/27 | Y10 | 1.0 | Initial draft | Miffy Lin |

**Warning:**

**The specification obtained arrives from individual testing result before integration; it has possibility to have the difference because of the mutual disturbing effect after integration. Therefore, the user must precede the full test and verification to conform the function and the reliability after integration. After the confirmation, and does not have any problem, it can enter the pilot run then the production run. YMC will not be responsible for the related responsibility and loss, if the procedure does not pass through the full test and verification.**