YMG8K16F18L5BR1
YMC Application Note

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General Description

End user designs IC products with the YMC non-volatile memory IP block embedded within. This documentation describes the requirements and recommendations for the end user to follow in order to design, layout and test the customers IC products, write the YMC IP core embedded within, and implement design for test for the SOC. Each of these topics is detailed in the following sections.

Smart Write mode and BUSY Check

1. YMC non-volatile memory IP implements the smart write mode, differing from industrial Flash IP with wait time mode. Users are able to benefit greatly by adopting the smart write mode. There are four kinds of configuration, single-ended type, differential type, OR type and AND type. It will be described clearly as follows.

Single-ended Type

The smart write mode of single-ended type is associated with three reference points, including:

(i) **PV** (program verify) for write "0" reference point
(ii) **Read Reference** for current read reference point
(iii) **EV** (erase verify) for write "1" reference point

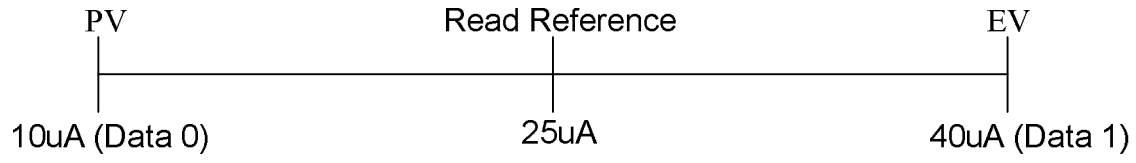


Figure 1.

- Firstly, how to define the write operation? When writing data in some bit cell, the **PV** and **EV** points are the significant reference criteria. If the current of bit cell comes to the level of **PV** (ex. 10uA) solidly in write operation, it shows that the bit is written to a

logic “0”. Similarly, when the bit cell current moves forward to the level of **EV** (ex. 40uA) firmly, it represents the bit is written to a logic “1”. Refer to Figure 1.

- If the circuitry sensing current value is bigger than **Read Reference** (ex. 25uA), the bit in read operation will be regarded as a logic “1”. On the contrary, the current value is smaller than **Read Reference** (ex. 25uA), the bit corresponds to a logic “0”.

Differential Type

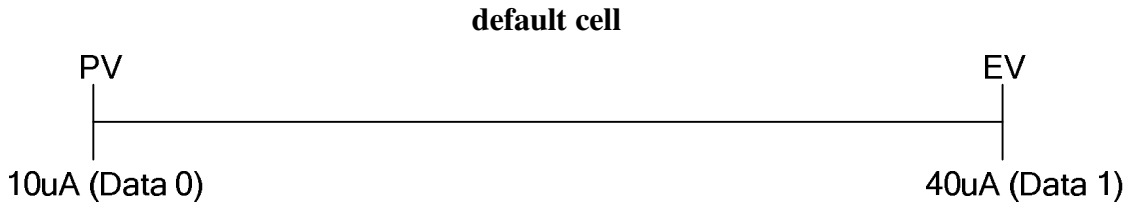


Figure 2.

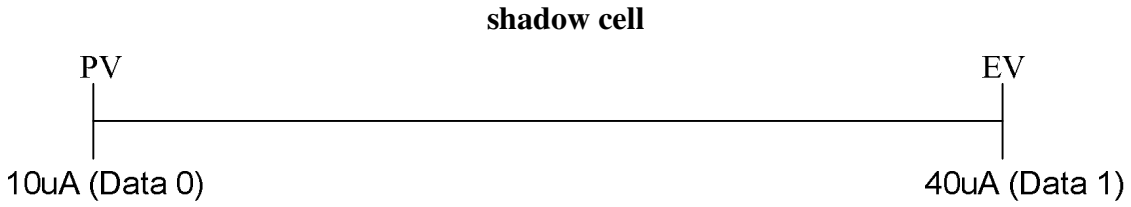


Figure 3.

- The differential type of YMC NVM IP consists of 2 cells per bit. One is default cell and the other is shadow cell. The write operation of differential type is similar to that of single-ended type. What the difference is when writing data code into default cell, the corresponding shadow cell would be written into a reverse code at the same time.
- If the circuitry sensing the default cell with current value of EV is bigger than PV (ex. 10uA) of the homologous shadow cell, the bit in read operation will be regarded as logic “1”. On the contrary, if the current value of PV of default cell is smaller than EV (ex. 40uA) of the corresponding shadow cell, the bit is treated as logic “0”. Please refer to Figure 2 and Figure 3 for reference.

OR Type

- The OR type of YMC NVM IP consists of 2 cells per bit. One is default cell and the other is shadow cell. The write and read operation of OR type is similar to that of single-ended type. When writing data code into default cell, the corresponding shadow cell would be written into a same code at the same time. Please refer to single-ended

type.

- After the baking of YMC NVM IP production test, the read value of the alternative for default cell and shadow cell is a logic “1”, and then the bit is treated as logic “1”.

AND Type

- The AND type of YMC NVM IP consists of 2 cells per bit. One is default cell and the other is shadow cell. The write and read operation of AND type is similar to that of single-ended type. When writing data code into default cell, the corresponding shadow cell would be written into a same code at the same time. Please refer to single-ended type.
- After the baking of YMC NVM IP production test, the read value of the alternative for default cell and shadow cell is a logic “0”, and then the bit is regarded as logic “0”.

2. The smart write mode is not writing in regular period like wait time mode. It must add **BUSY Check** mechanism together in write operation, which can monitor whether the write operation is complete or not. When the write operation is finished, it means all bit cell currents have come to PV or EV point, and then the **BUSY** signal will be pulled “low”. Refer to the Figure 4. If users implement the **BUSY Check** mechanism, it can make sure :

- The data have been written to current level rigidly.
- Besides, the **BUSY Check** could simplify the write time of every byte to reduce the whole chip write time. For example, assuming the period of wait time mode is 5ms. Oppositely, when executing **BUSY Check**, the first byte write time is 0.6ms and the second byte is 0.7ms, it is clear of 0.6ms+0.7ms << 5ms+5ms.

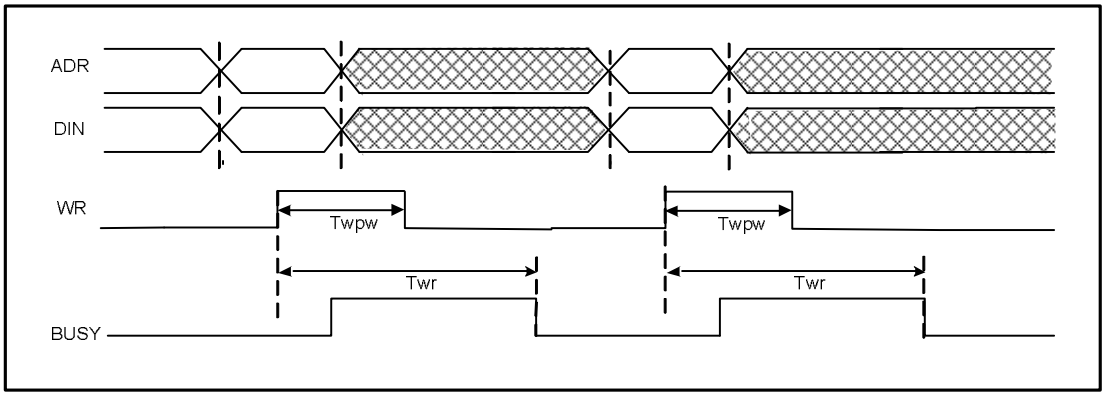


Figure 4.
(About the actual waveform please refer to SPEC)

3. If users write the same data again on the same location, the data will be written into memory array in a very short BUSY pulse. This BUSY pulse may be 200ns (min.) of byte write time. When the user’s system is designed to detect BUSY signal in regular period

time, the BUSY signal may be too short to be discriminated.

4. YMC NVM IP also provides WRFAIL operation executing with BUSY Check mechanism. Refer to Figure 5. When busy time exceeds the maximum Twr, WRFAIL signal is pulled "high" and BUSY signal is pulled "low" to interrupt the write operation. This will avoids BUSY signal keeping "high" all the time and user's system can still work well. WRFAIL signal will be cleared by next WR rising edge or when CS goes low. The maximum write fail time is 50ms under characterization. If WRFAIL signal pulled "high", but the data is read correct, it doesn't mean the data have been written to current level rigidly.

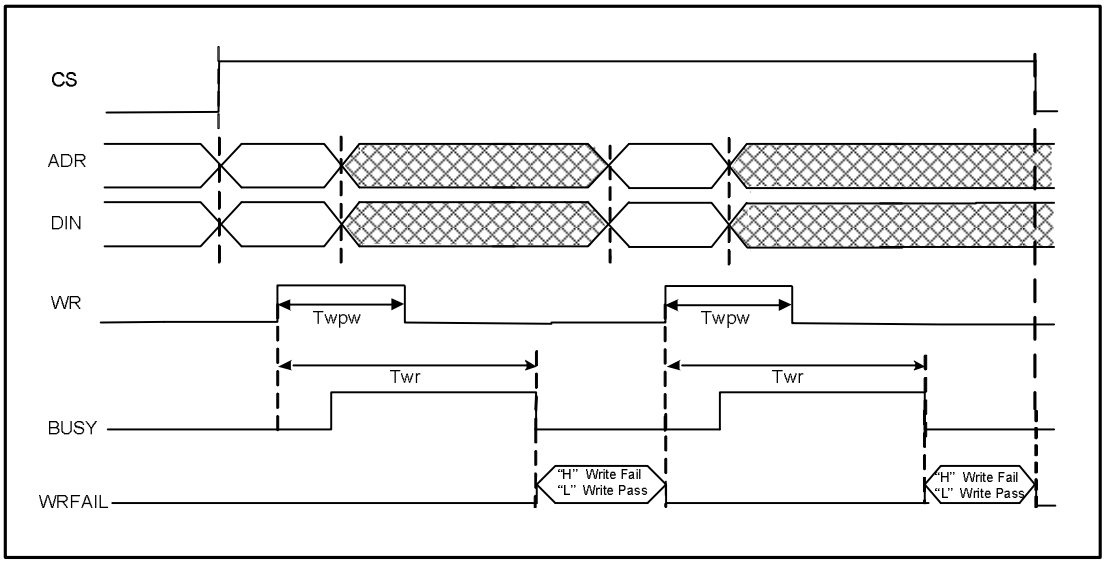


Figure 5.
(About the actual waveform please refer to SPEC)

5. YMC NVM IP implements byte write or word write operation (depending on x8 or x16 configuration), differing from traditional Flash IP which needs sector erase or chip erase first and then page program when programming. While executing YMC's byte write or word write operation, users can easily write one or more bytes in any location users want. It avoids sector erase or chip erase in advance and simplify the write algorithm.

Design Considerations

Please follow the implementation of the waveform provided by YMC.

1. **Power On Sequence:**
   - **1.1** Power supply should come up first. The RESETB must remain low until the power is turned on as shown in Figure 6.
   - **1.2** Regarding the power on sequence of dual power supply IP, the lower VDD should be

up prior to the higher VDD.

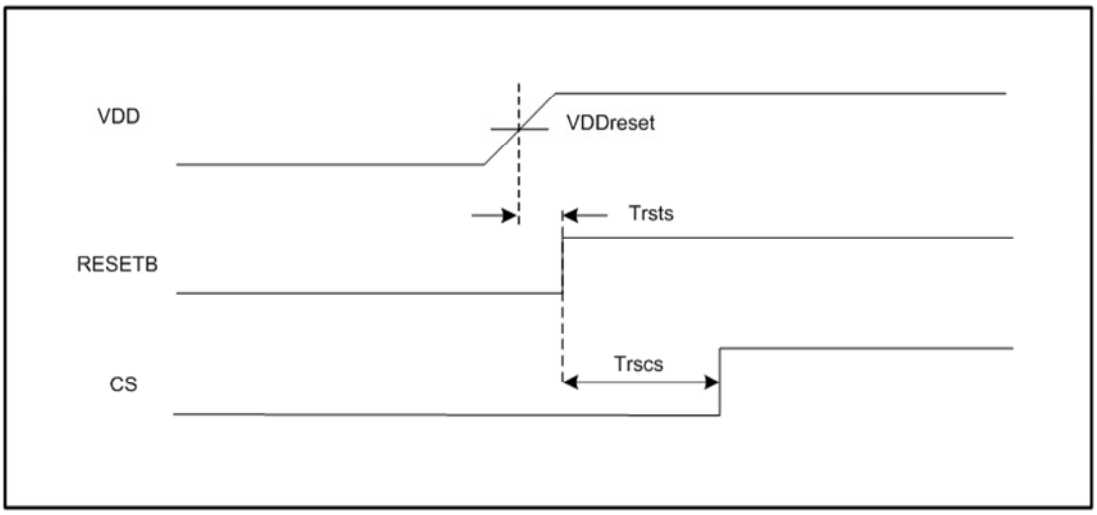


Figure 6. Reset Timing

(About the actual waveform please refer to SPEC)

2. YMC NVM IP provides user modes and test modes.

- User modes: Standby, Read and Write
- Test modes: Measure Cell Current

2.1 Standby mode:

- Please keep all control signals inactive.
- No recovery time required from standby to first byte read and write.
- DOUT is either a tri-state or a non tri-state bus. Please refer to the datasheet.

2.2 Read mode:

- There are two types of read mode. User can only use one of them for reading data, which is specified in YMC NVM IP data sheet.
  - A Type:
    Read signal is required to toggle when ADR changed for sequential read.
  - B Type:
    Read signal is not required to toggle when ADR changed for sequential read.

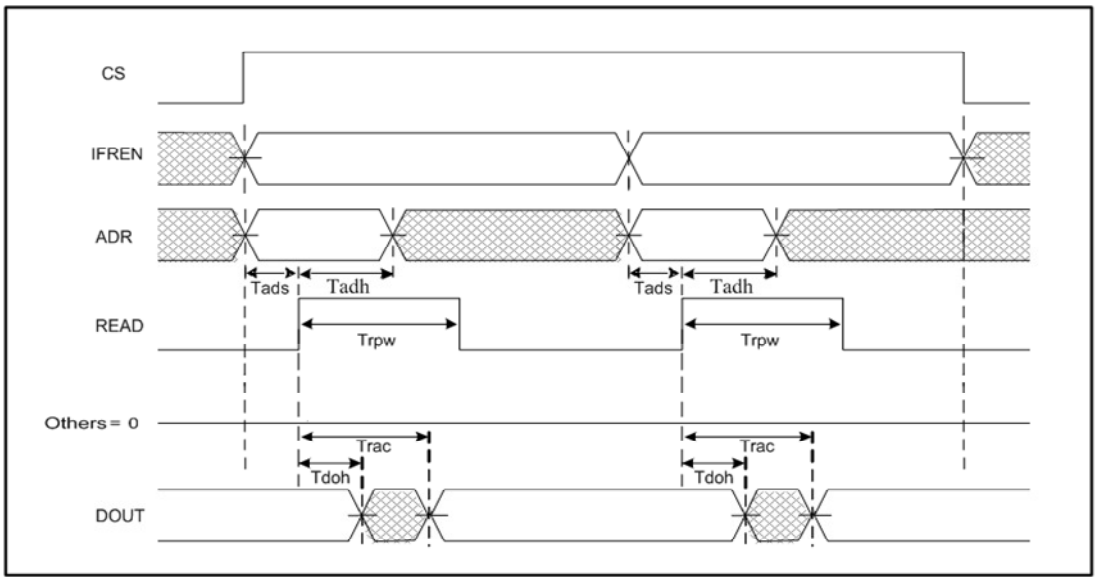


Figure 7. Read Cycle: A Type
(About the actual waveform please refer to SPEC)

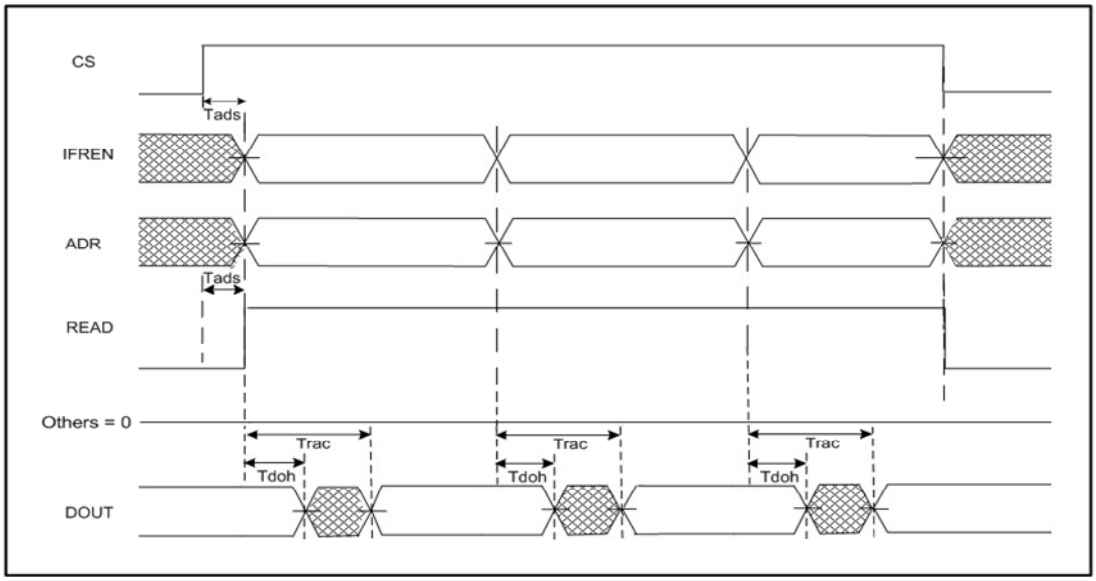


Figure 8. Read Cycle: B Type
(About the actual waveform please refer to SPEC)

2.3 Write mode:

- Data stored in NVM IP is updated byte by byte (X8 configuration) or word by word (X16 configuration) respectively.
- User can interrupt the write operation by a going LOW CS or RESETB.
- YMC recommends that user monitors the BUSY flag to judge whether the write operation is complete or not. If the busy time exceeds the maximum Twr, CS pin must be pulled-down for interrupting write operation.

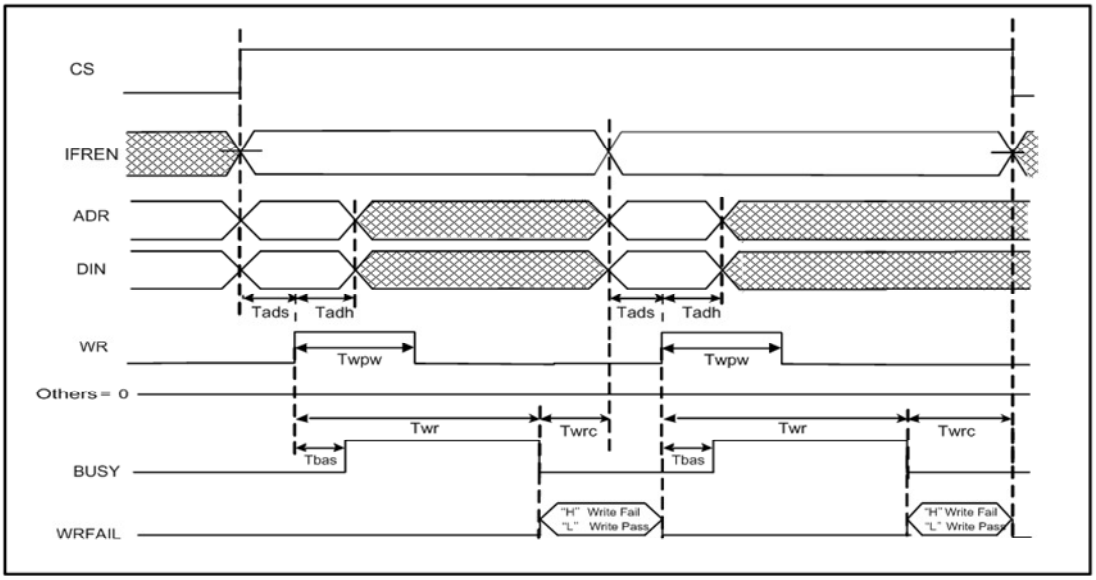


Figure 9 Write Cycle

(About the actual waveform please refer to SPEC)

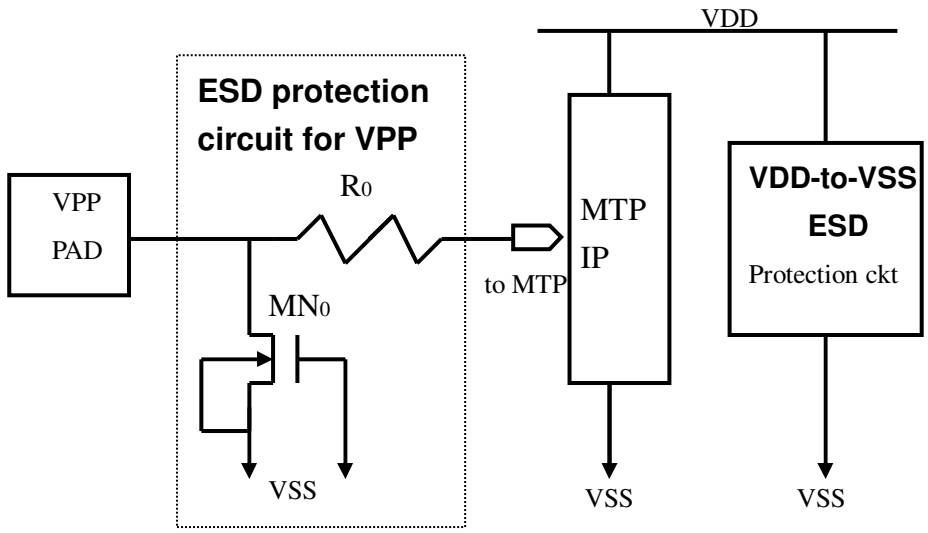
2.4 Measure Cell Current:

- The simulation model (Verilog) does not include test modes.

3. Notes:

- All input signals of YMC NVM IP must be controlled by user's read/write logic circuitry. Please refer to the timing waveforms in YMC NVM IP spec.
- YMC NVM IP does not have any hardware or software protection circuitry, so user has to implement some kind of control logic to avoid the wrong operation.
- The external high voltage supply pin (VPP) could be biased at VDD or VSS or floating, if a build-in charge pump is used to supply high voltage during write operation.
- In a read or write cycle of information block, ADR[n:5] and ADR[n:4] are don't-cared address bits for that of 32x8 and 16x16 MTP IP respectively. In the same way, ADR[n:7] and ADR[n:6] are don't-cared address bits for that of 128x8 and 64x16 MTP IP respectively.
- It is not allowed to have read operation while IP is still in write cycle.
- ECED pin is a flag indicating that internal ECC has been conducted or not. When "ECED" signal is pulled to "H", it means that data is corrected. ECED pin is specified in datasheet.
- If high voltage power supply, VPP, is tied to IO pad, this pad should have ESD protection circuit.

- In order to prevent from device damage, the VPP voltage level is recommended to be ramped up by stepping, such as 0V → VDD → HV.
- The alternative to prevent from device damage is to slow down the ramp up speed of VPP voltage level during writing data into memory.
- There are two gds files, PT(Phantom, gds frame including all layers above metal1) and PTO(gds outline) in design kit. For qualified IPs, YMC suggests customers to input PT instead of PTO during the design procedure. If customers would like to skip IP merge procedure of qualified IPs by using PT when taping out, please inform YMC beforehand.
- **ESD protection circuit design guide on VPP pin**



1. It is strongly recommended to have ESD protection circuit between VDD and VSS power lines in customer's chip area.
2. The ESD protection circuit for VPP pin includes resistor (R_0) and gate-grounded NMOS transistor (MN_0).
3. The resistance of R_0 is at least 200_ohm. Poly-Si resistor with silicide-blocking mask is preferred.
4. The channel width of IO device MN_0 is at least 300um. The diffusions of MN_0 have to be with silicided-blocking mask. (Fig. 10)

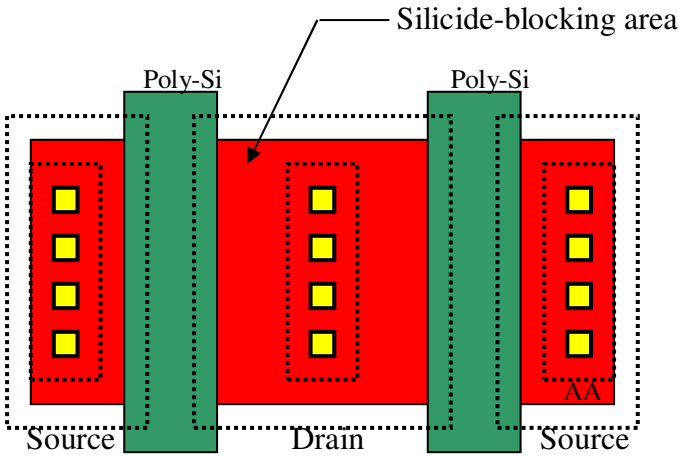
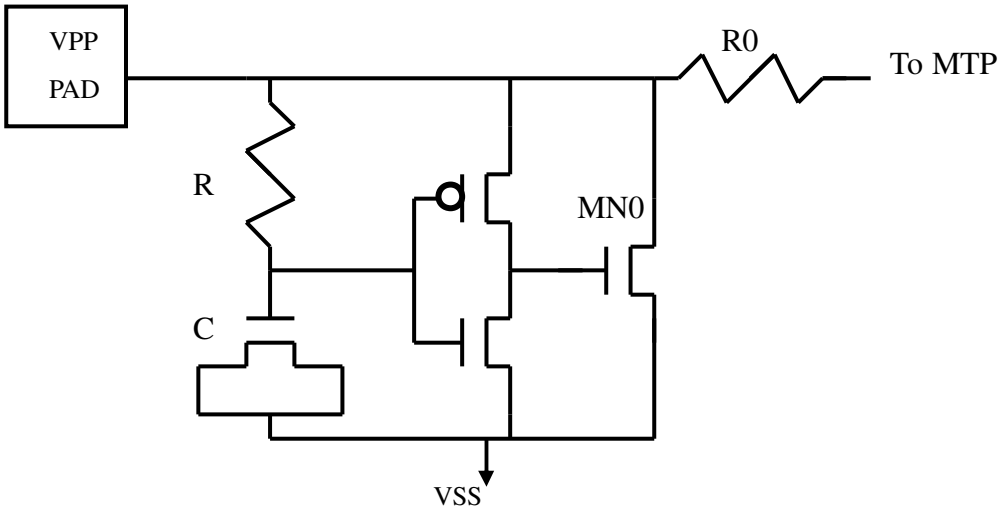


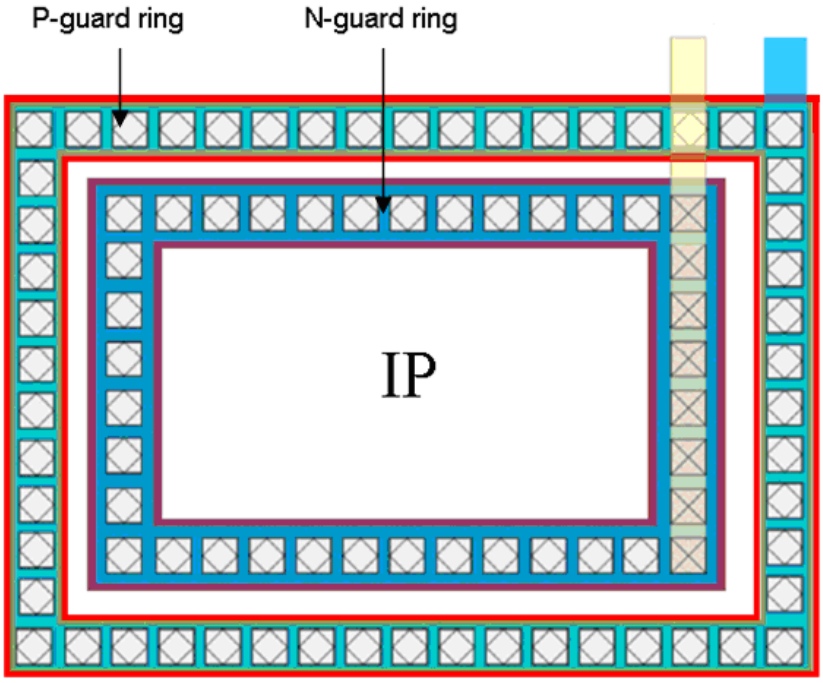
Figure 10. MOS layout with silicide-blocking mask

5. Detailed physical design rules please refer to related documents issued by wafer foundry vendors.
6. Alternative ESD protection circuit is strongly recommended:
   The time constant RC is designed at least as 100nsec.



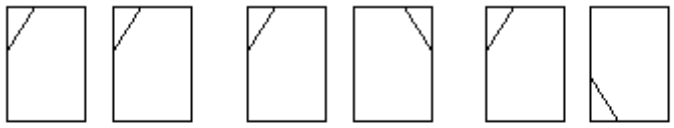
Layout Considerations

1. **Double Guard Ring:**
   - It is strongly recommended to have double guard ring around YMC NVM IP when using logic process technology or mixed mode process technology.
   - Double guard ring layout guide:

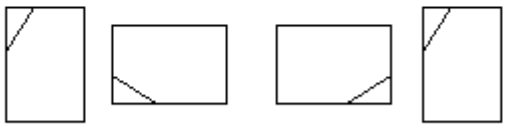


Note : If users would like to have only one guard ring around MTP IP, N-guard ring tight to the highest supply voltage level is recommended.

2. **Design Rule Check (DRC):**
   - In order to provide cost-effective MTP IP, there might be some layout rule violations in memory array. Those waived layout rules are listed in the specific IP's chip information file.
3. **Layout Versus Schematic (LVS):**
   - The phantom gds file of NVM IP contains the top-level pins. The user may use it to execute LVS check to ensure the correct connection to the IP interface.
4. **Place and route:**
   - It is not allowed to place NVM IP with 90 degree rotation clockwise or counter clockwise about the wafer notch or flat.



correct



wrong

- The NVM IP phantom boundary should be treated as a routing block layer i.e. do not route over the IP phantom. All polygons must keep at least minimum space to the NVM IP boundary except those polygons used for IP connection.

5. Notes:

- User has to follow wafer foundry vendor's CAD layer mapping file.
- User must check the connectivity of YMC NVM IP before tape out.
- The routing power width is at least 10um.
- The routing power length is less than 1000um.
- The routing ground length is less than 1000um.

Design for Test

In order to assure the quality and reliability of YMC's IP, a proper test methodology is applied in wafer level test. Each YMC's IP user has his own approach for implementing the test interface; so there may be a lot of test approaches for YMC's IP if there is not a standard test interface. YMC provides only some suggestions for reference herein.

1. YMC strongly recommends users to build the cell current measurement function. This function is an appropriate method to verify in engineering test mode. There are two kinds of operation for cell current measurement, such as "force voltage in VPP pin" and "force voltage in DIN pin". User should follow the IP spec. for the operation of cell current measurement.

1.1. In case YMC NVM IP adopts dual memory cells in one data bit, one is default memory cell and the other is shadow memory cell. CLEN operation is a test mode to measure the memory cell current. SRL can select default or shadow memory cell of one bit in CLEN operation.

1.2. "force voltage in VPP pin", refer to Figure 11. The external high voltage supply pin (VPP)

needs to be tied to IO pad to force one low voltage (ex. 1.5V). ADR[8:0] is used to select address. There is only one of DIN[7:0] buses indicating to the corresponding IO to be pulled as logic "L" at a time and others are logic "H". Thus it can be measured the cell current during CLEN high active period. For example of 512x8 IP shown as Figure 11, one address 00 is selected. When DIN[7:0] is 11111110, it can be measured for the cell current of IO 0 at address 00. The rest may be deduced by analogy. When DIN[7:0] is 01111111, it is for the cell current of IO 7.

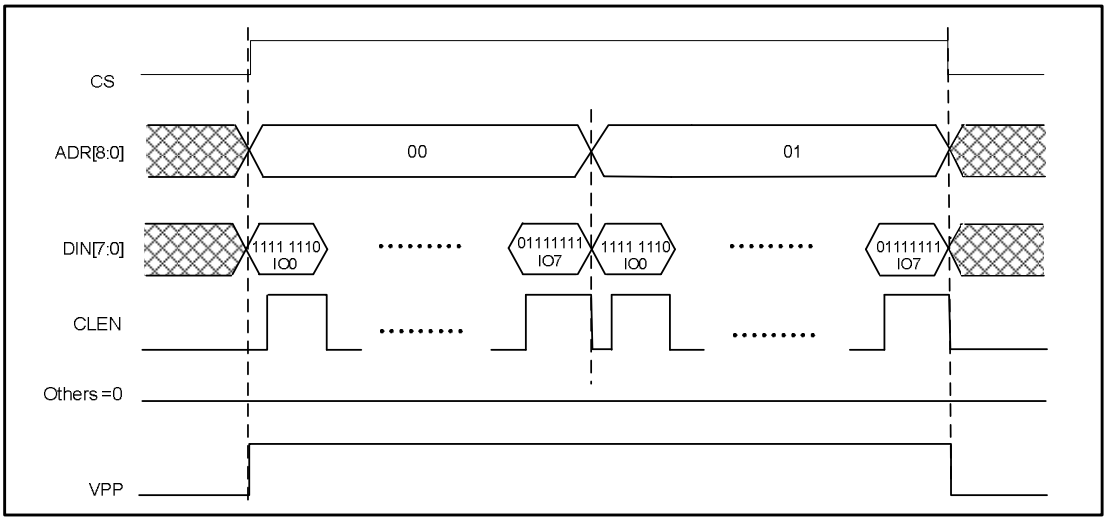


Figure 11
(About the actual waveform please refer to SPEC)

1.3. "force voltage in DIN pin", refer to Figure 12. Each DIN pin needs to be tied to IO pad to force a low voltage (ex. 1.5V). ADR[8:0] is used to select address, each DIN pin should be force a low voltage (ex. 1.5V). Thus it can be measured the cell current during CLEN high active period. For example of 512x8 IP shown as Figure 12, one address 00 is selected. When each DIN pin force a low voltage, it can be measured for the cell current of IO 0 ~ IO7 at address 00.

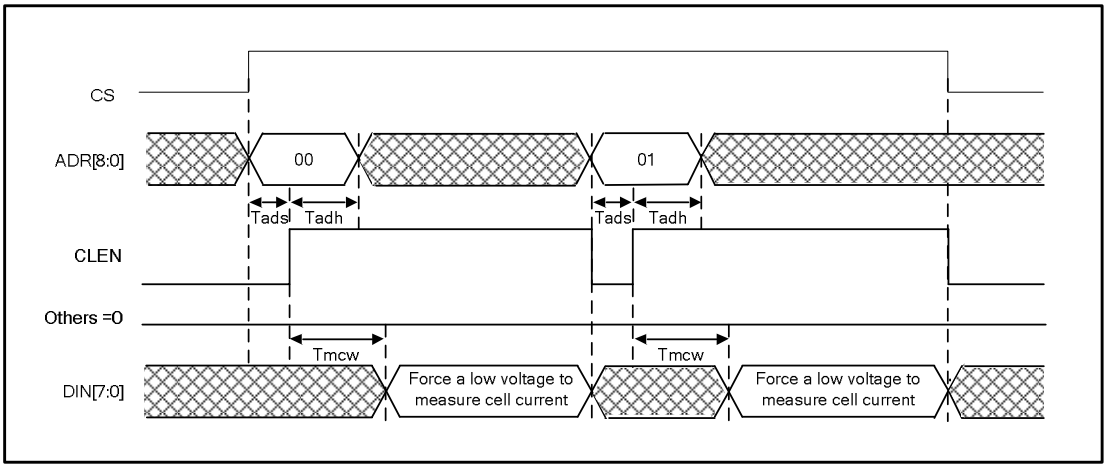
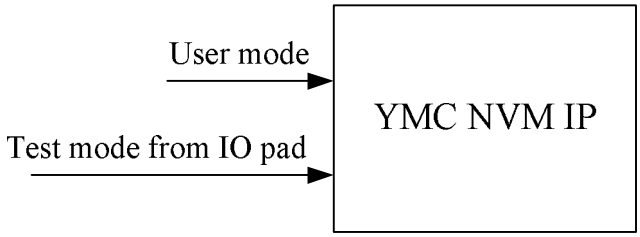


Figure 12
(About the actual waveform please refer to SPEC)

2. When user's IO pads may be a plenty enough, all the YMC NVM IP's interface ports can be tied with user's IO pads. This test structure is the most direct and simple approach. Such NVM IP can be tested easily and independent from all the other logic circuit.



3. When user's IO pads may not be a plenty enough and would still like to tie with YMC NVM IP directly, users can perform operation by serial in / serial out method (ex. I2C).

4. If users control YMC NVM IP by serial in / serial out method, it will spend a lot of time to issue commands. For example, 8Kx8 IP has 8K addresses. It will execute 8K times of commands. So YMC suggests users could set up the internal BIST (Built-in Self Test) mode to shorten test time.

Update history

Date	Rev	What	Who
2022/02/09	1.0	Initial draft	Miffy Lin