YMG8K16F18L5BR1

YMC Embedded NVM IP Testing Methodology

General Description

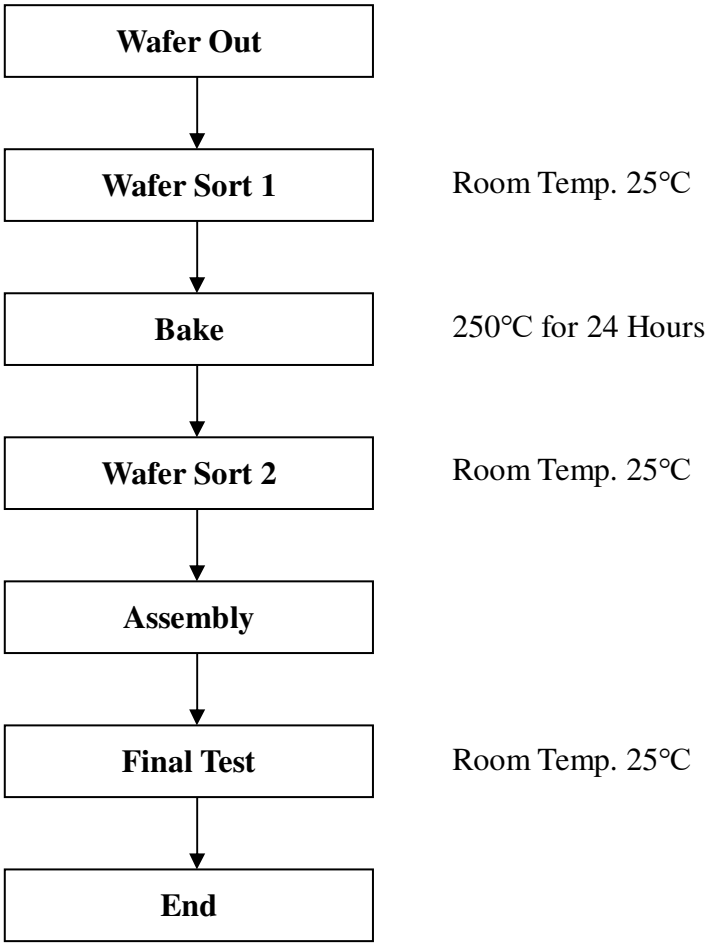
This document is a testing guideline for YMC Embedded NVM IP. It describes the requirements and recommendations for the customer to sort and test the customer's IC. It summarizes the test methodology that includes full production flow, wafer sort and final test flow.

Notes

1. This testing methodology is a testing concept based on YMC NVM IP block, which is able to be applied to YMC embedded NVM IP.
2. The DC testing flow (open/short, input/output leakage, standby current) can be added to customers' MTP and EEPROM testing flow.
3. Detailed testing timings and descriptions are shown in YMC NVM IP datasheets.
4. BUSY pin is a flag that indicates whether write operation is completed or not. It can make sure the data have been written to current level rigidly and it can reduce test time instead of wait time mode.
5. The final baking time depends on the foundry's reliability test and customer specification conditions.
6. The reading frequency of wafer sorting/final testing is consistent with the YMC datasheet, and the minimum access time will be a stricter screening method.

YMC MTP+EEPROM Full Production Test Flow

According to the design architecture, users are recommended to follow the test flow which includes two parts of MTP and EEPROM.



(1) Wafer Sort 1 Flow

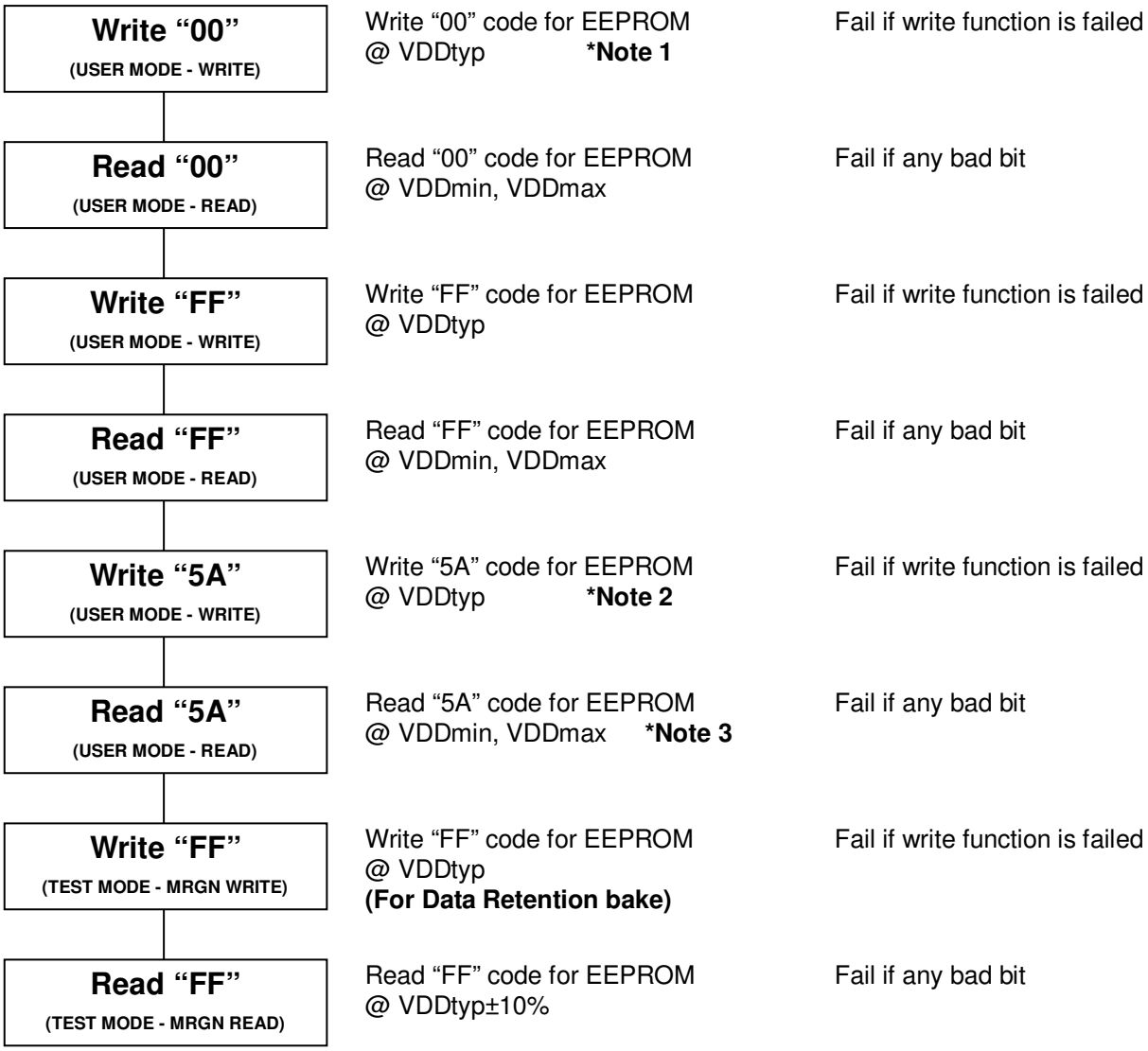
Test Order	Test Condition	Failure Criteria
Open/Short	Force I = -100uA Force I = -100uA	Measure V voltage < -1V Measure V voltage > -0.2V
Leakage	@ VDDmax , force 0V & VDDmax on pins	Measure I current IL>1uA or IL<-1uA
I standby	@ VDDmax	Customer specifies the failure criteria

(Those stages should be included inside customer's MTP and EEPROM test)

MTP

Write "00" (USER MODE - WRITE)	Write "00" code for MTP @ VDDtyp ***Note 1**	Fail if write function is failed
Read "00" (USER MODE - READ)	Read "00" code for MTP @ VDDmin, VDDmax	Fail if any bad bit
Write "FF" (USER MODE - WRITE)	Write "FF" code for MTP @ VDDtyp	Fail if write function is failed
Read "FF" (USER MODE - READ)	Read "FF" code for MTP @ VDDmin, VDDmax	Fail if any bad bit
Write "Diagonal" (USER MODE - WRITE)	Write partial "Diagonal" code for MTP @ VDDtyp ***Note 2**	Fail if write function is failed
Read "Diagonal" (USER MODE - READ)	Read "Diagonal" code for MTP @ VDDmin, VDDmax ***Note 3**	Fail if any bad bit
Write "FF" (USER MODE - WRITE)	Write "FF" code for MTP @ VDDtyp **(For Data Retention bake)**	Fail if write function is failed
Read "FF" (USER MODE - READ)	Read "FF" code for MTP @ VDDmin, VDDmax	Fail if any bad bit

EEPROM



(2) Wafer Sort 2 Flow

Test Order	Test Condition	Failure Criteria
Open/Short	Force I = -100uA Force I = -100uA	Measure V voltage < -1V Measure V voltage > -0.2V
Leakage	@ VDDmax , force 0V & VDDmax on pins	Measure I current IL>1uA or IL<-1uA
I standby	@ VDDmax	Customer specifies the failure criteria

(Those stages should be included inside customer's MTP and EEPROM test)

MTP

Read "FF" **(USER MODE - READ)**	Read "FF" code for MTP @ VDDmin, VDDmax **(For Data Retention check)**	Data Retention check, fail if any bad bit
Write "Checkerboard" **(USER MODE - WRITE)**	Write "Checkerboard" code for MTP @ VDDtyp	Fail if write function is failed
Read "Checkerboard" **(USER MODE - READ)**	Read "Checkerboard" code for MTP @ VDDmin, VDDmax	Fail if any bad bit

EEPROM

Read "FF" **(TEST MODE - MRGN READ)**	Read "FF" code for EEPROM @ VDDtyp±10% **(For Data Retention check)**	Data Retention check, fail if any bad bit
Write "Checkerboard" **(TEST MODE - MRGN WRITE)**	Write "Checkerboard" code for EEPROM @ VDDtyp ***Note 4**	Fail if write function is failed
Read "Checkerboard" **(TEST MODE - MRGN READ)**	Read "Checkerboard" code for EEPROM @ VDDtyp±10%	Fail if any bad bit

(3) Final Test Flow

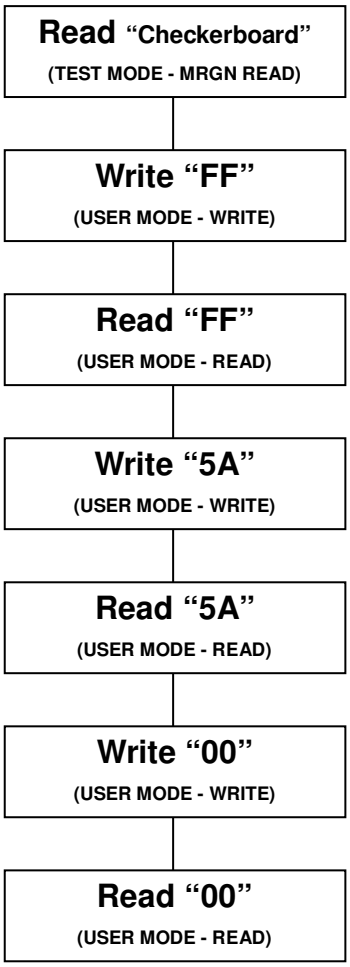
Test Order	Test Condition	Failure Criteria
Open/Short	Force I = -100uA Force I = -100uA	Measure V voltage < -1V Measure V voltage > -0.2V
Leakage	@ VDDmax , force 0V & VDDmax on pins	Measure I current IL>1uA or IL<-1uA
I standby	@ VDDmax	Customer specifies the failure criteria

(Those stages should be included inside customer's MTP and EEPROM test)

MTP

Read "Checkerboard" (USER MODE - READ)	Read "Checkerboard" code for MTP @ VDDmin, VDDmax	Fail if any bad bit
Write "FF" (USER MODE - WRITE)	Write "FF" code for MTP @ VDDtyp	Fail if write function is failed
Read "FF" (USER MODE - READ)	Read "FF" code for MTP @ VDDmin, VDDmax	Fail if any bad bit
Write "Diagonal" (USER MODE - WRITE)	Write partial "Diagonal" code for MTP @ VDDtyp	Fail if write function is failed
Read "Diagonal" (USER MODE - READ)	Read "Diagonal" code for MTP @ VDDmin, VDDmax	Fail if any bad bit
Write "00" (USER MODE - WRITE)	Write "00" code for MTP @ VDDtyp	Fail if write function is failed
Read "00" (USER MODE - READ)	Read "00" code for MTP @ VDDmin, VDDmax	Fail if any bad bit

EEPROM



Read " Checkerboard " code for EEPROM @ VDDtyp±10%	Fail if any bad bit
Write "FF" code for EEPROM @ VDDtyp	Fail if write function is failed
Read "FF" code for EEPROM @ VDDmin, VDDmax	Fail if any bad bit
Write "5A" code for EEPROM @ VDDtyp	Fail if write function is failed
Read "5A" code for EEPROM @ VDDmin, VDDmax	Fail if any bad bit
Write "00" code for EEPROM @ VDDtyp	Fail if write function is failed
Read "00" code for EEPROM @ VDDmin, VDDmax	Fail if any bad bit

Notes

1. VDD means all kinds of power supply specified in datasheet.
2. "Diagonal" pattern and address will be defined in another file.
3. Need to read whole chip, including non-diagonal area.
4. Coverage of checkerboard pattern can't guarantee 100% in EEPROM.

Update history

Date	Rev	What	Who
2022/01/26	1.0	Initial draft (MTP+EEPROM I)	Miffy Lin