CHIP INFORMATION

YMG8K16F18L5BR1_Y10

DSM Table

Process	0.18um 3.3V/(5V)6Vdual-gate MCU Technology Process
Design rule	GLOBALFOUNDRIES 0.18UM 3.3V/(5V)6V MCU TECHNOLOGY TOPOLOGICAL AND RELIABILITY DESIGN RULES Ver. 8
Spice model	YI-141-SM064 (SPICE Mode)
DRC(Calibre)	DRC-CC-000006_V15
LVS(Calibre)	EDA-CAD-018-LV131_V11

Layer Information

- **Formal Drawing Layer**

ITEM	Layer Name	GDSII	TYPE	Comment
1	Nwell	21	0	
2	COMP	22	0	Diffusion
3	Poly2	30	0	Gate
4	Pplus	31	0	
5	Nplus	32	0	
6	Contact	33	0	
7	Metal1	34	0	
8	Via1	35	0	
9	Metal2	36	0	
10	Via2	38	0	
11	Metal3	42	0	
12	SAB	49	0	
13	Dualgate	55	0	6V Gate Oxide

- **Dummy Drawing & Non Tooling Layer**

ITEM	Layer Name	GDSII	TYPE	Comment
1	TEXT0	0	0	YMC's marker
2	Metal1_TEXT	34	10	M1 signal note
3	Metal2_TEXT	36	10	M2 signal note
4	Metal3_TEXT	42	10	M3 signal note
5	IP Tag	63	63	IP Tag
6	RES_MK	110	5	Resistor marker
7	V5_XTOR	112	1	Define 5V Transistor
8	BJT_MK	118	5	BJT marker
9	BJT_DRC_MK	127	5	BJT marker
10	CELL_IMP	11	17	For YMC's Cell array
11	NLDD_BLK	86	17	For YMC's Cell array
12	F_Logo	158	21	GF's marker
13	F_Logo	159	21	GF's marker

DRC Information

- **DRC Rule**

ITEM	RULE	DECRIPTION	AMOUNT	COMMENT
1	GR.TOPO.No_GR_Mk	Customer guarding selected & GUARD_RING_MK is required.	1	Waived

Device Information

• Macro Information

Macro size	X=685um, Y=1230um
Power	VDD, VSS
ADRRESS	13
CNTL	11
IO	DIN*16, DOUT*16
OUTPUT	BUSY

• Device Information

TYPE	INFORMATION
nmos_5p0	5V NMOS
pmos_5p0	5V PMOS
ppolyf_u	P+ POLY Resistor (Unsalicided)
VPNP_10X10	BJT(Vertical_PNP_10X10)

GDS Version

Date	Project	GDS Version
2019/09/27	YEG8K16F18L5BS1_B10	YEG8K16F18L5BS1_B10_092719.gds
2020/10/19	YEG8K16F18L5BS1_Y11	YEG8K16F18L5BS1_Y11_101620.gds
2020/10/23	YEG8K16F18L5BS1_Y11	YEG8K16F18L5BS1_Y11_102320.gds
2020/11/06	YEG8K16F18L5BS1_C10	YEG8K16F18L5BS1_C10_110420.gds
2020/12/31	YEG8K16F18L5BS1_C10	YEG8K16F18L5BS1_C10_123120.gds
2022/04/29	YMG8K16F18L5BR1_Y10	YMG8K16F18L5BR1_Y10_042922.gds

SPI Version

Date	Project	SPI Version
2019/09/27	YEG8K16F18L5BS1_B10	YEG8K16F18L5BS1_B10_merge_092719.net
2020/10/19	YEG8K16F18L5BS1_ Y11	YEG8K16F18L5BS1_Y11_merge_101620.net
2020/10/23	YEG8K16F18L5BS1_ Y11	YEG8K16F18L5BS1_Y11_merge_102320.net
2020/11/06	YEG8K16F18L5BS1_C10	YEG8K16F18L5BS1_C10_merge_110420.net
2020/12/31	YEG8K16F18L5BS1_C10	YEG8K16F18L5BS1_C10_merge_123120.net
2022/04/29	YMG8K16F18L5BR1_Y10	YMG8K16F18L5BR1_Y10_merge_042922.net

Update history:

Date	Description	Version		Who
2019/09/27	Fab3E→Fab35, modify option	B10	V01	CPWu
2020/10/19	Follow FIB to Modify internal timing of SAE for LP/PS mode。	Y11	V10	CPWu
2020/10/23	Delete STATICEN/ISAVB(LP/PS mode)	Y11	V10	CPWu
2020/11/06	Rename : Y11→C10	C10	V01	CPWu
2020/12/31	Update option : RV<0>=H	C10	V02	CPWu
2022/04/29	1. Rename to Y10 2. Pin out : left side	Y10	V10	CPWu