EHB 335E TERM PROJECT

Due: 28 January 2024 @22 o'clock – **No late project report will be accepted.**

In this project, you will be designing a two-stage CMOS operational amplifier. The circuit schematic of the op-amp is shown below. **The project will be done individually. The deadline is chosen based on the last day of grading and it will not be extended.**

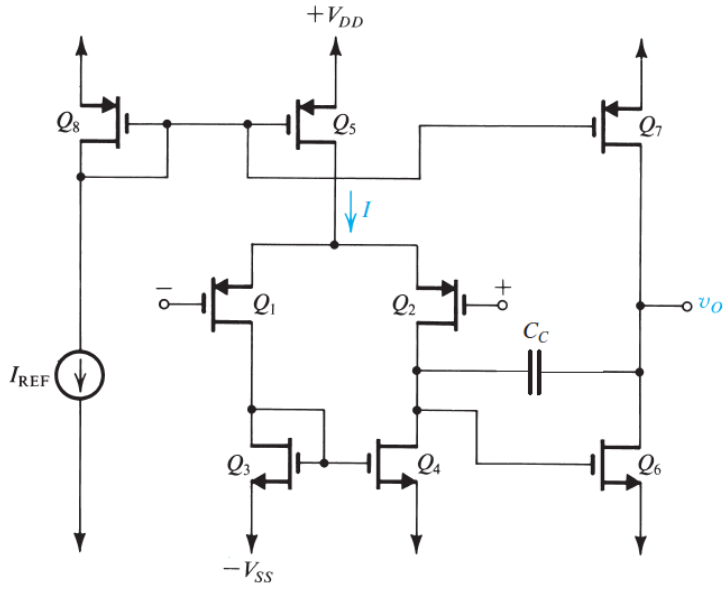

Figure 1: This is a PMOS-input two-stage operational amplifier. (Source: Sedra/Smith 7th edition)

Please note that you can also design an NMOS-input two-stage op-amp. The choice is left to you. You can also add other active/passive components to improve the design performance at your own risk. There are three important metrics that your design should meet:

Voltage Gain > 60 dB

Bandwidth (Unity Gain) > 200 MHz

Phase Margin > 55 degrees

Load Capacitance = 2 pF

Please note that you will only be given 60% of the total project grade if you fulfill these requirements. Of the remaining 40%, 20% percent will be reserved for the project report. The other 20% percent will be assigned based on the competition: They will be distributed regarding the best FOM and worst FOM using the following formula: (FOM – FOM,worst)/(FOM,best – FOM,worst) x 20. The rule of the competition is to get the highest figure of merit for the operational amplifier above.

$$\text{FOM} = \frac{\text{Gain } [\text{dB}] \times \text{Bandwidth } [\text{Hz}]}{\text{Settling Time } [\text{ns}] \times \text{Power } [\text{mW}]}$$

When optimizing FOM, you need to keep in mind that the phase margin must always be above the specified constraint.

You should perform an AC simulation to find out the gain, unity-gain bandwidth, and the phase margin. To measure the power consumption of your circuit, you should do a DC operating point simulation. To determine the settling time, you should perform a transient simulation and apply a square wave at the positive input that goes from 0 to 1 V with a period of 40 ns and a duty cycle of 50%. At the same time,

the negative input should be connected to the output such that the amplifier acts as a unity-gain amplifier. What you should observe is that the output will follow the input, albeit with a delay, until it settles to the same value with the input. The settling time is when the output converges to the input within a 5% variation. The following figure demonstrates the simulation process of the settling time.

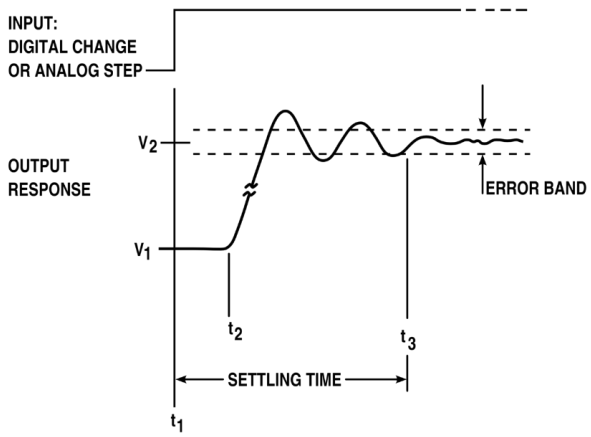

Figure 2: Settling time measurement based on a transient simulation (Source: Wikipedia)

During this project, you will use the following NMOS and PMOS models. You can import them into LTSpice or your favorite SPICE simulator. One helpful link regarding LTSpice is provided below.

Models: Already uploaded to Ninova

Incorporation of the models into LTSPICE: http://www.linear.com/solutions/1083

During this project, you should also consider the following constraints: The supply voltage for 90 nm CMOS technology is 1.2 V. There will be no negative supply. Thus, your rail-to-rail voltage will be between 0 and 1.2 V. Furthermore, you should use only full-integer multiples of the minimum channel length. In a realistic process, you will not be able to fabricate half-integer multiples. This means that you can use 90 nm, 180 nm, or 270 nm as channel length values. Finally, you should make sure that your bulk connections of NMOS are connected to the ground and those of PMOS transistors to the supply voltage. You should not connect your source and bulk terminals as this process will not allow you to do that.

This is a living document, i.e., it may be updated during the project timeline. You will be alerted if this document is altered in any way. If you have any questions, please do not hesitate to ask me or your TA. Also, please check your textbooks or other external resources to get more information about the two-stage operational amplifier design and/or simulation types and their setups to acquire desired performance metrics.

You will be graded based on your report. The report will be submitted on the due date. In the report, you should discuss how you achieved the design targets. The report should be no more than 6-7 pages, including the screenshots of AC and transient simulations, DC operating point analysis report, as well as the circuit schematic of your design with all the component parameters clearly visible. You should also submit your circuit simulation files via e-mail to your teaching assistant so that he can verify the results you mentioned in your reports.

Good luck!