ISTANBUL TECHNICAL UNIVERSITY

Faculty of Electrical and Electronics Engineering

Department of Electronics and Communication Engineering

Analog Electronic Circuits

Design and Analysis of a Two-Stage CMOS Amplifier

Term Project Report

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1) The Two-Stage CMOS Op Amp

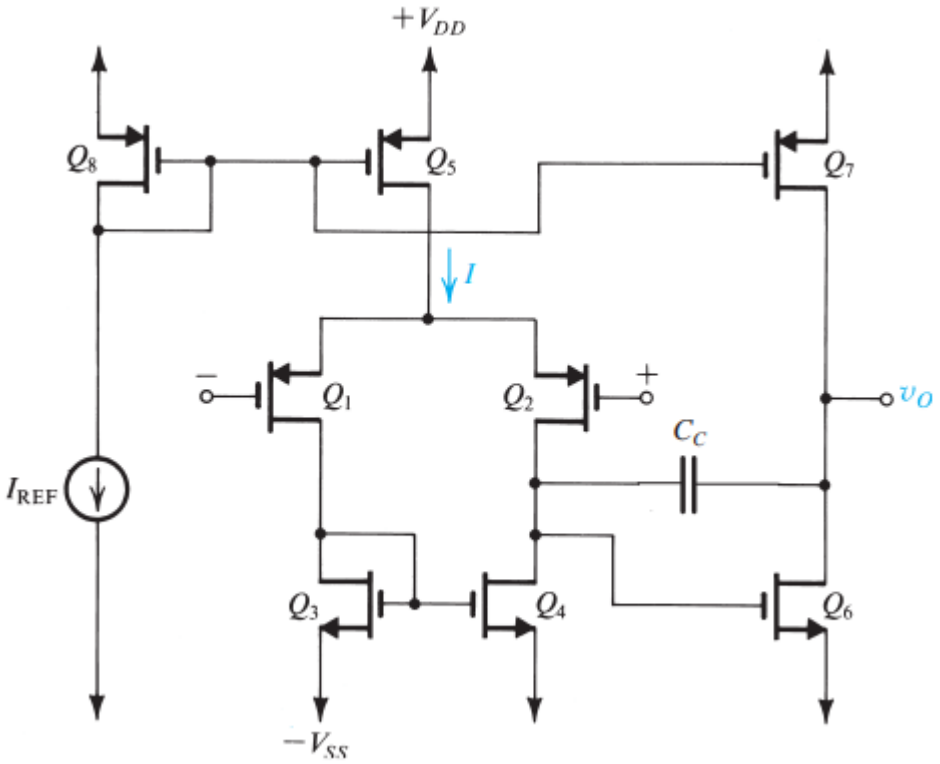


Figure 1. The Two-Stage CMOS Op Amplifier Circuit

This project focuses on the design and analysis of a two-stage operational amplifier, a fundamental component in analog circuit design widely used in various applications such as signal processing, data acquisition, and control systems. The two-stage topology provides high gain and wide output voltage swing, making it ideal for modern integrated circuits. The design incorporates a differential amplifier in the first stage for differential-to-single-ended conversion and a common-source amplifier in the second stage for additional gain. To ensure stability and achieve the desired phase margin, compensation techniques such as pole splitting are implemented using a compensation capacitor. This report outlines the circuit topology, design considerations, and performance analysis, emphasizing the importance of balancing gain, bandwidth, and stability in achieving an efficient operational amplifier design.

2) General voltage gain expressions:

$$A_1 = -G_{m1}R_1$$
$$= -g_{m1}(r_{o2} \| r_{o4})$$
$$= -\frac{2}{|V_{OV1}|} \Big/ \left[\frac{1}{|V_{A2}|} + \frac{1}{V_{A4}}\right]$$

$$A_2 = -G_{m2}R_2$$
$$= -g_{m6}(r_{o6} \| r_{o7})$$
$$= -\frac{2}{V_{OV6}} \Big/ \left[\frac{1}{V_{A6}} + \frac{1}{|V_{A7}|}\right]$$

$$A_v = A_1 A_2$$
$$= G_{m1}R_1 G_{m2}R_2$$
$$= g_{m1}(r_{o2} \| r_{o4}) g_{m6}(r_{o6} \| r_{o7})$$

3) Poles and Zeros Equations:

$$\omega_Z = \frac{G_{m2}}{C_C}$$

$$\omega_{P1} = \frac{1}{C_1R_1 + C_2R_2 + C_C(G_{m2}R_2R_1 + R_1 + R_2)}$$
$$= \frac{1}{R_1[C_1 + C_C(1 + G_{m2}R_2)] + R_2(C_2 + C_C)}$$

$$\omega_{P2} = \frac{G_{m2}C_C}{C_1C_2 + C_C(C_1 + C_2)}$$

4) Gain Analysis:

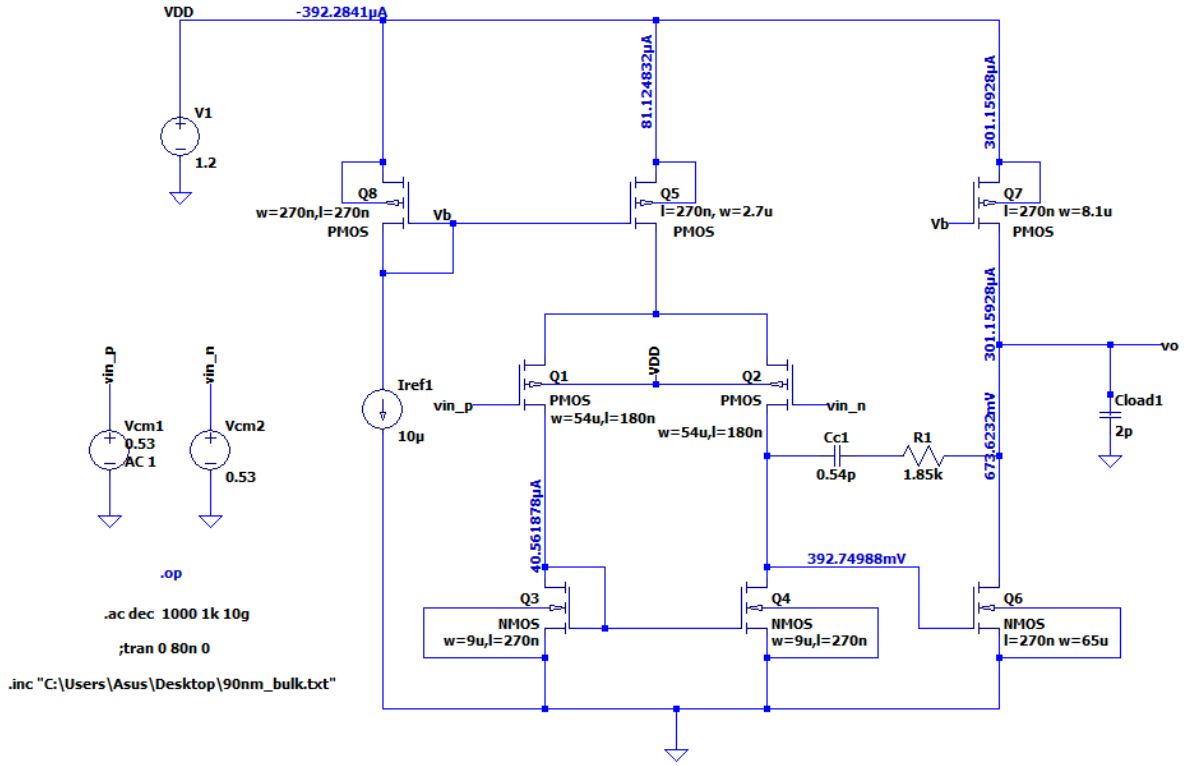


Figure2. Gain, Bandwidth and Phase Margin Circuit

Width/Channel-Lenght	Value
$\left(\frac{W}{L}\right)_1$	$\frac{54\mu}{180n}$
$\left(\frac{W}{L}\right)_2$	$\frac{54\mu}{180n}$
$\left(\frac{W}{L}\right)_3$	$\frac{9\mu}{270n}$
$\left(\frac{W}{L}\right)_4$	$\frac{9\mu}{270n}$
$\left(\frac{W}{L}\right)_5$	$\frac{2.7\mu}{270n}$
$\left(\frac{W}{L}\right)_6$	$\frac{65\mu}{270n}$
$\left(\frac{W}{L}\right)_7$	$\frac{8.1\mu}{270n}$
$\left(\frac{W}{L}\right)_8$	$\frac{270\mu}{270n}$

Figure 3. W/L Values of transistors

Component	Value
R1	1.85kΩ
Cc1	0.54pF
IREF	$10\mu A$
Vin	0.53V

Figure 4. Values of components

Figure 5. Gain Analysis Graph

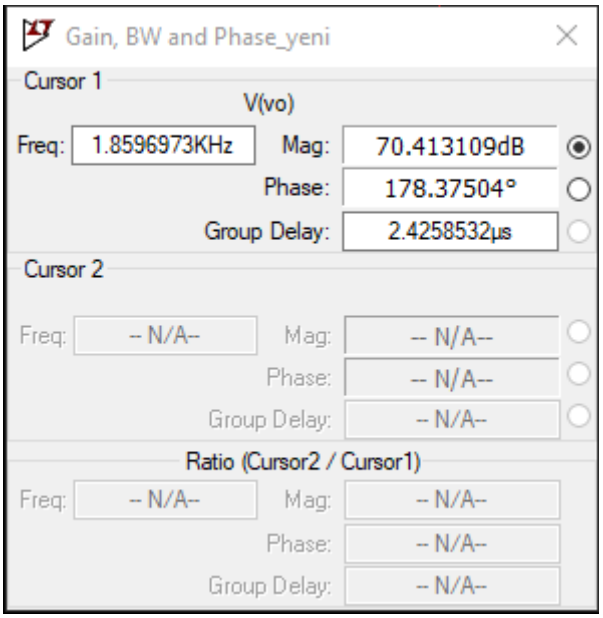


Figure 6. Gain graph values

Gain=70.41dB

5) -3dB Gain Analysis

Figure 7. -3dB Gain Analysis Graph

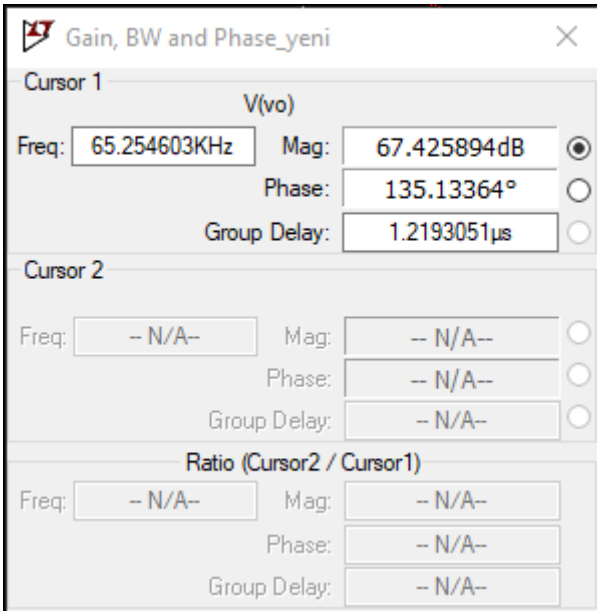


Figure 8. -3dB Gain Analysis parameters

-3 dB Gain = 67.42dB

-3 dB Bandwidth = 65.25 KHz

6) BandWidth and Phase Margin Analysis

Figure 9. Bandwidth and Phase Margin Analysis Graph

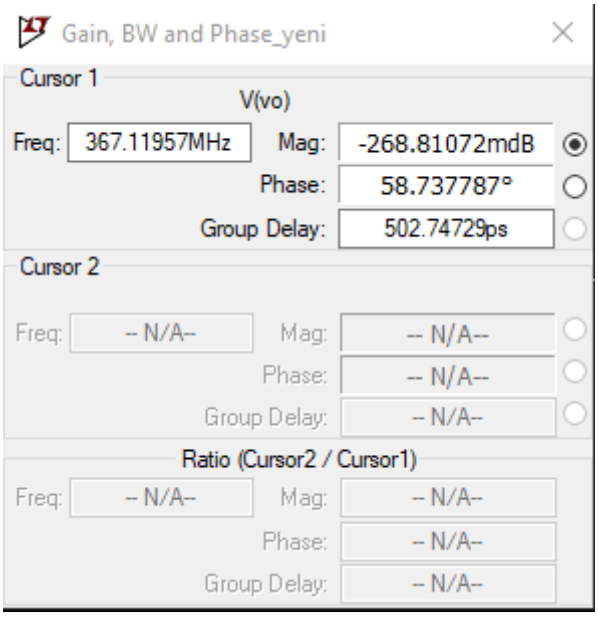


Figure 10. Bandwidth and Phase Margin Graph values

BandWidth = 367.12 MHz

Phase Margin = 58.74 degree

7) Settling Time

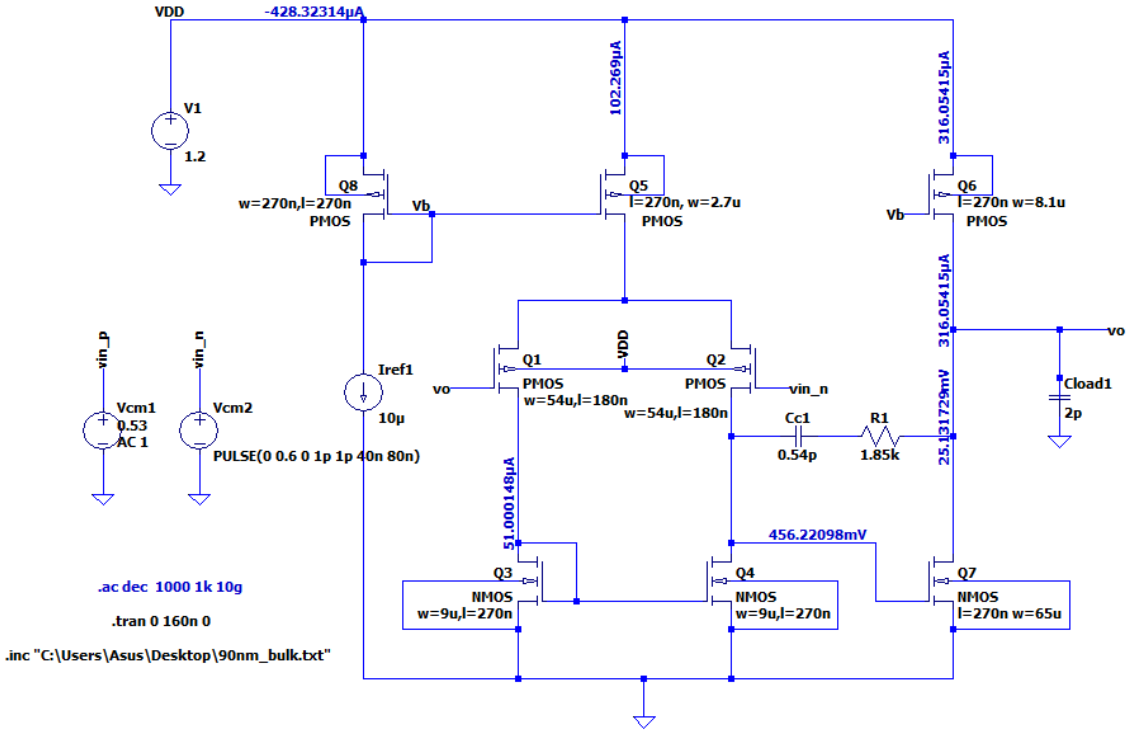


Figure 11. Settling Time Circuit

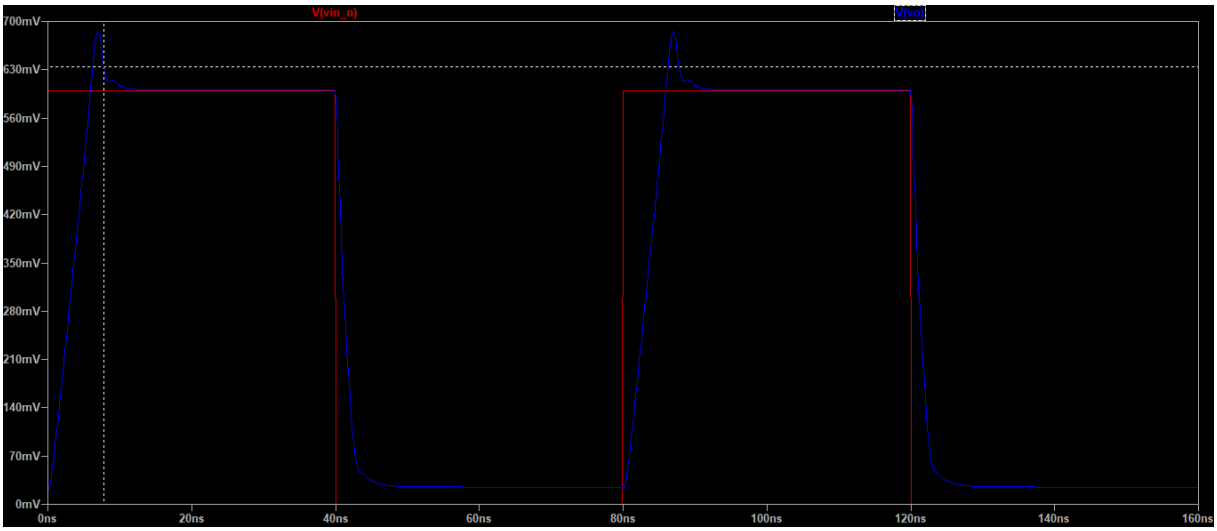
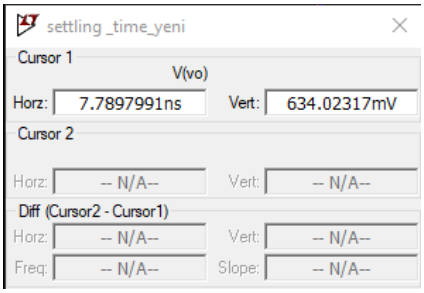


Figure 12. Settling Time Graph



Settling Time = 7.79 ns

Figure 13. Settling Time Graph values

8) FOM Calculation

Gain [dB]	70.41 [dB]
Bandwidth [Hz]	$65.25x10^3$ [Hz]
Settling Time [ns]	7.79 [ns]
Power [mW]	0.47 [mW]

$$\boldsymbol{F.O.M} = \frac{\text{Gain [dB]}\ x\ \text{Bandwidth [Hz]}}{\text{Settling Time [ns]}\ x\ \text{Power [mW]}} = \frac{\mathbf{70.41\ x\ 65.25\ x\ 10^3}}{\mathbf{7.79\ x\ 0.47}}$$

$$\boldsymbol{F.O.M = 1.255\ x\ 10^6}$$

9) Circuit Analysis and Explanation of Project Steps

- This circuit is a two-stage amplifier. The first stage is an active load differential pair, and the second stage is a common source amplifier.

First Stage: Differential Pair Circuit:

- Initially, to improve the current mirroring accuracy, the L values were selected as the highest available, which is 270 nm.
- The L (Length) values of Q1 and Q2 transistors were determined. The gmro value increases as Vov = Vgs – Vth decreases. Therefore, the L values of Q1 and Q2 were set to 180 nm.
- It was preferred to increase the W/L ratio since Vov could not be increased to increase the current and obtain the required current.
- owever, since the gain of the differential pair is not sufficiently high, a common source amplifier stage was added to the circuit.
- The other W/L ratios were optimized based on the aforementioned conditions.

Second Stage: Common Source Amplifier:

- The W/L ratios of Q6 and Q7 transistors were adjusted to ensure that they conduct the same current.

Phase Margin Issue and Solution:

- The phase margin value was found to be low. It was suspected that this might be due to the poles being too close to each other.
- To address this issue, the Miller compensation method, as learned in class, was applied. Using this method, the dominant pole was shifted to the left, separating the poles and increasing the phase margin.

Settling Time Improvement:

- For capacitors, according to the equation C=Q/V, the more electrons transferred, the faster the capacitor charges. Since electron movement is essentially current, increasing the current in that branch allows the load capacitor to charge more quickly.
- This reduces the **settling time** of the circuit.

10) Operating Points

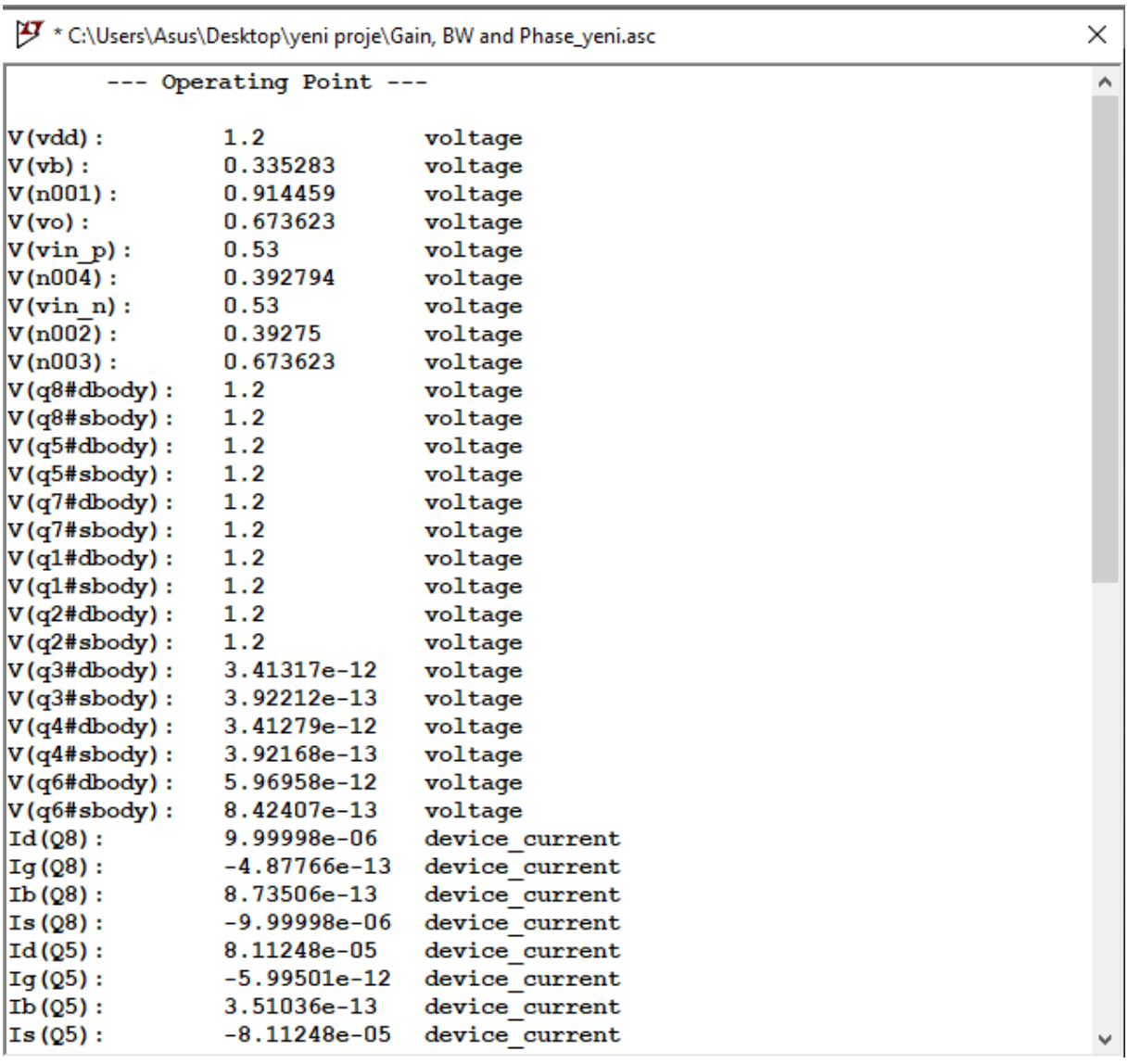


Figure 14. Operating point Values_1

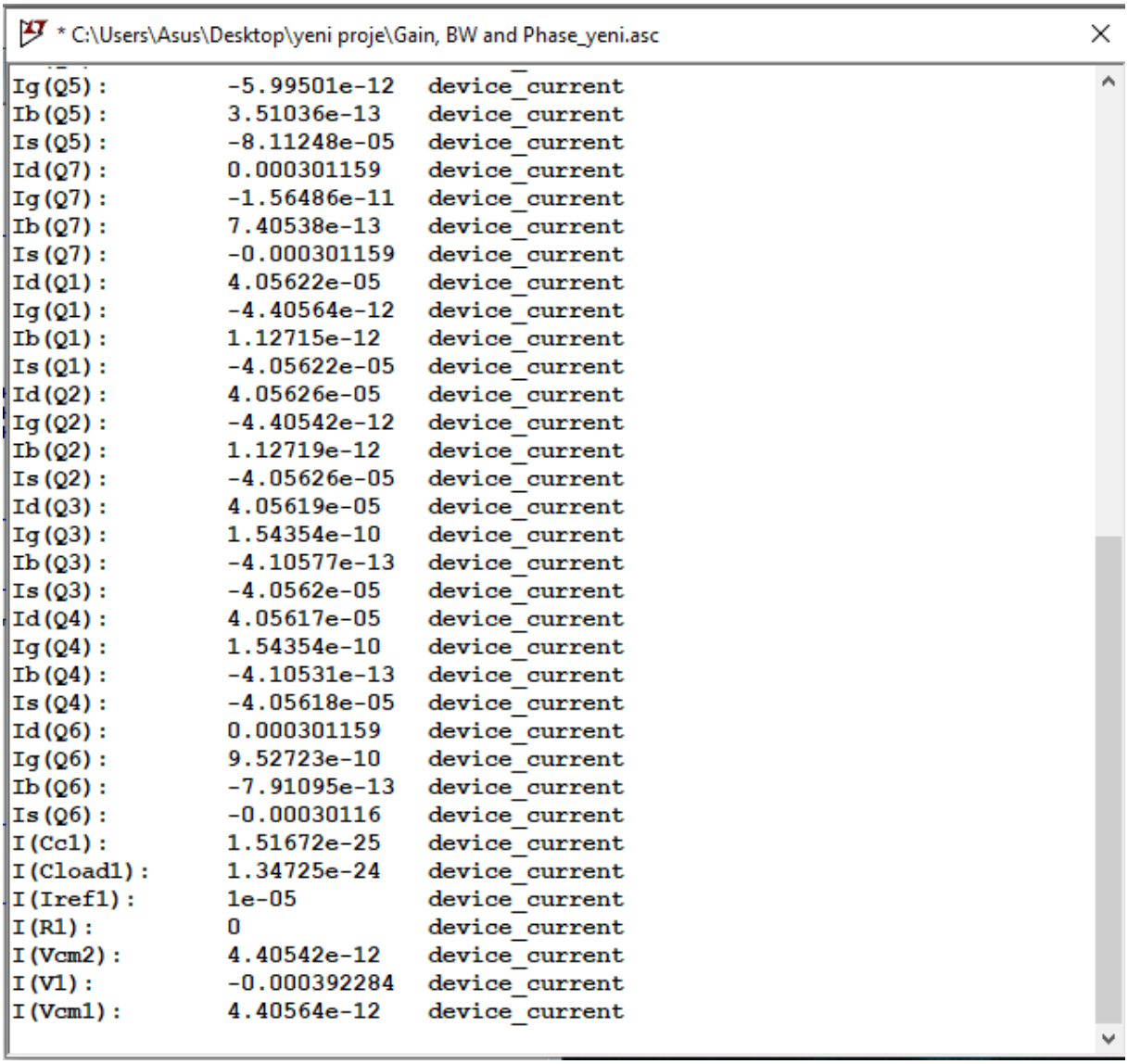


Figure 15. Operating point Values_2

11) References

S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. Oxford: Oxford University Press, 2015.

B. Razavi, *Fundamentals of Microelectronics*. 2nd ed., Hoboken, NJ, USA: Wiley, 2014.