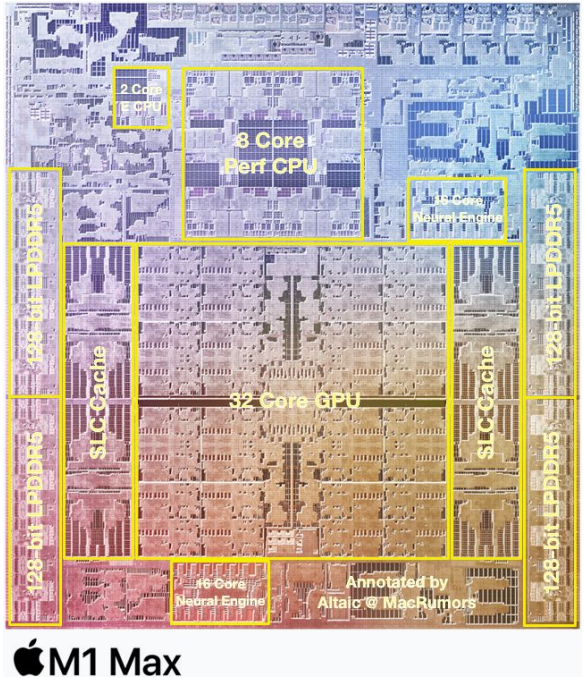
Access Control for Network-on-Chip (NoC) Architectures

Chi Chow | Brandon Erickson | Hosein Yavarzadeh

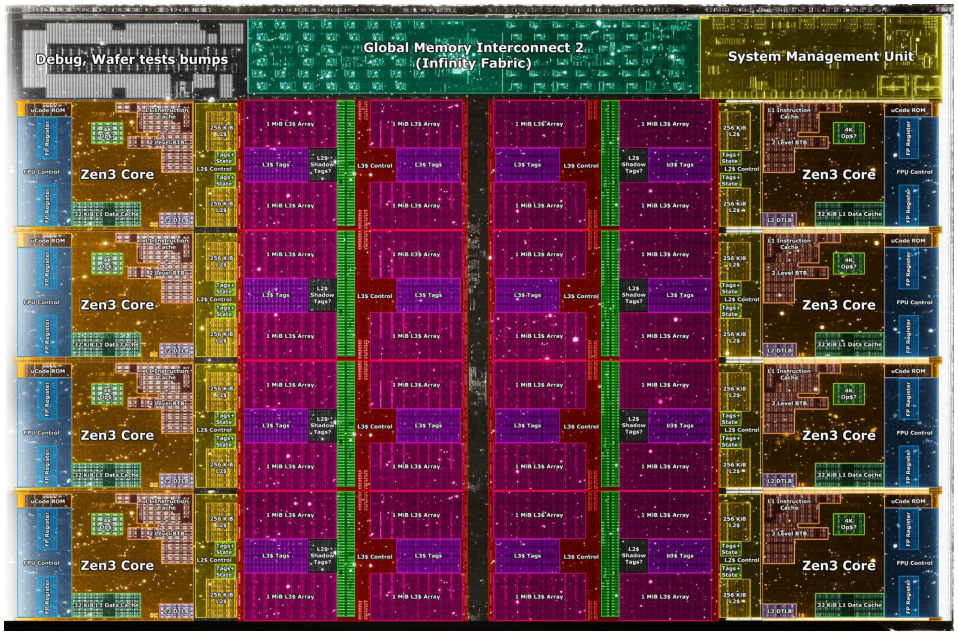
Oral Project Update - Spring 22

One More Time: SoCs and AKER's motivation

- **What is an SoC?**



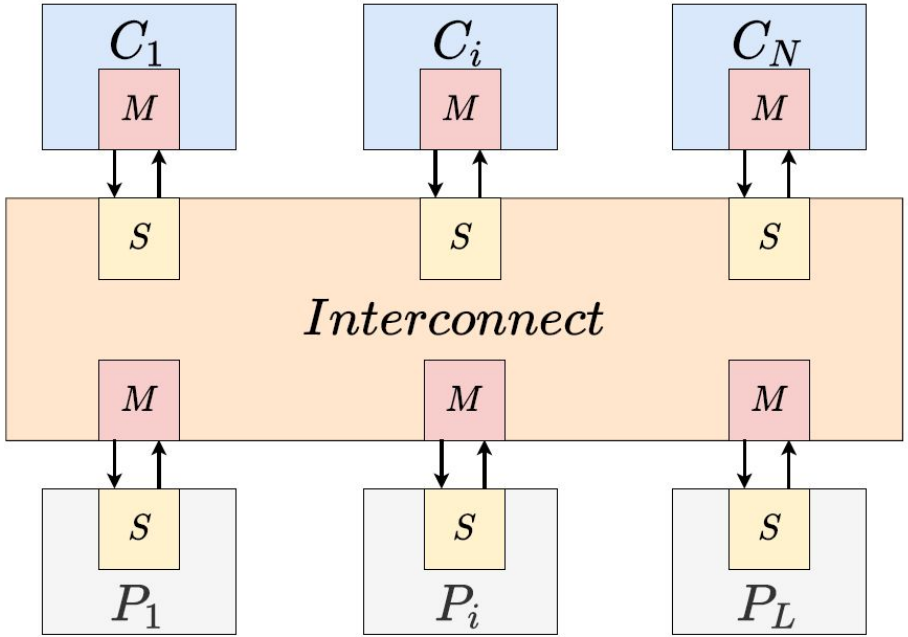
M1 Max



AMD Ryzen 5 5600X

One More Time: SoCs and AKER's motivation

- **Why AKER?**



Standardized Interconnect Architecture on an SoC (Network on a chip)

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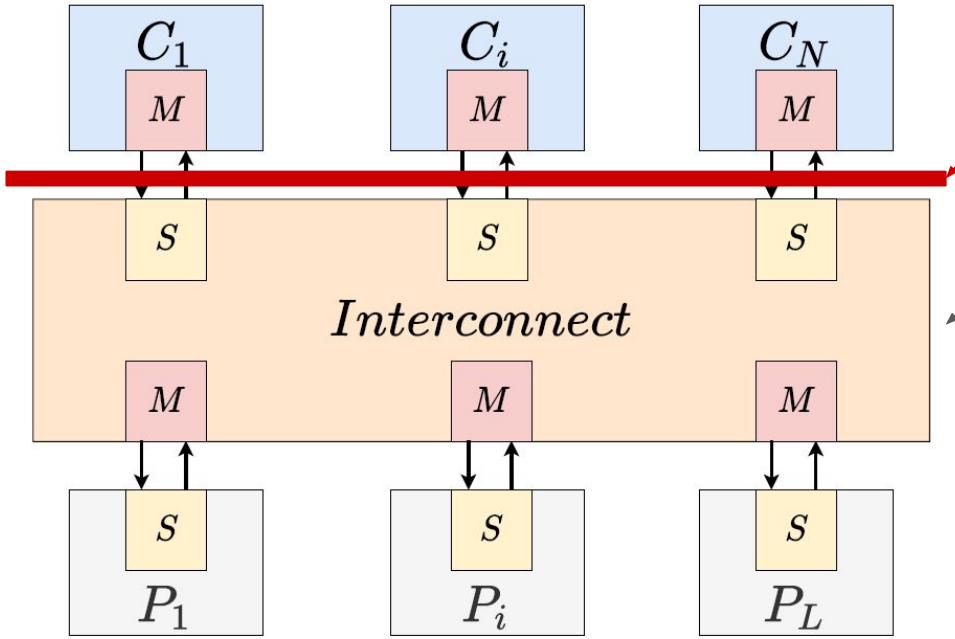

Access Control Black Magic

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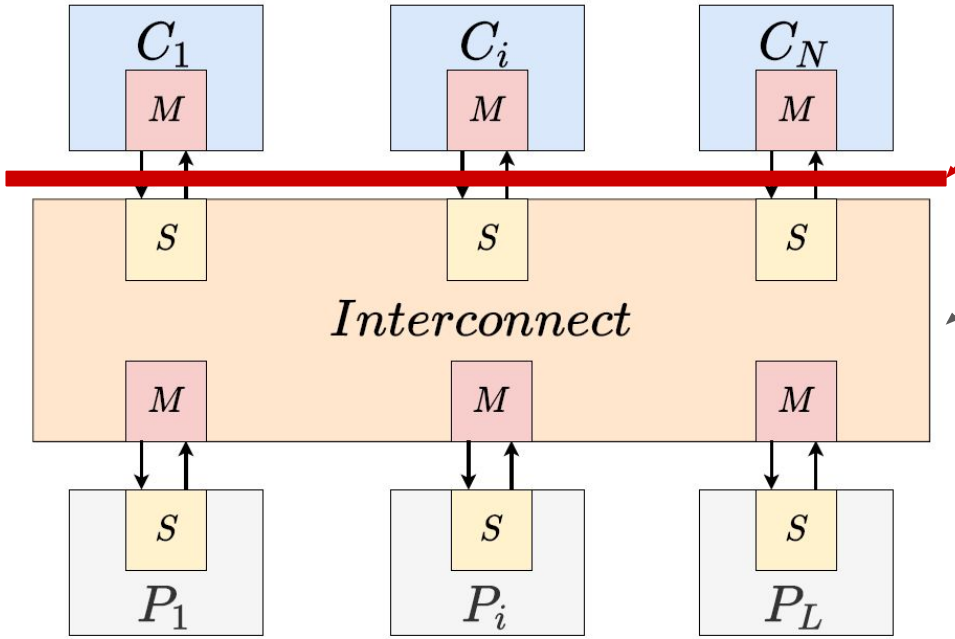


Access Control Black Magic

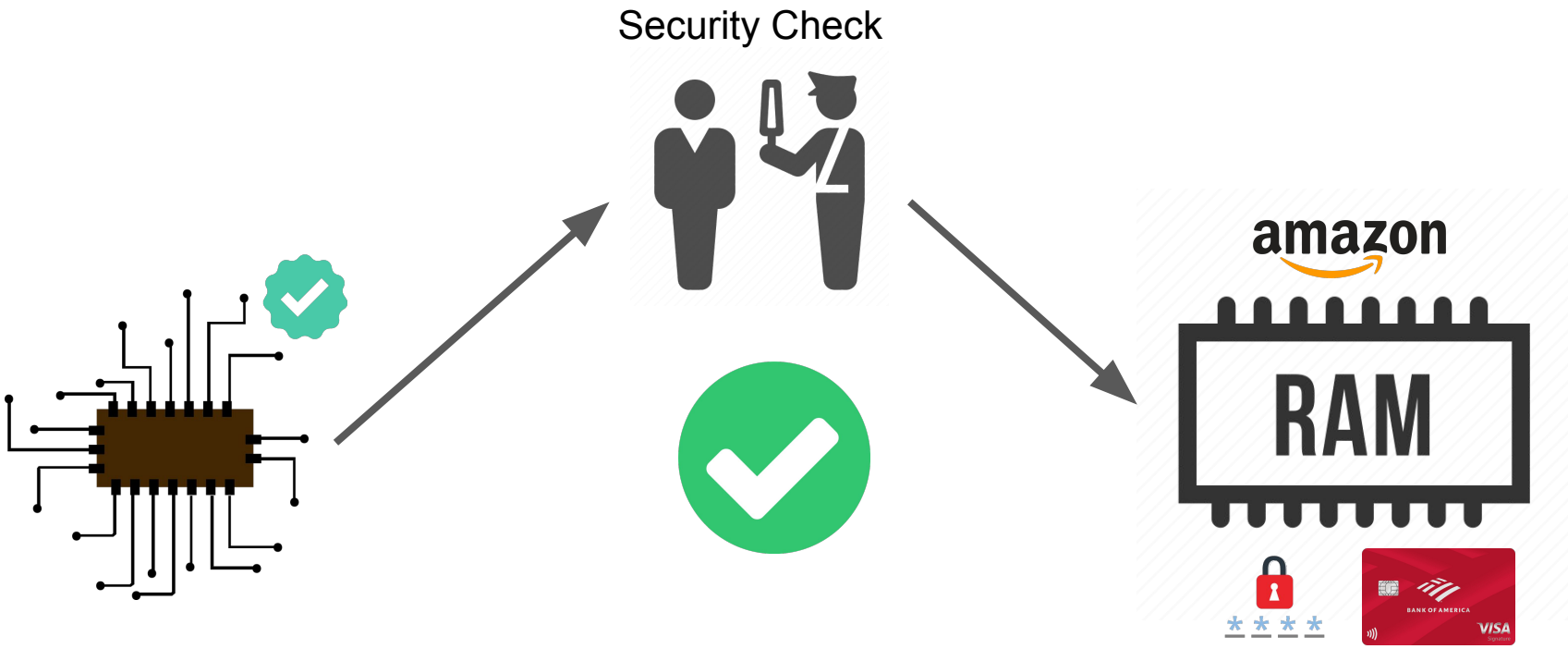
Standardized Interconnect Architecture on an SoC (Network on a chip)

Some Benefits:

- Interoperability
- Flexibility

Access Control System

Access Control System



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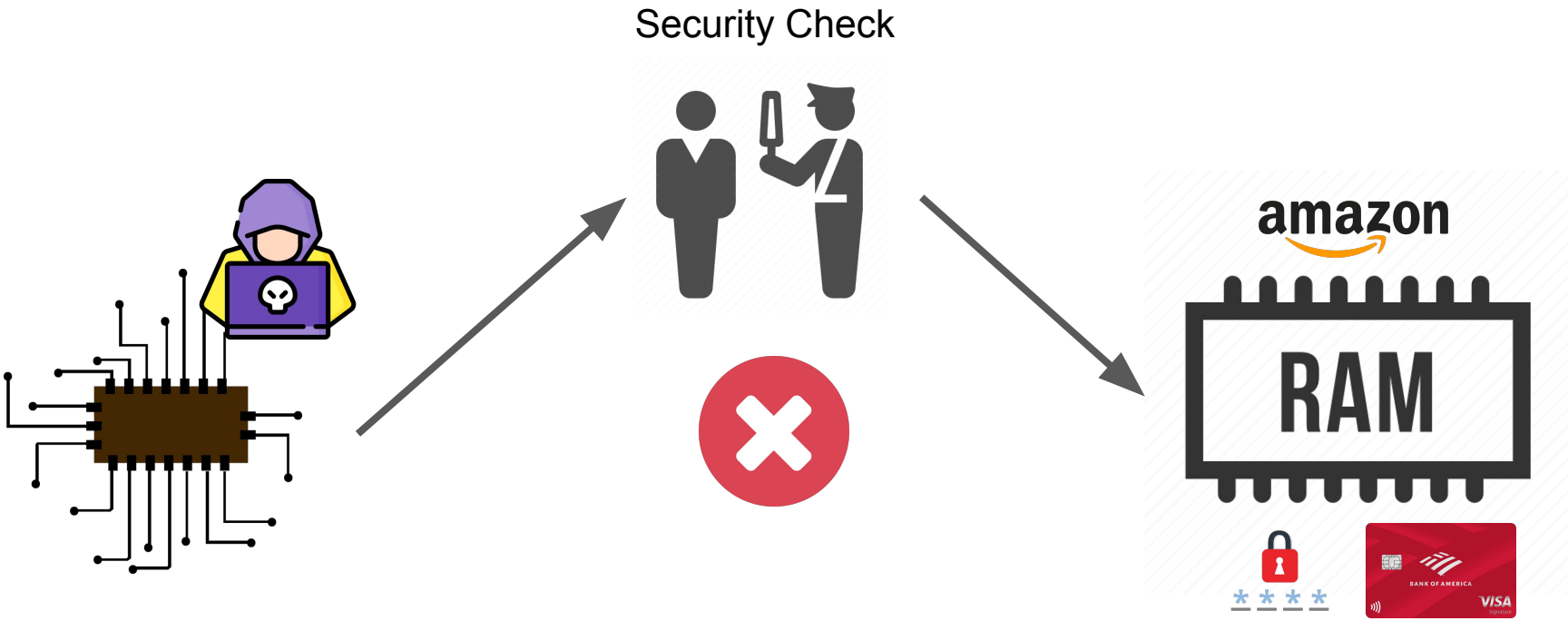

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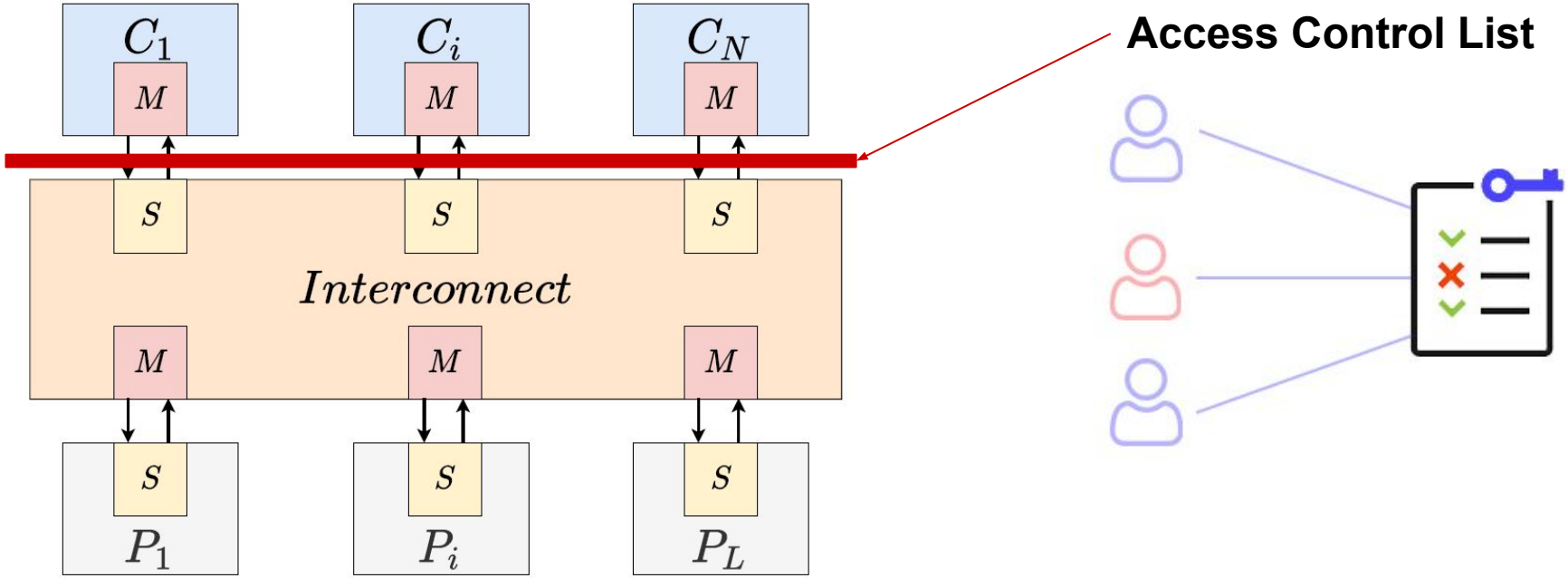
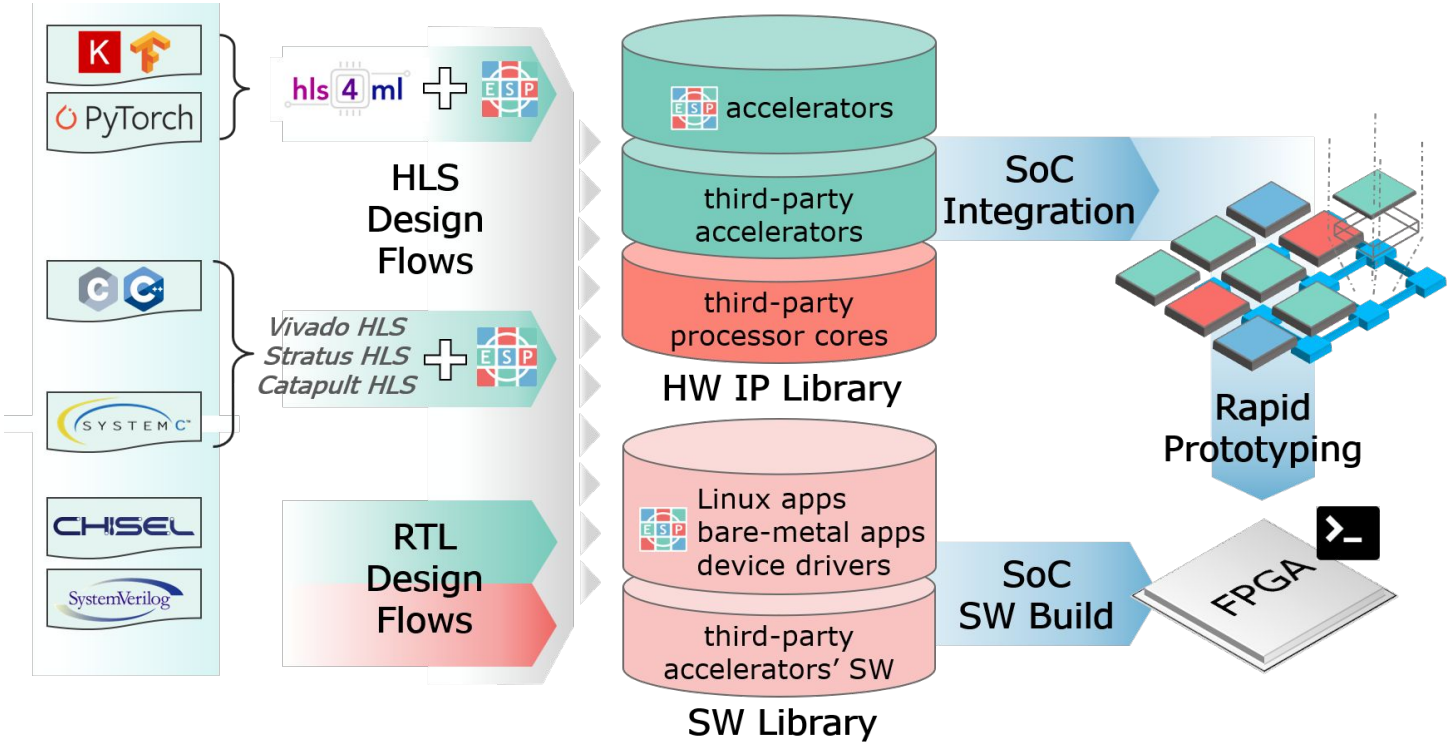
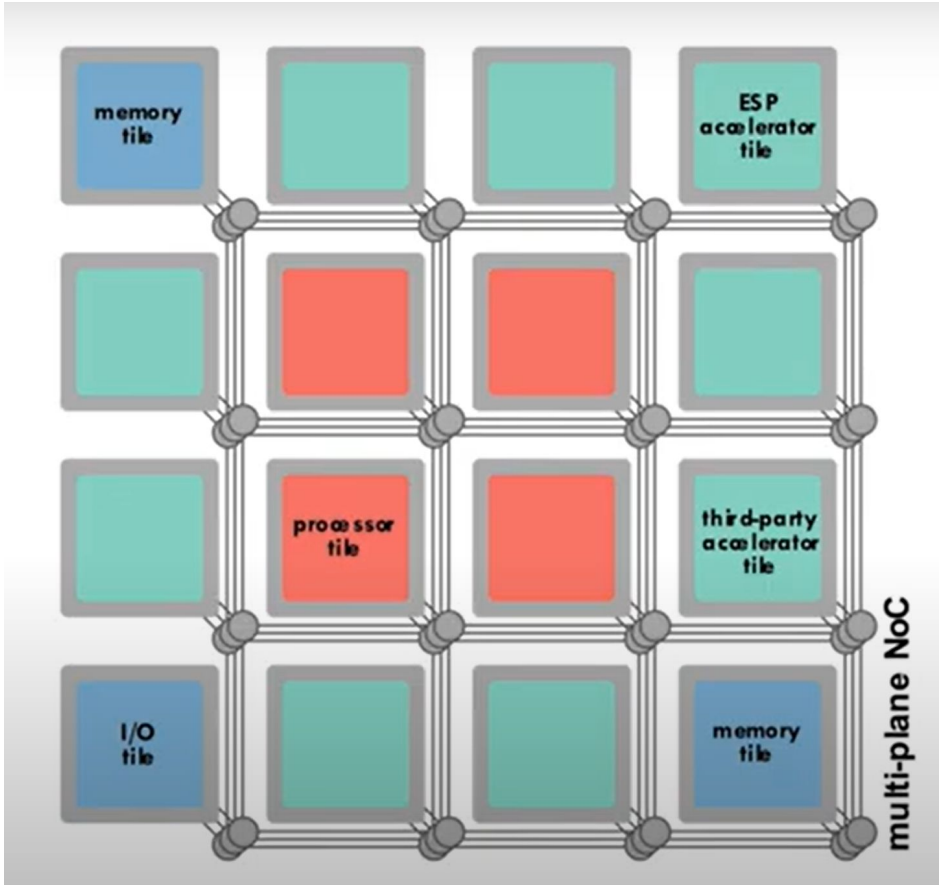


ESP: A Platform for Rapid SoC Development



AKER Integration in NoC

- AKER previously implemented for AMBA AXI interconnects
- ESP **tiles** interface with the network through **sockets**.
- **Goal: Adapt the AKER access control wrapper for socket compatibility.**



Timeline: Updates

<table>
<tr><th>Week</th><th>Goals</th><th>Deliverables</th></tr>
<tr><td>5</td><td rowspan="3">Implementation of AKER on the ESP platform
(C, C++, Verilog, etc.)
● Build target ESP architecture with NoC, routing protocol
● Develop compatible AKER access control module
● Integrate AKER + ESP platform</td><td></td></tr>
<tr><td>6</td><td></td></tr>
<tr><td>7</td><td rowspan="2">Milestone Update Presentation/Report (5/17)</td></tr>
<tr><td>8</td><td></td></tr>
<tr><td>9</td><td rowspan="2">Testing and Validation</td><td></td></tr>
<tr><td>10</td><td>Final Video and Report (week of 6/5)</td></tr>
</table>

Summary

Progress So Far

- Better understanding of the problem after research
- Consolidate our implementation goals
- Project setup

TODOs

- Complete analysis of the ESP codebase
- Implementation of the Access Control Wrapper