Access Control for Network-on-Chip (NoC) Architectures

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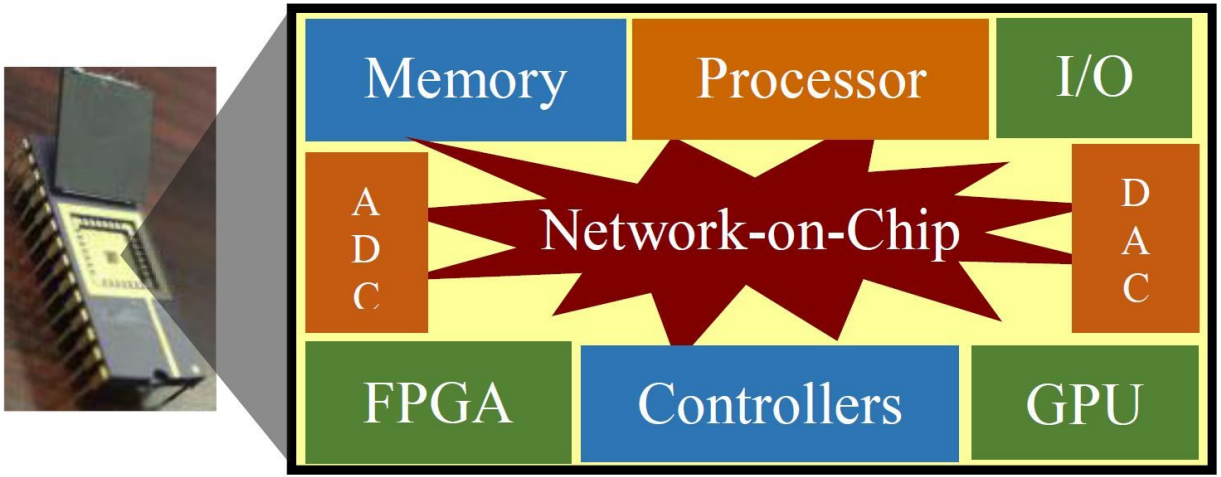
Project Overview - Spring 22

Background: SoC

Modern System on a Chip (SoC) have heterogeneous architectures comprised of:

Microprocessors, Hardware Accelerators, on-Chip Memory Hierarchies, and I/O.

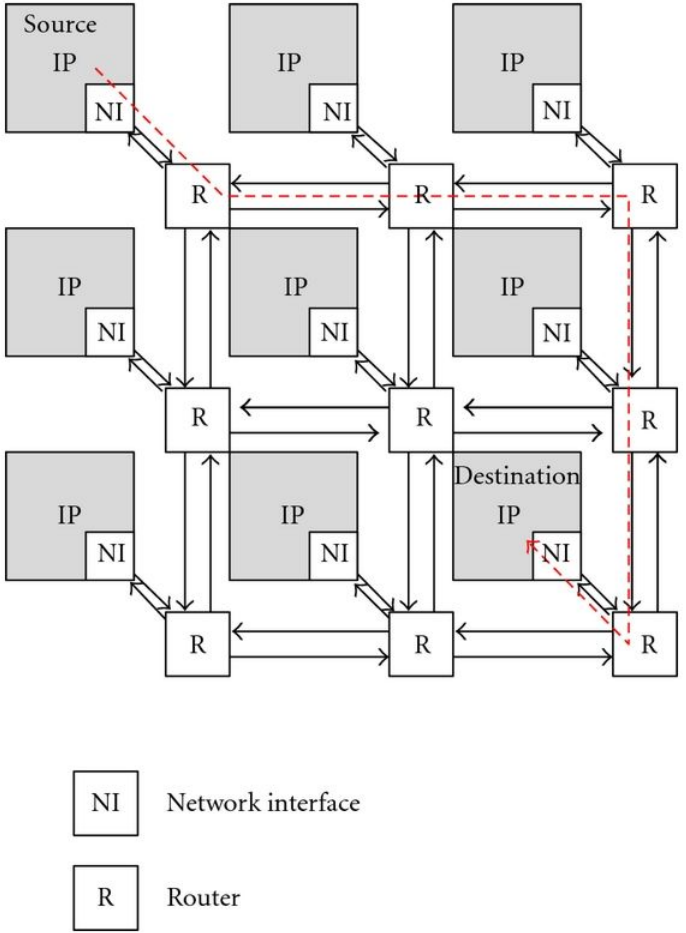


NoC

Network-on-Chip is:

A network-based communications subsystem on an integrated circuit.

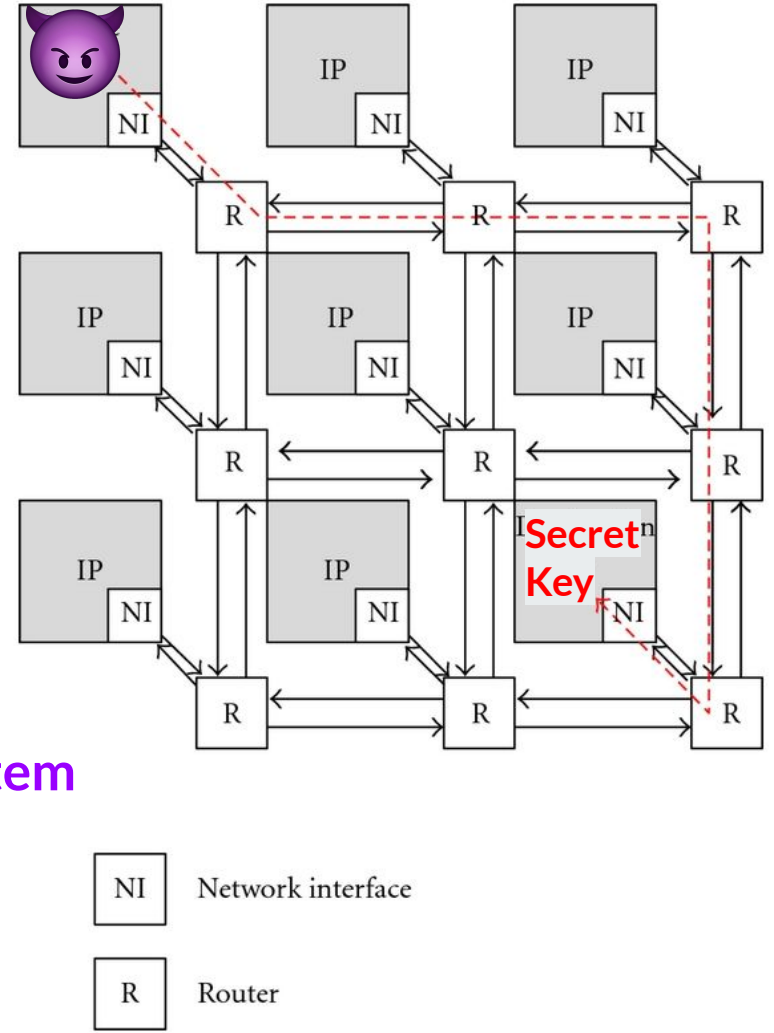
(most typically between modules in a SoC)



What is the problem?

Concurrent access to on-chip shared resources.

IP cores have different privilege levels for accessing shared resources.



MUST be regulated by an access control system

AKER: A Design and Verification Framework for Safe and Secure SoC Access Control

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Figure 1

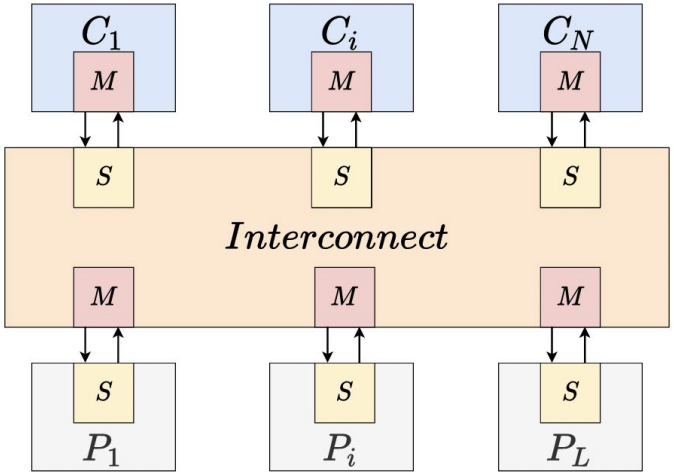
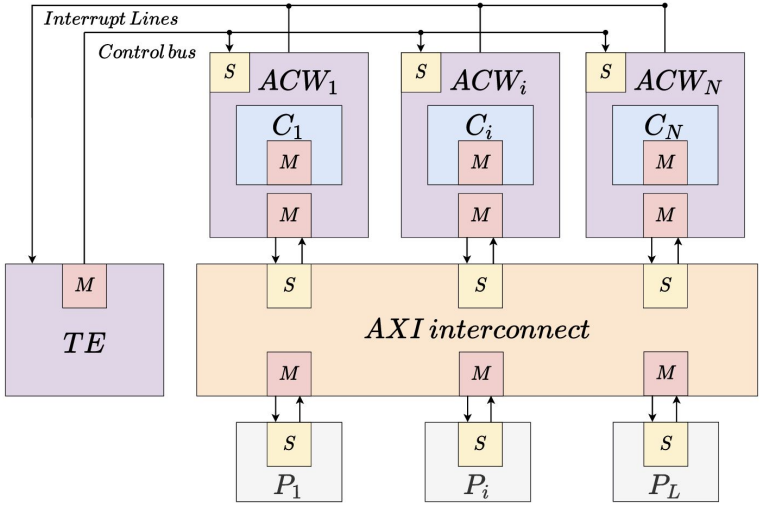
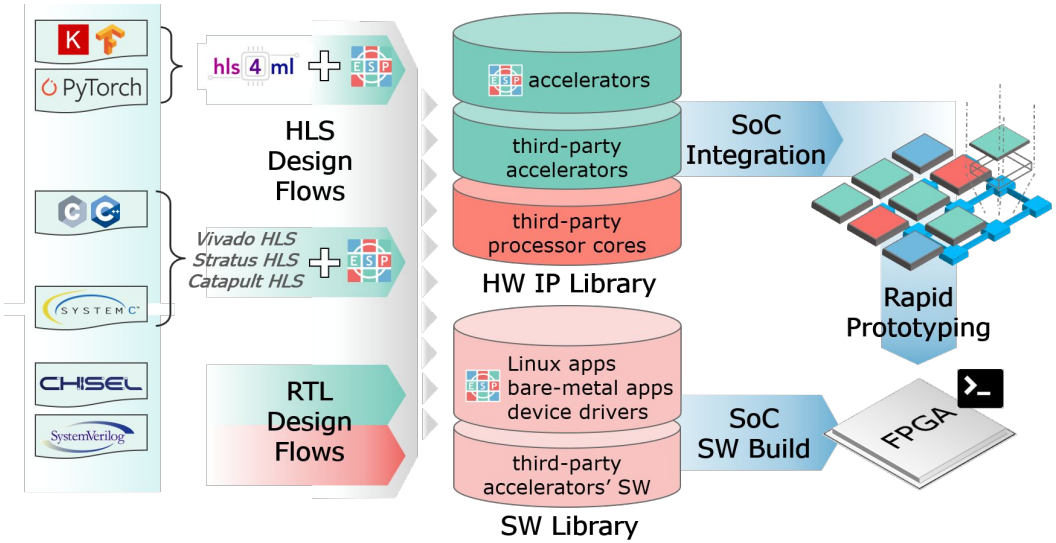


Figure 2



What is the goal of this project?

Integration of an AKER access control system into the ESP platform



Timeline

Week	Goals	Deliverables
3 4	Research ESP, NoC, AKER, Communication protocols, Internals of the NoC router, Project setup with ESP, documentation	Design Specification (4/19), ESP Architectural Analysis
5 6	Implementation of AKER on the ESP platform (C, C++, Verilog, etc.) ● Build target ESP architecture with NoC, routing protocol ● Develop compatible AKER access control module ● Integrate AKER + ESP platform	
7 8		Milestone Update Presentation/Report (5/17)
9 10	Testing and Validation	 Final Video and Report (week of 6/5)