

**Trinity College Dublin**

Coláiste na Tríonóide, Baile Átha Cliath

The University of Dublin

3C7 DIGITAL SYSTEMS DESIGN LABORATORY

Department of Electronic and Electrical Engineering

Assignment 1: MINI ALU

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Question:

MINI ARITHMETIC LOGIC UNIT (MINI-ALU)

You need to **design, write/modify** the Verilog modules for the following functions, and test a “mini” arithmetic logic unit. An **arithmetic logic unit (ALU)** uses combinatorial logic to implement common arithmetic and logical functions. A typical ALU has a wide range of functionality from **addition to bit shifting**. Your ALU will provide a **narrow range of functions** performed on **two 6-bit inputs A and B**. A and B are in **2's complement format**. The **output of the ALU is a 6-bit number X**, also in **2's complement** form as appropriate, and the input **fxn** controls the output as follows:

fxn	X[5:0]
000	A
001	B
010	-A
011	-B
100	A<B (is A less than B)
101	(A <i>nxor</i> B) (Bitwise XNOR)
110	A+B
111	A-B

IMPLEMENTATION:

The aim of the assignment was to design a Mini Arithmetic Logical Unit. The ALU takes in two 6-bit numbers as inputs, a 3-bit input for functionality (add, subtract, comparison, etc.) and outputs a 6-bit number depending upon the functionality. We were supposed to re-use our blocks of code from the previous labs such as the ripple carry adder and the comparator and use them as building blocks for the ALU.

The implementation of the mini ALU is done on the basys 3 board by using different modules in this assignment.

DESIGN STRATEGY :

1. Fxn = 000 (A)

For the above function, the expected output was the first input. I made use of a ripple carry adder to implement this. I passed in the first input and I passed the second input as 0. The functionality selected was addition. ($A + 0 = A$).

2. Fxn = 001 (B)

For the above function, the expected output was the second input. I made use of a ripple carry adder to implement this. I passed in the first input as 0 and the second input B. The functionality selected was addition. ($0 + B = B$).

3. Fxn = 010 (-A)

For the above function, the expected output was negation of the first input. I made use of a 2's complement module to implement this. It inverts all bits of the input and then adds 1 to the LSB of the inverted number and hence, gives the expected output.

4. Fxn = 011 (-B)

For the above function, the expected output was negation of the second input. I made use of a 2's complement module to implement this. It inverts all bits of the input and then adds 1 to the LSB of the inverted number and hence, gives the expected output.

5. Fxn = 100 (A<B) (This function does not run and gives an error)

For the above function, the expected output was supposed to be high when the condition $A < B$ was true. I made use of a 1-bit comparator as a building block for the 6-bit comparator. The 1-bit comparator asserts 1 if the first input is less than the second input.

6. Fxn = 101 (A xnor B)

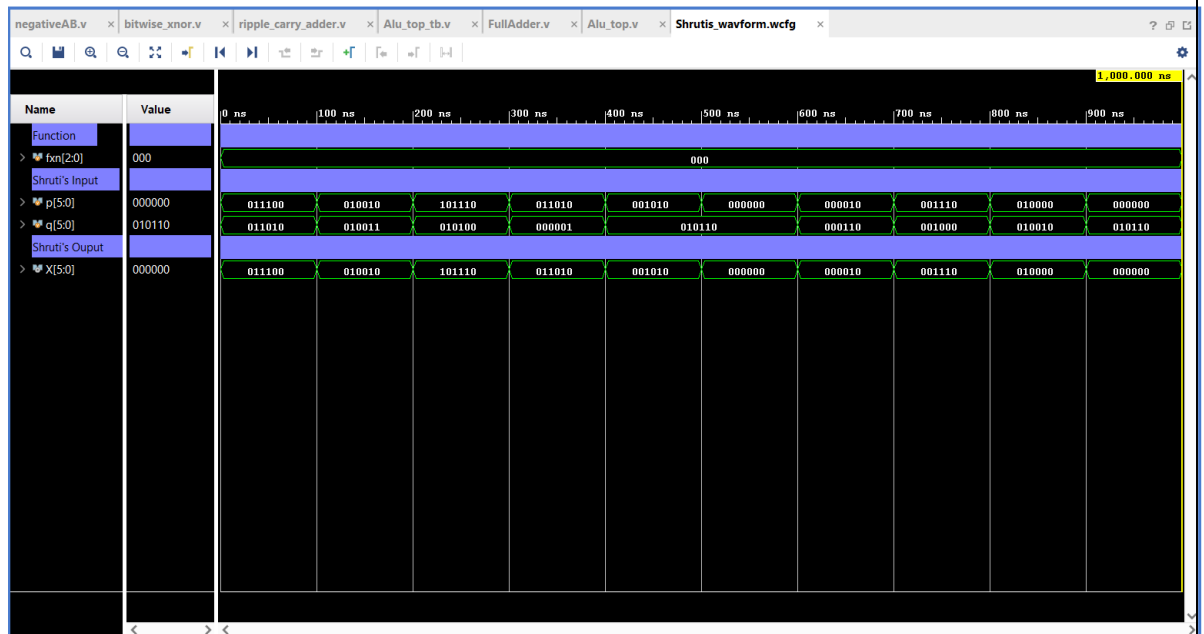
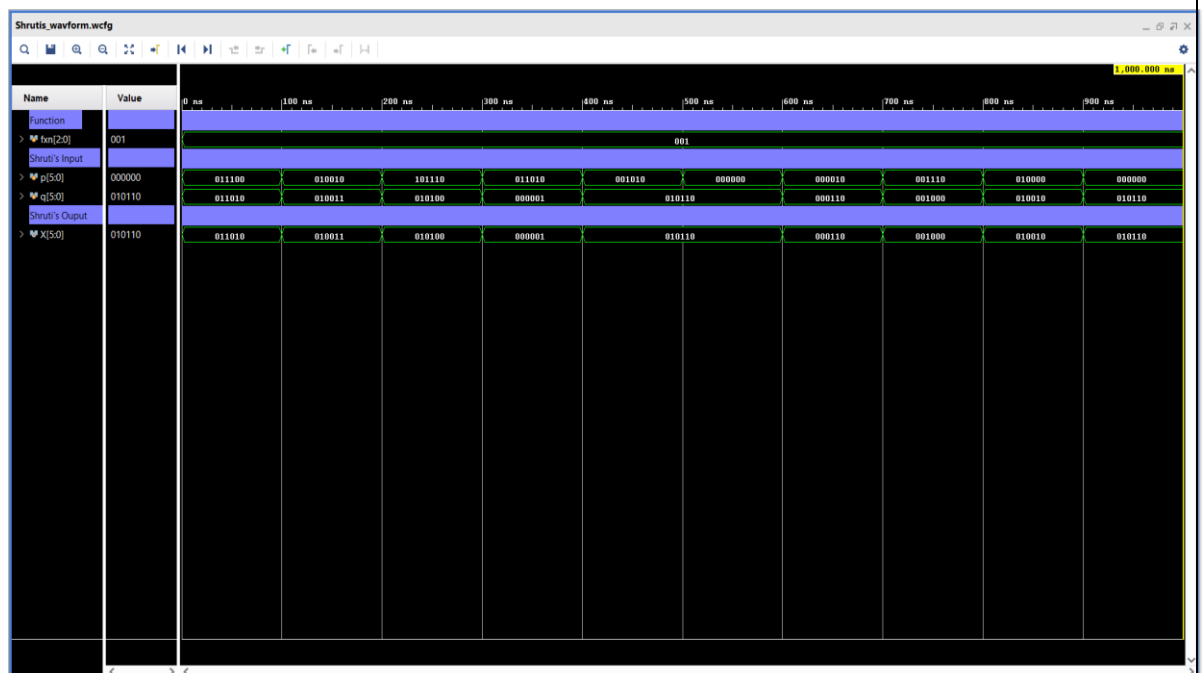
For the above function, the expected output was the bitwise xnor of the inputs. I made use of a 6-bit bitwise xnor module for this.

7. Fxn = 110 (A+B)

For the above function, the expected output was the sum of the inputs. I made use of the modules full adder and ripple carry adder/subtractor for this to implement this. The inputs were passed, and the function selected was 0 (sel=0, addition) when the ripple carry adder/subtractor module was instantiated.

8. Fxn = 111 (A-B)

For the above function, the expected output was the difference of the inputs. I made use of the modules full adder and ripple carry adder/subtractor for this to implement this. The inputs were passed, and the function selected was 1 (sel=1, subtraction) when the ripple carry adder/subtractor module was instantiated.

SIMULATIONS:**Fig: Fxn = b'000(Waveform for p=x)****Fig: Fxn = b'001 (Waveform for q=x)**

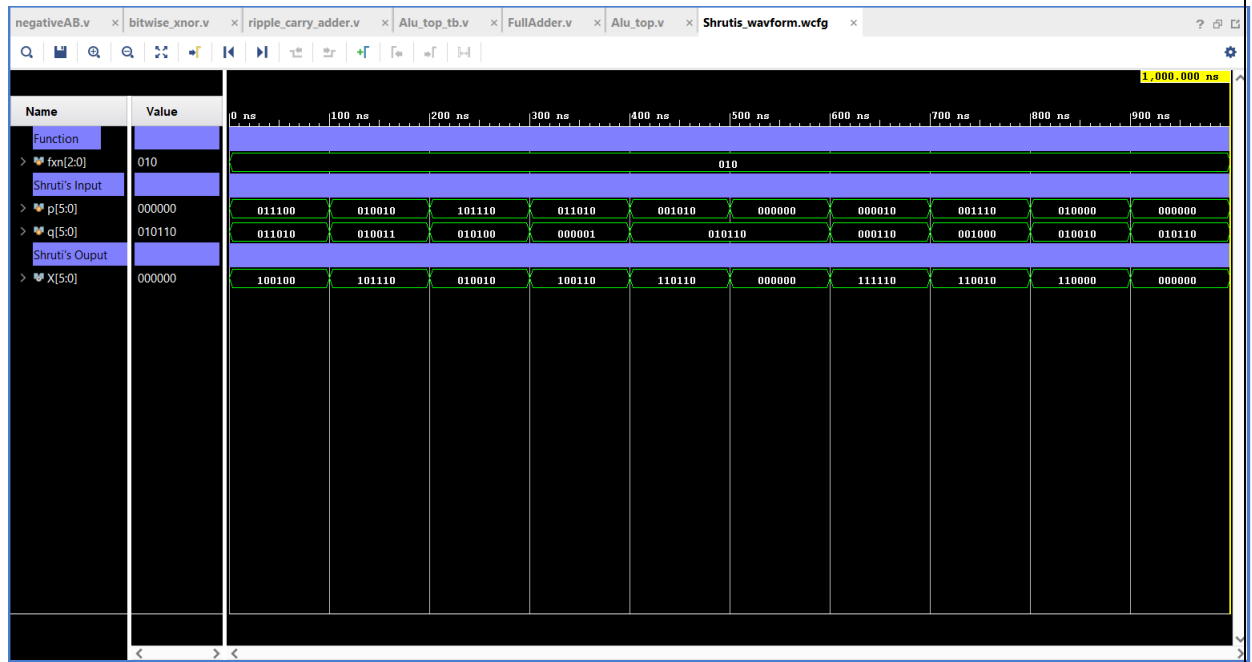


Fig: Fxn = b'010 (Waveform for -p=x)



Fig: Fxn = b'011 (Waveform for -q=x)



Fig: Fxn = b'101(Waveform for pxnorq)

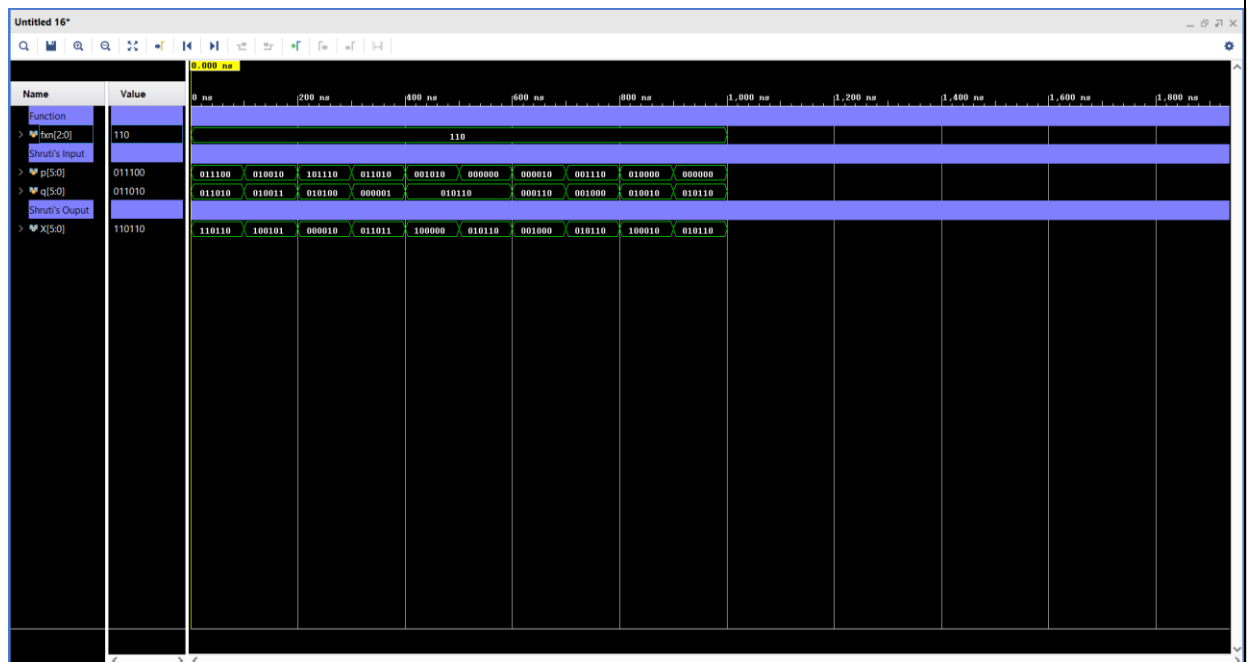


Fig: Fxn = b'110(Waveform for Addition)

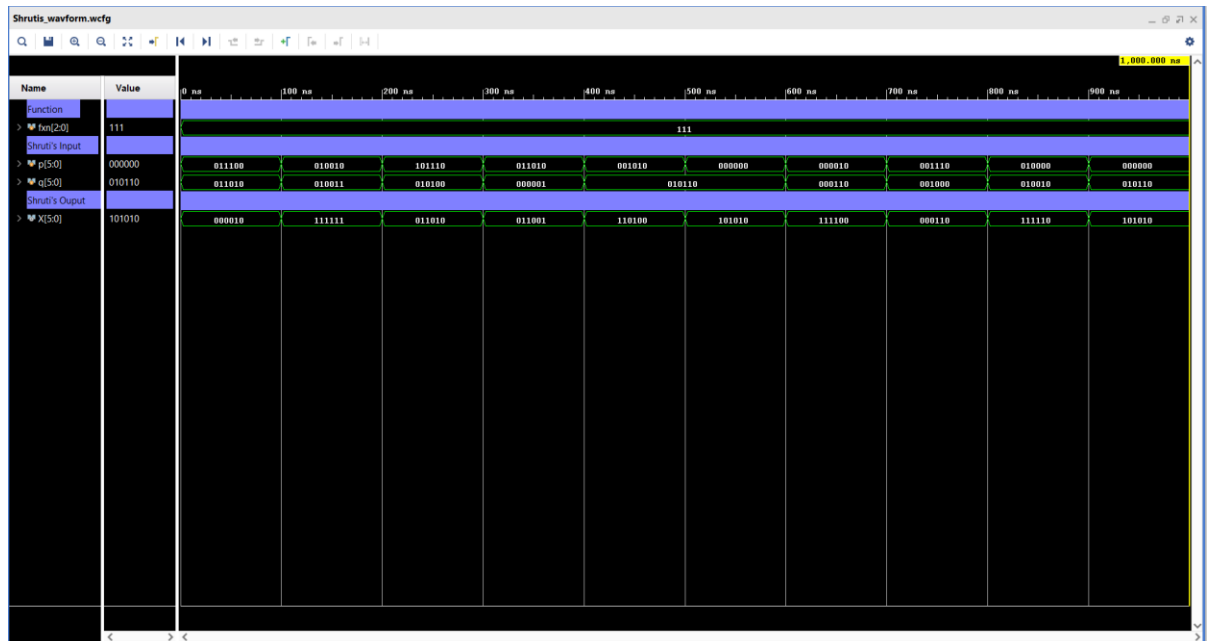


Fig: Fxn = $b'111$ (Waveform for Subtraction)

SOURCES:

The modules that I have used for the implementation of the project are as follows:

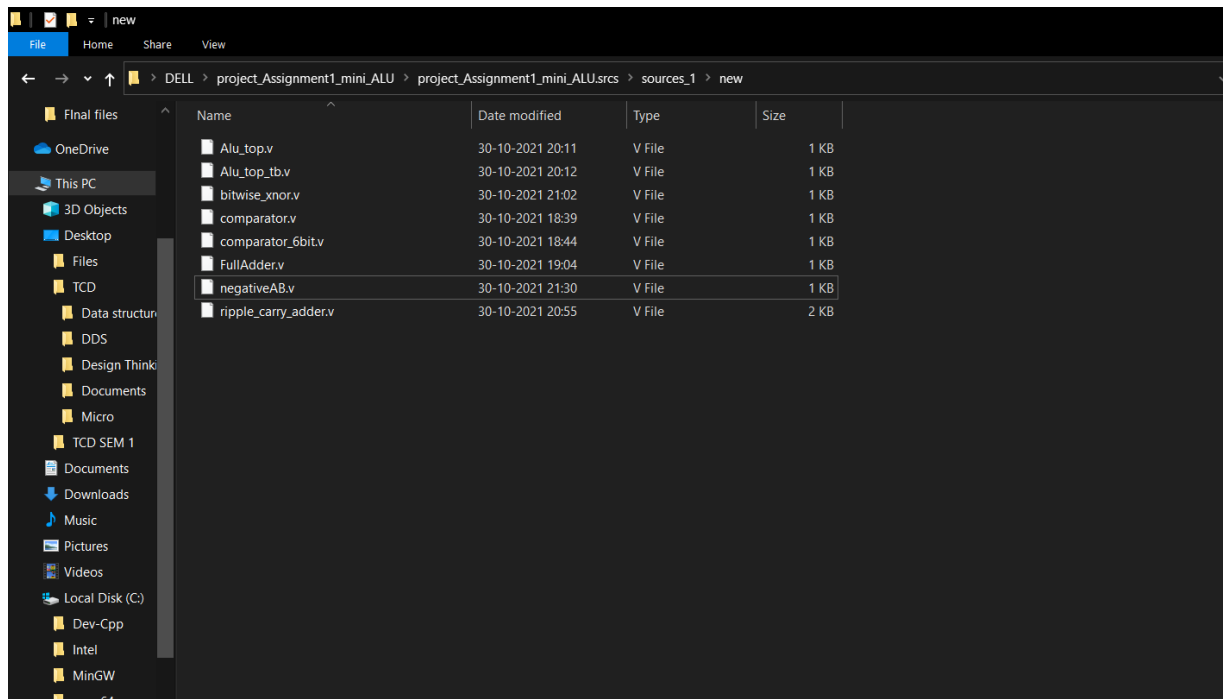


Fig: Directory with the sources in it

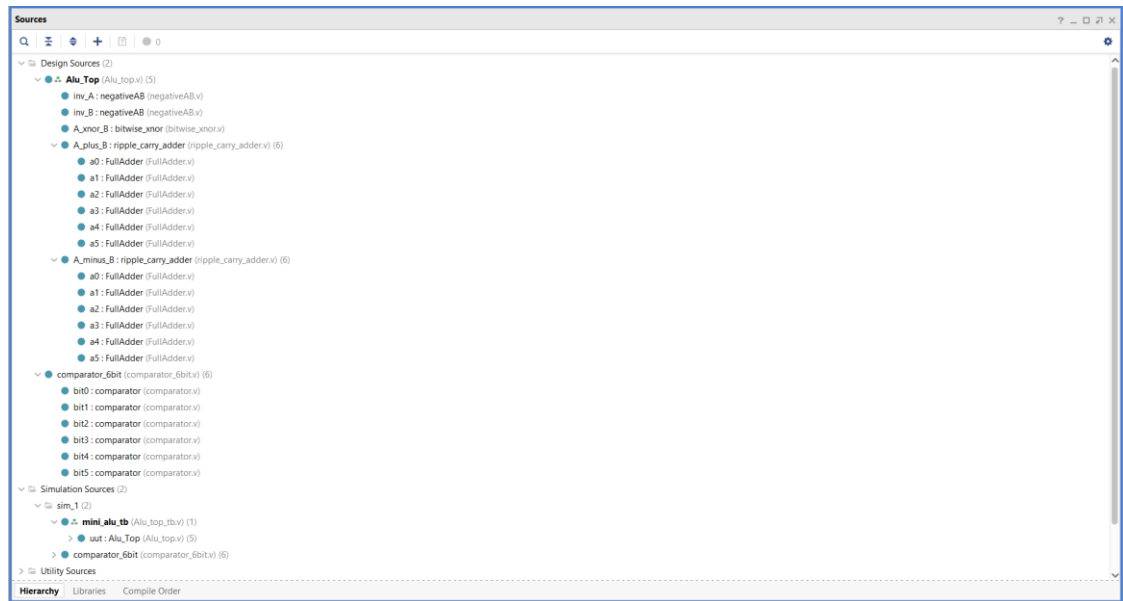


Fig: Design Sources(Hierarchy of the design)

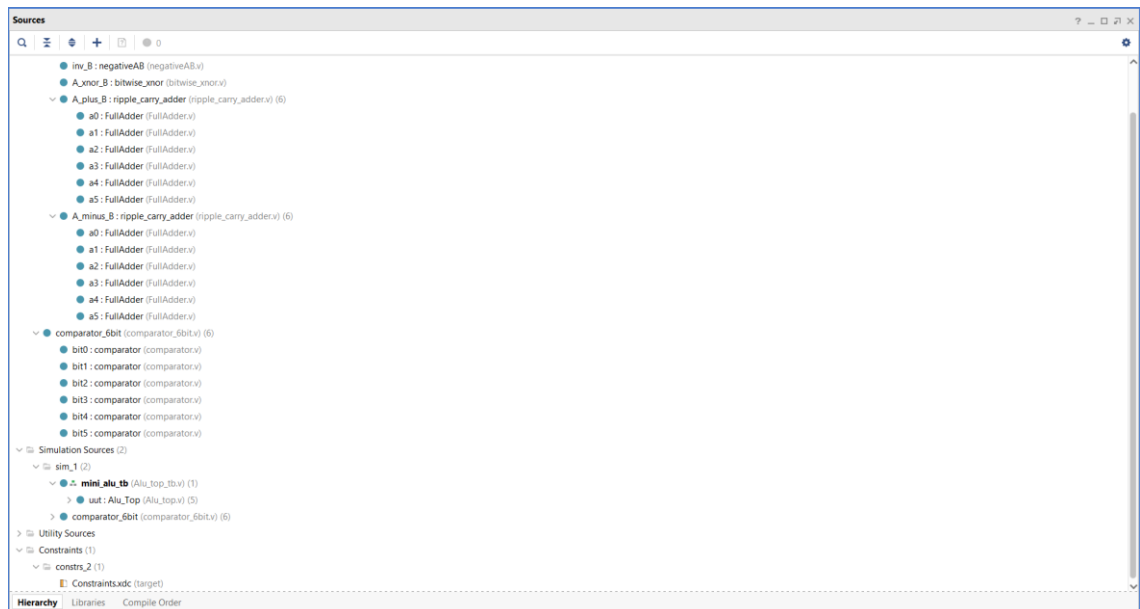
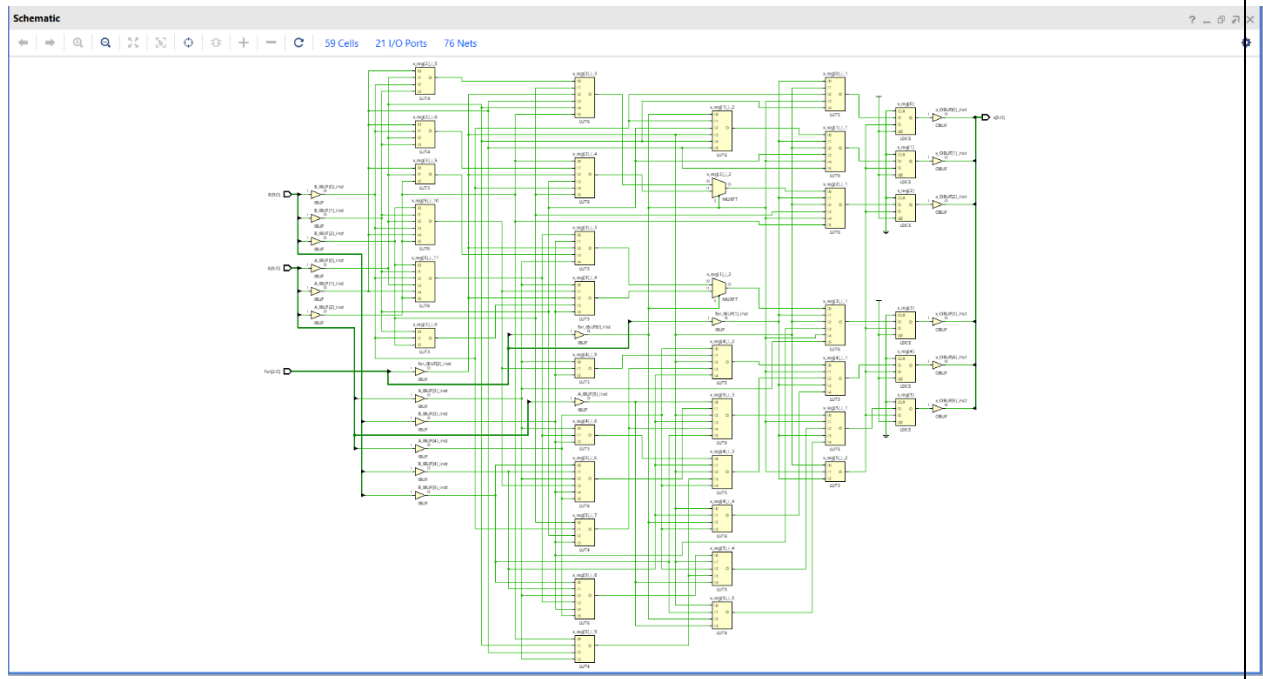


Fig: Design Sources

Scope		
Sources		
Name	Design Unit	Block Type
mini_alu_tb	mini_alu_tb	Verilog Module
uut	Alu_Top	Verilog Module
inv_A	negativeAB	Verilog Module
inv_B	negativeAB	Verilog Module
A_x...	bitwise_xor	Verilog Module
A_p...	ripple_carry_adder	Verilog Module
A_...	ripple_carry_adder	Verilog Module
gbl	gbl	Verilog Module

Fig:Sources

SCHEMATICS:**Fig: Elaborated design****Fig: Package**

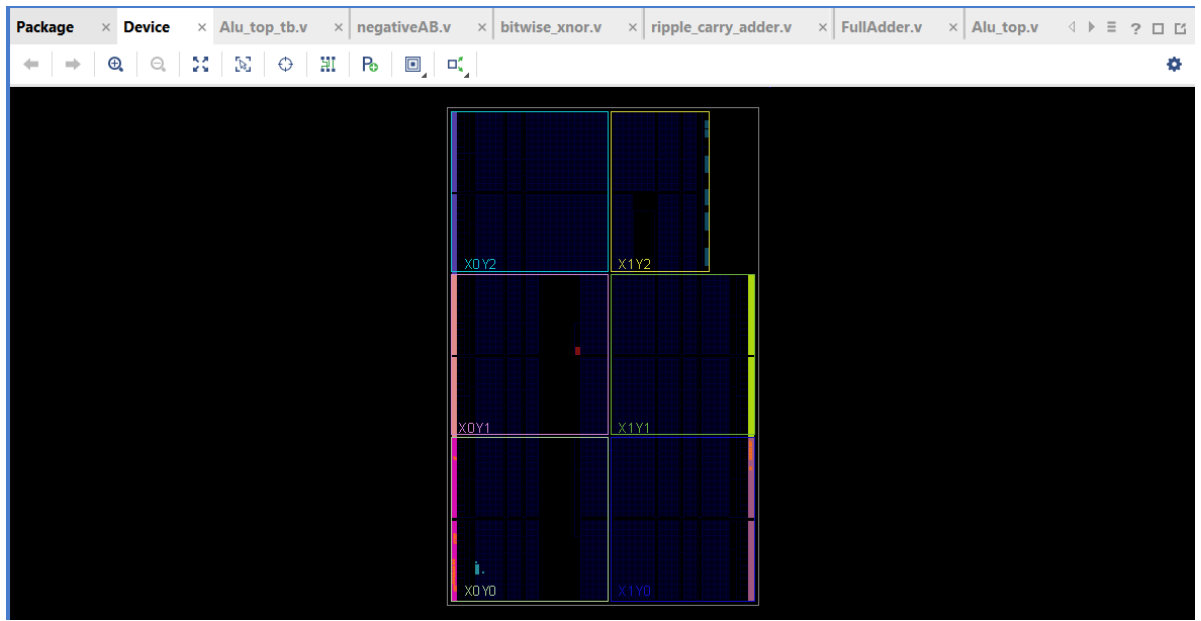


Fig: Implemented Device

CODE SNAPSHOTS:

1. Alu_top_tb testbench code:

```
Alu_top_tb.v
C:/Users/DELL/project_Assignment1_MINIALU/project_Assignment1_MINIALU.srcs/sources_1/imports/project_Assignment1_MiniALU_1.srcs/sim_1/imports/new/Alu_top_tb.v

1 //SETTING TIMESCALE
2 timescale 1 ns/10 ps
3
4 module mini_alu_tb;
5     reg [5:0] p, q;
6     reg [2:0] fcn;
7     wire [5:0] K;
8
9     Alu_Top uut (.A(p), .B(q), .fcn(fcn), .K(K));
10
11 //TEST VECTORS
12 initial
13 begin
14     // initialize selected fcn
15     // initialize selected fcn
16
17     //test vector 1
18     fcn = 3'b111;
19     p = 6'b011100;
20     q = 6'b011010;
21     # 100;
22     //test vector 2
23     fcn = 3'b111;
24     p = 6'b010010;
25     q = 6'b010011;
26     # 100;
27     //test vector 3
28     fcn = 3'b111;
29     p = 6'b011110;
30     q = 6'b010100;
31     # 100;
32     //test vector 4
33     fcn = 3'b111;
34     p = 6'b011010;
35     q = 6'b000001;
36     # 100;
37     //test vector 5
38     fcn = 3'b111;
39     p = 6'b001010;
40     q = 6'b010110;
41     # 100;
42 end
```

```

Alu_top.tb.v
C:/Users/DELL/project_Assignment1_MINIALU/project_Assignment1_MINIALU.srscs/sources_1/imports/project_Assignment1_MinIALU_1.srscs/sim_1/imports/new/Alu_top.tb.v

29: p = 6'b101110;
30: q = 6'b010100;
31: # 100;
32: //test vector 4
33: fcn = 3'b111;
34: p = 6'b011010;
35: q = 6'b000001;
36: # 100;
37: //test vector 5
38: fcn = 3'b111;
39: p = 6'b001010;
40: q = 6'b010110;
41: # 100;
42: //test vector 6
43: fcn = 3'b111;
44: p = 6'b000000;
45: q = 6'b010110;
46: # 100;
47: //test vector 7
48: fcn = 3'b111;
49: p = 6'b000010;
50: q = 6'b000110;
51: # 100;
52: //test vector 8
53: fcn = 3'b111;
54: p = 6'b001110;
55: q = 6'b001000;
56: # 100;
57: //test vector 9
58: fcn = 3'b111;
59: p = 6'b010000;
60: q = 6'b010010;
61: # 100;
62: //test vector 10
63: fcn = 3'b111;
64: p = 6'b000000;
65: q = 6'b010110;
66: # 100;
67:
68: end//STOP
69: endmodule

```

2.Alu_Top code

```

Alu_top.v
C:/Users/DELL/project_Assignment1_MINIALU/project_Assignment1_MINIALU.srscs/sources_1/imports/project_Assignment1_MinIALU_1.srscs/sources_1/imports/new/Alu_top.v

1: // THIS MODULE IMPLEMENTS THE ALU BY CALLING OTHER MODULES FOR EACH FUNCTION
2: module Alu_Top
3: {
4:   input wire [5:0] A, B, // 6-bit - inputs a,b
5:   input wire [2:0] fcn, // 3-bit - input fcn
6:   output reg [5:0] x // 6-bit - output x
7: };
8:
9: wire [5:0] invA, invB, AxorB, AplusB, AminusB; //TEMPORARY 6-BIT WIRES FOR THE OUTPUT OF EACH MODULE
10: wire AlessthanB; //TEMPORARY 1-BIT VARIABLE FOR THE 1-BIT OUTPUT OF THE >= CIRCUIT
11:
12: // instantiation to modules
13: negativeAB inv_A (.a(A), .s(invA)); // X = -A
14: negativeAB inv_B (.a(B), .s(invB)); // X = -B
15:
16: bitwise_xor A_xor_B(.a(A), .b(B), .xor(AxorB)); // X = A ^ B
17: ripple_carry_adder A_plus_B (.x(A), .y(B), .sel(0), .sum(AplusB)); // X = A + B
18: ripple_carry_adder A_minus_B (.x(A), .y(B), .sel(1), .sum(AminusB)); // X = A - B
19:
20: // control for fcn call
21: always @(*)
22: begin
23:   if (fcn == 3'b000) [x] = [A]; // X = A This is according to the question given.
24:   if (fcn == 3'b001) [x] = [B]; // X = B
25:   if (fcn == 3'b010) [x] = [invA]; // X = -A
26:   if (fcn == 3'b011) [x] = [invB]; // X = -B
27:
28:   if (fcn == 3'b101) [x] = [AxB]; // X = A ^ B
29:   if (fcn == 3'b110) [x] = [AplusB]; // X = A + B
30:   if (fcn == 3'b111) [x] = [AminusB]; // X = A - B
31: end
32: endmodule
33:

```

3.bitwise xnor code

```
bitwise_xnor.v
C:/Users/DELL/project_Assignment1_MINIALU/project_Assignment1_MINIALU.srscs/sources_1/imports/project_Assignment1_MinIALU_1.srscs/sources_1/imports/new/bitwise_xnor.v

1 // timescale lns / lps
2 // Company:
3 // Engineer:
4 // Create Date: 30.10.2021 18:35:48
5 // Design Name:
6 // Module Name: bitwise_xnor
7 // Project Name:
8 // Target Devices:
9 // Tool Versions:
10 // Description:
11 // Dependencies:
12 // Revision:
13 // Revision 0.01 - File Created
14 // Additional Comments:
15 //
16 //
17 //
18 //
19 //
20 //
21 //
22 //
23 // timescale lns / lps
24 module bitwise_xnor(
25     input [5:0] a,
26     input [5:0] b,
27     output [5:0] xor_
28 );
29
30 assign xor_ = a ^ b;
31 endmodule
32
```

4. Full Adder code

```
FullAdder.v
C:/Users/DELL/project_Assignment1_MINIALU/project_Assignment1_MINIALU.srscs/sources_1/imports/project_Assignment1_MinIALU_1.srscs/sources_1/imports/new/FullAdder.v

1 // timescale lns / lps
2 // Company:
3 // Engineer:
4 // Create Date: 30.10.2021 19:04:51
5 // Design Name:
6 // Module Name: FullAdder
7 // Project Name:
8 // Target Devices:
9 // Tool Versions:
10 // Description:
11 // Dependencies:
12 // Revision:
13 // Revision 0.01 - File Created
14 // Additional Comments:
15 //
16 //
17 //
18 //
19 //
20 //
21 //
22 module FullAdder(a, b, cin, s, cout);
23 // a and b are the bits to add
24 // cin is carry in
25 input wire a, b, cin;
26
27 // s is the sum of a and b, cout is any carry out bit
28 // wires since just using assign here
29 output wire s, cout;
30
31 // logic for sum and carry
32 assign s = cin ^ a ^ b;
33 assign cout = (b & cin) | (a & cin) | (a & b);
34
35 endmodule
36
37
38
```

5. Six bit Comparator code

```
comparator_6bit.v
C:/Users/DELL/project_Assignment1_MINIALU/project_Assignment1_MINIALU.srscs/sources_1/imports/project_Assignment1_MinIALU_1.srscs/sources_1/imports/new/comparator_6bit.v

1 // timescale 1ns / 1ps
2 //////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 30.10.2021 18:40:42
7 // Design Name:
8 // Module Name: comparator_6bit
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22 `timescale 1ns / 1ps
23 module comparator_6bit (
24     input [5:0] in1,
25     input [5:0] in2,
26     output [5:0] y
27 );
28
29 comparator bit0 (.i1(in1[0]), .i2(in2[0]), .less_than(y[0]));
30 comparator bit1 (.i1(in1[1]), .i2(in2[1]), .less_than(y[1]));
31 comparator bit2 (.i1(in1[2]), .i2(in2[2]), .less_than(y[2]));
32 comparator bit3 (.i1(in1[3]), .i2(in2[3]), .less_than(y[3]));
33 comparator bit4 (.i1(in1[4]), .i2(in2[4]), .less_than(y[4]));
34 comparator bit5 (.i1(in1[5]), .i2(in2[5]), .less_than(y[5]));
35
36 endmodule
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7. Ripple carry adder code

```
ripple_carry_adder.v
C:/Users/DELL/project_Assignment1_MINIALU/srcs/sources_1/imports/project_Assignment1_MinIALU_1/srcs/sources_1/imports/new/ripple_carry_adder.v

1 module ripple_carry_adder(
2   input [5:0]x, // 6 bit input
3   input [5:0]y, // 6 bit input
4   input sel, // functionality - add/subtract
5   // 1 bit MSB carry out from sum
6   output [5:0] sum,
7   output overflow, // 1 bit Overflow in sum output
8   output c_out
9   // 6 bit sum of inputs x and y
10  );
11  //If y xor 0 = y
12  // y xor 1 = not(y)
13  //If sel = 1 = x + (not y) == subtraction
14  // therefore, if sel=0 -> add and if sel=1 -> sub
15
16  wire c0; //carry out for a0
17  wire c1; //carry out for a1
18  wire c2; //carry out for a2
19  wire c3; //carry out for a3
20  wire c4; //carry out for a4
21  wire c5; //carry out for a5
22
23  wire in0; // xor of y[0] and sel
24  wire in1; // xor of y[1] and sel
25  wire in2; //xor of y[2] and sel
26  wire in3; //xor of y[3] and sel
27  wire in4; //xor of y[4] and sel
28  wire in5; //xor of y[5] and sel
29
30  xor(in0, y[0], sel);
31  xor(in1, y[1], sel);
32  xor(in2, y[2], sel);
33  xor(in3, y[3], sel);
34  xor(in4, y[4], sel);
35  xor(in5, y[5], sel);
36
37  xor(c_out, c5, sel);
38  xor(overflow, c5, c4);
39
40  //Instantiating full adder
41
42  FullAdder a0(x[0], in0, sel, sum[0], c0);
43  FullAdder a1(x[1], in1, c0, sum[1], c1);
44  FullAdder a2(x[2], in2, c1, sum[2], c2);
45  FullAdder a3(x[3], in3, c2, sum[3], c3);
46  FullAdder a4(x[4], in4, c3, sum[4], c4);
47  FullAdder a5(x[5], in5, c4, sum[5], c5);
48
49 endmodule
50
51
```

```
Constraints.xdc
C:/Users/DELL/project_Assignment1_MiniALU_1/project_Assignment1_MiniALU_1/srcs/constrs_2/new/Constraints.xdc

3. set_property PACKAGE_PIN W17 [get_ports {A[3]}]
4. set_property PACKAGE_PIN W16 [get_ports {A[2]}]
5. set_property PACKAGE_PIN V16 [get_ports {A[1]}]
6. set_property PACKAGE_PIN V17 [get_ports {A[0]}]
7. set_property IOSTANDARD LVCMOS33 [get_ports {A[5]}]
8. set_property IOSTANDARD LVCMOS33 [get_ports {A[4]}]
9. set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
10. set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
11. set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
12. set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
13. set_property IOSTANDARD LVCMOS33 [get_ports {B[5]}]
14. set_property IOSTANDARD LVCMOS33 [get_ports {B[4]}]
15. set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]
16. set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
17. set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
18. set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
19. set_property PACKAGE_PIN R3 [get_ports {B[5]}]
20. set_property PACKAGE_PIN T2 [get_ports {B[4]}]
21. set_property PACKAGE_PIN T3 [get_ports {B[3]}]
22. set_property PACKAGE_PIN V2 [get_ports {B[2]}]
23. set_property PACKAGE_PIN W3 [get_ports {B[1]}]
24. set_property PACKAGE_PIN W14 [get_ports {B[0]}]
25. set_property IOSTANDARD LVCMOS33 [get_ports {fxn[2]}]
26. set_property IOSTANDARD LVCMOS33 [get_ports {fxn[1]}]
27. set_property IOSTANDARD LVCMOS33 [get_ports {fxn[0]}]
28. set_property PACKAGE_PIN R2 [get_ports {fxn[2]}]
29. set_property PACKAGE_PIN T1 [get_ports {fxn[1]}]
30. set_property PACKAGE_PIN U1 [get_ports {fxn[0]}]
31. set_property PACKAGE_PIN U15 [get_ports {x[5]}]
32. set_property PACKAGE_PIN W10 [get_ports {x[4]}]
33. set_property PACKAGE_PIN V19 [get_ports {x[3]}]
34. set_property PACKAGE_PIN U19 [get_ports {x[2]}]
35. set_property PACKAGE_PIN E19 [get_ports {x[1]}]
36. set_property PACKAGE_PIN U16 [get_ports {x[0]}]
37. set_property IOSTANDARD LVCMOS33 [get_ports {x[5]}]
38. set_property IOSTANDARD LVCMOS33 [get_ports {x[4]}]
39. set_property IOSTANDARD LVCMOS33 [get_ports {x[3]}]
40. set_property IOSTANDARD LVCMOS33 [get_ports {x[2]}]
41. set_property IOSTANDARD LVCMOS33 [get_ports {x[1]}]
42. set_property IOSTANDARD LVCMOS33 [get_ports {x[0]}]
43.
```

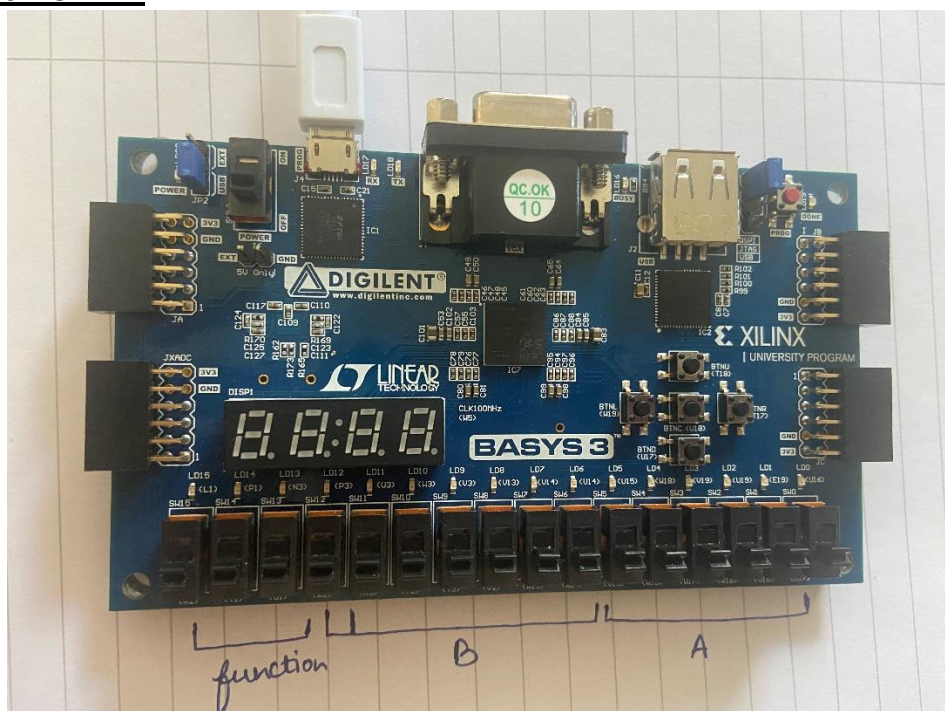
DEMO SECTION:**Demo on board:**

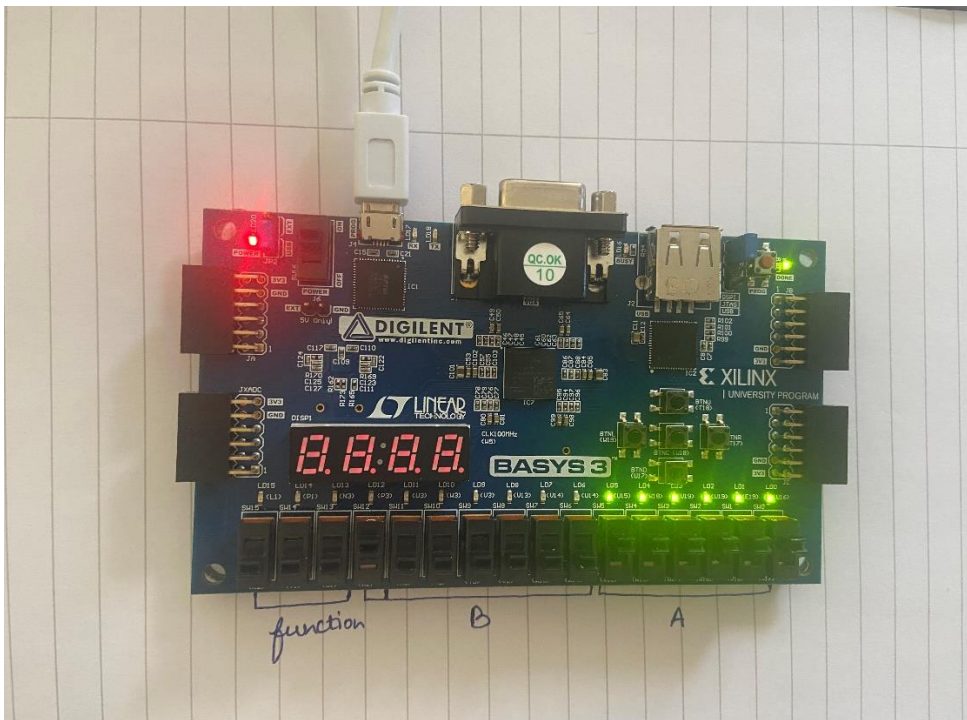
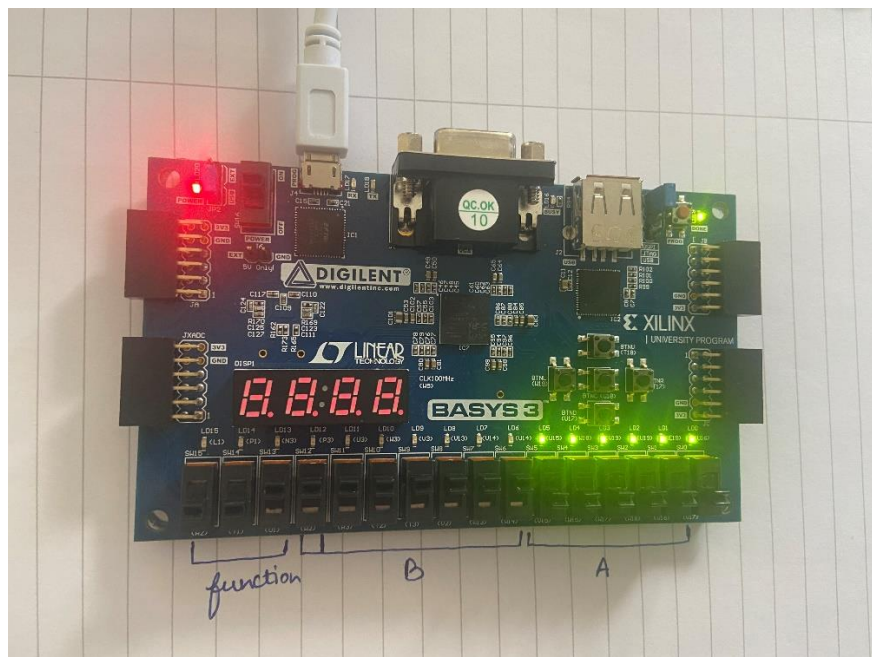
Fxn	Switch
Fxn[0]	U1
Fxn [1]	T1
Fxn [2]	R2

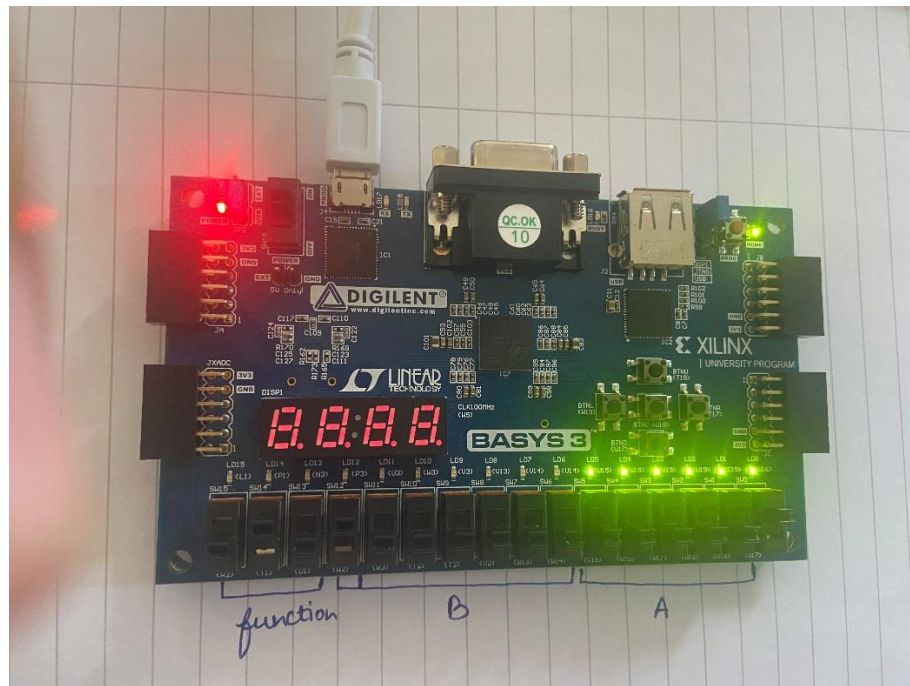
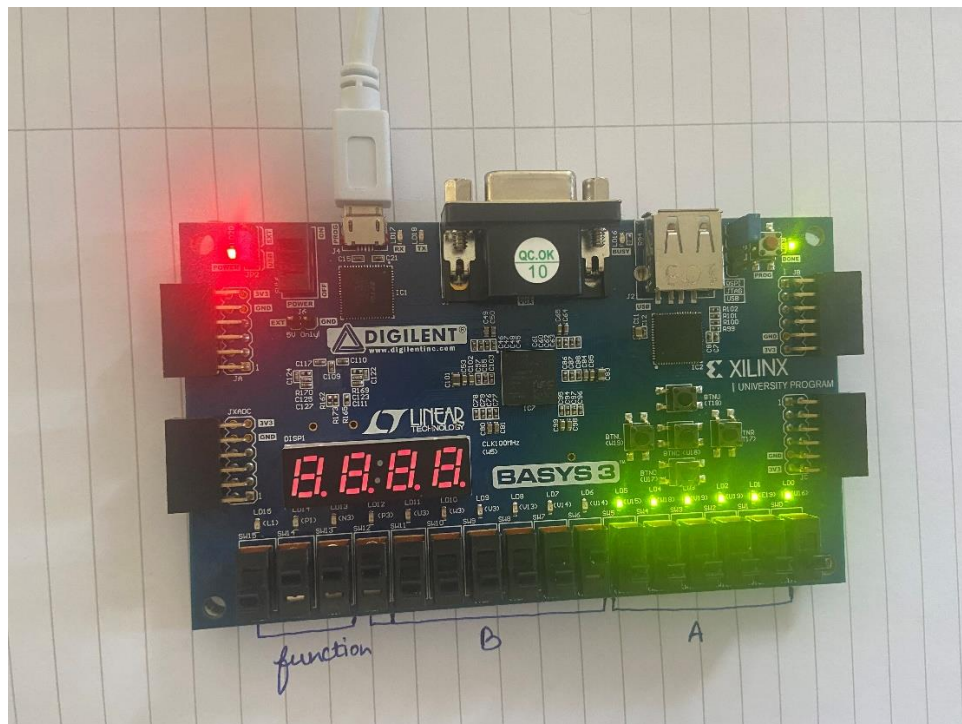
A	Switch
A[0]	V17
A[1]	V16
A[2]	W16
A[3]	W17
A[4]	W15
A[5]	V15

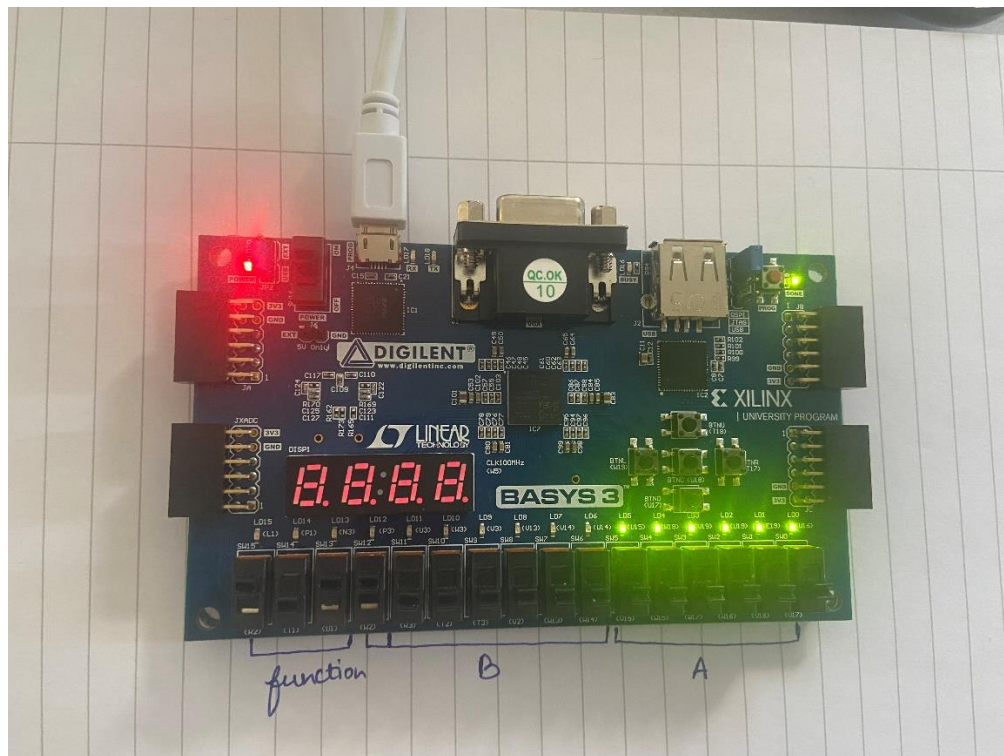
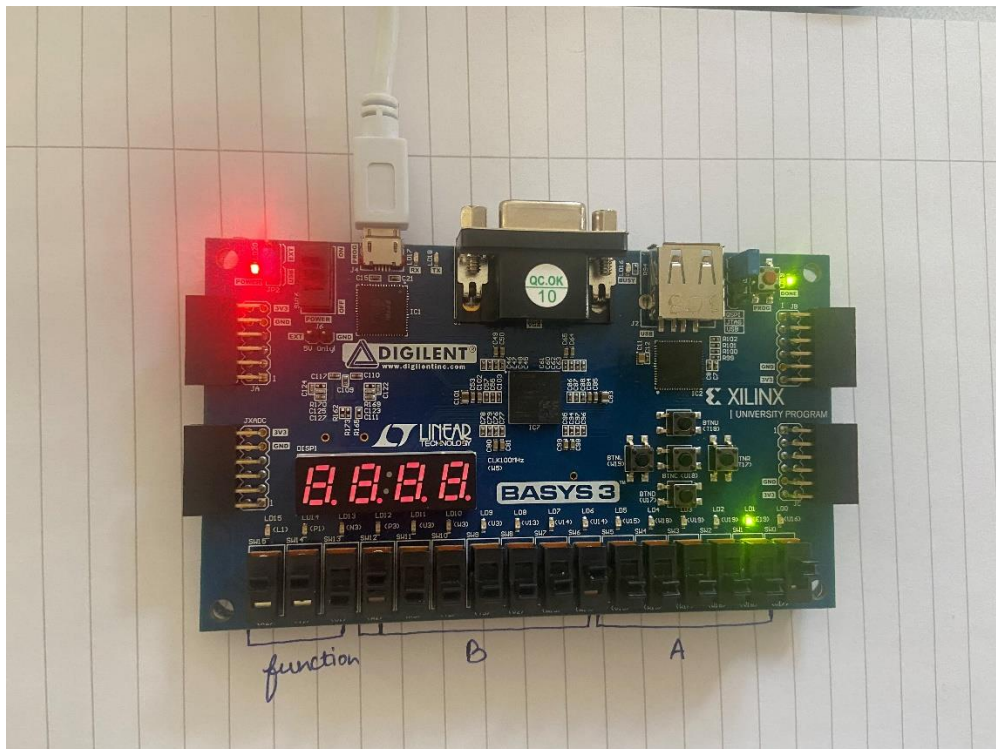
B	Switch
B[0]	W14
B[1]	W13
B[2]	V2
B[3]	T3
B[4]	T2
B[5]	R3

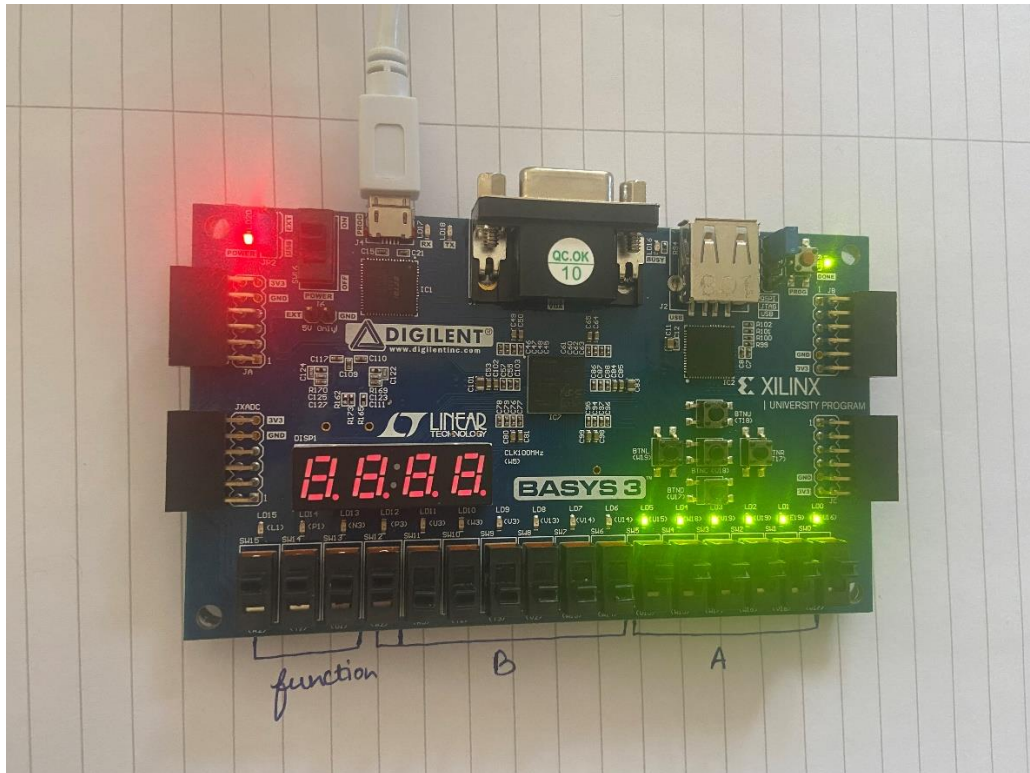
X	LED
X[0]	U16
X[1]	E19
X[2]	U19
X[3]	V19
X[4]	W18
X[5]	U15

BASYS 3 BOARD:

TEST CASES:**CASE1: $fxn=b'000$** **CASE 2: $fxn=b'001$** 

CASE 3: $fxn=b'010$ **CASE 4: $fxn=b'011$** 

CASE 5: $fxn=b'101$ **CASE 6: $fxn=b'110$** 

CASE 7 : $fxn=b'111$ **CONCLUSIONS:**

In this assignment I learned how to make modules and add constraints and then form different cases and upload the program upto the basys 3 board and check different functions on it.

APPENDIX:

LabB_ShrutiKathuria, ripple_carry_adder, full_adder, and LabC_ShrutiKathuria which were submitted in the last labs.

