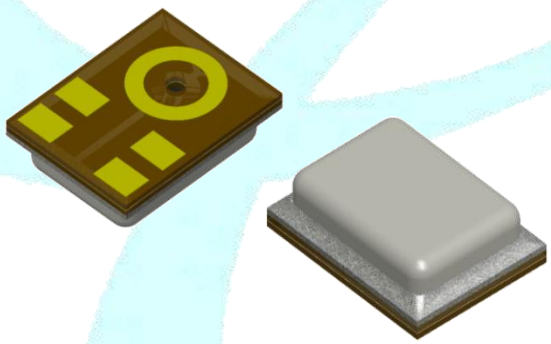
F4-(A)HDMOE-J098R26-5P

High SNR / Multiple Clock Mode
/ Narrow Sensitivity

OMNI-DIRECTIONAL
BOTTOM PORT



1. INTRODUCTION

- Digital MEMS Microphone - ½ Cycle PDM 16bit, Full Scale=120dBSPL
- Bottom Port Type – Sensitivity is Typical -26dBFS at LPM and STM
- **High Signal to Noise Ratio(SNR) – Typical 64.5dB (A-weighted, 20Hz~20kHz) at fclk=2.4MHz**
- **Multiple Clock Mode – Stand by Mode, Low-Power Mode(LPM), Standard Mode(STM)**
- **Narrow Sensitivity – +/-1dB**
- Omni-directional
- Dual Channel supported
- RF Shielded – with embedded Capacitor
- Compatible with Sn/Pb and Halogen-free solder process
- RoHS compliant
- SMD reflow temperature of up to 260℃ for over 30 seconds

2. APPLICATIONS

- Smartphones
- Ear-sets, Bluetooth Headsets
- Smart Speaker, Set Top Box
- Tablet Computers
- Wearable Devices
- Electrical Appliances
- Voice Recognition Systems of Appliances

3. MODEL NO.

F4-(A)HDMOE-J098R26-5P

4. ABSOLUTE MAXIMUM RATINGS

Parameter	Absolute maximum rating	Units
Vdd , Data to Ground	**3.6**	V
Clock to Ground	**3.6**	V
Select to Ground	**3.6**	V
Input Current	**2**	mA
Short Circuit Current to/from Data	**Infinite to Ground or Vdd**	sec

Caution : Stresses above those listed in “Absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated under “ELECTRO-ACOUSTIC CHARACTERISTICS” is not implied. Exposure beyond those indicated under “ELECTRO-ACOUSTIC CHARACTERISTICS” for extended periods may affect device reliability.

5. GENERAL MICROPHONE SPECIFICATIONS

Test Condition : 23 ± 2℃, Room Humidity = 55 ± 20 %, Vdd=1.8V, fclk = 2.4㎒, SELECT Pin is grounded, CLOAD = 1㎌, unless otherwise noticed

Parameter		Conditions	Min	Typ	Max	Units
*** Clock Frequency Range**	**Stand by Mode**	Max. Tolerance ±5%	**0**	**-**	**350**	㎑
	Low-Power Mode	Generally at ±10% of typical value	**450**	**768**	**850**	㎑
	Standard Mode		**1.536**	**-**	**3.072**	㎒
Standby Mode Current		f_{CLK} < 350㎑	**-**	**25**	**50**	㎂
Short Circuit Current		Grounded DATA pin	**1**	**-**	**20**	㎃
Clock off Mode Current		Clock pulled low	**-**	**<1**	**35**	㎂
Vdd Ramp-up Time (Power-up)		Vdd ≥ Vdd (min)	**-**	**-**	**50**	㎳
Startup Time		Time to start up in any mode after VDD and CLOCK applied	**-**	**-**	**50**	㎳
Reset Time		Time to start up in any mode after VDD has been off for more than10ms, while CLOCK remained on	**-**	**-**	**50**	㎳
Mode-Change Time		Time to switch between modes. VDD remains on during the mode switch	**-**	**-**	**50**	㎳

*** Note : Must be consulted when used another clock frequency without the typical clock frequencys.**

6. ELECTRO-ACOUSTIC CHARACTERISTICS

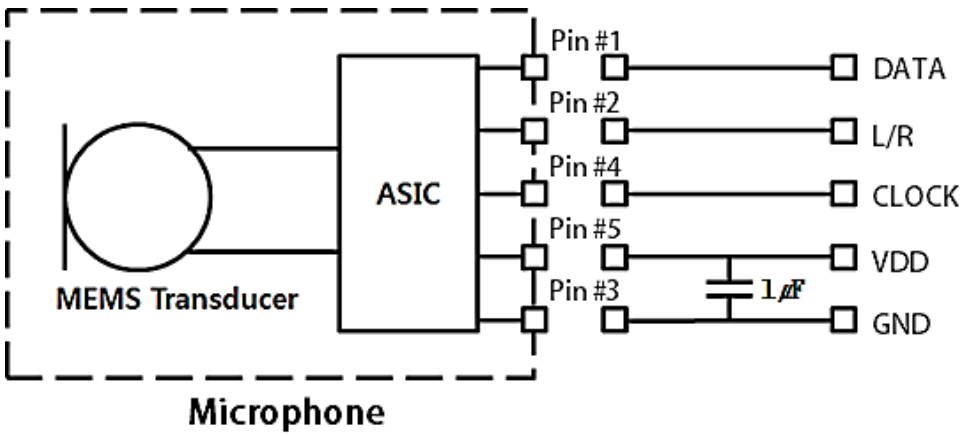
Test Condition : 23 ± 2℃, Room Humidity = 55 ± 20 %, Vdd=1.8V, fclk = 2.4㎒, SELECT Pin is grounded, CLOAD = 1㎌, unless otherwise noticed

Parameter	Conditions	Min	Typ	Max	Units
Directivity		Omni-directional			
Supply Voltage (Vdd)		**1.62**	**-**	**3.6**	V
Sensitivity Change across Voltage	Vdd=1.62~3.6V, fclk=2.4㎒	**No change**			dB
Data Format		**½ Cycle PDM 16bit**			-
Full Scale Acoustic Level			**120**		dBSPL
Current Consumption (Idd)	fclk = 1.536㎒, load on DATA output	**490**	**-**	**690**	µA
	fclk = 2.4㎒, load on DATA output	**640**	**-**	**840**	
	fclk = 3.072㎒, load on DATA output	**760**	**-**	**960**	
● **Standard Mode** **Test Conditions : Measurement Clock Frequency=2.4MHz, Vdd=1.8V**					
Sensitivity	94dB SPL at 1㎑	**-27**	**-26**	**-25**	dBFS
Signal to Noise Ratio (SNR)	94dBSPL at 1㎑, A-weighted (20㎐~20㎑)	**-**	**64.5**	**-**	dB(A)
Equivalent Input Noise (EIN)	94dBSPL at 1㎑, A-weighted (20㎐~20㎑)	**-**	**29.5**	**-**	dB(A)SPL
Total Harmonic Distortion (THD)	94dBSPL at 1㎑	**-**	**-**	**0.4**	%
	103dBSPL at 1㎑	**-**	**-**	**1.0**	%
	112.5dBSPL at 1㎑	**-**	**-**	**3.0**	%
	117dBSPL at 1㎑	**-**	**-**	**5.0**	%
Acoustic Overload Point (AOP)	THD>10%, at 1㎑	**120**	**121**	**-**	dBSPL
Power Supply Rejection Raito (PSRR)	Measured with 1㎑ sine wave and broad band noise, both 200mVpp	**-**	**52**	**-**	dBV/FS
Power Supply Rejection (PSR)	Measured with 217㎐ square wave and broad band noise, both 100mVpp, A-weighted	**-**	**-84**	**-**	dBFS(A)
● **Low Power Mode** **Test Conditions : Measurement Clock Frequency=768kHz, Vdd=1.8V**					
Current consumption (Idd)	load on DATA output	**180**	**-**	**380**	µA
Sensitivity	94dB SPL at 1㎑	**-27**	**-26**	**-25**	dBFS
Signal to Noise Ratio (SNR)	94dBSPL at 1㎑, A-weighted (20㎐~8㎑)	**-**	**63.5**	**-**	dB(A)
Equivalent Input Noise (EIN)	94dBSPL at 1㎑, A-weighted (20㎐~8㎑)	**-**	**30.5**	**-**	dB(A)SPL
Total Harmonic Distortion (THD)	94dBSPL at 1㎑	**-**	**-**	**0.4**	%
	103.5dBSPL at 1㎑	**-**	**-**	**1.0**	%
	112.5dBSPL at 1㎑	**-**	**-**	**3.0**	%
	116.5dBSPL at 1㎑	**-**	**-**	**5.0**	%
Acoustic Overload Point (AOP)	THD>10%, at 1㎑	**119**	**120**	**-**	dBSPL
Power Supply Rejection Raito (PSRR)	Measured with 1㎑ sine wave and broad band noise, both 200mVpp	**-**	**52**	**-**	dBV/FS
Power Supply Rejection (PSR)	Measured with 217㎐ square wave and broad band noise, both 100mVpp, A-weighted	**-**	**-84**	**-**	dBFS(A)

7. INTERFACE PARAMETER

Parameter	Conditions	Min	Typ	Max	Units
Clock Frequency	Min. tolerance ±5%	**0.35**	-	**3.3**	MHz
Stand by Clock Frequency	Max. tolerance ±5%	-	-	**350**	kHz
Clock Duty Cycle	f_{CLK} <= 3.072MHz	**40**	-	**60**	%
	f_{CLK} > 3.072MHz	**48**	-	**52**	
Input Logic Low Level		**-0.3**	-	**0.35 x Vdd**	V
Input Logic High Level		**0.65 x Vdd**	-	**Vdd + 0.3**	V
Hysteresis Width		**0.1 x Vdd**	-	**0.29 x Vdd**	V
Output Logic Low Level		-	-	**0.3 x Vdd**	V
Output Logic High Level		**0.7 x Vdd**	-	-	V
Output Load Capacitance on DATA		-	-	**200**	pF
Clock Rise / Fall Time		-	-	**13**	ns
Delay Time for Data driven	Delay time from CLOCK edge(50% VDD) to DATA driven	**40**	-	**80**	ns
Delay Time for High Z	Delay time from CLOCK edge(50% VDD) to DATA high impedance state	**5**	-	**30**	ns
Delay Time for Valid Data	Delay time from CLOCK edge(0.50 x VDD) to DATA valid(<0.30 x VDD or >0.70 x VDD) Rload, min = 100kΩ Cload, max = 100pF	-	-	**100**	ns

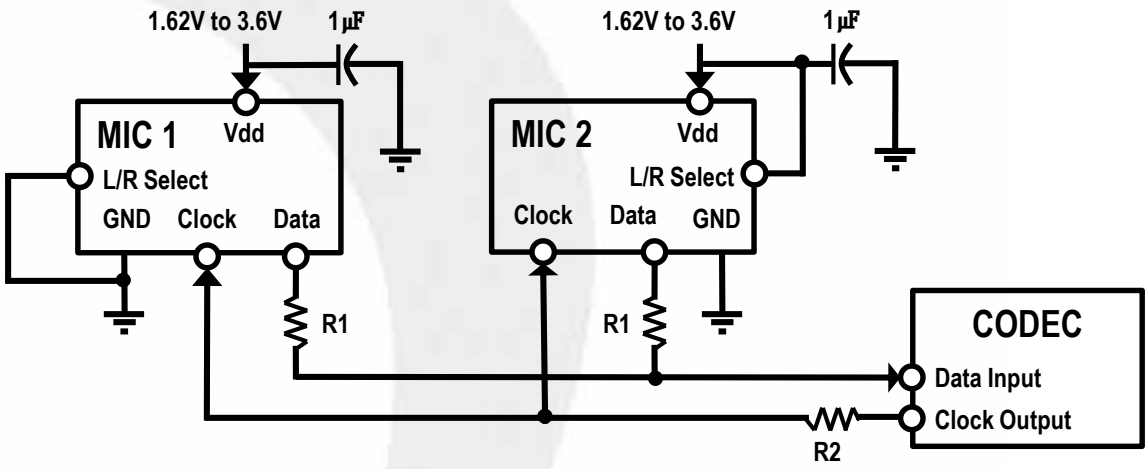
8. MEASUREMENT CIRCUIT



9. PIN DESCRIPTION

Pin Name	Description
Vdd	Supply and IO voltage for the microphone
L/R Select	Left/Right (DATA2 / DATA1) Channel selection
CLOCK	Clock input to the microphone
DATA	PDM data output from the microphone
GND	Ground

10. INTERFACE CIRCUIT & CHANNEL DATA CONFIGURATION



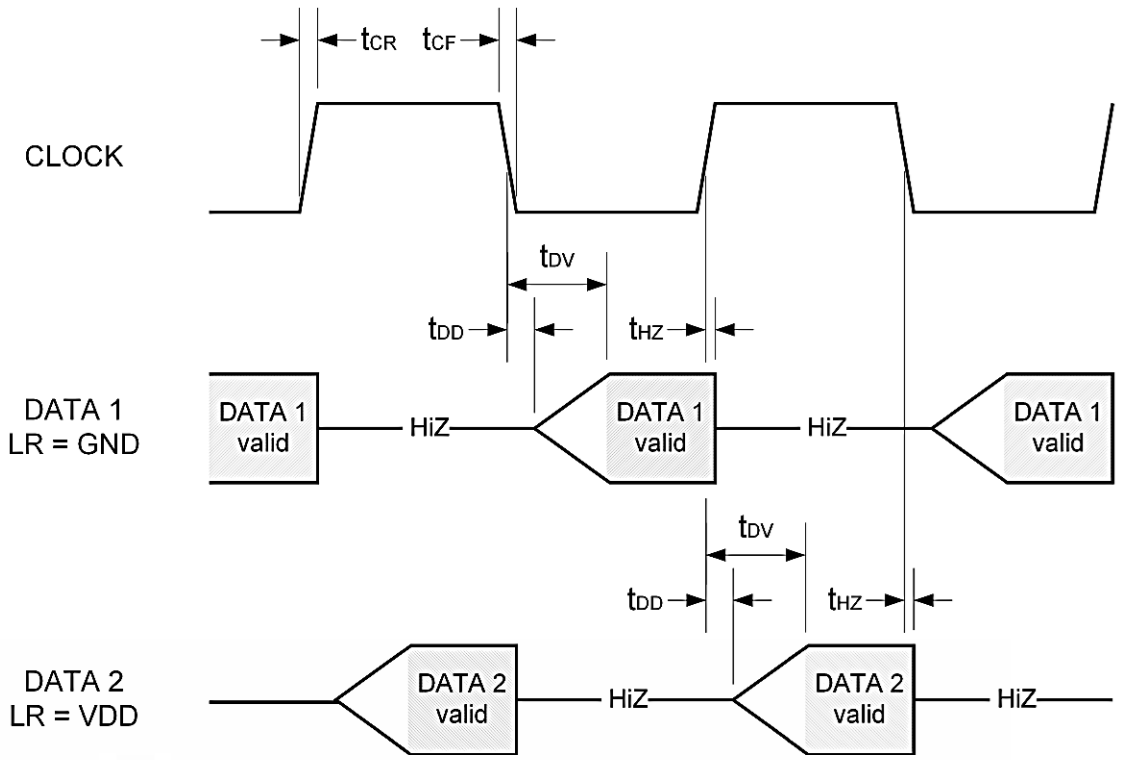
Data symbol in interface timing chart	L/R Select connected to	Data asserted at	Data sampled at
DATA1 [MIC1(Low)]	GND	Falling clock edge	Rising clock edge
DATA2 [MIC2(High)]	Vdd	Rising clock edge	Falling clock edge

Note 1 : Stereo operation is accomplished by connecting the L/R Sel. pin either to Vdd or GND on the phone PWB. Bypass Capacitors near each MIC. on Vdd are recommended to provide maximum SNR performance.

Note 2 : R1(Data source termination Resister) should be as close as possible to each the MIC. (50Ω~100Ω)

Note 3 : R2(Clock source termination Resister) should be as close as possible to the CODEC. (50Ω~100Ω)

11. INTERFACE TIMING CHART



With defining a minimum value for t_{DD} and a maximum value for t_{HZ} it is secured that the driven DATA signals of the right and the left channel don't overlap.
A definition of a maximum value for t_{DD} is not necessary, instead t_{DV} defines the time until the driven DATA is valid.

12. ENVIRONMENTAL CHARACTERISTICS AND STANDARD CONDITIONS

Item	Min	Typ	Max	Unit
Operating temperature range	-40	-	+100	**℃**
Storage temperature range	-40	-	+100	**℃**
Relative humidity	25	-	85	**%**
Air Pressure	860	-	1060	**mBar**
Standard temperature range	15	20	25	**℃**
Standard Relative humidity	40	-	60	**%**

13. TYPICAL FREQUENCY RESPONSE CURVE

Far Field Measurement Condition
Temperature : 23 ± 2 ℃
Supply Voltage : 1.8V
Clock Frequency : 2.4㎒
Acoustic stimulus : 1Pa (94dB SPL at 1㎑) at 50 ㎝ from the loud-speaker.
The loud-speaker must be calibrated to make a flat frequency response input signal.
Position : The frequency response of microphone unit measured at 50㎝ from the loud-speaker

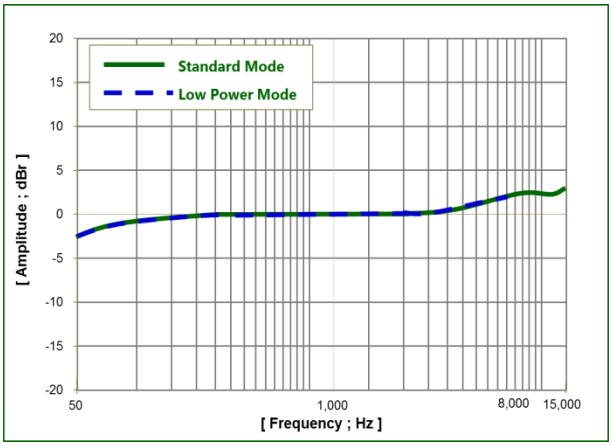


Figure 1. Typical Frequency Response, Normalized to 1㎑

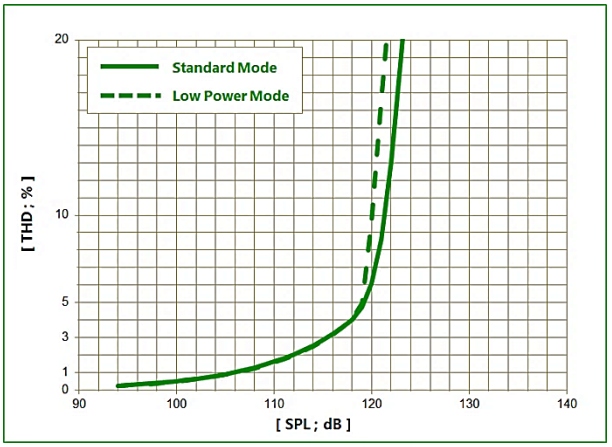


Figure 2. THD vs. Input Level, Standard and Low-Power Modes

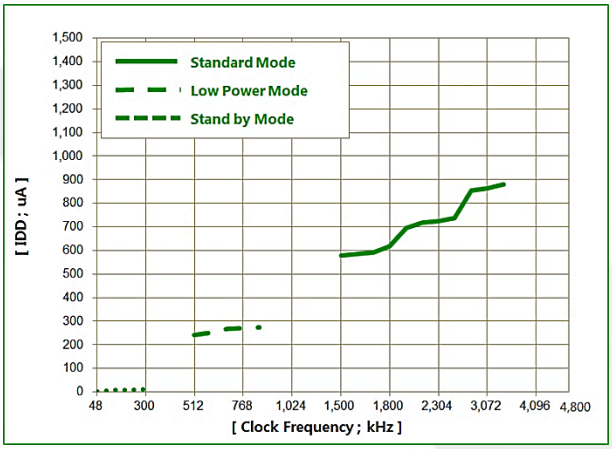


Figure 3. Typical IDD vs Clock Frequency, All Mode

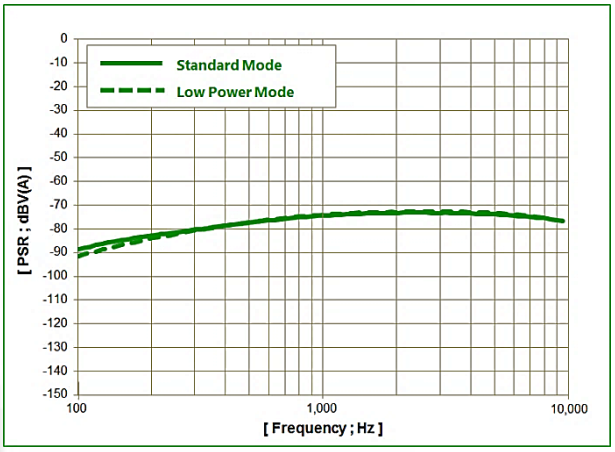


Figure 4. Typical Power Supply Rejection (PSR) vs. Frequency, Standard and Low-Power Modes

■ Frequency Mask Specification

Frequency [Hz]	Lower Limit [dBr]	Upper Limit [dBr]	Note
50	-4	+2	0dBr = dBFS at 1㎑
100 ~1000	-2	+2	
1000	0	0	
1000 ~ 5000	-2	+2	
10000	-2	+5	
15000	-2	+8	

Note : Band Frequency Range
1. Narrow Band : 300㎐ ~ 3.4㎑
2. Wide Band : 100㎐ ~ 7㎑
3. Super Wide Band : 50㎐ ~ 14㎑

14. MECHANICAL CHARACTERISTICS

※ PCB design & Pin size can be changed by model No.

SMD Type

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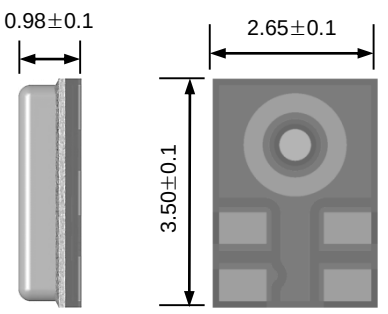
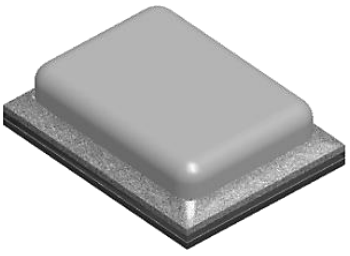
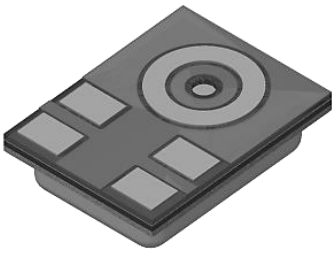






Lettering

V1.0 F 4 H

Version1

E : Engineering Sample
P : Pre-Production
M : Mass Production

M E 18 17

Week

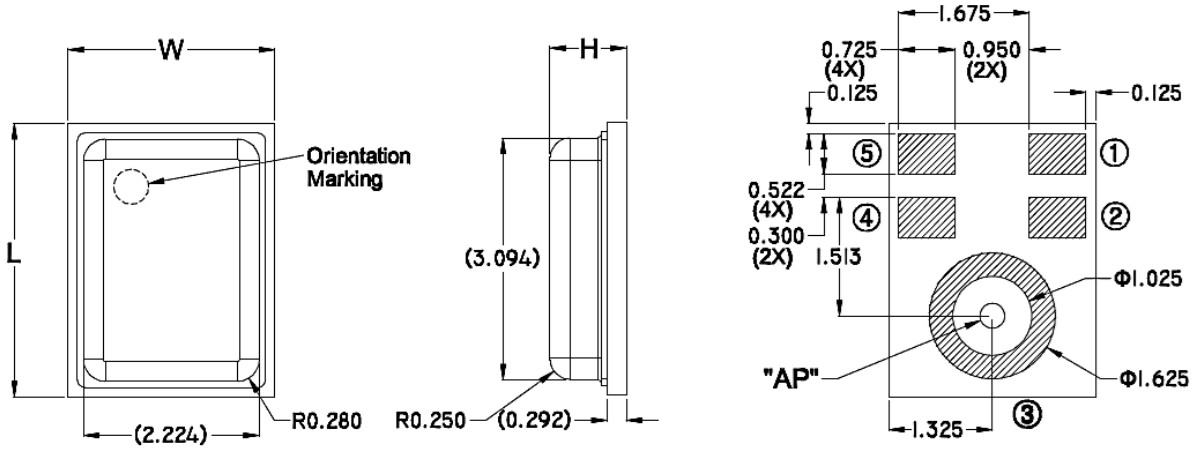
Version2

Year

14. MECHANICAL CHARACTERISTICS

- Mechanical dimensions & Pad Lay-out

Dimensions (Unit : mm)



TOP VIEW SIDE VIEW BOTTOM VIEW

Item	Dimension	Tolerance (+/-)	Units
Length (L)	3.50	0.10	mm
Width (W)	2.65	0.10	mm
Height (H)	0.98	0.10	mm
Acoustic Port (AP)	Φ 0.325	0.05	mm

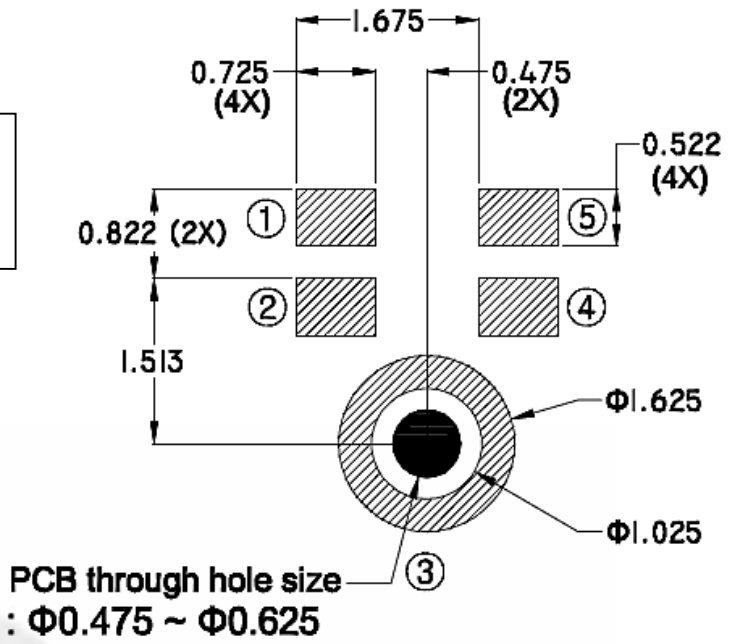
Pin #	Pin Name	Type	Description
1	DATA	Digital O	PDM data output
2	L/R	L/R Select	Left/Right channel selection
3	GND	Ground	Ground
4	CLK	Clock	Clock input
5	VDD	Power	Supply and I/O voltage

Note : All ground Pins must be connected to ground.
"3"Pin must be sealed by solder paste on the PWB.
General Tolerance ±0.08mm.

14. MECHANICAL CHARACTERISTICS

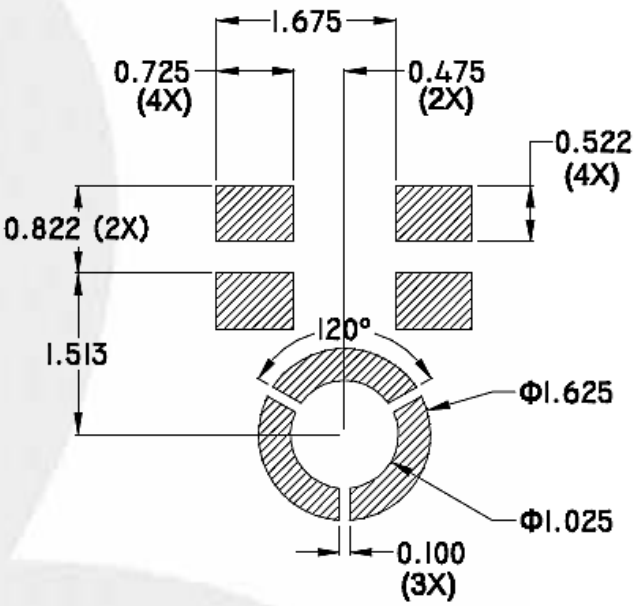
- Recommended Land Pattern & Stencil Pattern

Recommended
PCB land pattern
(Unit : mm)



Recommended
solder stencil pattern
(Unit : mm)

(thickness of metal mask: 0.10T)



15. RELIABILITY TEST CONDITIONS

Note : After test conditions are performed, the sensitivity of the microphone shall not deviate more than ±1dB from its initial value.	
TEST	**DESCRIPTION**
TEMPERATURE STORAGE	[High Temperature Storage] +80℃±3℃ x 200hrs (The measurement to be done after 2 hours of conditioning at room temperature)
	[Low Temperature Storage] -30℃±3℃ x 200hrs (The measurement to be done after 2 hours of conditioning at room temperature)
TEMPERATURE CYCLE	(-25℃±2℃ x 30min -> +20℃±2℃ x 10min -> +70℃±2℃ x 30min -> +20℃±2℃ x 10min) x 5cycles (The measurement to be done after 2 hours of conditioning at room temperature)
THERMAL SHOCK	(+85℃±2℃ -> -40℃±2℃Change time : 20sec) x 96cycles Maintain : 30min (The measurement to be done after 2 hours of conditioning at room temperature)
HIGH TEMPERATURE AND HUMIDITY	+85℃±2, 85±%RH, Bias(3.6V) x 200hrs (The measurement to be done after 2 hours of conditioning at room temperature)
	+70℃±2, 95±%RH x 200hrs (The measurement to be done after 2 hours of conditioning at room temperature)
ESD (Electrostatic Discharge)	Air discharge : ±8kV, ±10kV, ±12kV, ±15kV Vdd, Data, CLK, L/R, GND Pad each 5 times (Non-ground)
	Contact discharge : ±2kV, ±4kV, ±6kV, ±8kV Vdd, Data, CLK, L/R, GND Pad each 5 times (Non-ground)
VIBRATION	Signal 5Hz to 500Hz, acceleration spectral density of 0.01g^2/Hz in each of 3 axes, 120 min in each axis (360min in total)
DROP	To be no interference in operation after dropped to steel floor 18 times from 1.52 meter height in state of packing
REFLOW SENSITIVITY	5 reflow cycles. Refer to reflow profile from specification item 18.

16 . TEMPERATURE CONDITIONS (Maximum Ratings)

16.1 STORAGE TEMPERATURE : -40℃ ~ +100℃

16.2 OPERATING TEMPERATURE : -40℃ ~ +100℃