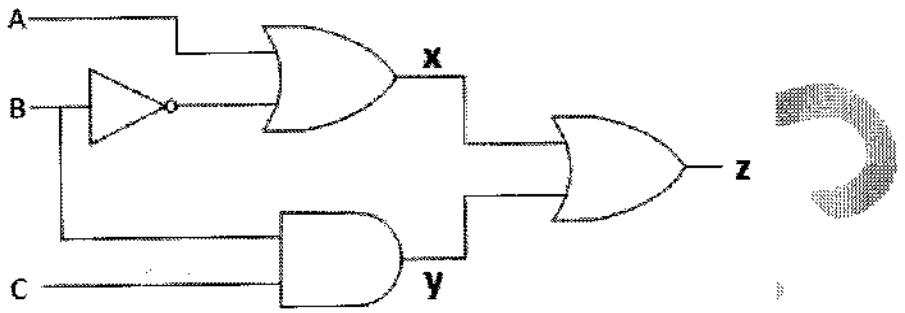
**2401 – Computer Architecture**

**[ 2nd Year, Second semester : 2017 ]**

**Marking scheme**

**Q 1. [Total 25 marks]**

**(i)** A, B, and C are inputs of following circuit.




**a)** Write the Boolean expressions of x, y and z **(04 marks)**

**b)** Draw the truth table for the above circuit outputs of x,y and z **(04 marks)**

*Answer:*

a) X=A+B' (1 mark)

Y= B.C (1 mark)

Z= (A+B')+B.C (2 marks)

b)

| A | B | C | z |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**(ii)**

**a)** Consider the following truth table

| A | B | x |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Which is basic logic gate initiated in the above table? **(02 marks)**

**b)** In which type of circuit, is output also considered as feedback (input)s? **(02 marks)**

*Answer:*

a) NAND gate

b) In sequential circuit

**(iii)** Simplify the following Boolean expressions using by algebra. Mention suitable laws in each step.

**a)** F= A.(A+B) **(02 marks)**

**b)** F= AB + AB' + C **(02 marks)**

**c)** F= B + (AB)' **(03 marks)**

*Answer:*

a) F = A.(A+B)
= A {Absorption}

b) F = AB + AB' + C
= A(B+B') + C {Distributive}
= A.1 + C {Inverse}
= A + C {Identity}

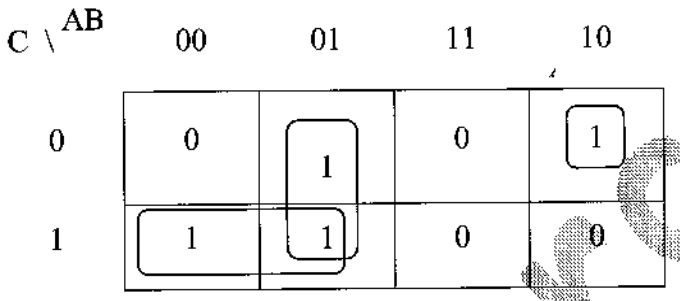
c) F = B + (A' + B') {DeMorgan's}
= B + (B' +A') {Commutative}
= (B +B') + A' {Associative}
= 1 + A' {Inverse}
= 1 {Null}

Remark – in each answer 1 mark for correct simplification + 1 mark if student has given at least one Law correctly.

(iv) Simplify the following Boolean function F by K-Map **(06 marks)**

F= A'BC' + AB'C' + A'BC + A'B'C

*Answer:*




F = A'B + A'C + AB'C'

**Q 2. [25 marks]**

**(i)** List 3 main functions of CPU (Central Processing Unit) **(03 marks)**

*Answer:*

Any 3 of following CPU functions

- Fetch instructions
- Interpret/decode instructions
- Fetch data
- Process data
- Write data
- Any others

**(ii)** Briefly explain 3 types of DMA (Direct Memory Access) configurations. **(06 marks)**

*Answer:*

1.Single-bus, detached DMA –I/O configuration:

Answer points

- All modules share the same system bus
- Each transfer uses bus twice (I/O to DMA then DMA to memory)
- CPU is suspended twice
- Inexpensive but inefficient

2. Single-bus, Integrated DMA- I/O configuration:

Answer points

- Number of required bus cycle can be reduced
- DMA controller may support more than once device (May be a part of an I/O module. May be separate module that controls one or more I/O s.)
- Each transfer uses bus once. (DMA to memory)
- CPU is suspended once

3. Using separate I/O bus:

Answer points

- I/O modules are connected to the DMA through another I/O bus. In this case the DMA module is reduced to one
- Separate I/O bus
- Each transfer uses bus once
- Bus supports all DMA enabled devices
- Processor is not suspended when the data is transferred between I/O module and DMA module
- Processor is suspended when the data is transferred between DMA module and memory

**(iii)** Briefly explain followings

**a)** Indirect cycle **(02 marks)**

**b)** IR (Instruction Register) **(02 marks)**

**c)** PC (Program Counter) **(02 marks)**

**d)** MBR (Memory Buffer Register) **(02 marks)**

*Answer:*

a) Indirect cycle – Same address can refer to different arguments. Can be thought of as additional instruction sub cycle.

b) IR – Part of a CPU's control unit that holds the next instruction to be executed having been fetched from the memory.

c) PC – Part of a CPU's control unit which holds the address of the next instruction to be executed in the program.

d) MBR – which holds either the data just read from the memory or data ready to be written to memory.

**(iv)** In the design of computers, an instruction pipeline is a technique which is used to increase the instructions throughput of computer. Pipelining consists of 6 six stages.

**a)** State 2 stages of pipelining. **(02 marks)**

**b)** Explain 3 types of pipeline hazards. **(06 marks)**

*Answer:*

a) Any 2 of followings

1. Fetch instruction
2. Decode instruction
3. Calculate operands (i.e., EAs)
4. Fetch operands
5. Execute instructions
6. Write result

b)

- Structural hazards
  Arise from resource conflicts when the hardware can't support all possible combinations of overlapping instructions.
- Data hazards
  Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline.
- Control hazards
  Arise from the pipelining of branches and other instructions that change the PC (Program Counter).

**Q 3. [25 marks ]**

**(i)** Capacity of a DVD-ROM is high compared to a physically same size CD-ROM. What is the technology behind this? **(03 marks)**

*Answer:*

Bits are packed more closely on a DVD. The spacing between loops of a spiral (tracks) on a DVD is less compared to a CD. TheDVDuses a laser with shorter wavelength. DVD also has layer technology.

**(ii)** Define the terms, "**Seek time**", "**Rotational delay**", and "**Transfer rate**" in hard disk operation. **(06 marks)**

*Answer:*

**"Seek time"** the time it takes for a disk arm to position itself over the required track.

**"Rotational delay"** is the delay waiting for the rotation of the disk to bring the required disk sector under the read-write head.

**"Transfer rate"** is the speed at which data is transferred to and from the disk media (actual disk platter) and is a function of the recording frequency.

**(iii)** Suppose a harddisk drive has the following characteristics

- 4 platters
- 1024 tracks per surface
- 128 sectors per track
- 512 bytes per sector
- Average seek time = 5 ms
- Disk rotational speed = 5000 rpm

**a)** What is the capacity of theharddisk? **(02 marks)**

**b)** Calculate the data transfer rate. **(02 marks)**

**c)** Calculate the average rotational latency. **(02 marks)**

**d)** Calculate the access time. **(02 marks)**

*Answer:*

a) Capacity of the disk = 4x128x1024x512 = 268435456 bytes = 256 Mb

b) Data transfer rate = 5000/60 x4x128x512 = 21845333 B/sec = 20.83 Mb/sec

c) Average rotational latency = [ (60/5000) x1000] / 2 = 6 ms

d) Access time = 5 ms + 6 ms = 11 ms

**(iv)** In computer architecture, the Memory hierarchy separates computer storage into a hierarchy based on response time.

**a)** What memory type has the fastest response as well as it is at the top of the memory hierarchy? **(02 marks)**

**b)** Compare and contrast SRAM and DRAM. **(06 marks)**

*Answer:*

a) Registers

b)

Static RAM (SRAM)

- Each cell stores bit with a six-transistor circuit.
- Retains value indefinitely, as long as it is kept powered.
- Relatively insensitive to disturbances such as electrical noise.
- Faster and more expensive than DRAM.

Dynamic RAM (DRAM)

- Each cell stores bit with a capacitor and transistor.
- Value must be refreshed every 10-100 ms.
- Sensitive to disturbances.
- Slower and cheaper than SRAM.

(Any of three compression 2x3 =6 marks)

**Q 4. [ 25 marks]**

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**(i)** List 3 major functions of I/O (Input/output) module. **(03 marks)**

*Answer:*

Any 3 out of following 5

1. Control and timing
2. CPU communication
3. Device communication
4. Data buffering
5. Error detection

**(ii)** Describe the purpose of using "cache memory" and "virtual memory"

**(06 marks)**

*Answer:*

**Cache memory** is a type of memory that lies between the CPU (Central Processing Unit) and the RAM (Random Access memory). The purpose of cache memory is to reduce the memory access time of the CPU from the RAM. The cache memory is much faster than RAM. So access time on cache is much lesser than the access time on RAM.

**Virtual memory** is a memory management technique used in computers systems. The purpose of virtual memory is **to use the hard disk as an extension of RAM**, thus increasing the available address space a process can use.

**(iii)** Compare and contrast CISC and RISC by using at least four features of them.

**(08 marks)**



*Answer:*

| CISC | RISC |
|---|---|
| Emphasis on hardware. | Emphasis on software. |
| Includes multi-clockcomplex instructions. | Single-clock,reduced instruction only. |
| Memory-to-memory:"LOAD" and "STORE"incorporated in instructions. | Register to register:"LOAD" and "STORE" are independent instructions. |
| Small code sizes,high cycles per second. | Low cycles per second,large code sizes. |
| Transistors used for storingcomplex instructions. | Spends more transistorson memory registers. |

Any of four (2x4)

**(iv)** **a)** Explain the term of "Multiprogramming". **(02 marks)**

**b)** Calculate the average waiting time for the processes given below by uising Round Robin algorithm. **(06 marks)**

| Process | Arrival time (in seconds) | Service time (in seconds) |
|---|---|---|
| P1 | 0 | 5 |
| P2 | 1 | 3 |
| P3 | 2 | 8 |
| P4 | 3 | 6 |

*Answer:*

a) In a multiprogramming system there are one or more programs loaded in main memory which are ready to execute. Only one program at a time is able to get the CPU for executing its instructions (i.e., there is at most one process running on the system) while all the others are waiting their turn.

The main idea of multiprogramming is to maximize the use of CPU time. /

A number of programs can be in memory at the same time. Allows overlap of CPU and I/O.

b) Average wait time = (9 + 2 + 12 + 11) / 4 = 8.5

**Q 5. [ 25 marks ]**

**(i)** CPU scheduling decisions may take place under the four circumstances. State 3 of them. **(03 marks)**

*Answer:*

1. When a process switches from the **running** state to the **waiting** state(for I/O request or invocation of wait for the termination of one of the child processes).
2. When a process switches from the **running** state to the **ready** state (for example, when an interrupt occurs).
3. When a process switches from the **waiting** state to the **ready** state(for example, completion of I/O).
4. When a process **terminates**.

**(ii)** Consider the data given below regarding a CPU.

- Clock rate = 2.8
- Average cycles per instruction = 4
- Number of instructions in program = 400

What is the CPU execution time of this program ? **(06 marks)**

*Answer:*

$= 400 \times 4 \times \frac{1}{2.8 \times 10^9}$

**(iii)** There are many different criteria to check to consider considering the **best scheduling algorithm** in CPU scheduling. Briefly explain 4 of them.

**(08 marks)**

*Answer:*

- **Utilization**- The fraction of time a device is in use. ( ratio of in-use time / total observation time )
- **Throughput** - The number of job completions in a period of time. (jobs / second )
- **Service Time -** The time required by a device to handle a request. (seconds)
- **Queueing Time -** Time on a queue waiting for service from the device. (seconds)
- **Residence Time -** The time spent by a request at a device. (Residence Time = Service Time + Queueing Time).
- **Response Time-** Time used by a system to respond to a User Job. ( seconds )
- **Think Time -** The time spent by the user of an interactive system to figure out the next request. (seconds)

**(iv)**

**a)** What is the meaning of deadlock in operating system? **(02 marks)**

**b)** Explain 3 methods of handling deadlocks. **[06 marks]**

*Answer:*

a) A **deadlock** is a situation in which two computer programs sharing the same resource are effectively preventing each other from accessing the resource, resulting in both programs ceasing to function.

b)

1. Allow the system to enter a deadlock state and then recover.
2. Ensure that the system will never enter a deadlock state. The system can use either a deadlock prevention or avoidance.
3. Ignore the problem and pretend that deadlocks never occur in the system; used by most operating systems, including UNIX (need to restart your computer if a deadlock occur).