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SLIATE

SRI LANKA INSTITUTE OF ADVANCED TECHNOLOGICAL EDUCATION

(Established in the Ministry of Higher Education, vide in Act No. 29 of 1995)

Higher National Diploma inInformation Technology

2nd Year, First Semester Examination – 2014

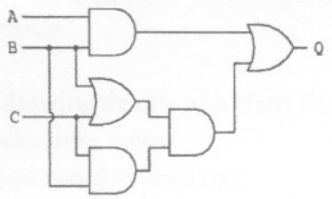
IT 3002 - Computer Architecture

Instructions for Candidates:
Answer only any 4 questions

No. of questions : 05
No. of pages : 04
Time : 2 hrs

Q1.

1. Write the Boolean expression for the following logic circuit. (05 Marks)



Consider the following truth table which is designed for a Full Adder.

Inputs			Outputs	
x	y	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2. Drive logic equations for Sum and Carry Out using the above truth table. (08 Marks)
3. Construct a logic circuit using XOR gates and basic gates for the Full Adder using the logic equations derived in b) above. (06 Marks)
4. Simplify the following Boolean function F using K-Map

   F = ABC + A'B'C' + AB'C + ABC' (06 Marks)

[Total 25]

Q2.

1. Briefly explain the following :
   (a) Program Counter
   (b) Flag Register / PSW
   (c) Memory Address Register
   (d) ALU

   (8Marks)
2. Briefly explain Opcode ?

   (2 Marks)
3. A CPU capable to perform 32 different instructions. How many bits needed to represent the opcode for this CPU?

   (4 Marks)
4. What is meant by fetch and execute cycles in CPU operations?

   (6Marks)
5. Explain briefly how CPU handles an interrupt operation.

   (5Marks)

   [Total 25]

Q3.

1. What is mean by instruction pipelining?

   (3 Marks)
2. State weather the following statements are true or false?
   a. Execution time of an instruction will be increased by Pipelining. (True/False)?
   b. Execution time of a program will be increased by Pipelining. (True/False)?
   c. We can increase the performance of a CPU by Pipelining. (True/False)?
   d. We can increase the clock speed of a CPU by Pipelining. (True/False)?

   (4x1=4 Marks)
3. "Pipelining will always increases performance" do you agree? Explain?

   (4 Marks)
4. What are the three types of hazards related to pipelining?

   (6 Marks)
5. Consider the following information about a CPU architecture:
   Number of pipeline stages =5
   clock cycles needed to perform each pipeline stage=3
   If a program has 50 instructions without any branch or loops, calculate the number of clock cycles required to execute the program?

   (8 Marks)

   [Total 25]

Q4.

1. If I = number of instructions in a program, CPI = average cycles per instruction And T = clock cycle time,

(a) Define CPU Execution Time in terms of I, CPI and T

(5 Marks)

Consider the data given below:

Clock Rate = 3 GHz

Average Cycles per Instruction = 3

Number of instructions in a program = 310

(b) Calculate clock cycle time?

(4 Marks)

(c) Calculate the CPU execution time of this program?

(4Marks)

2. Briefly explain "Seek Time" , "Rotational latency (delay)" and Access time of hard disk drive operation.

(6 Marks)

3. Consider the following details of a Hard Disk

Average seek time = 6ms.

Disk rotation speed = 7600 rpm

512 bytes/sector

300 sectors/track (on average)

20,000 tracks/surface

Disk has 3 platters

(a) Calculate the average rotational latency

(b) Calculate the capacity of this hard disk

(c) Calculate the total time needed to read 150KB data file (assume the file is not fragmented)

(6 Marks)

[Total 25]

Q5.

1. Why process scheduling is important?

(3 Marks)

2. What is the difference between preemptive and non-preemptive scheduling?

(4 Marks)

3. Describe FCFS and Round Robin scheduling algorithms?

(6 Marks)

4. Using **preemptive shortest job first** algorithm, indicate the order of execution of each process in a time line and calculate the average waiting time for the processes given below.

Process	Arrival Time (in Sec)	Service Time (In Sec)
P1	0	7
P2	2	4
P3	4	1
P4	5	4
P5	15	6

(8 Marks)

5. What is mean by deadlock?

(4 Marks)

[Total 25]