Some More Practice Questions

1. Name two components of a modern super scalar processor whose delay scales quadratically with the issue width?
2. Why is it necessary to have a Load Store Queue on out of order processors?
3. Name one advantage and one disadvantage of VLIW compared to superscalar processors
4. Compare the scalability of VLIW and superscalar processors as ILP increases.
5. Explain why binary compatibility is a major challenge for VLIW architectures. Suggest one mechanism that could mitigate this issue.
6. Describe the role of VMASK registers in handling conditional operations within VLIW architectures that incorporate vector processing.
7. Role of Strip Mining
8. Why Chaining
9. Using MMX, SSE2/3/4 etc. For example, In the context of Intel's MMX instruction set, explain how packed integer operations can be utilized to accelerate multimedia applications, such as image processing.
10. Design a dynamic dataflow graph for a simple 1-D FIR filter:

$$y[n] = \sum_{k=0}^{M-1} h[k] \cdot x[n-k]$$

    Explain how token matching ensures correctness when multiple samples are in flight, and propose a hardware mechanism for matching.

11. Consider a dynamic dataflow machine that supports multiple tokens per arc. Design a *matrix multiplication kernel* in a dataflow model.