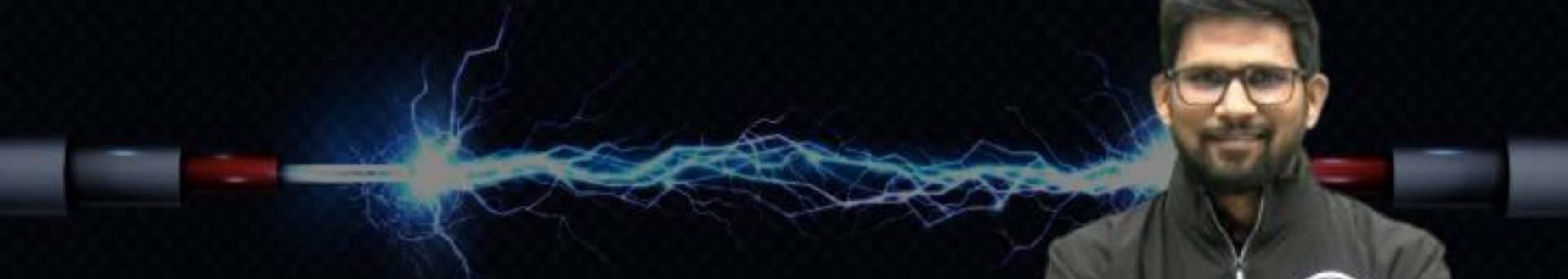


COMPUTER SCIENCE & IT

DIGITAL LOGIC




Lecture No. 02

Combinational Circuit



By- Chandan Gupta Sir



Recap of Previous Lecture

H.A. , F.A



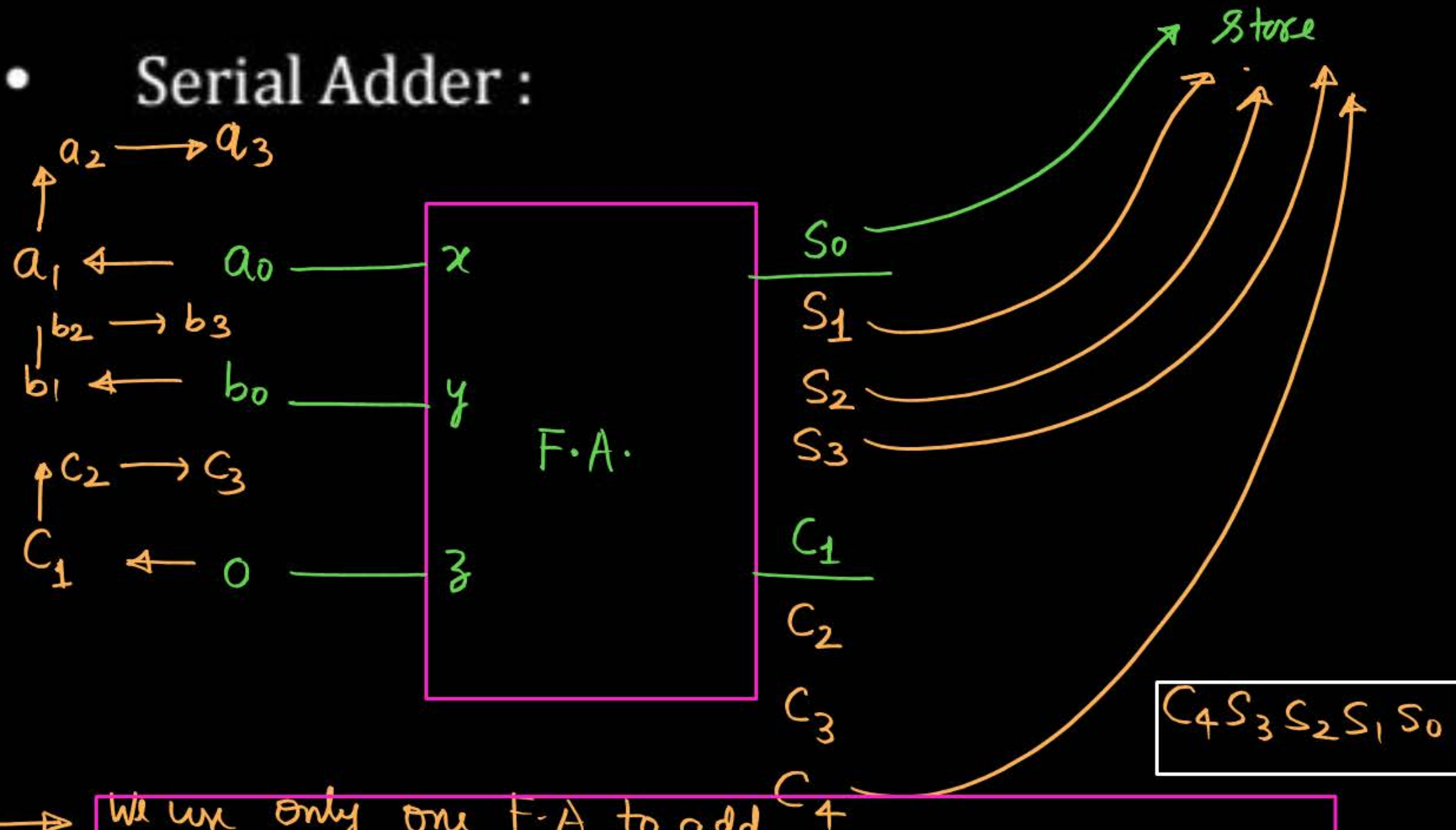


Topics to be Covered

F.A Cont.

H.S., F.S.

Serial Adder :



→ We use only one F.A to add two n -bit numbers and addition is performed serially and due to this delay is very high in serial adder to complete one addition.

$$A = a_3 a_2 a_1 a_0$$

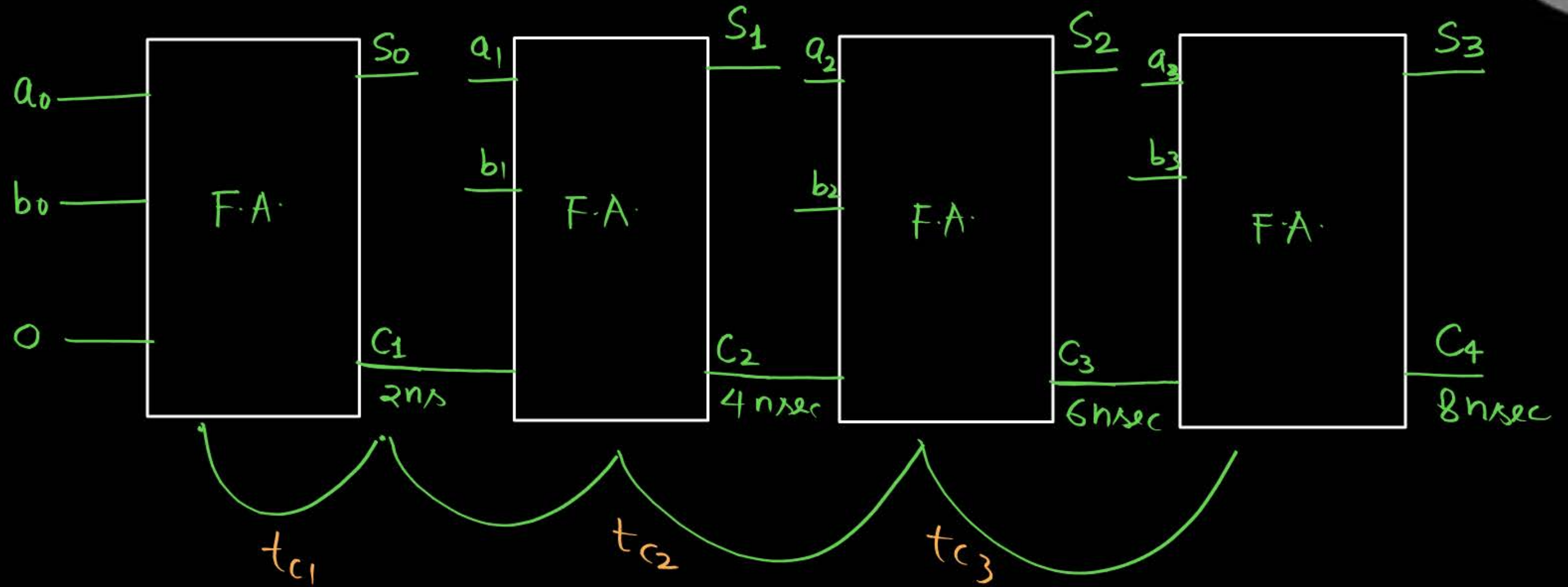
$$B = b_3 b_2 b_1 b_0$$

$$+ C_3 C_2 C_1 0$$

$$C_4 S_3 S_2 S_1 S_0$$

↓
Final result of addition

- Parallel Adder : or ripple carry adder



Case-I

Each F.A has sum delay $t_s = 3\text{ns}$
& carry delay $t_c = 2\text{nsec}$

$$\begin{array}{rcccc} & 6\text{ns} & 4\text{ns} & 2\text{ns} & \\ & a_3 & a_2 & a_1 & \underline{\underline{a_0}} \\ + & & b_3 & b_2 & b_1 & \underline{\underline{b_0}} \\ & c_3 & c_2 & \underline{\underline{c_1}} & 0 \\ \hline c_4 & s_3 & s_2 & s_1 & s_0 \\ 8\text{ns} & 9\text{ns} & 7\text{ns} & 5\text{ns} & 3\text{ns} \end{array}$$

Overall delay $\Rightarrow T_d = \underline{\underline{9\text{ns}}}$

Case-II

Each F.A has sum delay $t_s = 1.5\text{ns}$
Carry delay $t_c = 2\text{nsec}$

$$\begin{array}{rcccc} & 6\text{ns} & 4\text{ns} & 2\text{ns} & \\ & a_3 & a_2 & a_1 & a_0 \\ + & & b_3 & b_2 & b_1 & b_0 \\ & c_3 & c_2 & c_1 & 0 \\ \hline c_4 & s_3 & s_2 & s_1 & s_0 \\ \underline{\underline{8\text{nsec}}} & 7.5 & 5.5 & 3.5 & 1.5\text{nsec} \\ & \text{nsec} & \text{nsec} & \text{nsec} & \end{array}$$

\Rightarrow Overall delay $T_d = 8\text{nsec}$

Overall delay $T_d = [t_{c1} + t_{c2} + t_{c3} + \dots + (n-1) \text{ F.A.}] + \max[t_{cn}, t_{sn}] \checkmark$

$$t_{c1} = t_{c2} = \dots = t_{cn} = t_c$$

$$t_{s1} = t_{s2} = \dots = t_{sn} = t_s$$

$$T_d = (n-1)t_c + \max(t_c, t_s)$$

↓ overall delay or worst case delay or maximum delay

↳ time taken to complete one complete addition of two n -bit numbers.

[Question 1]



We have to add two 4-bit numbers A and B using parallel adder. Sum delay and carry delay of each F.A. is 3-nsec and 2-nsec respectively, then time required to perform complete addition

- ☒ (a) 9 nsec
- (b) 8 nsec
- (c) 12 nsec
- (d) 20 nsec

$$t_s = 3 \text{ ns}$$

$$t_c = 2 \text{ ns}$$

$$T_d = 3t_c + \max(t_c, t_s) = 3 \times 2 + t_s = 9 \text{ nsec}$$

[Question 2]



If in above question sum delay is 2 nsec and carry delay is 3 nsec then time require to perform complete addition will be 12 nsec.

$$t_s = 2 \text{ ns}$$

$$t_c = 3 \text{ ns}$$

$$T_d = 3t_c + \max(t_c, t_s) = 9 + 3 = 12 \text{ nsec}$$

[Question 3]



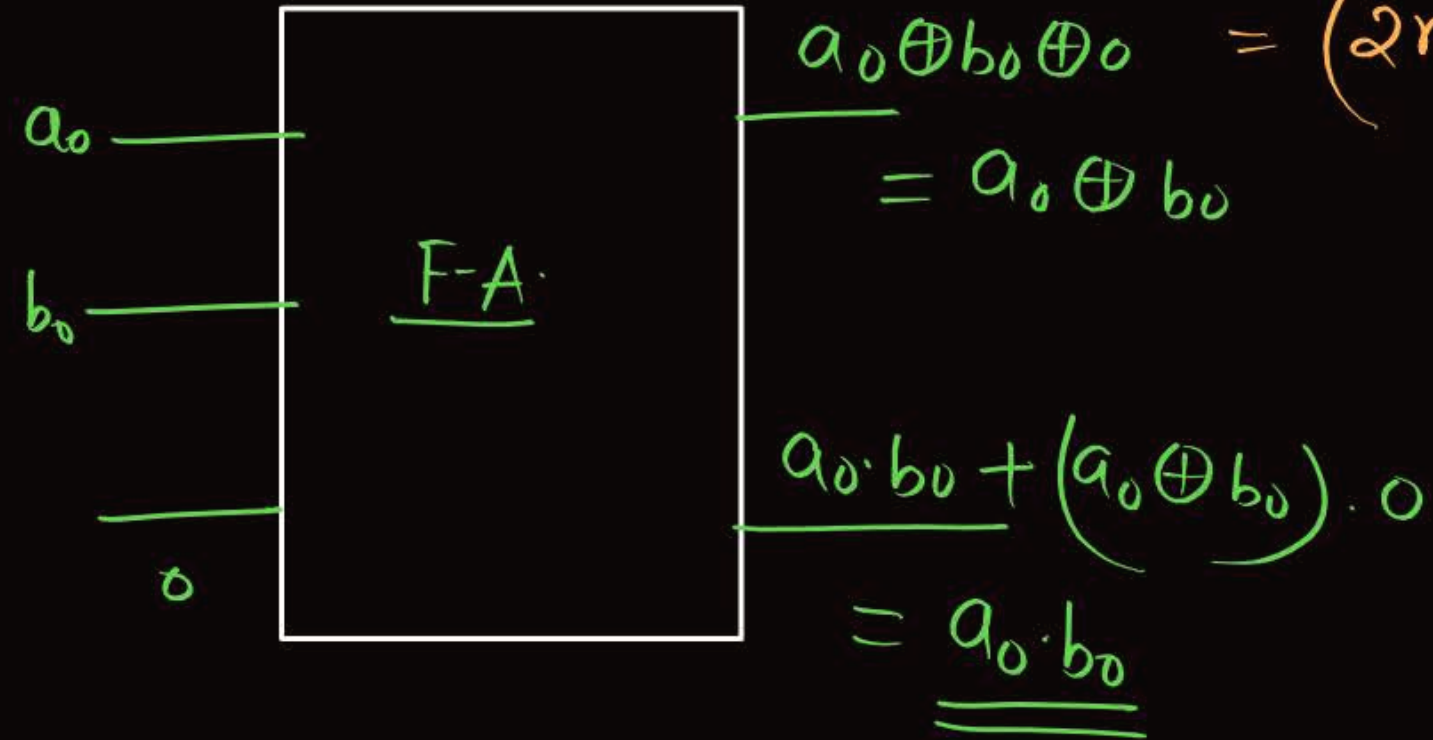
We have two 100 bit numbers added using parallel adder. Sum and carry delay of each F.A. used are 2.24 nsec and 1.24 nsec respectively, then number of addition performed by this parallel adder in 1 sec 8 $\times 10^6$ /sec.

$$\begin{array}{l} t_s = 2.24 \text{ ns} \\ t_c = 1.24 \text{ ns} \end{array} \longrightarrow T_d = 99t_c + \max(t_c, t_s) = 99 \times 1.24 + 2.24 = 125 \text{ ns}$$

$$\text{no. of addition in 1 sec } N = \frac{1 \text{ sec}}{125 \text{ nsec}} = \frac{1 \times 10^9 \text{ nsec}}{125 \text{ nsec}} = \underline{8 \times 10^6} \text{ additions}$$

To add two n -bit numbers, how many H.A's & OR gates required :

$a_3 a_2 a_1 a_0$
 $b_3 b_2 b_1 b_0$
 $c_3 c_2 c_1 c_0$



$$= (n-1) F.A + 1 H.A$$

$$= (n-1) [2 H.A + 1 OR] + 1 H.A$$

$$= 2(n-1) H.A + (n-1) OR + 1 H.A$$

$$= (2n-1) H.A + (n-1) OR$$

[Question 4]



To add two 4-bit numbers, minimum number of H.A.s require is m and minimum number of OR gates require is n then value of $(m + n)$ is 10.

$$\Rightarrow 3 \text{ FA} + 1 \text{ H.A}$$

$$6 \text{ H.A} + 3 \text{ OR} + 1 \text{ H.A}$$

$$7 \text{ H.A} + 3 \text{ OR}$$

$$m = 7$$

$$n = 3$$

$$(m+n) = \underline{\underline{10}}$$



2 Minute Summary

→ Delay in F.A.

Thank you

GW
Soldiers !

