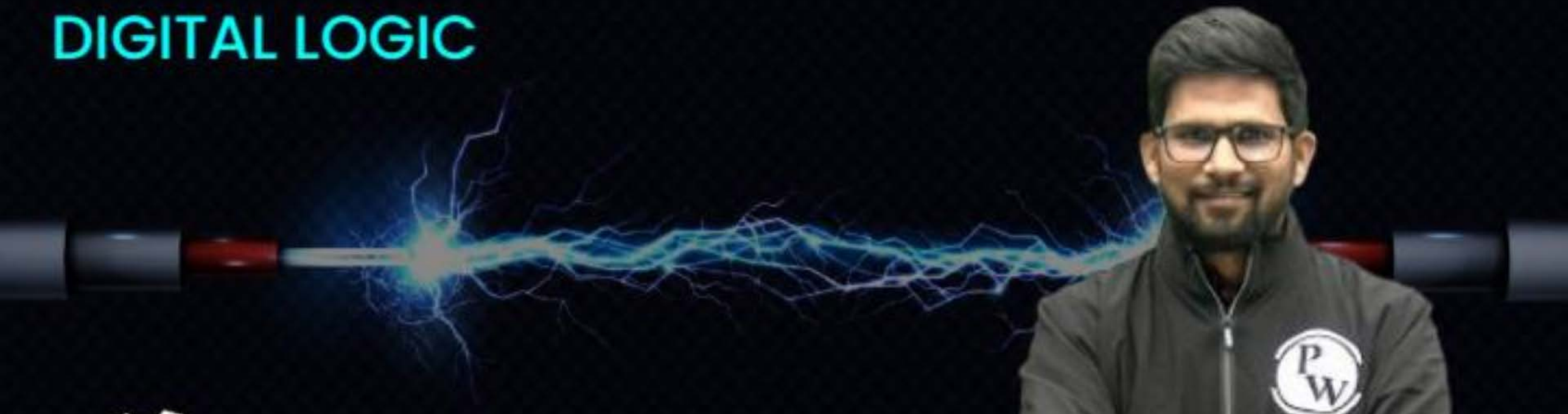
COMPUTER SCIENCE & IT

DIGITAL LOGIC



Lecture No: 07

Sequential Circuit

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Recap of Previous Lecture

- Questions on Synchronous Counter
- Ring Counter
-

- Ring Counter
- Johnson Counter

Self Starting Ring Counter Circuit

$Q_2(n+1) = Q_3(n)$

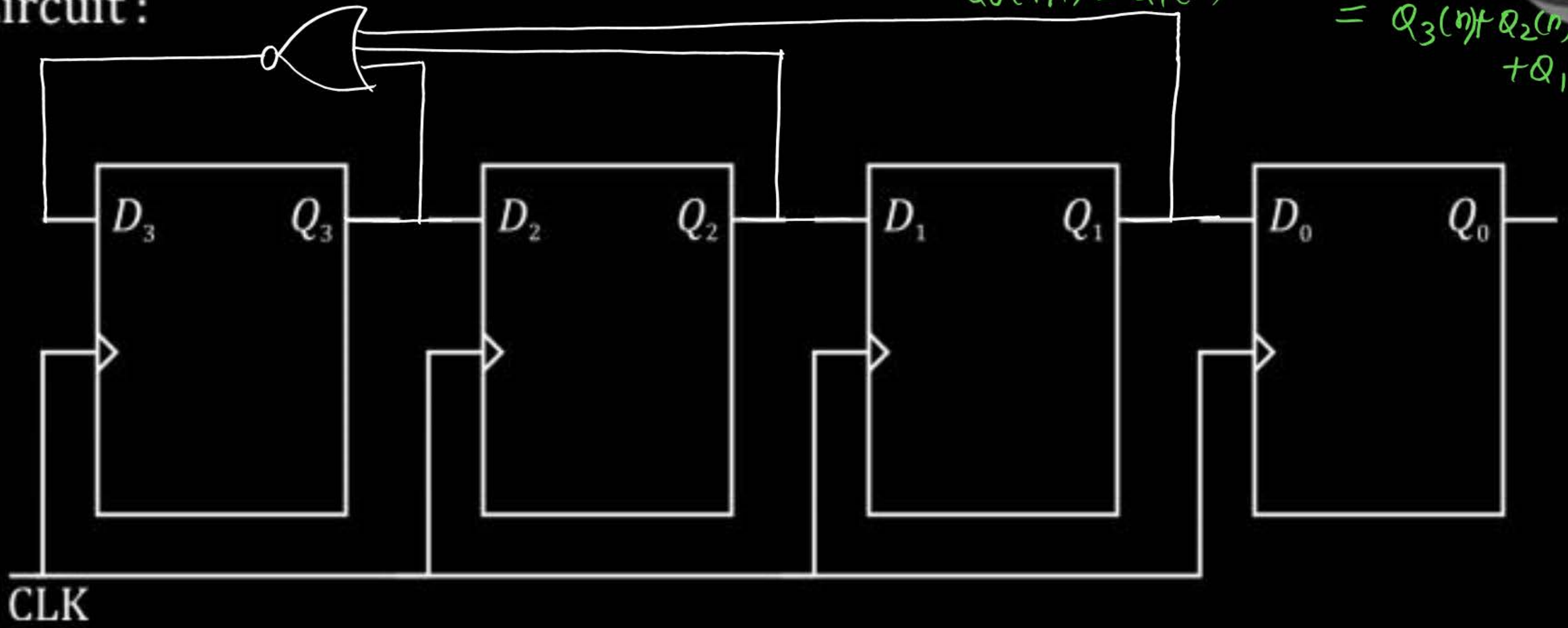
$Q_1(n+1) = Q_2(n)$

$Q_0(n+1) = Q_1(n)$

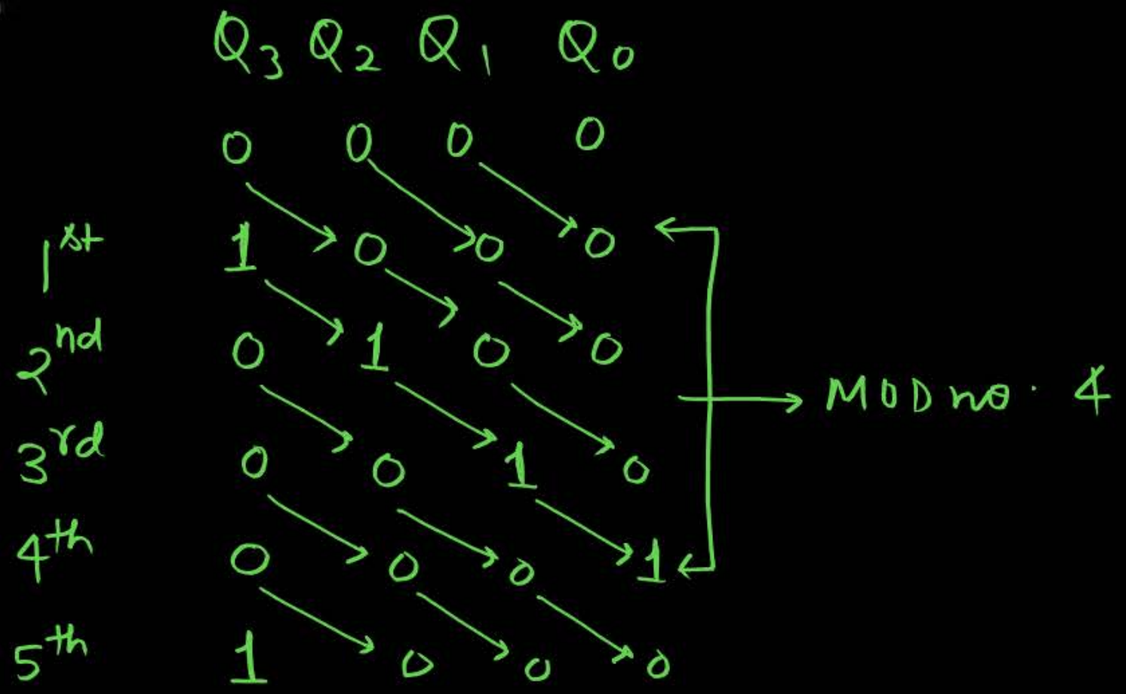
$Q_3(n+1) = D_3$

$= Q_3(n) + Q_2(n) + Q_1(n)$

Circuit :

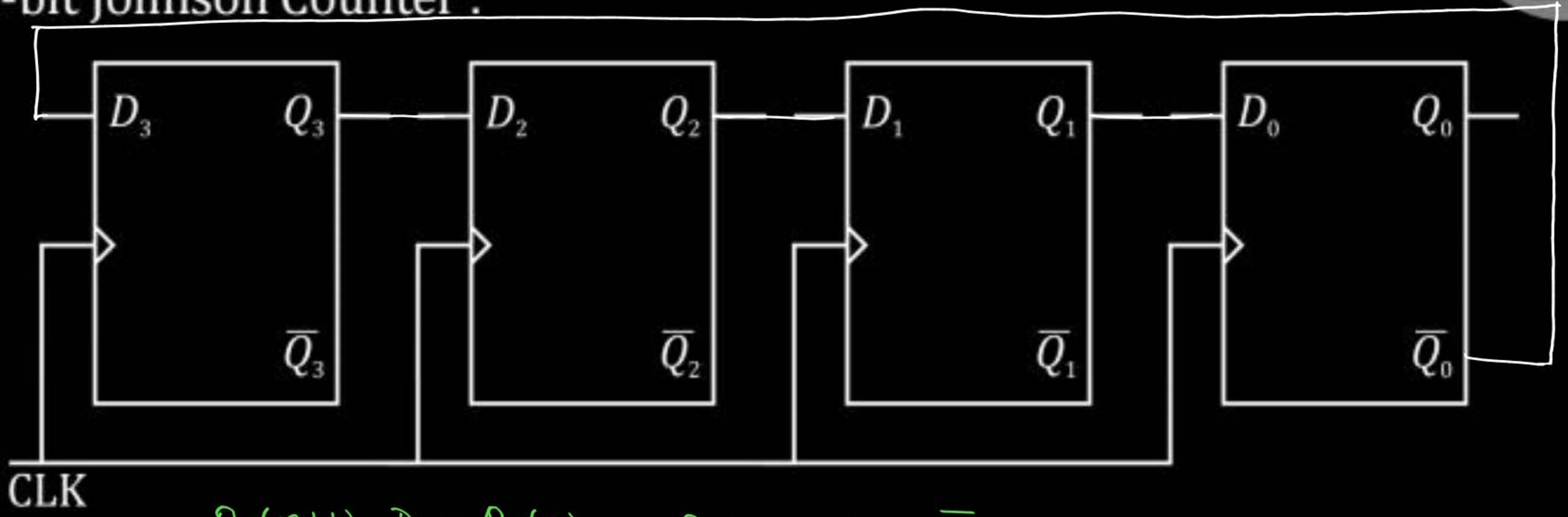


Working :


Q_3 Q_2 Q_1 Q_0
0 0 0 0
1st 1 0 0 0
2nd 0 1 0 0
3rd 0 0 1 0
4th 0 0 0 1
5th 1 0 0 0
MOD no. 4

Johnson Counter or Twisted Ring Counter

4-bit Johnson Counter :



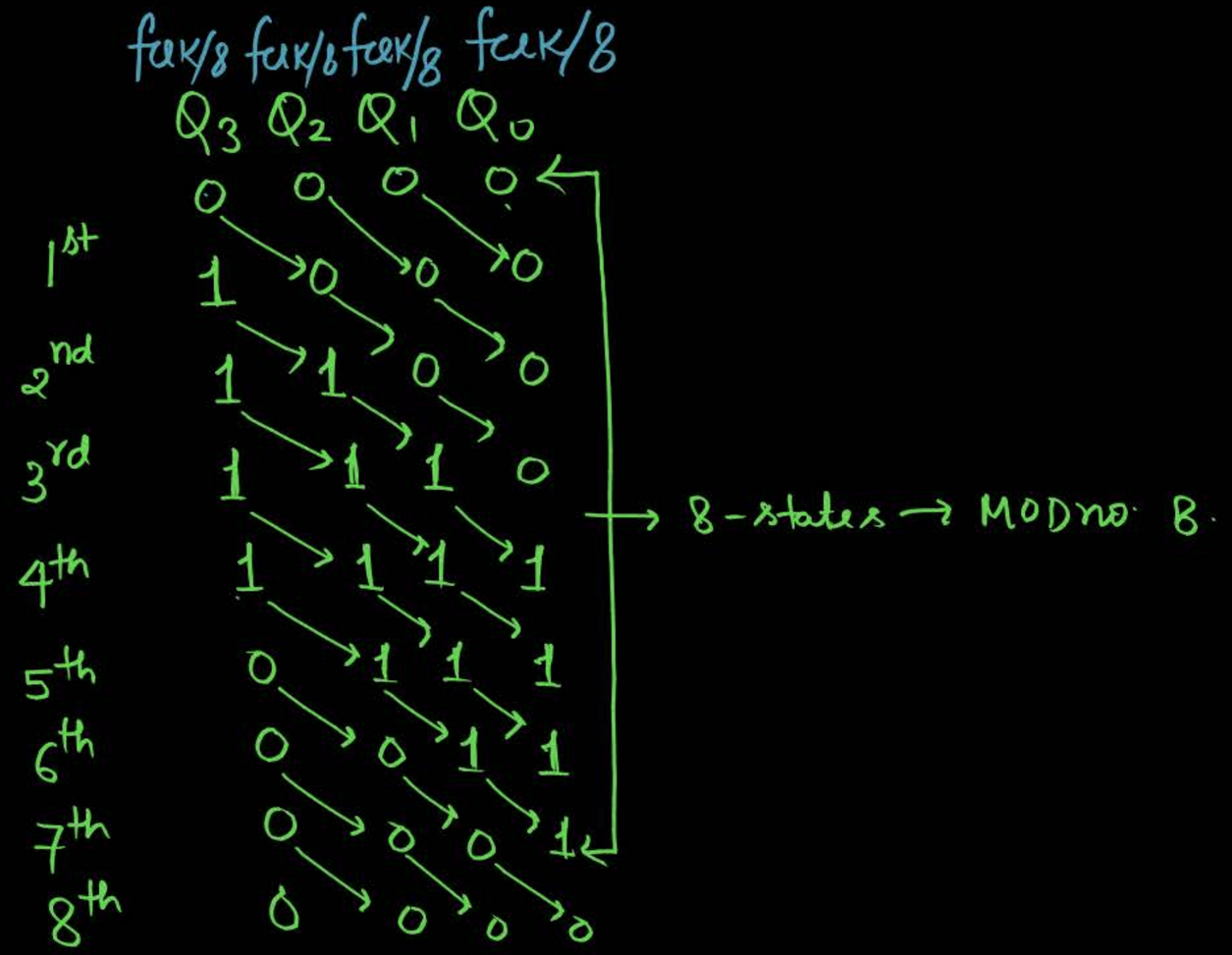
$Q_2(n+1) = D_2 = Q_3(n)$

$Q_1(n+1) = D_1 = Q_2(n)$

$Q_0(n+1) = D_0 = Q_1(n)$

$Q_3(n+1) = D_3 = \overline{Q}_0(n)$

Working :


fclk/8 fclk/8 fclk/8 fclk/8
Q3 Q2 Q1 Q0
1st
2nd
3rd
4th
5th
6th
7th
8th
8-states → MOD no. 8.

Imp points of Johnson Counter : →

- MOD no. of the Johnson counter designed with n-FF $= 2n$
- No. of unused states $= 2^n - 2n$
- Frequency (Clock frequency) is divided by MOD no. at each O/P.

- Duty cycle of the O/P waveform at each O/P will be 50% [$T_{ON} = nT_{clk}$, $T_{off} = nT_{clk}$ at each O/P

$T_Q = 2nT_{clk} \rightarrow f_Q = \frac{f_{clk}}{2n}$

$\%\ \text{duty cycle} = \frac{T_{ON}}{T_{ON}+T_{off}} \times 100\% = 50\%$

While duty cycle of each wave form in ring Counter will be

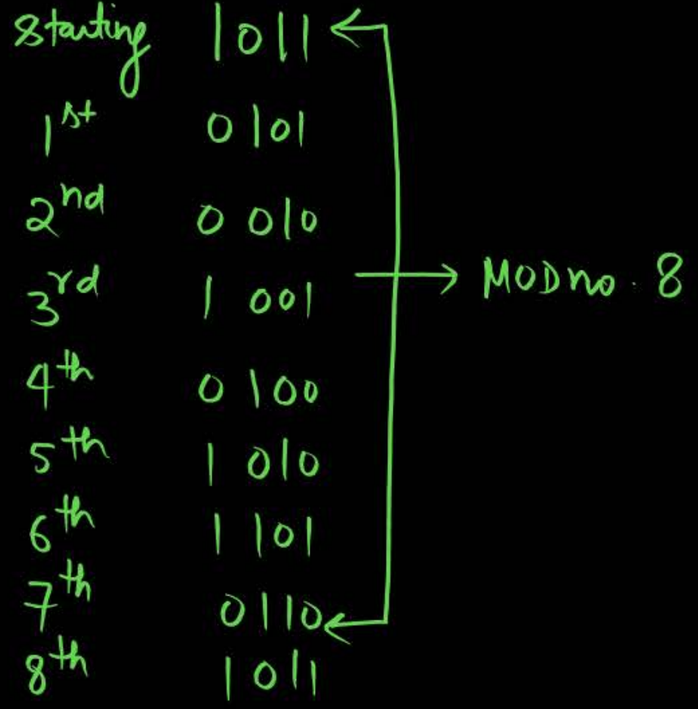
$T_{ON} = 1T_{clk}$, $T_{off} = (n-1)T_{clk}$ → at each O/P

$\%\ \text{duty cycle} = \frac{1T_{clk}}{nT_{clk}} \times 100\% = \frac{1}{n} \times 100\%$

1 0 1 1 0 1 ⟶ 0 1 0 1 1 0 ⟶ 1 0 1 0 1 1

Question

We have 4-bit Johnson counter. Its starting state is $(1011)_2$. Then it will be in what state after 22 CLK pulses $(\ 13\ )_{10}$.



$(1011)_2 \xrightarrow{2\times 8} (1011)_2 \xrightarrow{6\ CLK} (1101)_2$

$(8-5-2-9-4-10-13-6)$.

Question

We have 3-bit Johnson counter whose starting state is $(010)_2$. If input clock frequency 12 MHz then value of output frequency will be

(a) 6 MHz

$$f_{out} = \frac{f_{clk}}{\text{MOD no}} = \frac{12\ \text{MHz}}{2} = 6\ \text{MHz}$$

	0 1 0	← MOD no. 2
1st	1 0 1	←
2nd	0 1 0	

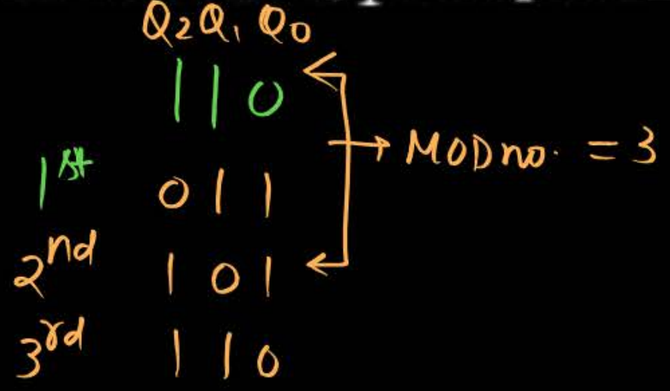
(b) 2 MHz

(c) 4 MHz

(d) 8 MHz

Question

In a 3-bit ring counter with starting state $Q_2Q_1Q_0 = (110)_2$, then duty cycle of the waveform generated at Q_1 output _____%.



$Q_1 \rightarrow T_{ON} = 2T_{clk}$

$T_{OFF} = T_{clk}$

$\rightarrow T_{Q_1} = 3T_{clk}$

$f_{Q_1} = f_{clk}/3$

$\%$ duty cycle $= \dfrac{2T_{clk}}{3T_{clk}} \times 100$

$= 66.67\%$

Shift Register

For what purpose shift registers are used ?

Registers ⟶ to store the information

Shift registers ⟶ Input & Output mechanism involves shifting operation and that's why called shift registers.

- Types of shift registers :

→ Serial IN – Serial OUT (SISO)

→ Serial IN – Parallel out (SIPO)

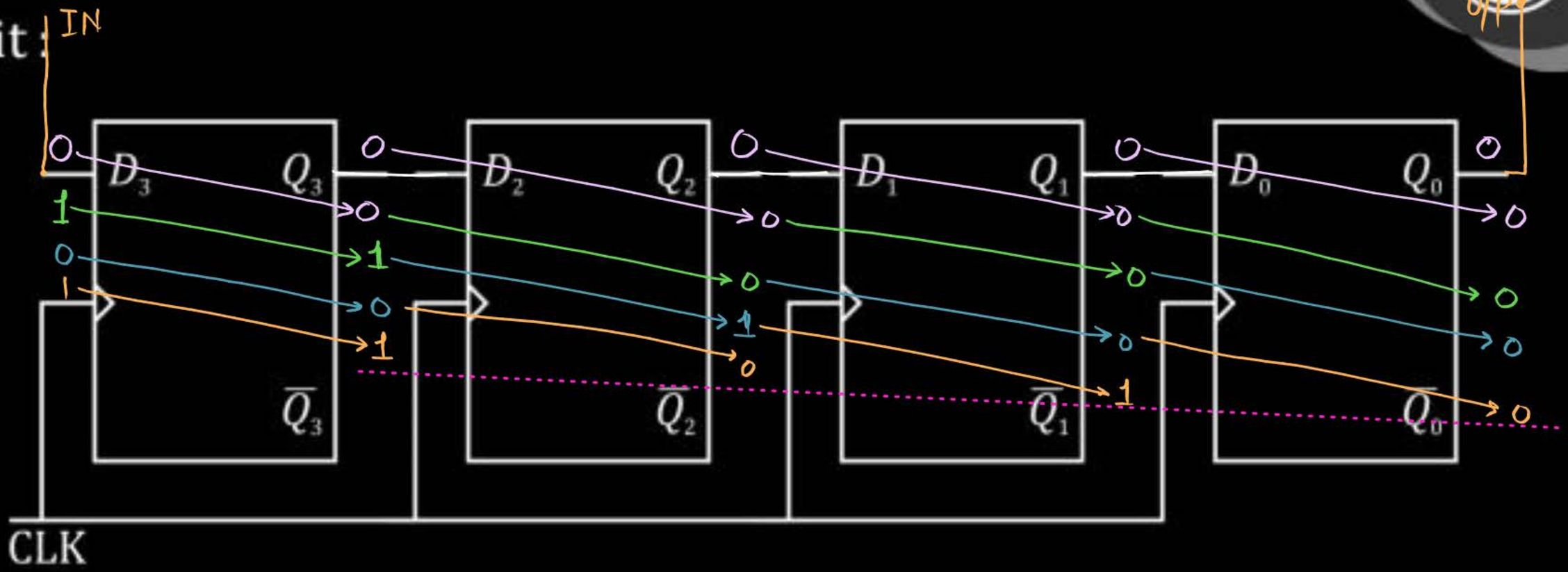
→ Parallel IN – Parallel out (PIPO)

→ Parallel IN – Serial Out (PISO)

1. SISO : 4 bit

1010

Circuit :



1st
2nd
3rd
4th

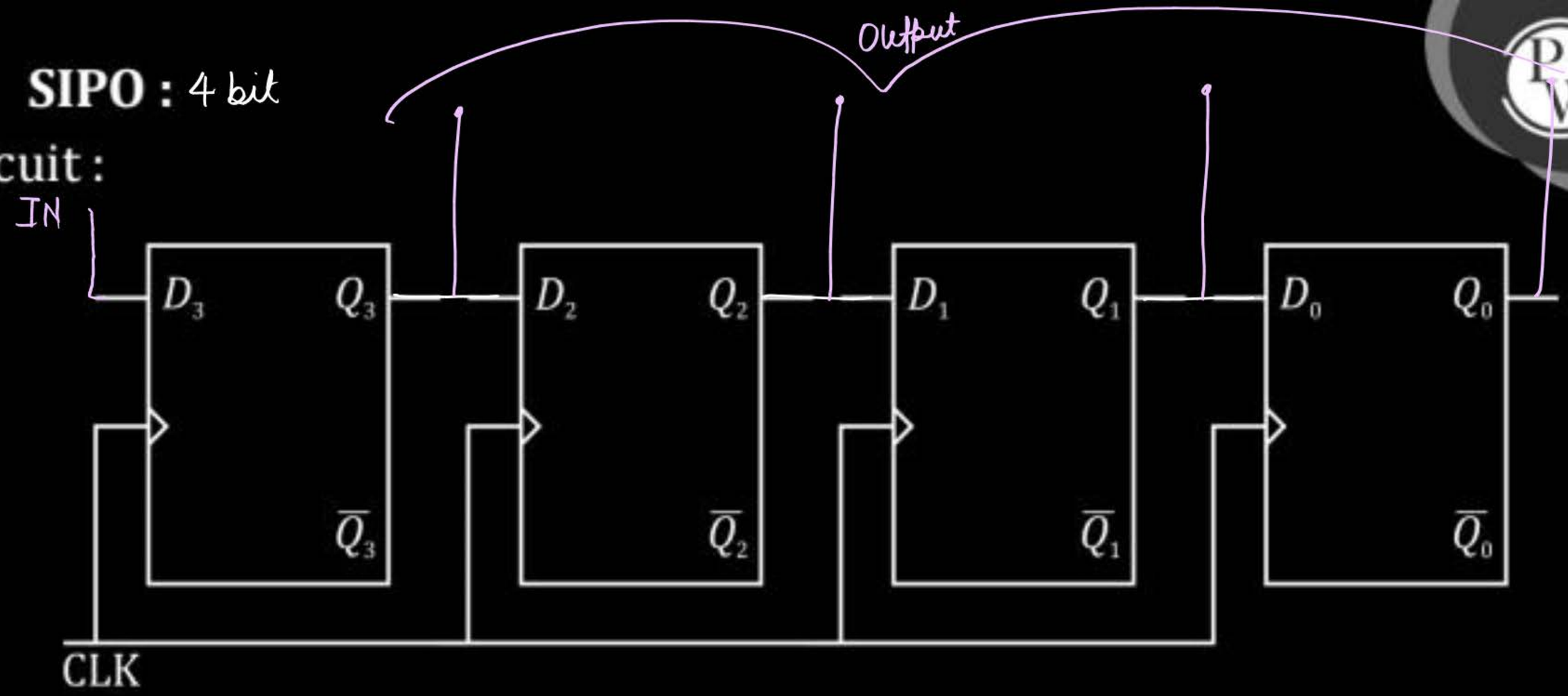
IMP Points :

n-bit SISO

- In SISO register, we require n-clk pulses [nT_{clk}] for serially storing (IN) the data.
- In SISO register, we require (n-1) clk pulses [$(n-1)T_{clk}$] for serially accessing (Out) the data.

2. SIPO : 4 bit

Circuit :



Serial IN → 4 CLK pulses

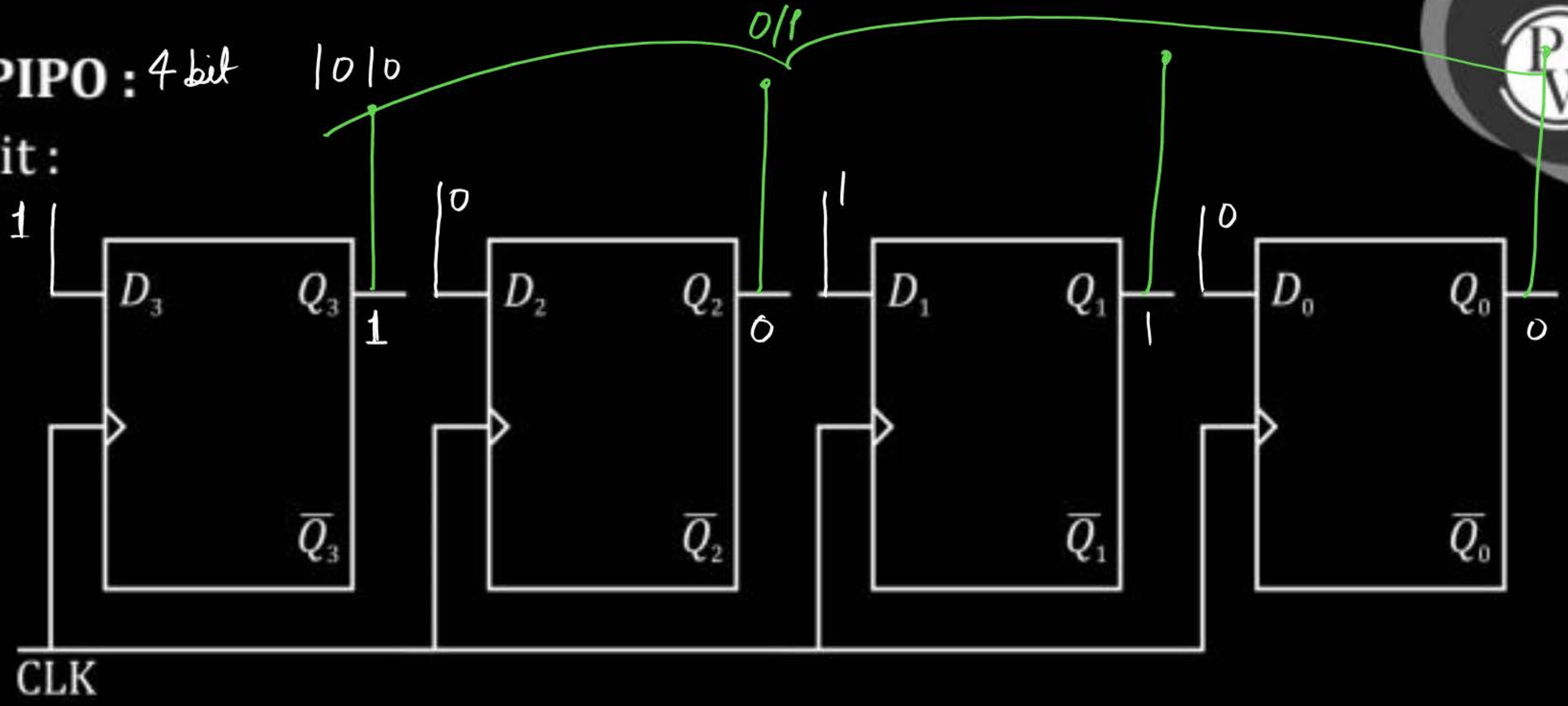
IMP Points :

n-bit SIPO

- We require n-clock pulses [n-Tclk] for serially storing the n-bit data.
- We require 0-clock pulses [0-Tclk] for parallely accessing the n-bit data.

3. PIPO : 4 bit

Circuit :



1st

IMP Points : n-bit PIPO

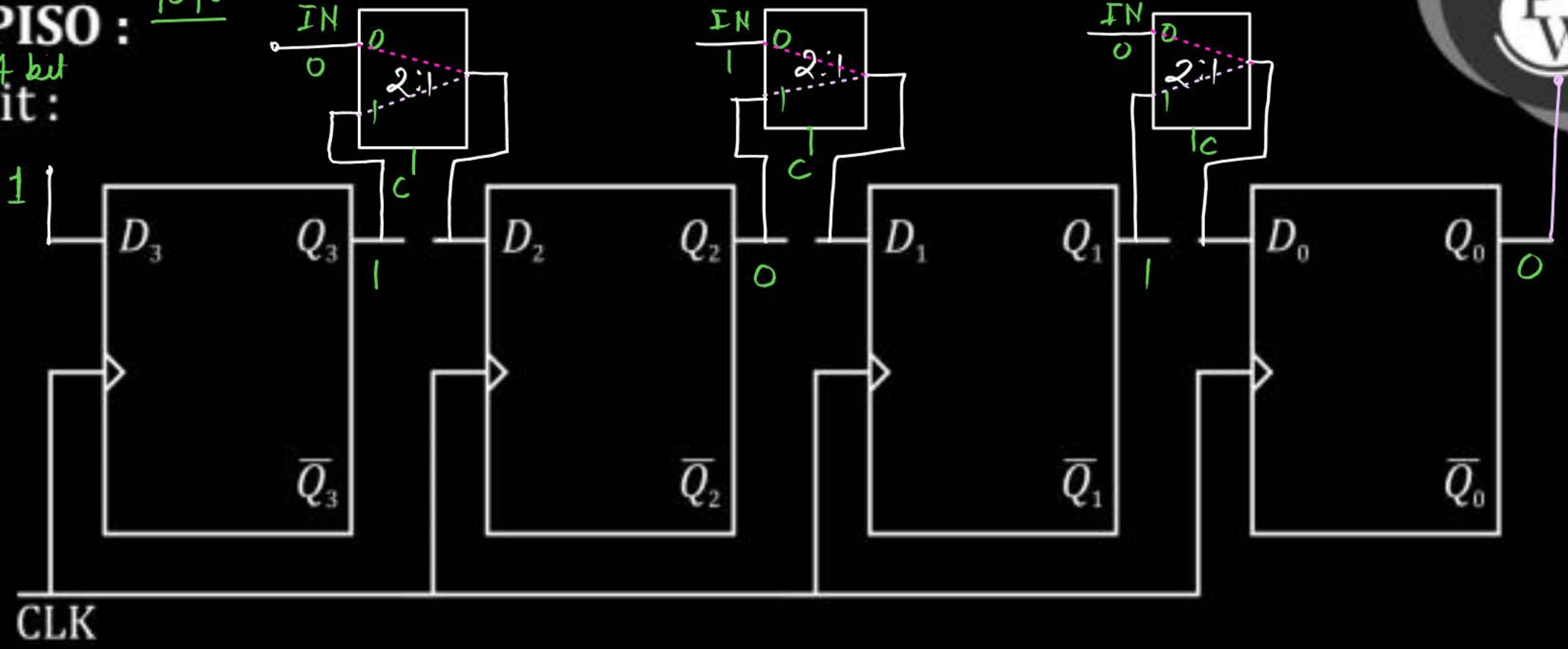
For storing n-bit data parallelly we require 1-clock [1Tclk].

For accessing n-bit data parallelly we require 0-clock [0Tclk]

4. PISO : 1010

4 bit

Circuit :



Control i/p C = 0 for writing data

1st clock

Control i/p C = 1 for accessing / reading data

IMP Points :

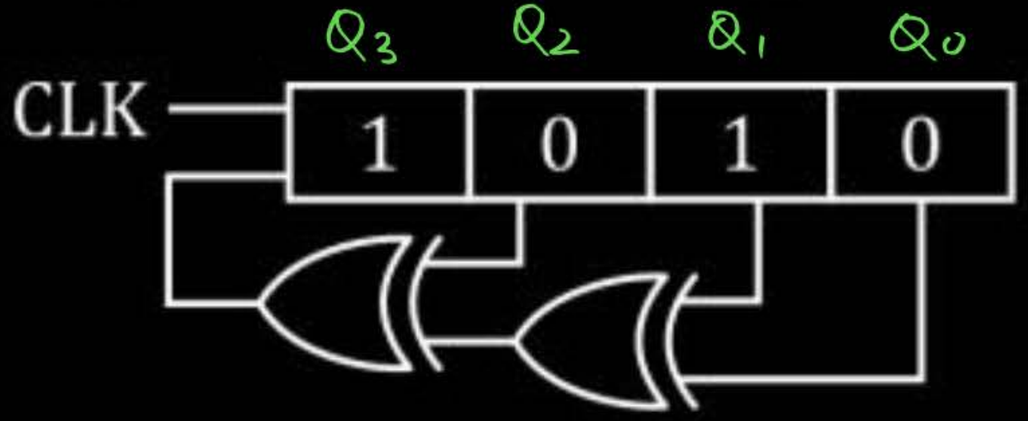
For parallel storing n-bit data, we require 1-clock [1-Tclk].

For serially accessing n-bit data, we require (n-1) clock [(n-1) Tclk].

Register	IN	OUT
SISO	n-Tclk	(n-1) Tclk
SIPO	n- Tclk	0 -Tclk
PISO	1-Tclk	(n-1) Tclk
PIPO	1 -Tclk	0- Tclk

Question

A four bit SIPO register is shown in fig. with starting state $(1010)_2$.



After application of how many clock pulses content of SIPO will again will be $(1010)_2$ 7

	Q_3	Q_2	Q_1	Q_0
	1	0	1	0
1st	1	1	0	1
2nd	0	1	1	0
3rd	0	0	1	1
4th	0	0	0	1
5th	1	0	0	0
6th	0	1	0	0
7th	1	0	1	0

$Q_2(n+1) = D_2 = Q_3(n)$

$Q_1(n+1) = D_1 = Q_2(n)$

$Q_0(n+1) = D_0 = Q_1(n)$

$Q_3(n+1) = D_3$

$= Q_2(n) \oplus Q_1(n) \oplus Q_0(n)$

Question

A 4-bit shift register circuit configured the right shift operation i.e. D_{in} – A, A – B, B – C, C – D is shown. If the present state of shift register is ABCD = $(1101)_2$, then the no. of clock cycle required to reach the state ABCD = $(1111)_2$ 10 .

	A	B	C	D
.	1	1	0	1
1st	0	1	1	0
2nd	0	0	1	1
3rd	1	0	0	1
4th	0	1	0	0
5th	0	0	1	0
6th	0	0	0	1
7th	1	0	0	0
8th	1	1	0	0
9th	1	1	1	0
10th	1	1	1	1

$$Q_3(n+1) = Q_3(n) \oplus Q_0(n)$$

$$Q_2(n+1) = Q_3(n)$$

$$Q_1(n+1) = Q_2(n)$$

$$Q_0(n+1) = Q_1(n)$$

Question

H.W.

Design a counter that follows the sequence :

0 – 1 – 3 – 2 – 1 – 0 → using D-FF

↓

MOD-5 Counter

Topic : 2 Min Summary

- Johnson Counter
- Shift register

Thank you

GW

Soldiers !