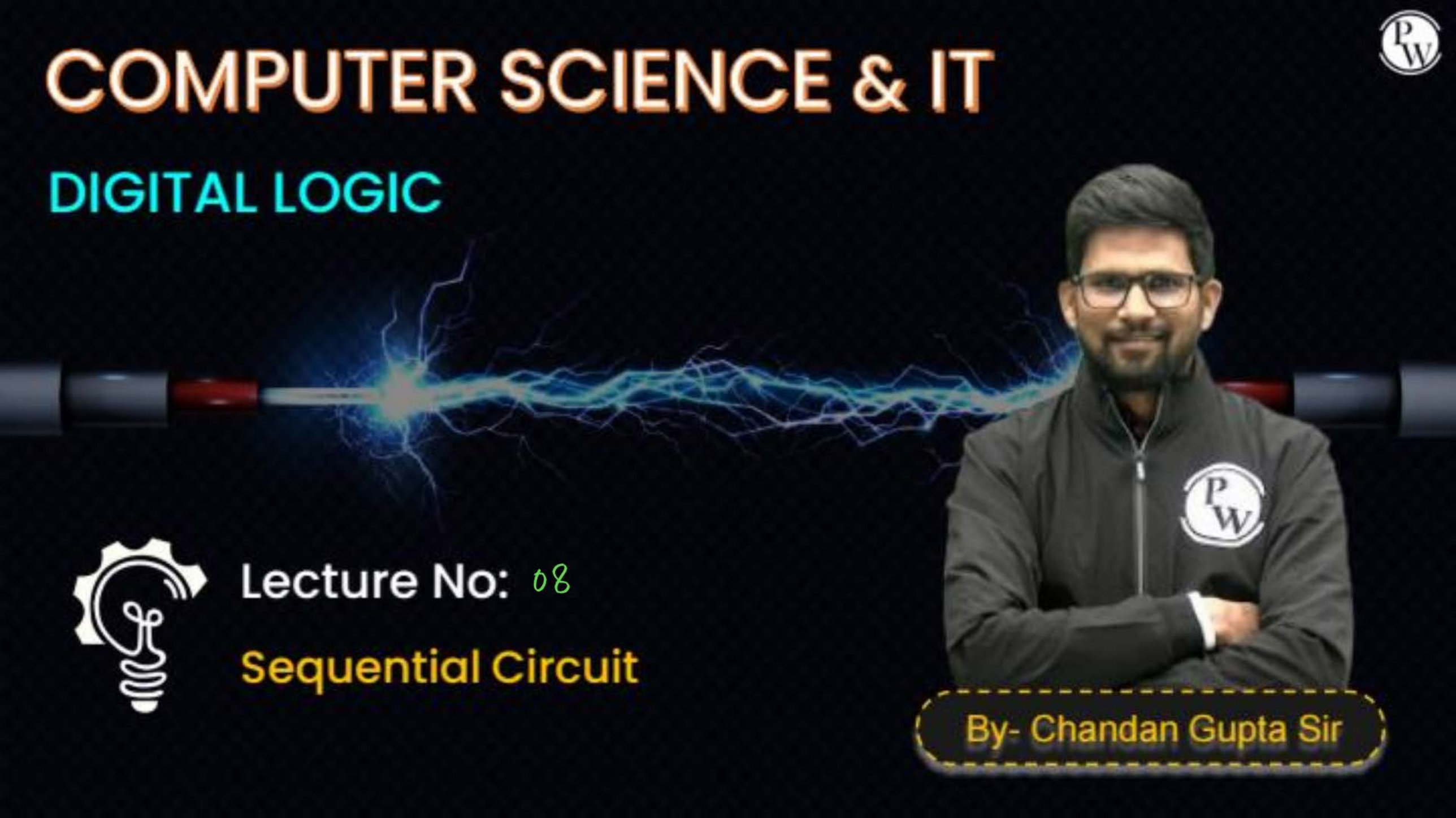
COMPUTER SCIENCE & IT

DIGITAL LOGIC



Lecture No: 08

Sequential Circuit

By- Chandan Gupta Sir

Recap of Previous Lecture

- Synchronous Counter
- Shift Register
-

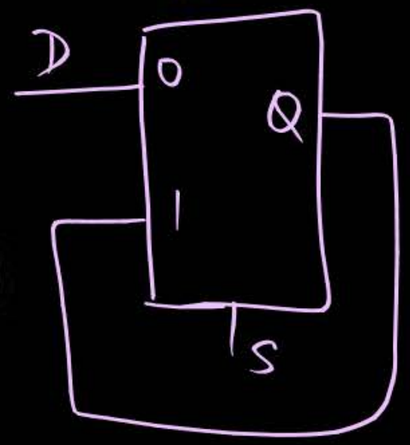
Question Discussion

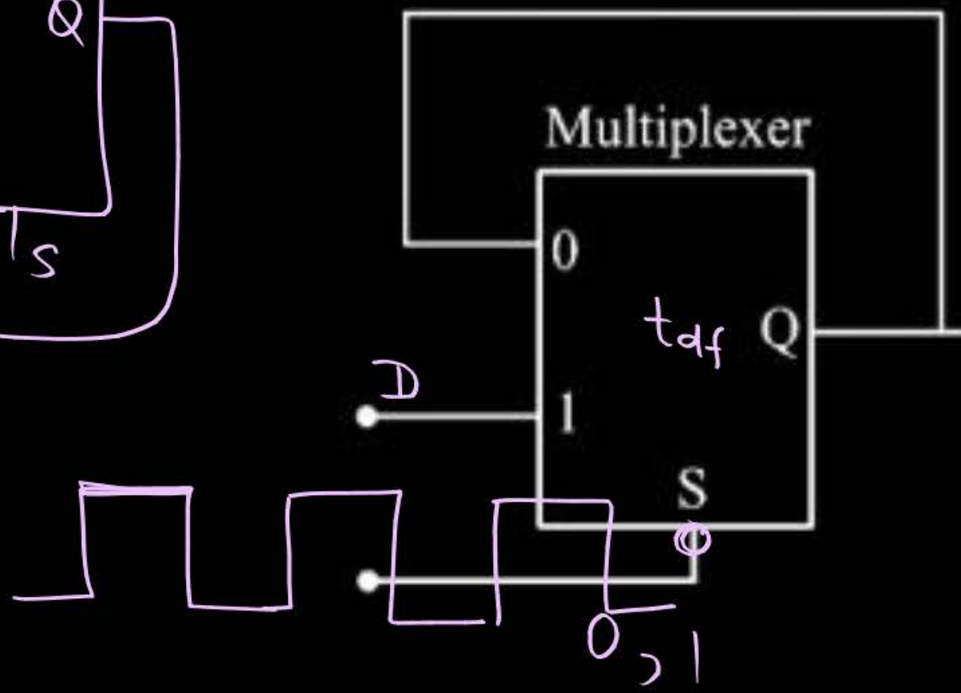
[MCQ]

The output of a 2-input multiplexer is connected back to one of its inputs as shown in the figure.

Match the function equivalence of this circuit to one of the following options.

[GATE-2023-CS: 1M]





A. D Flip-flop

B. D Latch

C. Half-adder ✗

D. Demultiplexer ✗

$S=0,\ Q(n+1)=Q(n)$

$S=1,\ Q(n+1)=D=I_1$

+ve level triggered D-FF

#Q. Given below is the diagram of a synchronous sequential circuit with one J-K flip-flop and one T flip-flop with their outputs denoted as A and B respectively, with $J_A = (A' + B')$, $K_A = (A + B)$, and $T_B = A$.
Starting from the initial state (AB = 00), the sequence of states (AB) visited by the circuit is

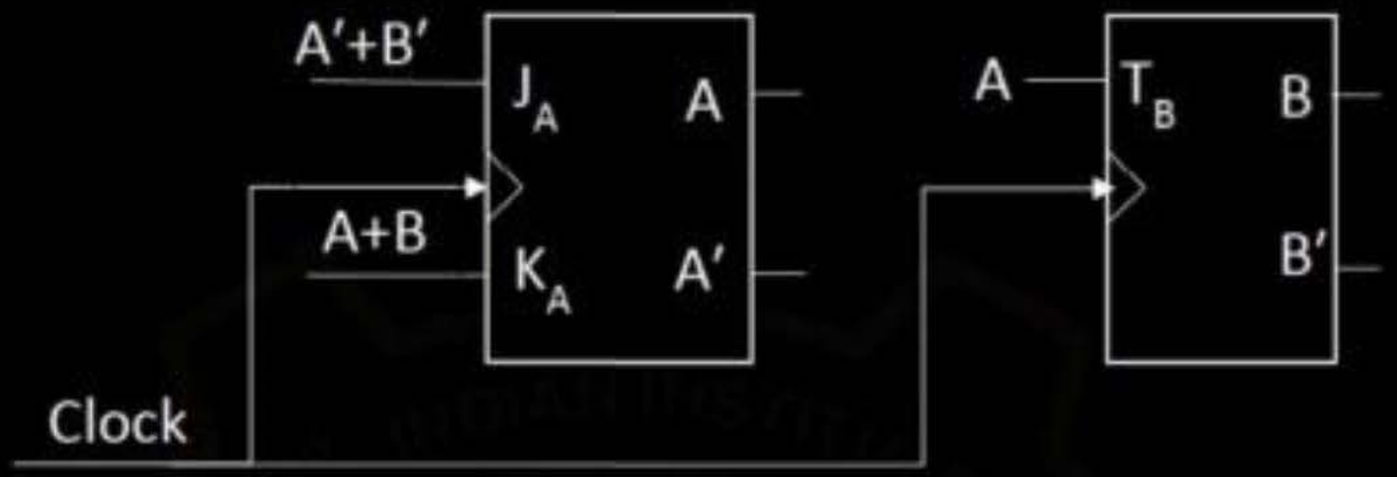
H.W.

A 00 – 01 – 10 – 11 – 00

B 00 – 10 – 01 – 11 – 00

C 00 – 10 – 11 – 01 – 00

D 00 – 01 – 11 – 00



[MCQ]

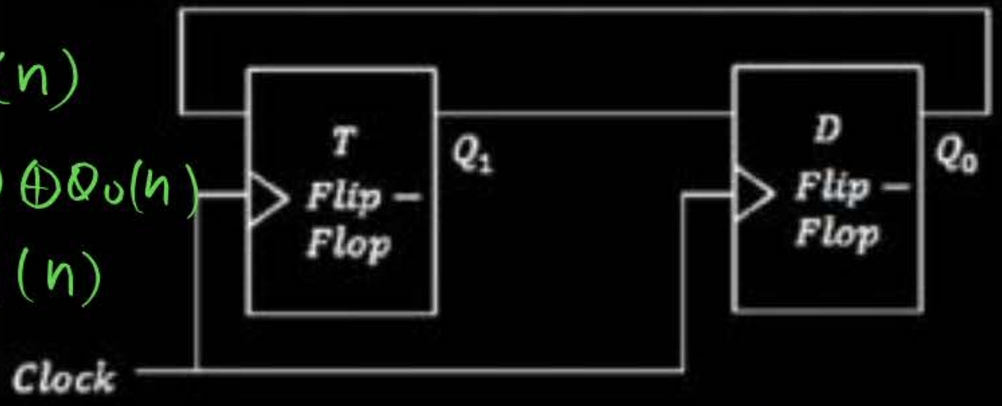
Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.
Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

[GATE-2017-CS: 1M]

$Q_1(n+1) = T \oplus Q_1(n)$

$= Q_1(n) \oplus Q_0(n)$

$Q_0(n+1) = D = Q_1(n)$



	Q_1	Q_0
	1	1
1st	0	1
2nd	1	0
3rd	1	1
4th	0	1

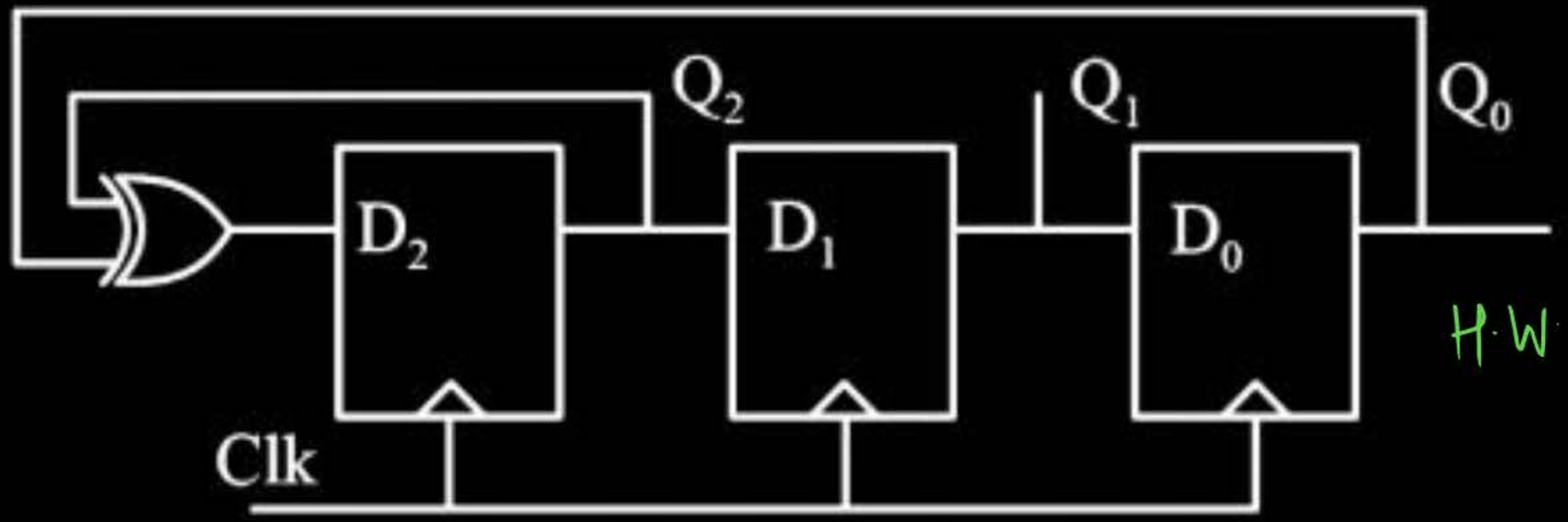
A. Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively

B. Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 01 respectively

C. Q_1Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively

D. Q_1Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively.

#Q. The propagation delay of the exclusive-OR (XOR) gate in the circuit in the figure is 3 ns. The propagation delay of all the flip-flops is assumed to be zero. The clock (CLK) frequency provided to the circuit is 500 MHz



H.W

Starting from the initial value of the flip-flop outputs $Q_2\ Q_1\ Q_0 = 1\ 1\ 1$ with $D_2 = 1$, the minimum number of triggering clock edges after which the flip-flop outputs $Q_2\ Q_1\ Q_0$ becomes 1 0 0 (in integer) is _____.

[MCQ]

A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that J = K = 1 is the toggle mode and J = K = 0 is the state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays. [GATE-2015-CS: 1M]

$J,K \leftarrow Q_1(n+1) = J_1\overline{Q}_1 + \overline{K}_1 Q_1 = Q_0\overline{Q}_1 + \overline{Q}_0 Q_1 = Q_1(n) \oplus Q_0(n)$

$D \leftarrow Q_0(n+1) = D_0 = Q_1(n)$

(A) 0110110...

(B) ✗ 0100100...

(C) ✗ 011101110...

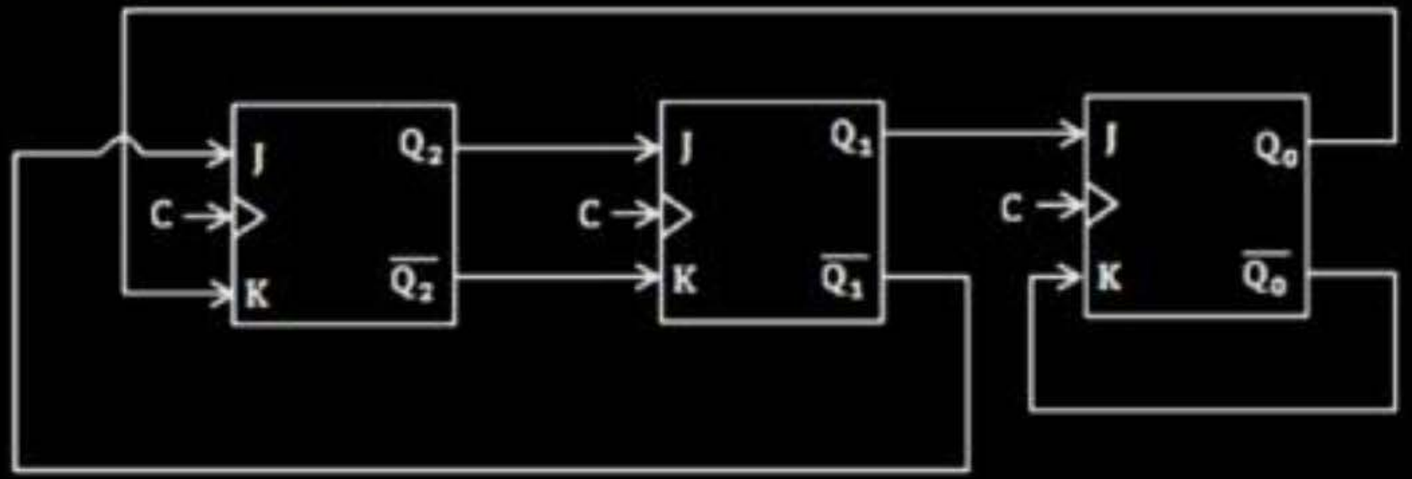
(D) ✗ 011001100...

	Q_1	Q_0
	0	1
1st	1	0
2nd	1	1
3rd	0	1
	1	0
	1	1
	0	1

[MCQ]

The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is :

[GATE-2014-CS: 1M]



	Q_2	Q_1	Q_0
	0	0	0
1st	1	0	0
2nd	1	1	0
3rd	1	1	1

$Q_2(n+1) = J_2\overline{Q}_2 + \overline{K}_2Q_2$, $Q_1(n+1) = J_1\overline{Q}_1 + \overline{K}_1Q_1$

$= \overline{Q}_1\overline{Q}_2 + \overline{Q}_0Q_2$ $= Q_2\overline{Q}_1 + Q_2Q_1$

$= \overline{Q_1+Q_2} + Q_2\overline{Q}_0$ $= Q_2(n)$

$Q_0(n+1) = J_0\overline{Q}_0 + \overline{K}_0Q_0 = Q_1\overline{Q}_0 + Q_0\cdot Q_0 = (Q_1+Q_0)$

A ✗ 001, 010, 011

B ✗ 111, 110, 101

C ✓ 100, 110, 111

D ✗ 100, 011, 001

[MCQ]

The minimum number of D flip-flops needed to design a mod-258 counter is :

[GATE-2011-CS: 1M]

H.W.

(A) 9

(B) 8

(C) 512

(D) 258

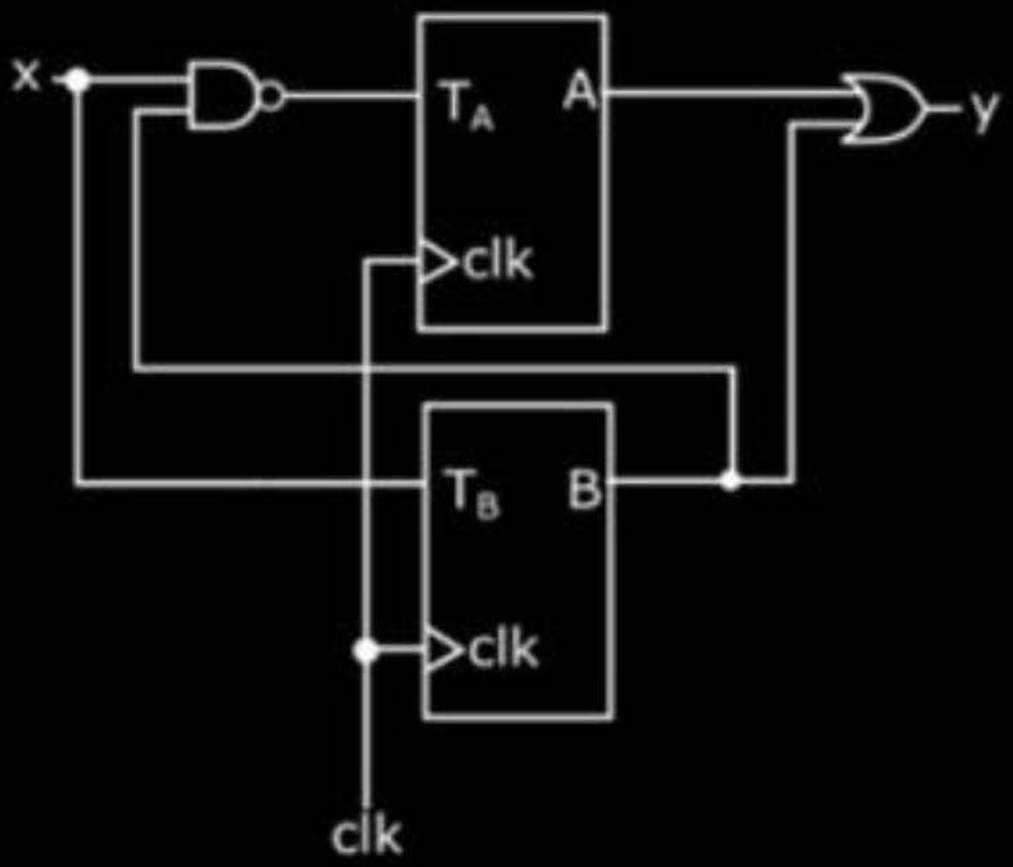
#Q. Two T-flip flops are interconnected as shown in the figure. The present state of the flip flops are: A = 1, B = 1. The input x is given as 1, 0, 1 in the next three clock cycles. The decimal equivalent of $(ABy)_2$ with A being the MSB and y being the LSB, after the 3rd clock cycle is 7

$Q_A(n+1) = T_A \oplus Q_A(n)$

$= \overline{x Q_B(n)} \oplus Q_A(n)$

$Q_B(n+1) = T_B \oplus Q_B(n)$

$= x \oplus Q_B(n)$



	Q_A	Q_B	y
	1	1	1
1st	1	0	1
2nd	0	0	0
3rd	1	1	1

$(ABy)_2 = (111)_2$

$= (7)_{10}$

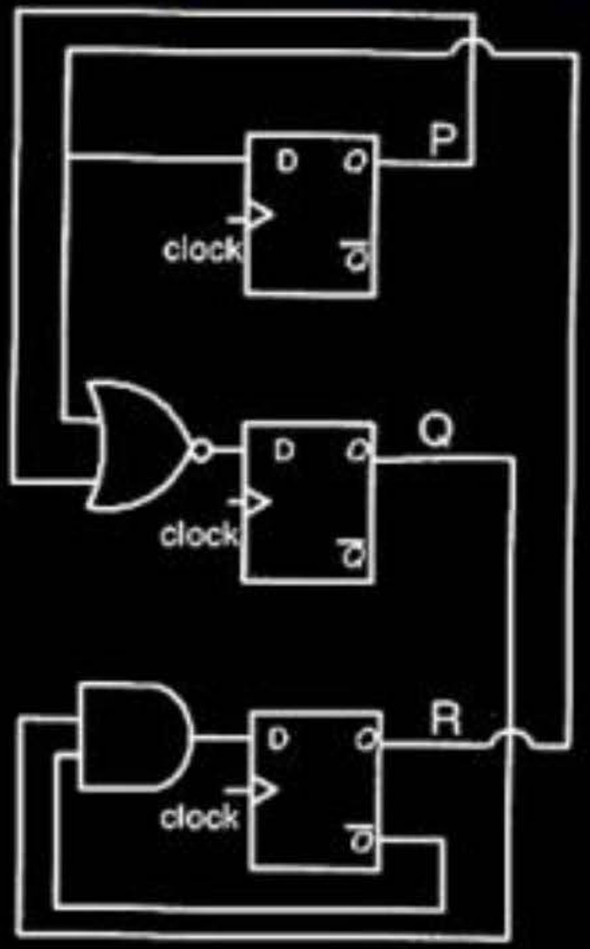
[MCQ]

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter ? [GATE-2011-CS: 1M]

$$Q_P(n+1) = D_P = Q_R(n)$$

$$Q_Q(n+1) = D_Q = \overline{Q_P(n) + Q_R(n)}$$

$$Q_R(n+1) = D_R = Q_Q(n) \cdot \overline{Q}_R(n)$$



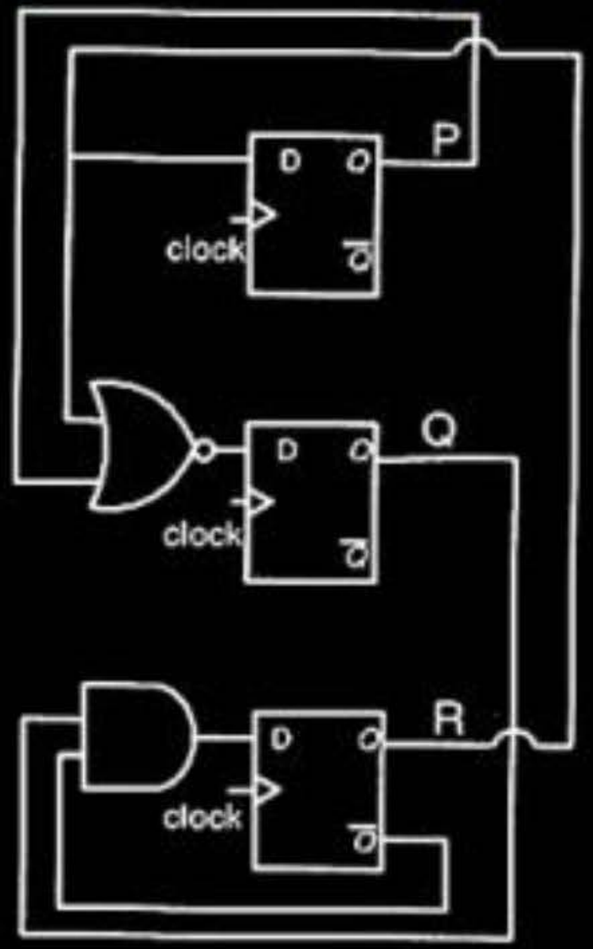
	Q_P	Q_Q	Q_R
	0	0	0
1st	0	1	0
2nd	0	1	1
3rd	1	0	0
4th	0	0	0

MOD – No. 4

- A 3
- B 4
- C 5
- D 6

[MCQ]

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge? [GATE-2011-CS: 1M]



H.W.

(A) 000

(B) 001

(C) 010

(D) 011

[MCQ]

Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. CLKIN is the clock input to the circuit. At the beginning, Q1, Q2 and Q3 have values 0, 1 and 1, respectively.

Which one of the given values of (Q1, Q2, Q3) can NEVER be obtained with this digital circuit? [GATE-2023-CS: 2M]

A. (0, 0, 1)

B. (1, 0, 0)

C. (1, 0, 1)

D. (1, 1, 1)

MOD-7

$Q_1(n+1) = T_1 \oplus Q_1(n)$

$= \overline{Q_3(n)} \oplus Q_1(n)$

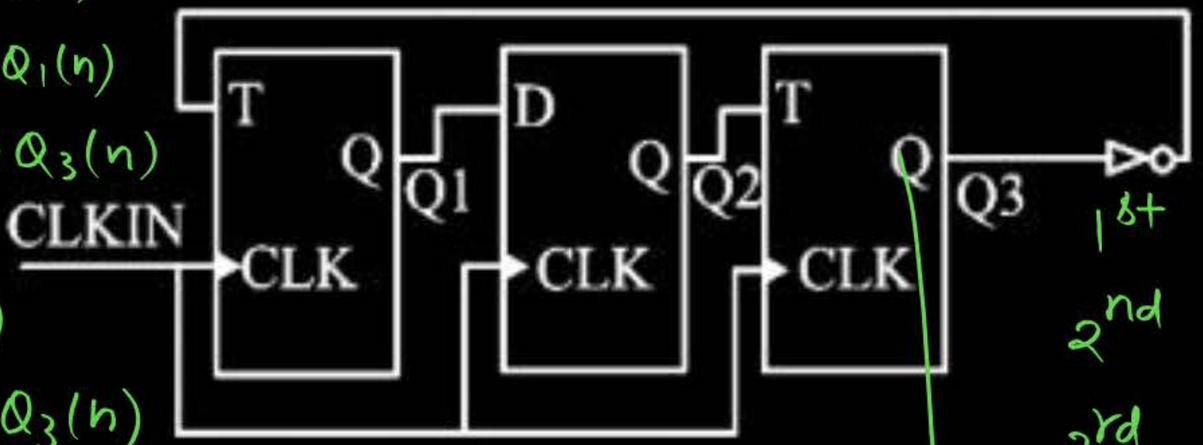
$= Q_1(n) \odot Q_3(n)$

$Q_2(n+1) = D_2$

$= Q_1(n)$

$Q_3(n+1) = T_3 \oplus Q_3(n)$

$= Q_2(n) \oplus Q_3(n)$



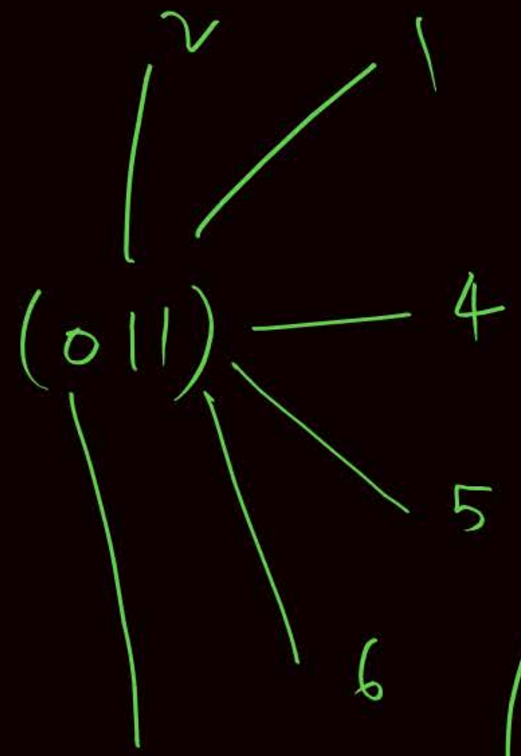
	Q_1	Q_2	Q_3
1st	0	1	1
	0	0	0
2nd	1	0	0
3rd	0	1	0
4th	1	0	1
5th	1	1	1
6th	1	1	0
7th	0	1	1

(3-0-4-2-5-7-6)

Lockout

(0 - 1 - 2 - 4) — 3FF

3 — xxx
5 — xxx
6 — xxx
7 — xxx



0 0 1
↓
0 1 1

(0 - 1 - 2)

- xx

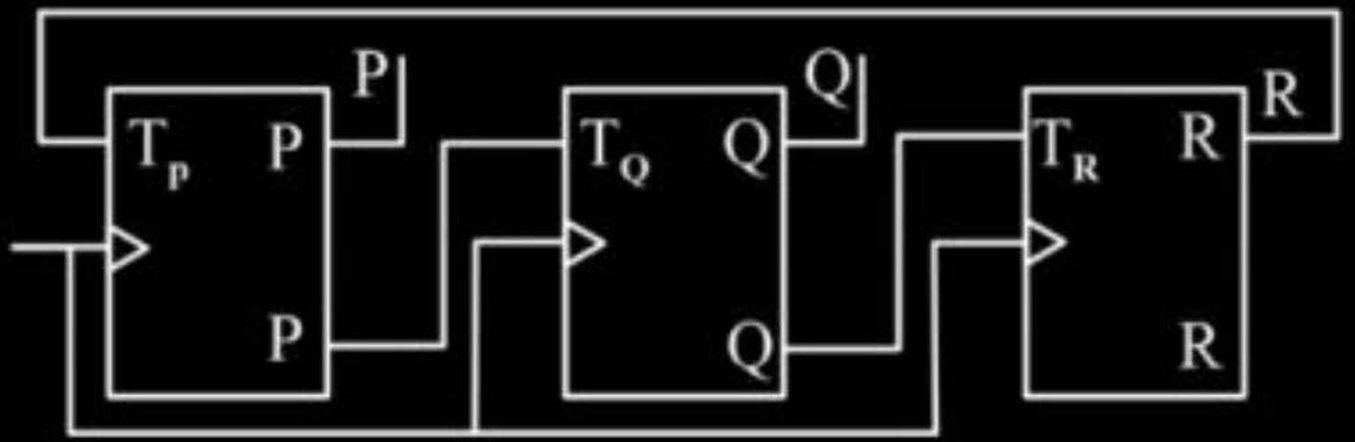
3 - 5 - 6

[MCQ]

Consider a 3-bit counter, designed using T flip-flops, as shown below. Assuming the initial state of the counter given by PQR as 000. What are the next three states ?

H.W.

[GATE-2021-CS: 1M]



(A) 011,101,000

(B) 001,010,111

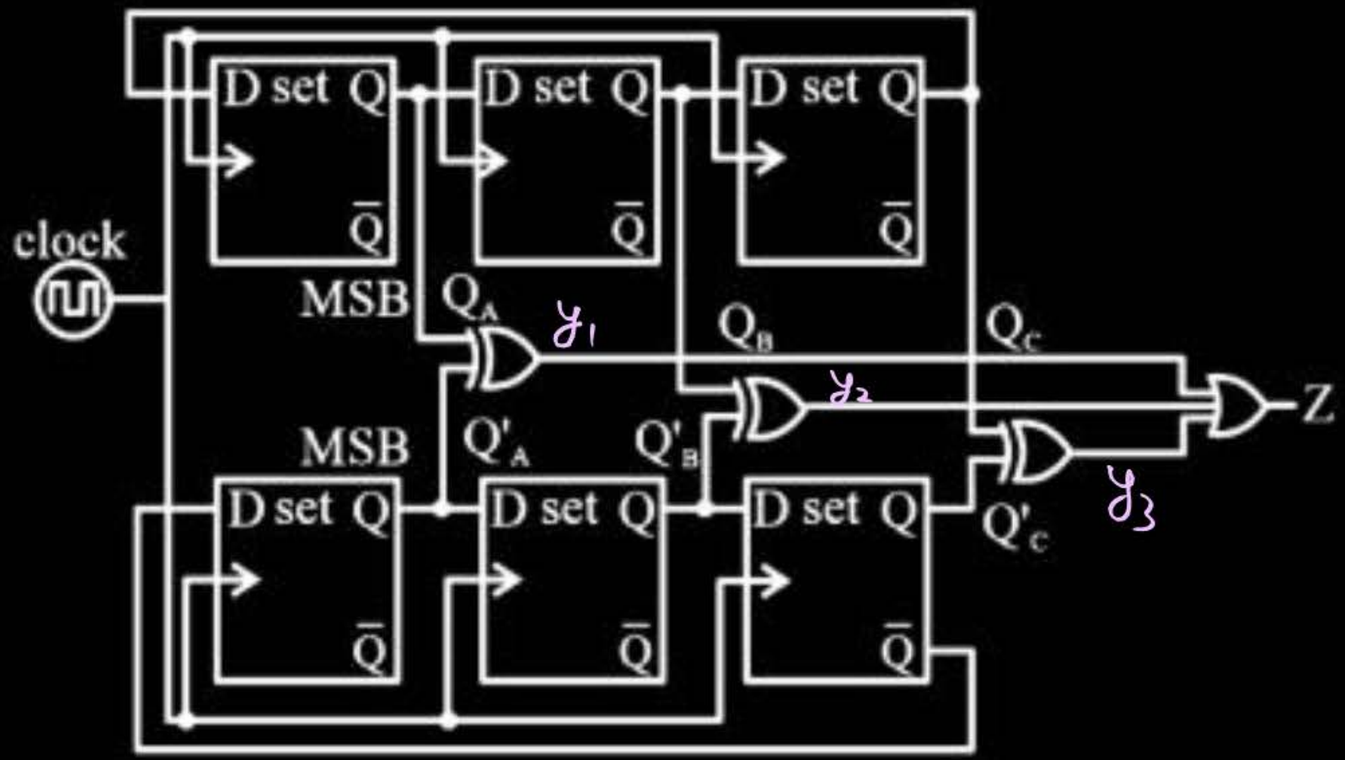
(C) 011,101,111

(D) 001,010,000

#Q. For the synchronous sequential circuit shown below, the output Z is zero for the initial conditions

$$Q_A Q_B Q_C = Q'_A Q'_B Q'_C = 100$$

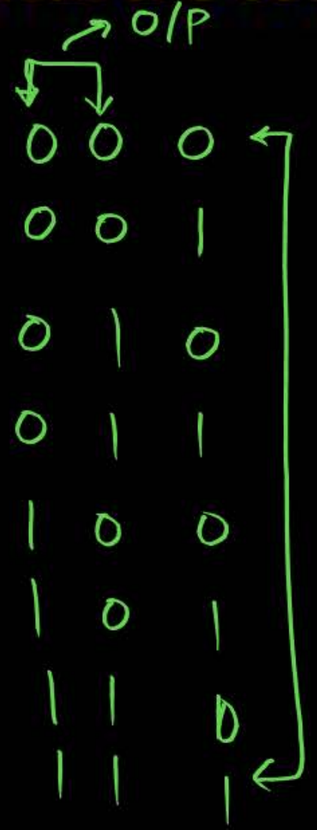
The minimum number of clock cycles after which the output z would again become zero is ____6____.



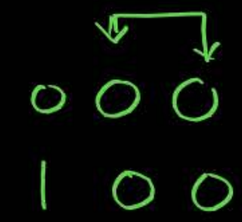
	Q_A	Q_B	Q_C	Q_A'	Q_B'	Q_C'	Z
	1	0	0	1	0	0	0
1st	0	1	0	1	1	0	1
2nd	0	0	1	1	1	1	1
3rd	1	0	0	0	1	1	1
4th	0	1	0	0	0	1	1
5th	0	0	1	0	0	0	1
6th	1	0	0	1	0	0	0

[NAT]

The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0,0,1,1,2,2,3,3,0,0....)is. [GATE-2021-CS: 2M]



MOD – 8 – 3 FFs

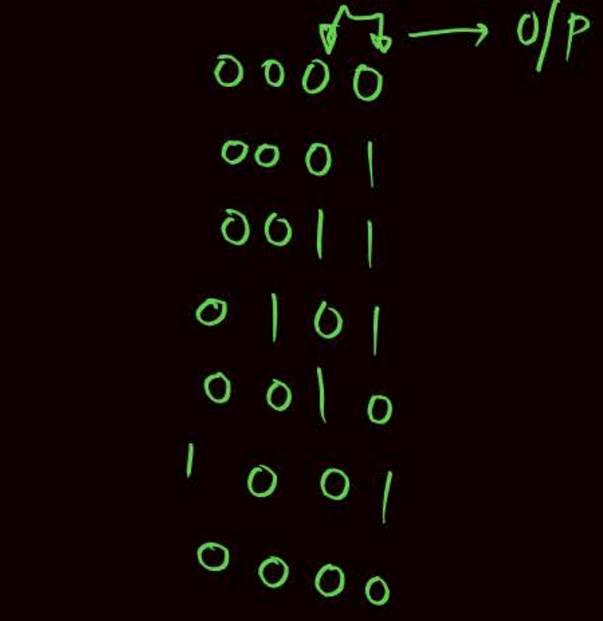


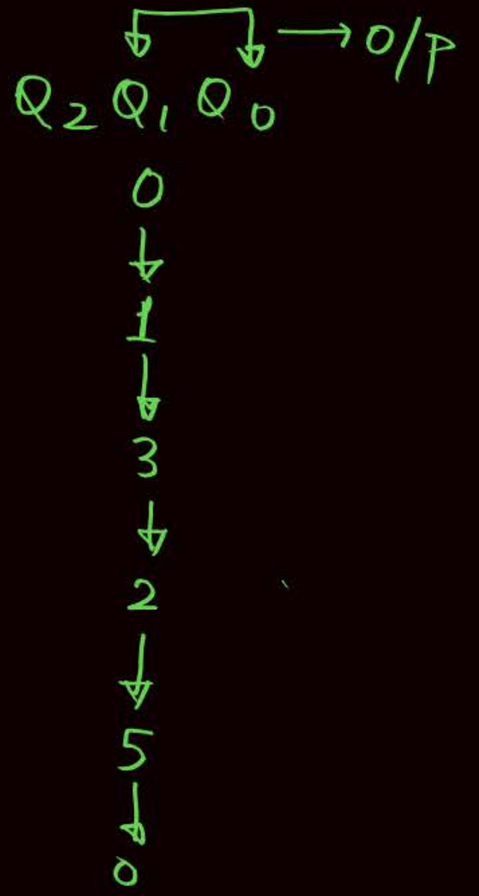
0 – 1 – 3 – 2 – 1

MOD-5

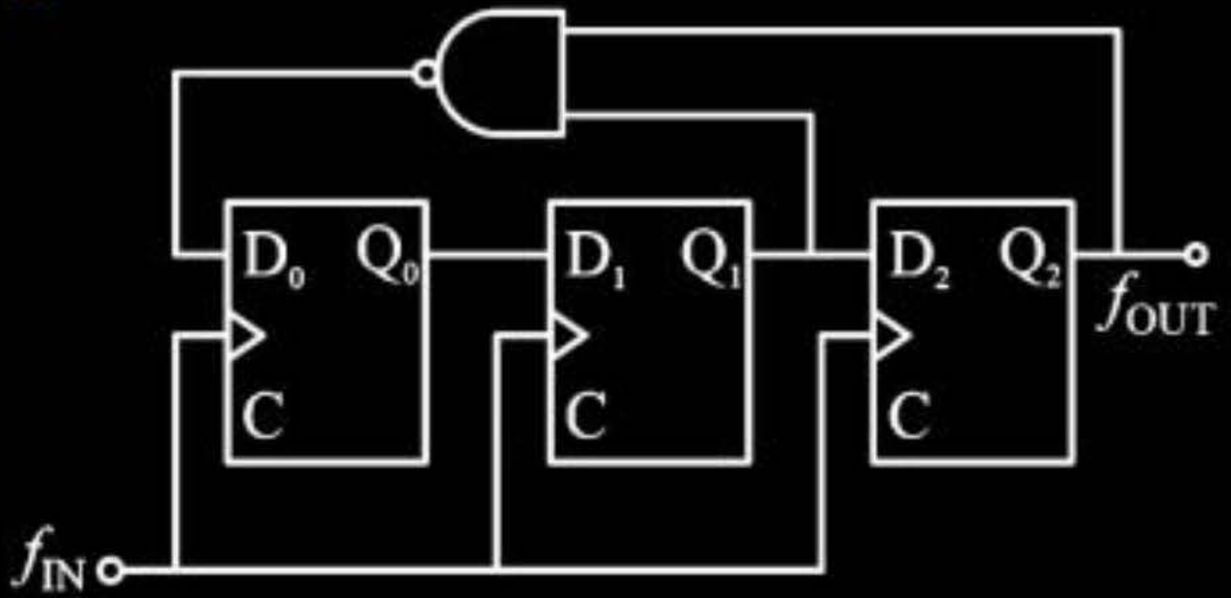
0 – 1 – 3 – 1 – 2 – 1

MOD-6





#Q. Which one of the following statements is true about the digital circuit shown in the figure?



H.W.

A It can be used for dividing the input frequency by 3.

B It can be used for dividing input frequency by 5.

C It can be used for dividing the input frequency by 7.

D It cannot be reliably used as a frequency divider due to disjoint internal cycles.

[MCQ]

The next state table of a 2-bit saturating up-counter is given below.
The counter is built as a synchronous sequential circuit using T flip-flops.
The expressions for T_1 and T_0 are [GATE-2017-CS: 1M]

H.W.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

A. $T_1 = Q_1Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

B. $T_1 = \overline{Q_1}Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

C. $T_1 = Q_1 + Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

D. $T_1 = \overline{Q_1}Q_0, T_0 = Q_1 + Q_0$

[MCQ]

Consider a 4-bit Johnson counter an initial value of 0000. The counting sequence of this counter is -

[GATE-2015-CS: 1M]

0000 — 0

1000 — $(8)_{10}$

1100 → $(12)_{10}$

A 0,1,3,7,15,14,12,8,0

B 0,1,3,5,7,9,11,13,15,0

C 0,2,4,6,8,10,12,14,0

D 0,8,12,14,15,7,3,1,0

[MCQ]

Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to- 2^n bit decoder. This circuit is equivalent to a

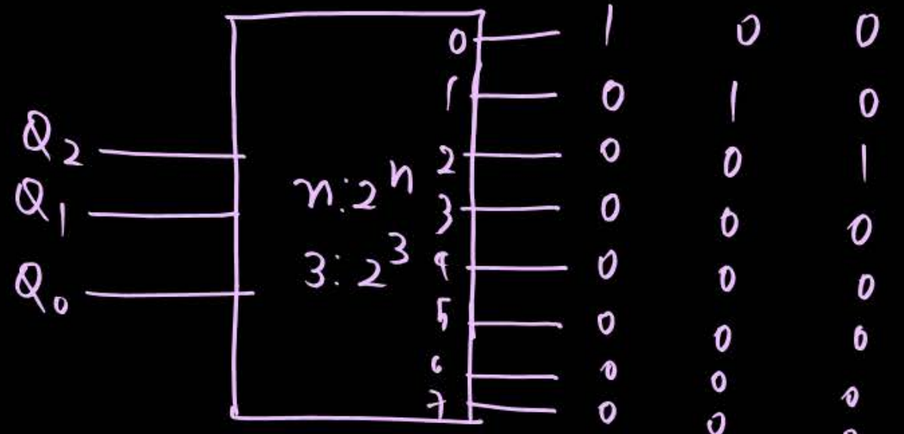
[GATE-2014-CS: 1M]

$0 - (2^k - 1)$

$Q_2 Q_1 Q_0$

$0 - (2^n - 1)$

$0 - 7$



2^n - bit ring counter

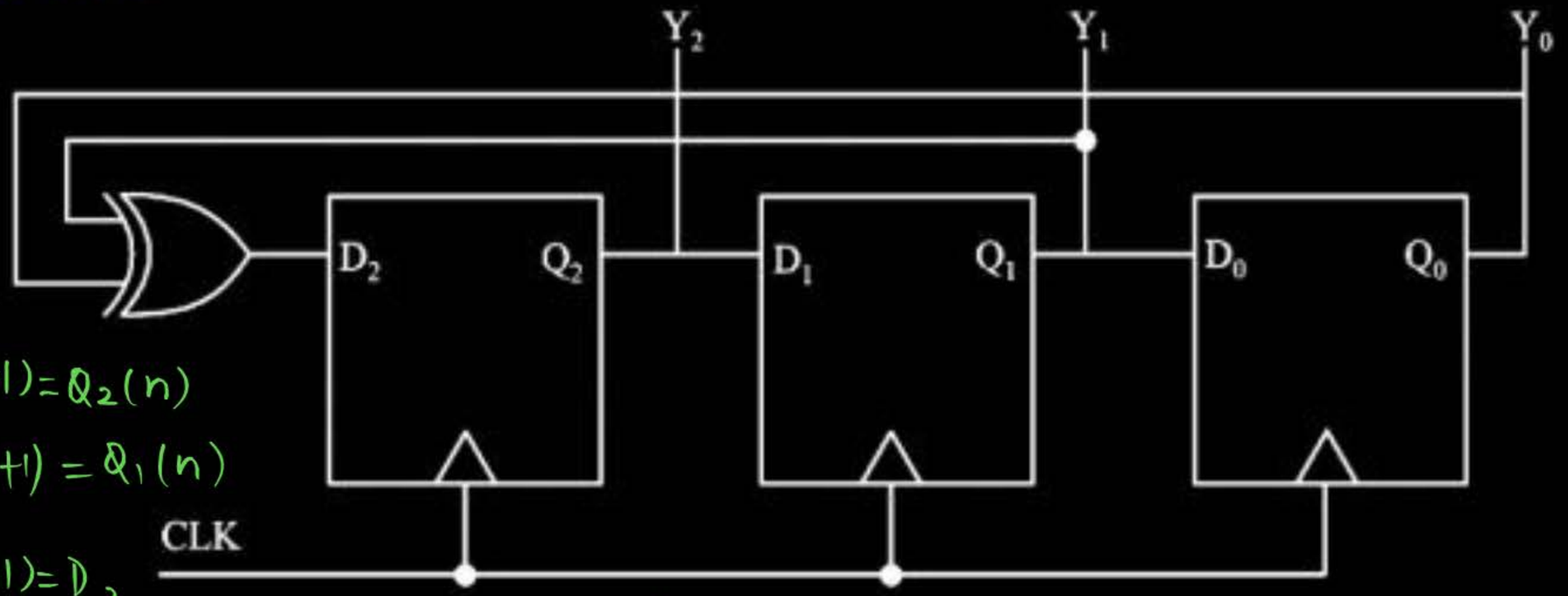
A. k-bit binary up counter.

B. k-bit binary down counter.

C. k-bit ring counter.

D. k-bit Johnson counter.

#Q. A three-bit pseudo random number generator is shown. Initially the value of output $Y = Y_2\ Y_1\ Y_0$ is set to 111. The value of output Y after three clock cycles is



A 000

B 001

C 010

D 100

$Q_1(n+1) = Q_2(n)$

$Q_0(n+1) = Q_1(n)$

$Q_2(n+1) = D_2$

$= Q_1(n) \oplus Q_0(n)$

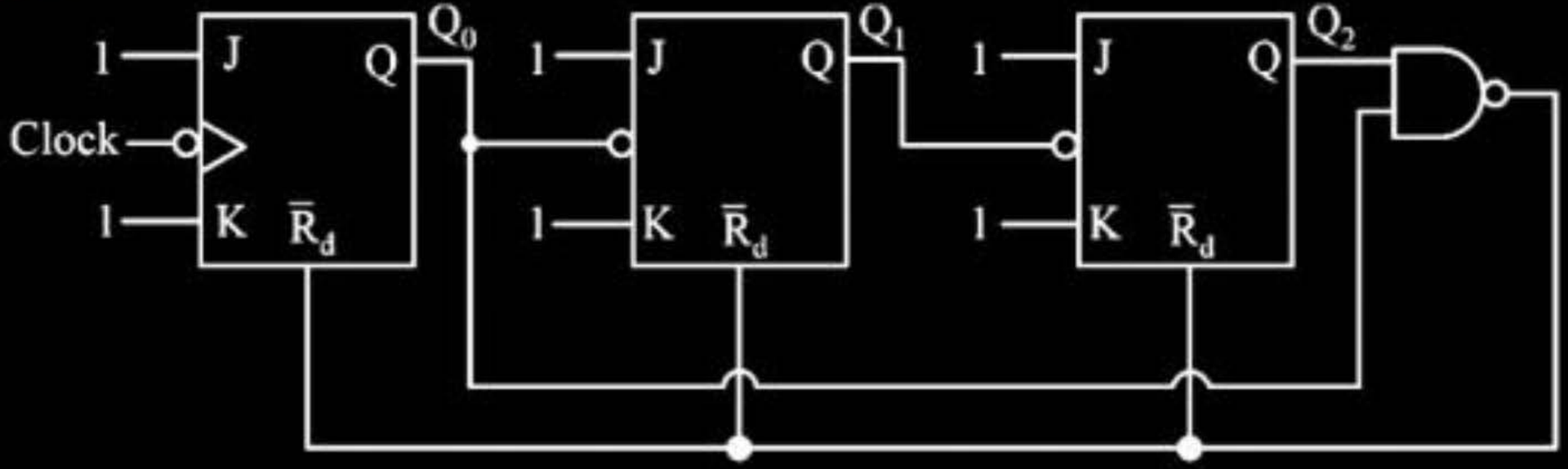
$Q_2 Q_1 Q_0$ 3rd 100

1 1 1

1st 0 1 1

2nd 0 0 1

#Q. The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset ($\overline{R_d}$ input). The counter corresponding to this circuit is



H.W.

A a modulo-5 binary up counter

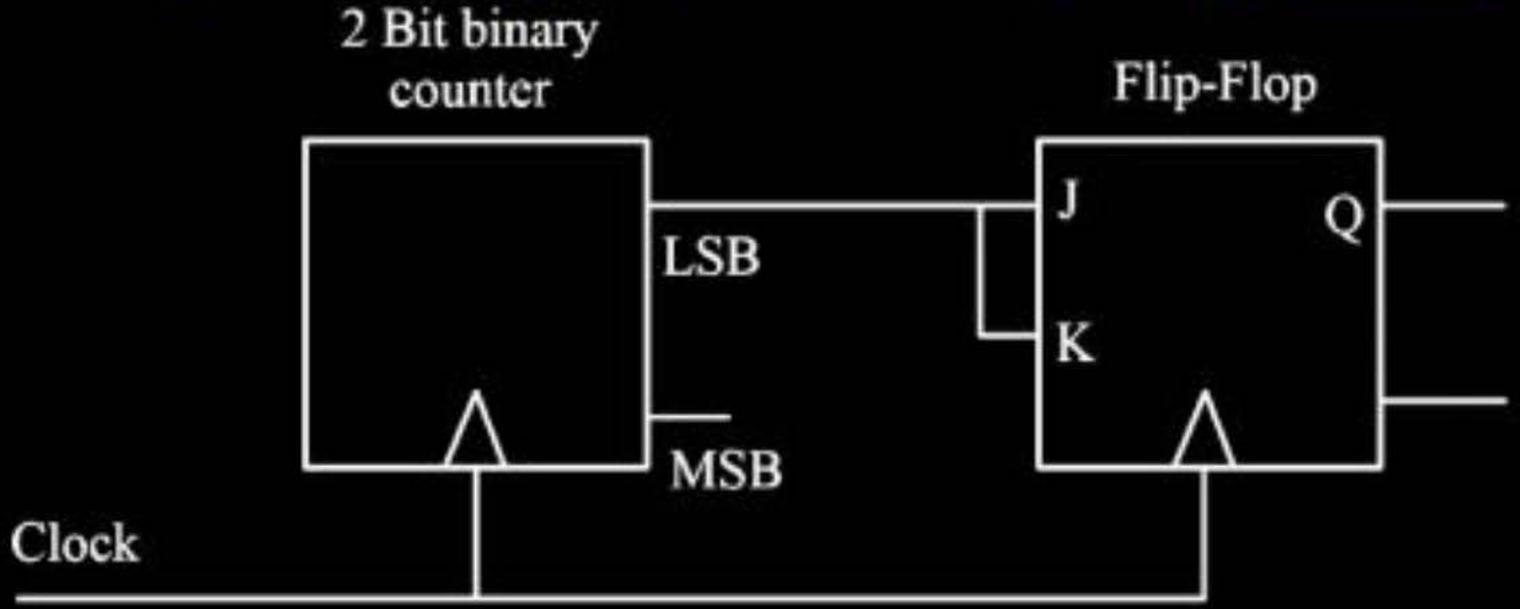
B a modulo-6 binary down counter

C a modulo-5 binary down counter

D a modulo-6 binary up counter

#Q. For the circuit shown, the clock frequency is f_0 and the duty cycle is 25%. For the signal at the Q output of the Flip-Flop, _____.

H.W



A frequency is $f_0/4$ and duty cycle is 50%

B frequency is $f_0/4$ and duty cycle is 25%

C frequency is $f_0/2$ and duty cycle is 50%

D frequency is f_0 and duty cycle is 25%

#Q. In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1\ Q_0 = 00$. The state $(Q_1\ Q_0)$, immediately after the 333^{rd} clock pulse is

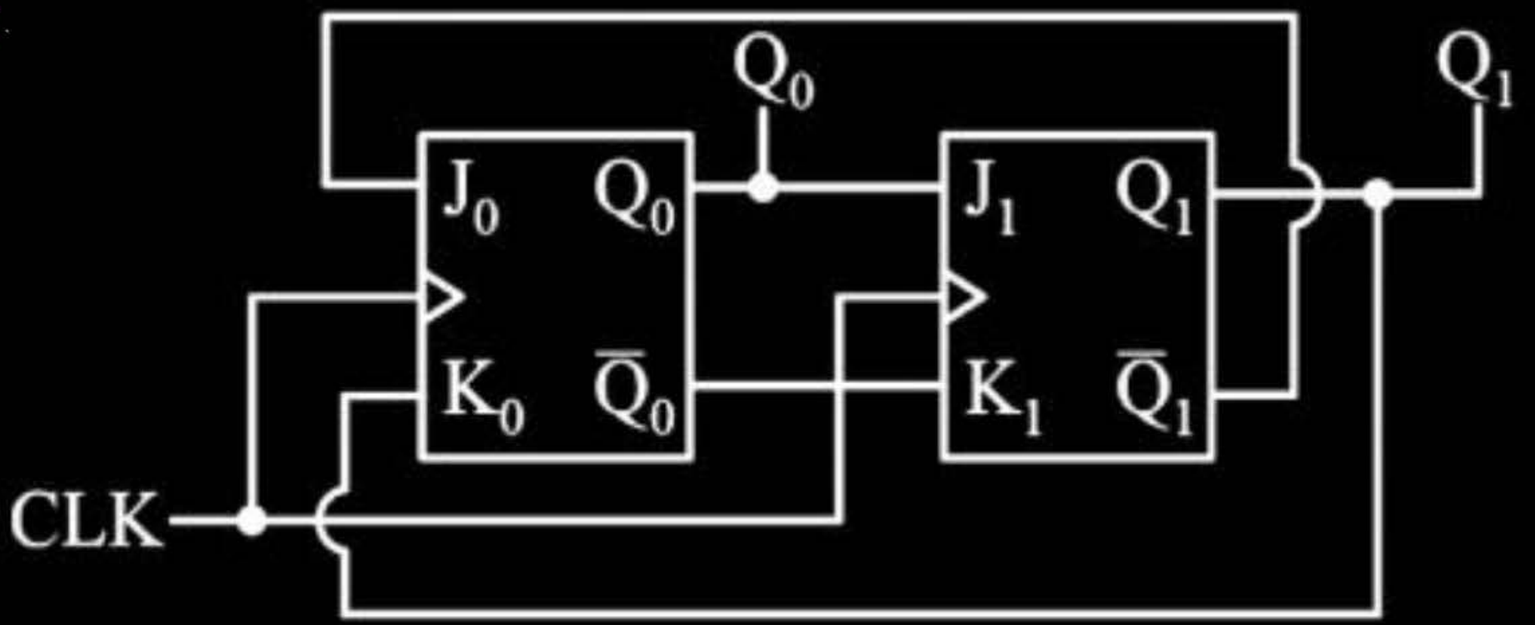
H.W.

A 00

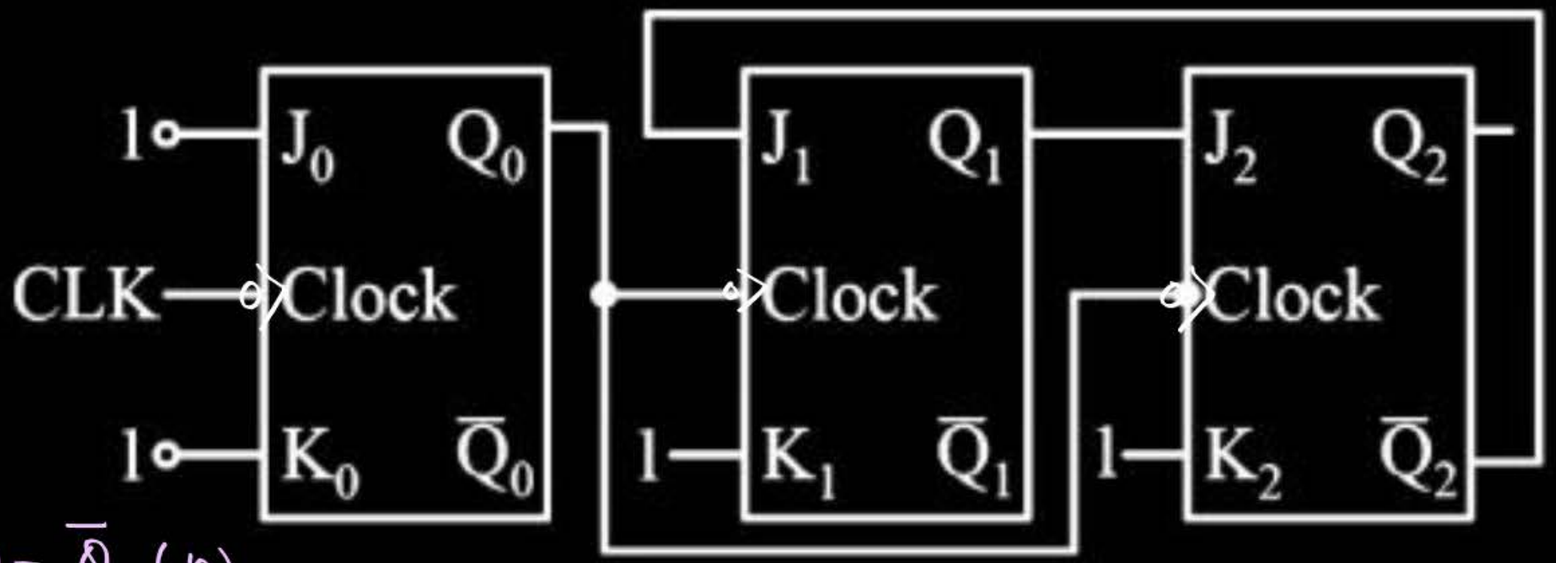
B 01

C 10

D 11



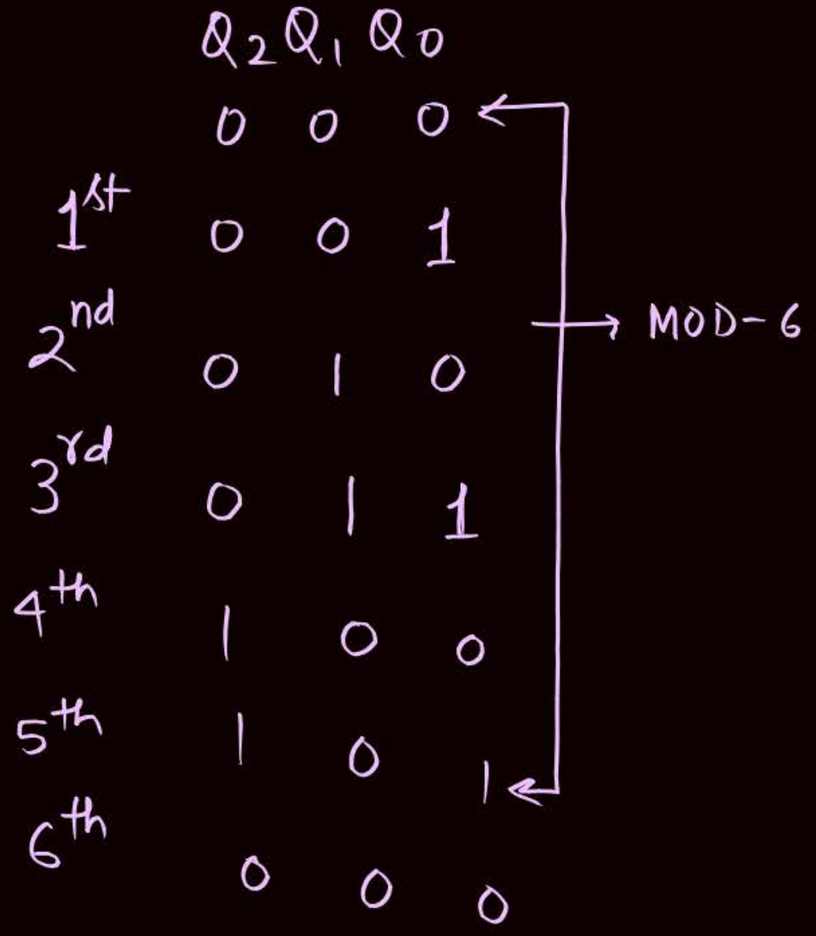
#Q. The figure shows a digital circuit constructed using negative edge triggered J-K flip flops. Assume a starting state of $Q_2\ Q_1\ Q_0 = 000$ will repeat after ___6___ number of cycles of the clock CLK



$Q_0(n+1) = \bar{Q}_0(n)$

$Q_1(n+1) = \bar{J}_1\bar{Q}_1 + \bar{K}_1 Q_1 = \bar{Q}_2\bar{Q}_1 + 0 = \overline{Q_2(n) + Q_1(n)}$ when triggered [when $Q_0 \to (1-0)$]

$Q_2(n+1) = J_2\bar{Q}_2 + \bar{K}_2 Q_2 = Q_1(n)\cdot\bar{Q}_2(n) = \bar{Q}_2(n)\cdot Q_1(n)$ [when $Q_0 \to (1-0)$]


$Q_2 Q_1 Q_0$
0 0 0
1st 0 0 1
2nd 0 1 0
3rd 0 1 1
4th 1 0 0
5th 1 0 1
6th 0 0 0
MOD-6

Topic : 2 Min Summary

→ Question Discussion on sequential CKt.

Thank you

GW

Soldiers !