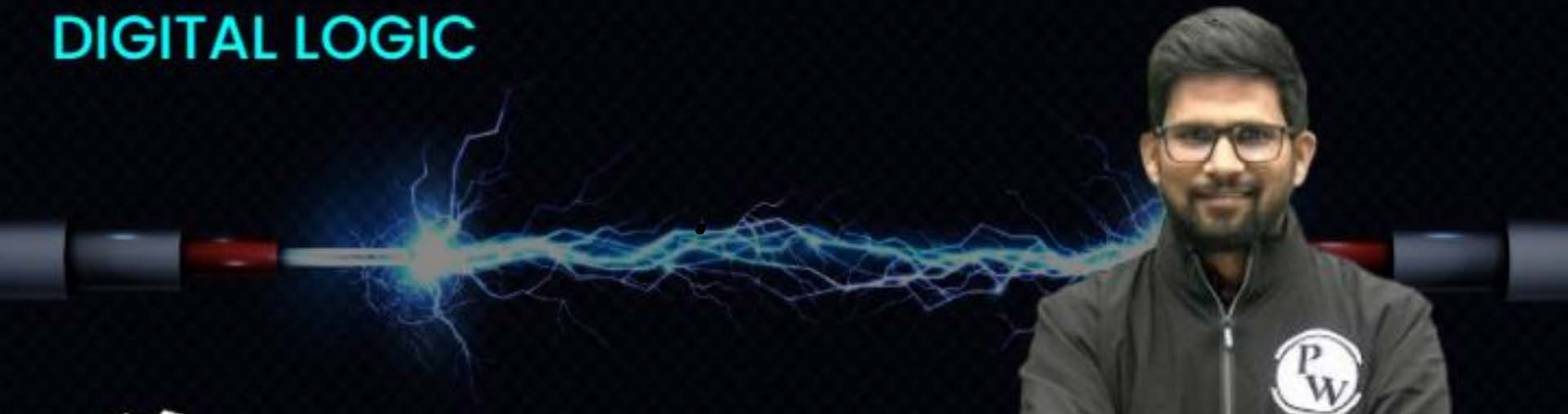
COMPUTER SCIENCE & IT

DIGITAL LOGIC



Lecture No: 04

Sequential Circuit

By- Chandan Gupta Sir

Recap of Previous Lecture

- Counters and its basics
- Asynchronous Counter design
-

Counters Cont.

Clear and Preset input

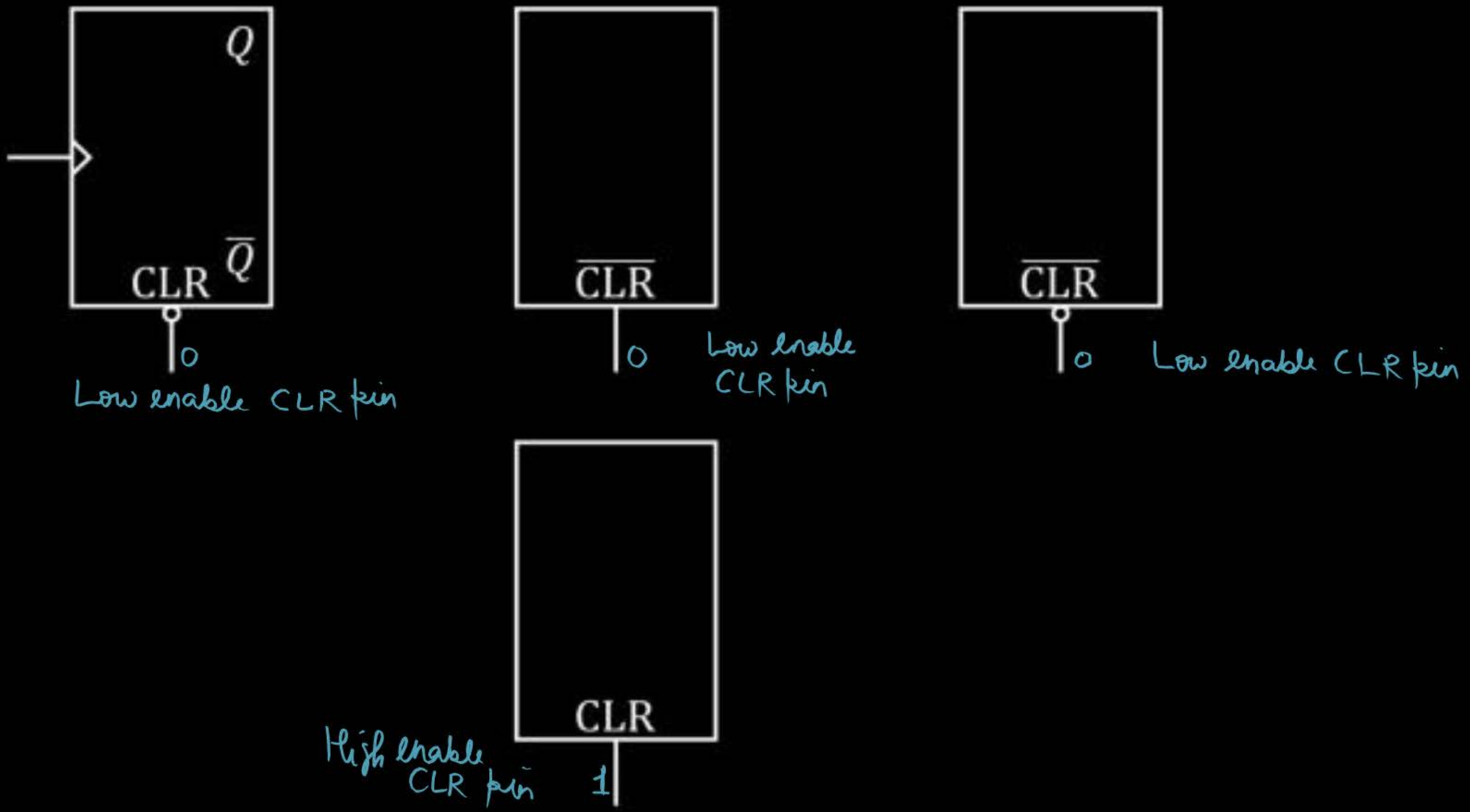
Input pin of FF

Clear input or CLR PIN input : It is asynchronous in nature and when it is activated then irrespective of clock i/p & inputs it will reset (clear) the o/p Q.

Input of FF

Preset input or PRE PIN input : It is asynchronous in nature and when it is activated then irrespective of clock i/p & inputs it will set the o/p Q.

Low Enable and High Enable CLR and PRE input :

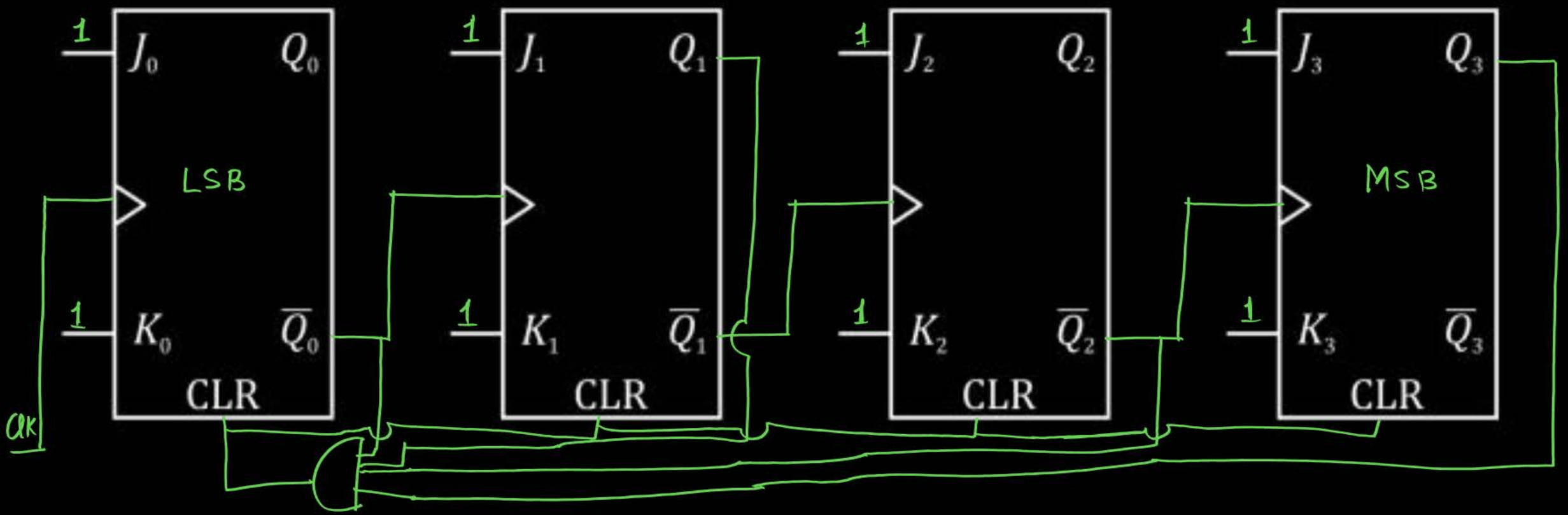


Designing of Asynchronous Counter with MOD no. other than 2^n

- BCD Counter Design :

  BCD Counter Counts → 0-1-2-3-4-5-6-7-8-9 → MOD-10 Counter

- Design :



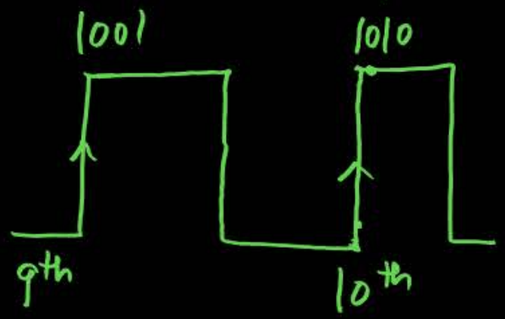
- Table :

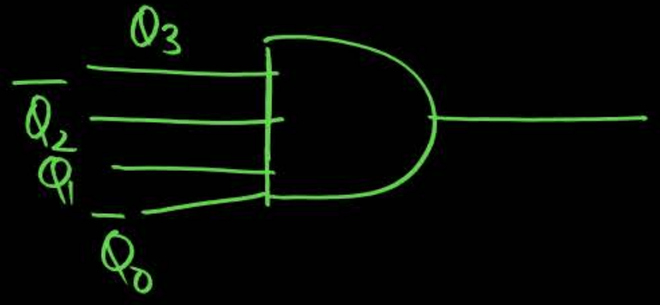
CLK	Q_3	Q_2	Q_1	Q_0
Start	0	0	0	0
1st	0	0	0	1
2nd	0	0	1	0
3rd	0	0	1	1
4th	0	1	0	0
5th	0	1	0	1
6th	0	1	1	0
7th	0	1	1	1
8th	1	0	0	0

fclk/10 fclk/10 fclk/10 fclk/2

0000 — 11
— 00 — 11

CLK	Q_3	Q_2	Q_1	Q_0
9^{th}	1	0	0	1
10^{th}	1 ↓CLR 0	0 ↓CLR 0	1 ↓CLR 0	0 ↓CLR 0
this state	exist momentarily and will	not be counted	in MOD no.	





MOD-12 up counter (0 – 11)

12 → CLR

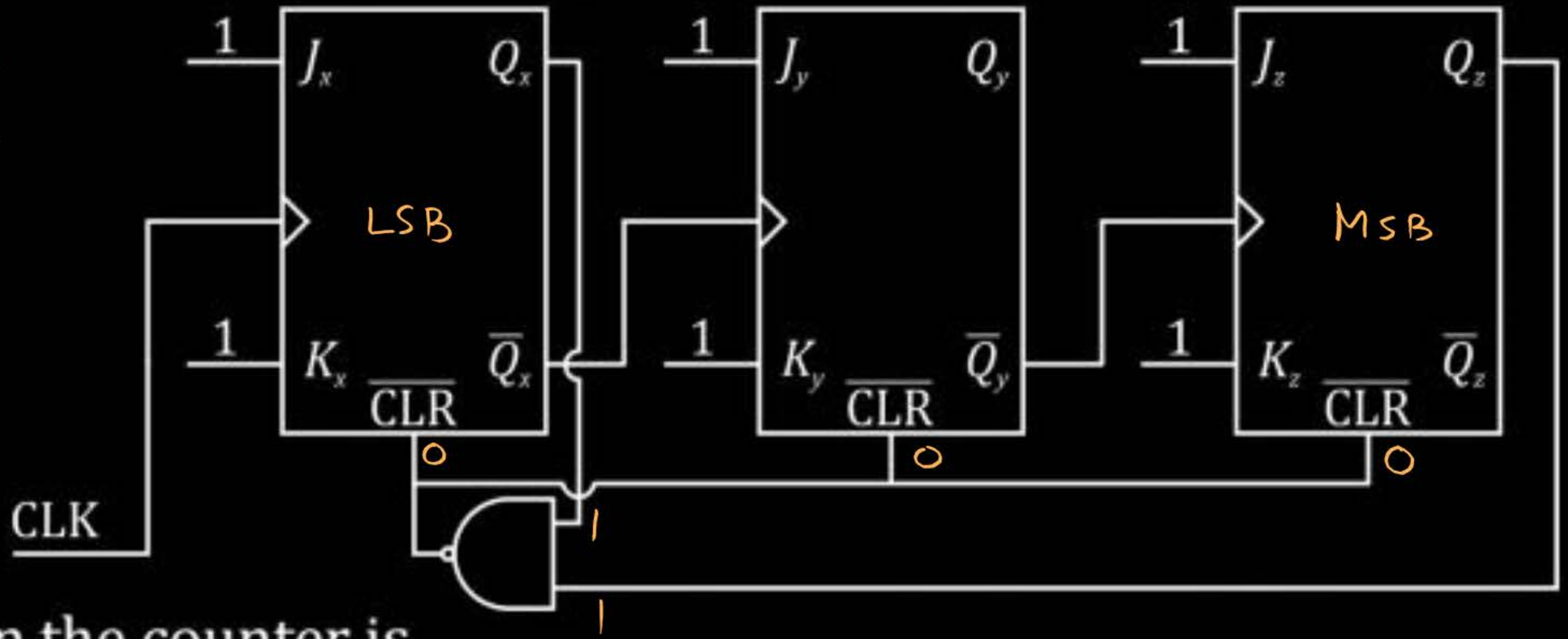
Imp:

- BCD counter is MOD-10 counter but not all MOD-10 counters are BCD counter.

Question

up counter

A Counter is designed as given below :



$Q_x = 1$

$Q_z = 1$

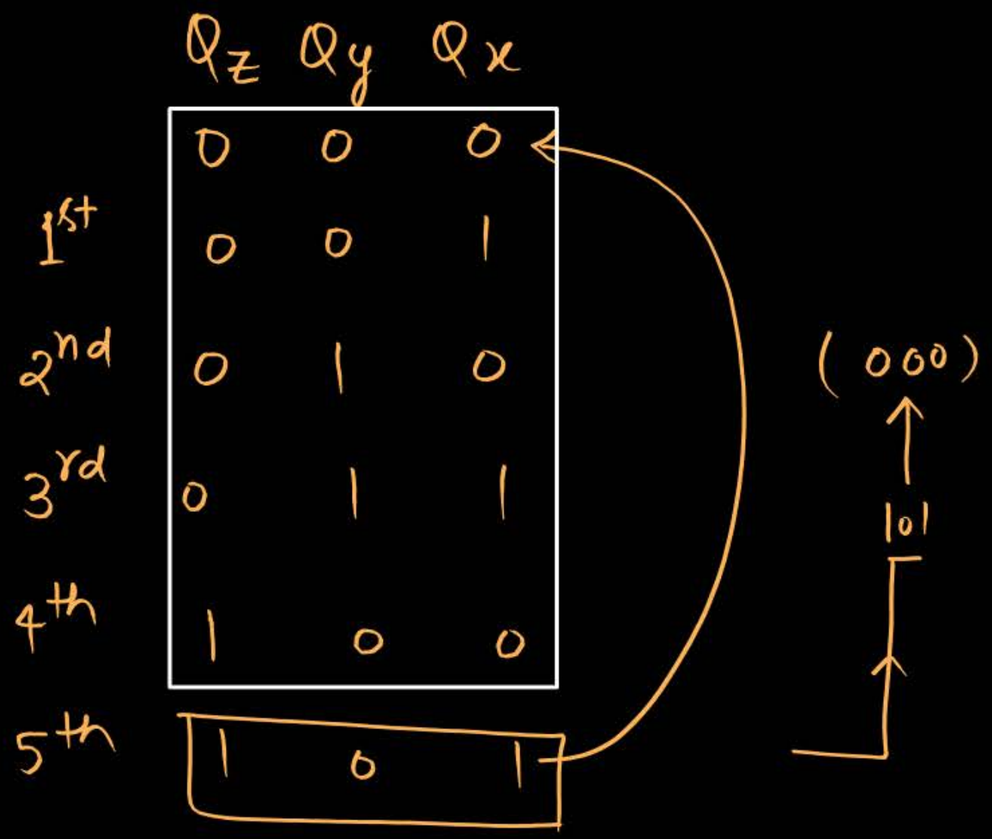
Then the counter is

(a) MOD-6 up counter

(b) MOD-5 down counter

(c) MOD-5 up counter

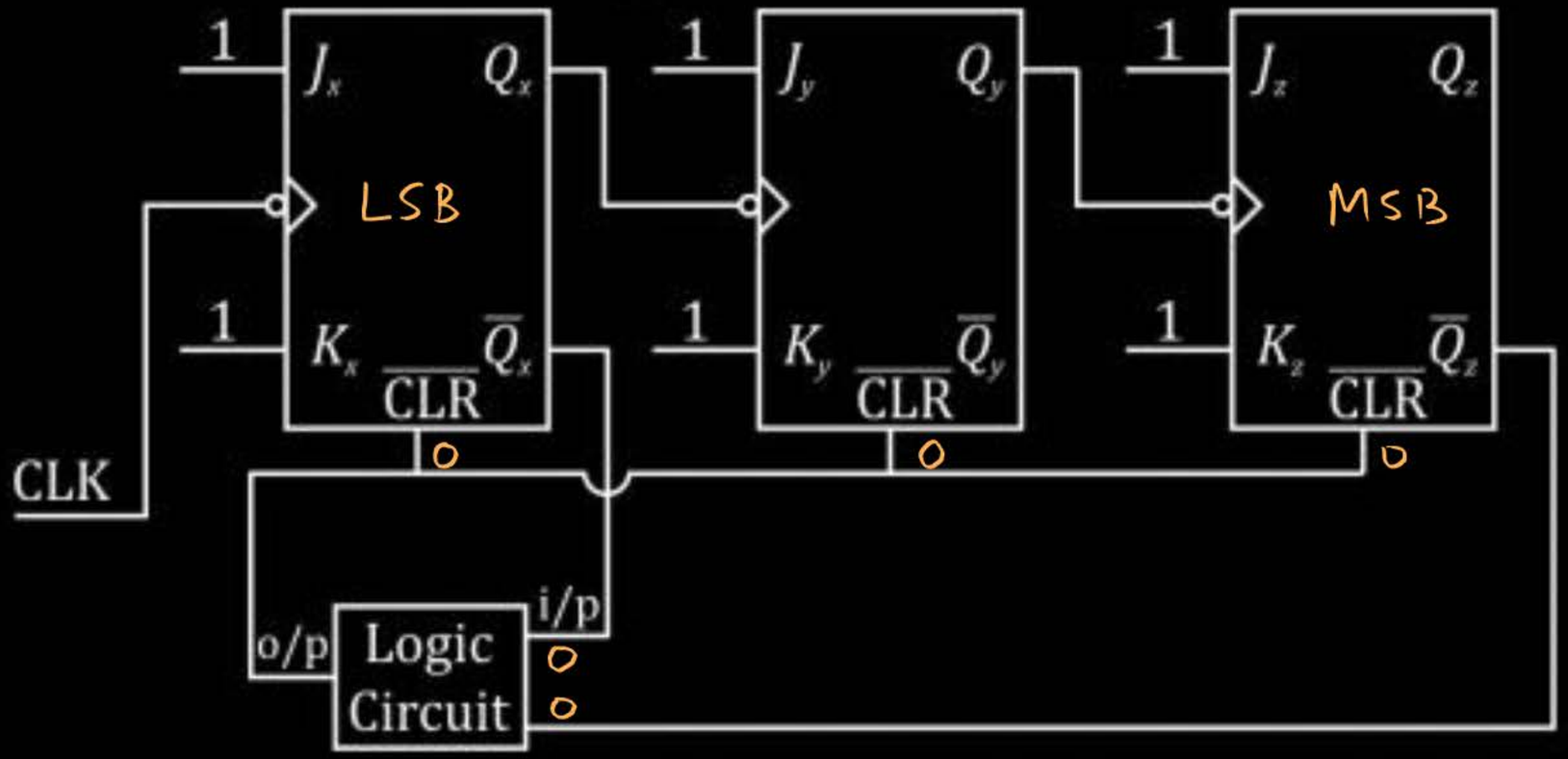
(d) MOD-6 down counter


Q_z Q_y Q_x
0 0 0
1st 0 0 1
2nd 0 1 0
3rd 0 1 1
4th 1 0 0
5th 1 0 1
(000)
101

Question

up counter

A sequential circuit is designed as shown :



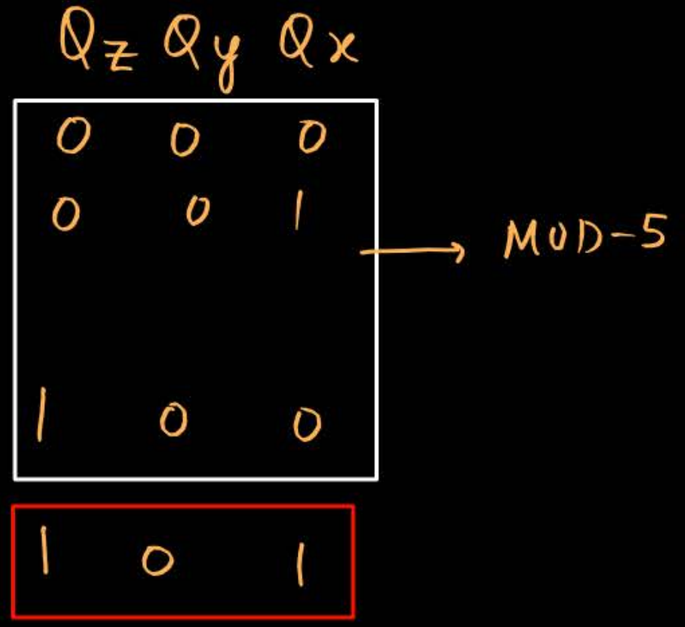
For above circuit to work as MOD-5 counter, the logic circuit will be

(a) 2-input OR GATE

(b) 2-input AND GATE

(c) 2-input NAND GATE

(d) 2-input NOR GATE


Q_z Q_y Q_x
0 0 0
0 0 1
1 0 0
MOD-5
1 0 1

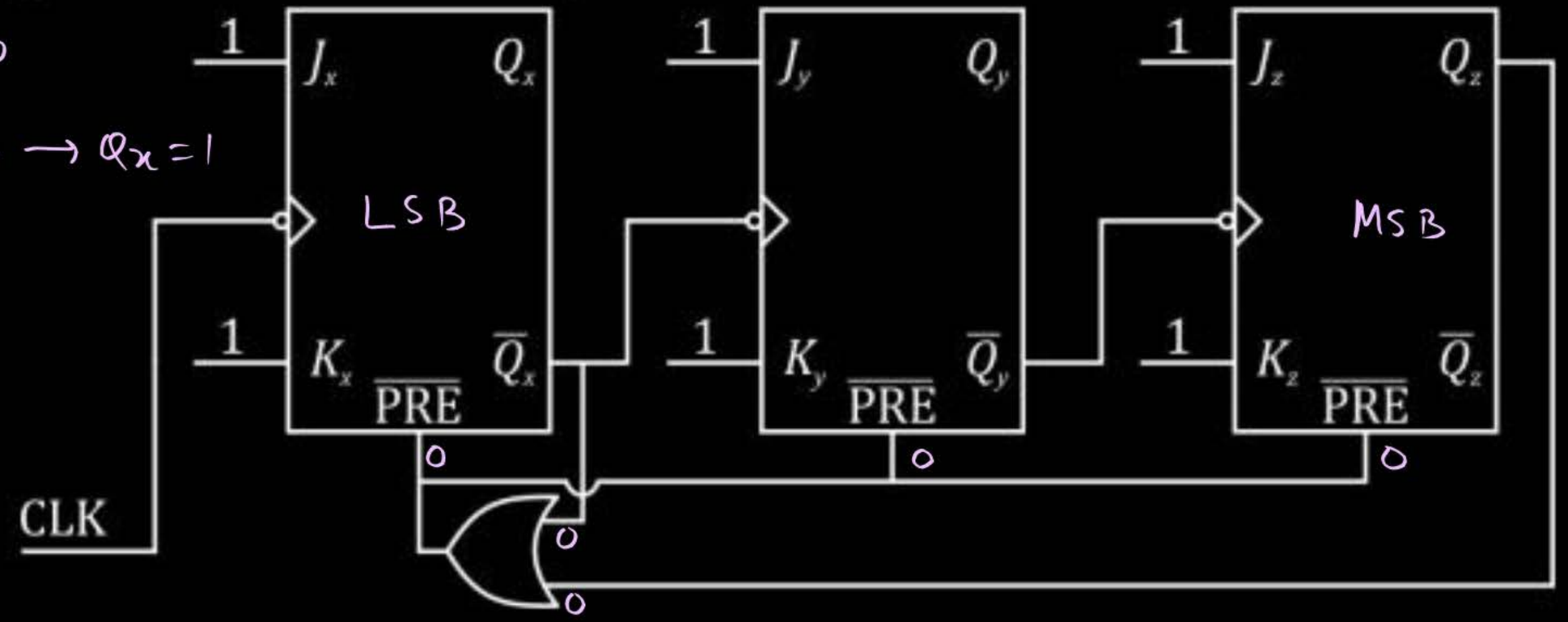
Question

down counter

A sequential circuit is as given below :

$Q_z = 0$

$\overline{Q_x} = 0 \rightarrow Q_x = 1$



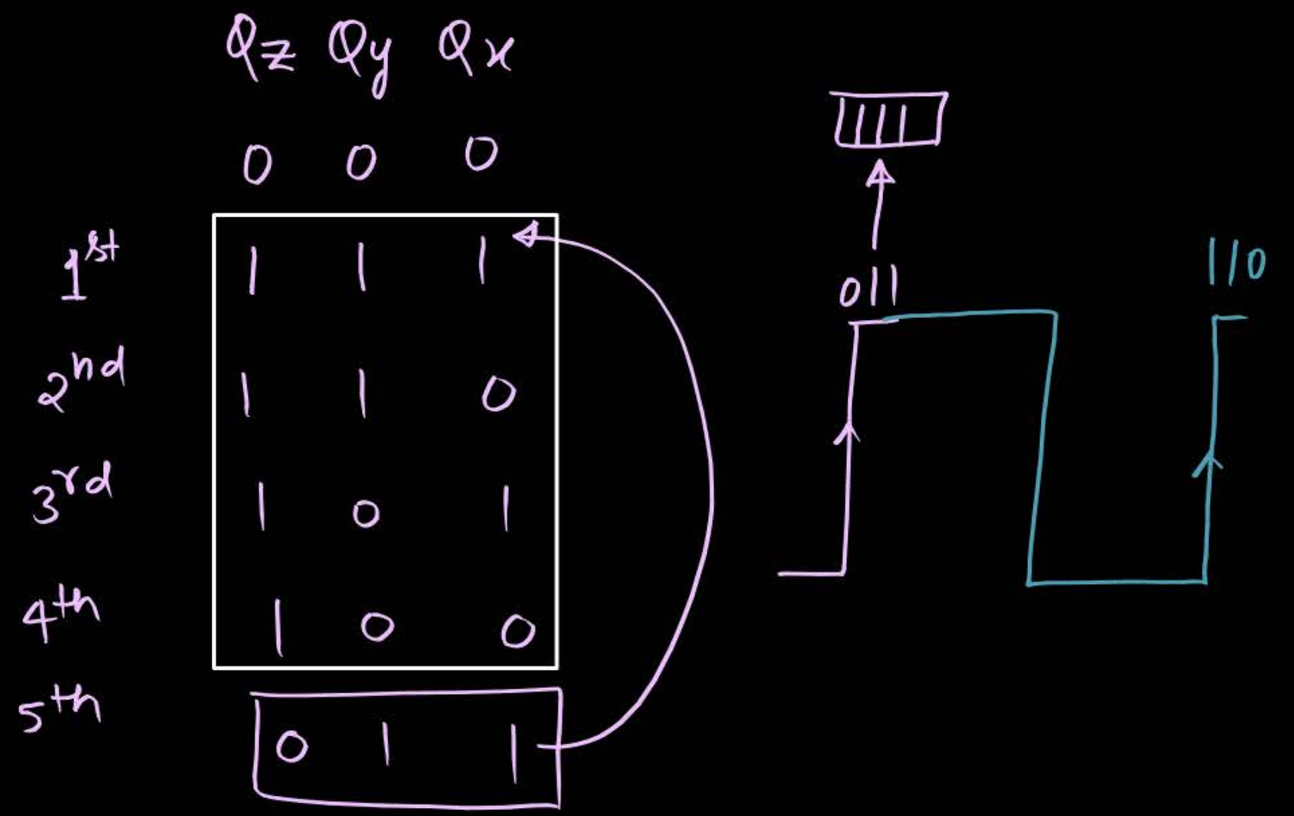
The circuit works as :

(a) MOD-5 down counter

(b) MOD-4 down counter

(c) MOD-6 down counter

(d) MOD-5 up counter


Qz Qy Qx
0 0 0
1st
2nd
3rd
4th
5th
1 1 1
1 1 0
1 0 1
1 0 0
0 1 1
111
011
110

Question

We have a MOD-32 down counter. If its starting state is $(3)_{10}$ then after application of 72 clock pulses the count of the counter will be $(27)_{10}$.

$31 \rightarrow 0$

$(3)_{10} \xrightarrow{2\times32} (3)_{10} \xrightarrow{3\text{ clk}} (0)_{10} \xrightarrow{1\text{ clk}} (31)_{10} \xrightarrow{4\text{ clk}} (27)_{10}$

Question

In module-6 ripple counter shown in figure, the output of 2-input gate is used to clear the J-K FF.

H·W

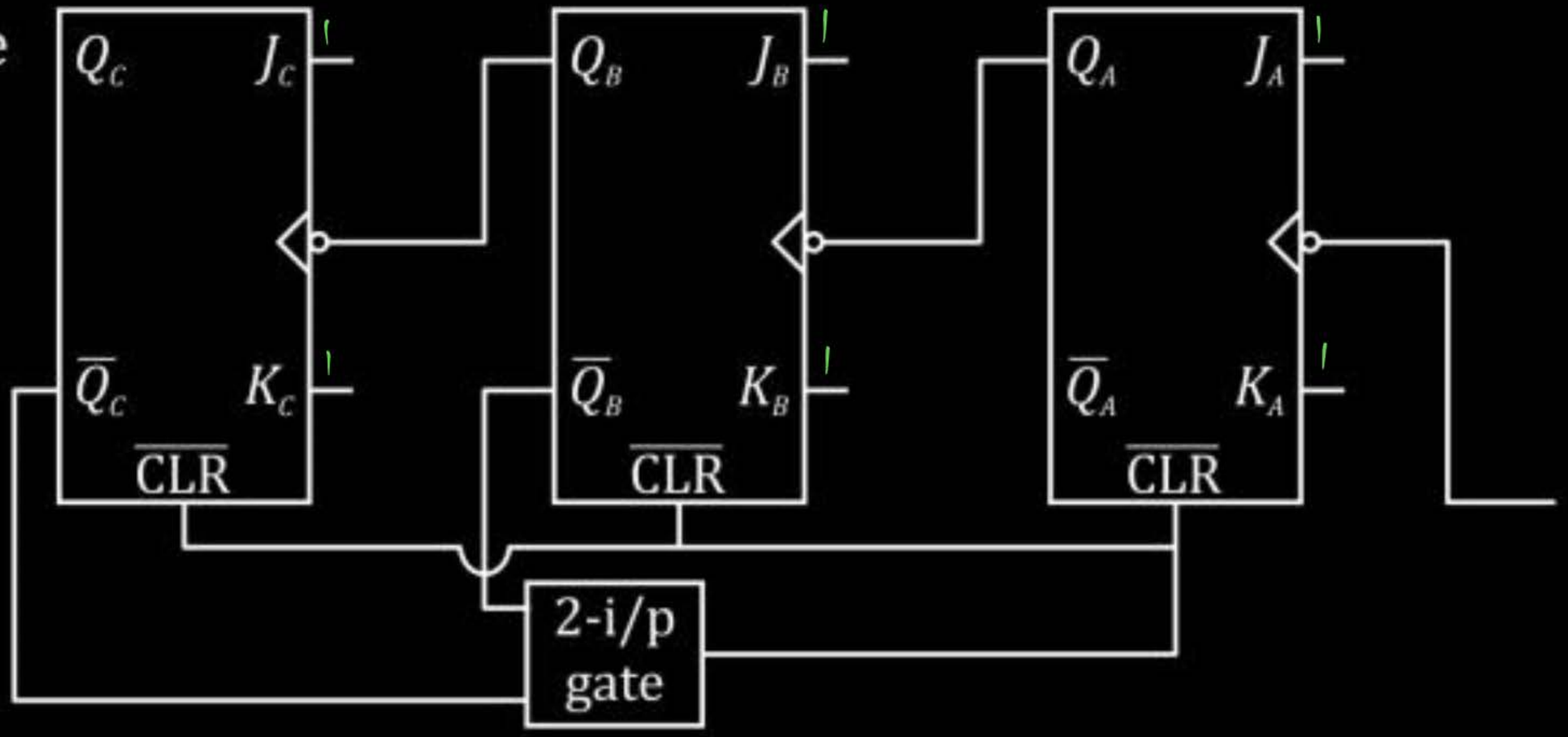
The gate will be

(a) NAND

(b) NOR

(c) OR

(d) AND



Question

We have 10-bit ripple counter which is counting in up sequence. Two most significant bits are NAND together to generate an output y. Output y is periodic waveform with T_{ON} (time duration for which y is high in one period) 15000 μsec. Then the clock frequency (kHz) 51.2 KHz

$MOD = 2^{10} = 1024 \longrightarrow$ 0 – 1023

No

$$f_{clk} = \frac{256}{5} KHz$$

$$= 51.2 KHz$$

2^9 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0

Q_9 Q_8 Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0

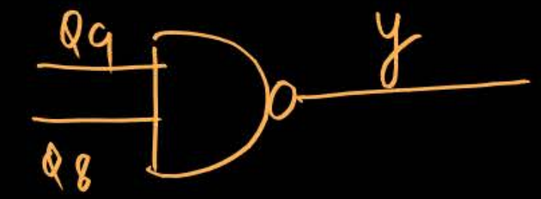
0 0 0 0 0 0 0 0 0 0

0 to 2^9 | 0 to 2^8

2^9 to 2^9+2^8-1 | 2^8 to 2^9-1

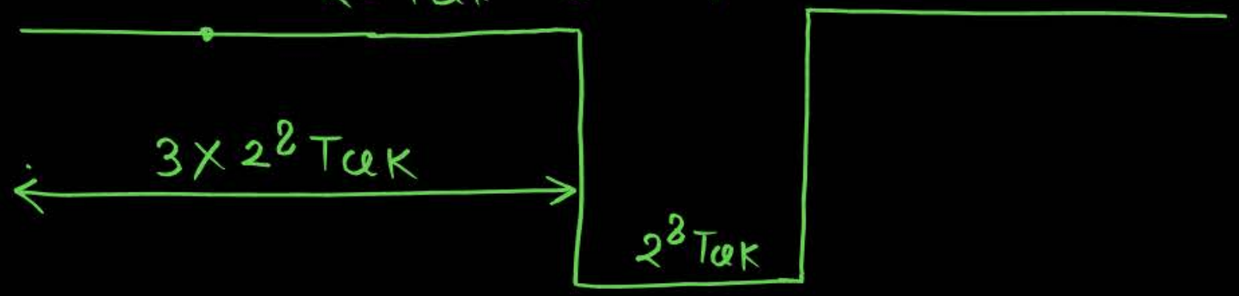
2^9 to 2^9+2^8-1 | 2^9 to 2^9+2^8-1

2^9+2^8 to $2^{10}-1$ | 2^9 to 2^9+2^8-1



$3 \times 2^8 T_{clk} = 15000\ \mu sec$

$2^8 T_{clk} = 5000\ \mu sec$



$T_y = T_{ON} + T_{off} = 3 \times 2^8 T_{clk} + 2^8 T_{clk}$

$= 2^{10} T_{clk}$

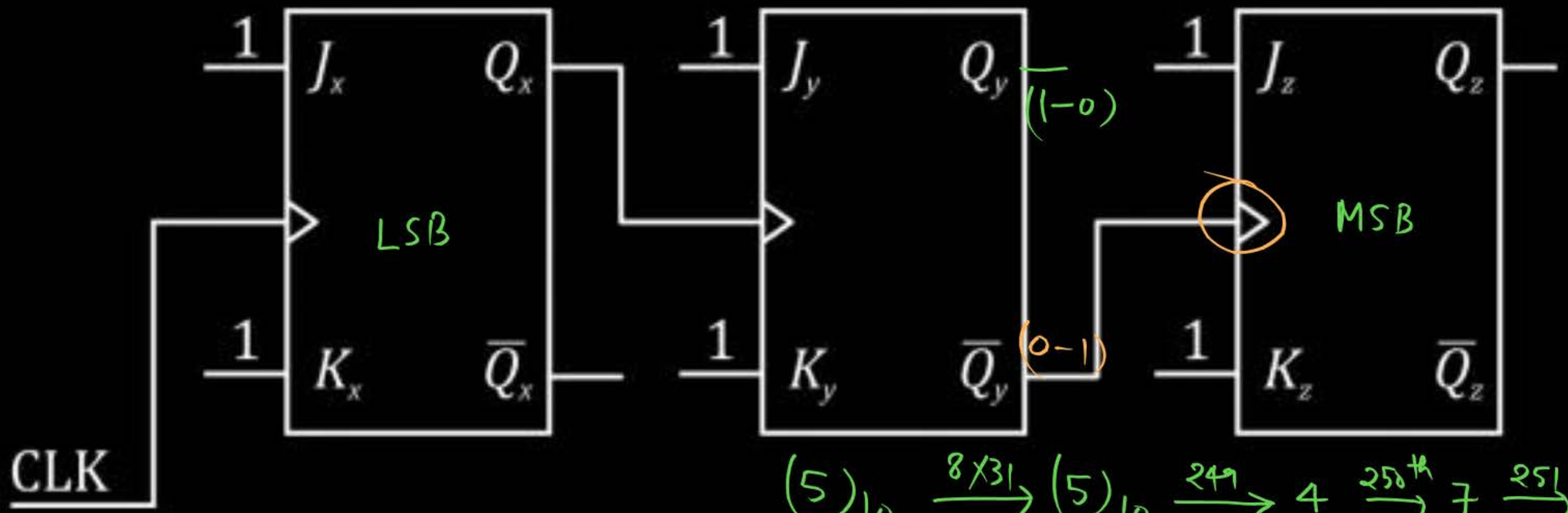
$f_{clk} = \frac{2^8}{5000\ \mu sec} = \frac{2^8 \times 10^3}{5}\ Hz$

$= 2^8/5\ KHz$

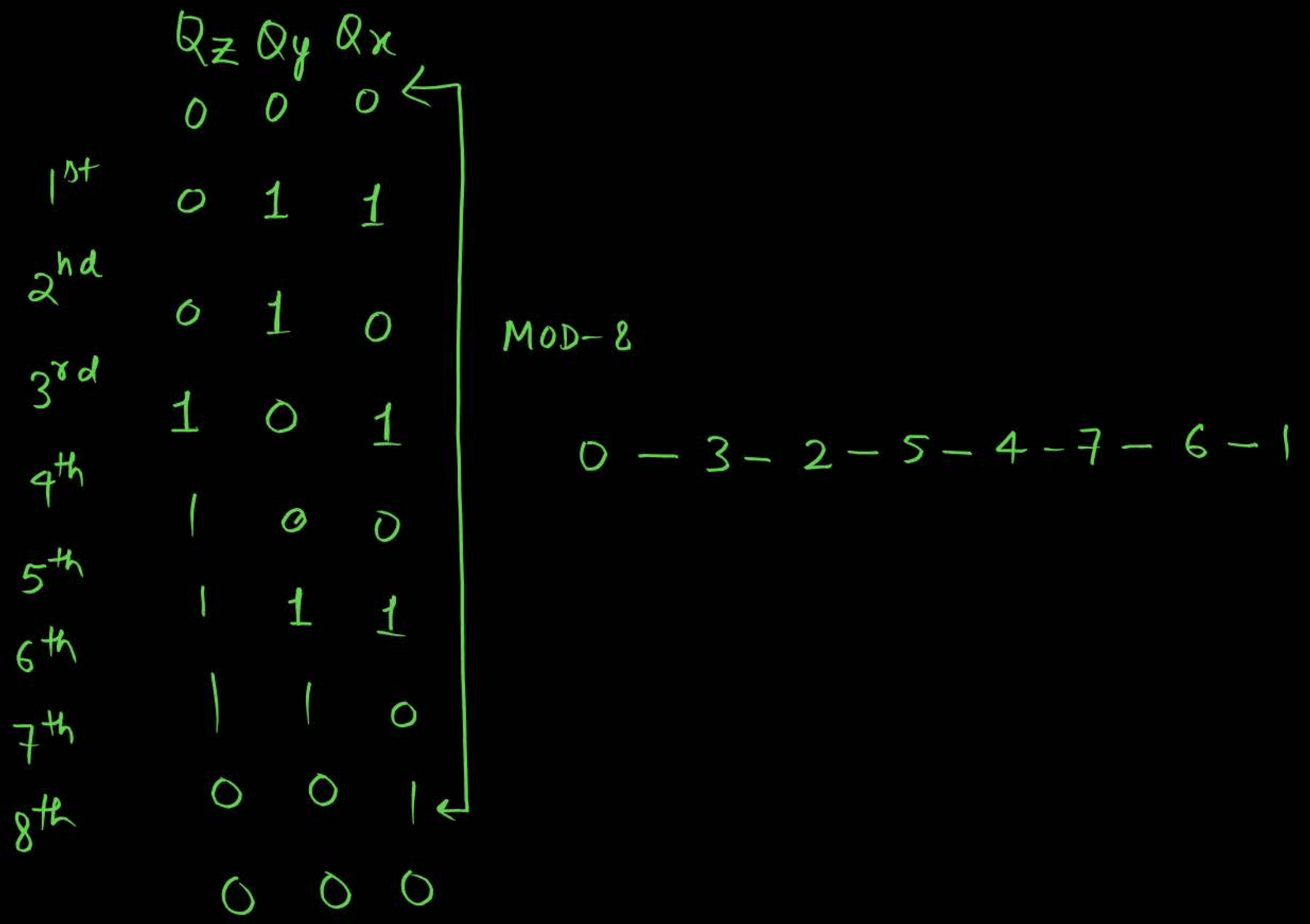
$f_y = f_{clk}/2^{10}$

Question

A sequential circuit is as given below :

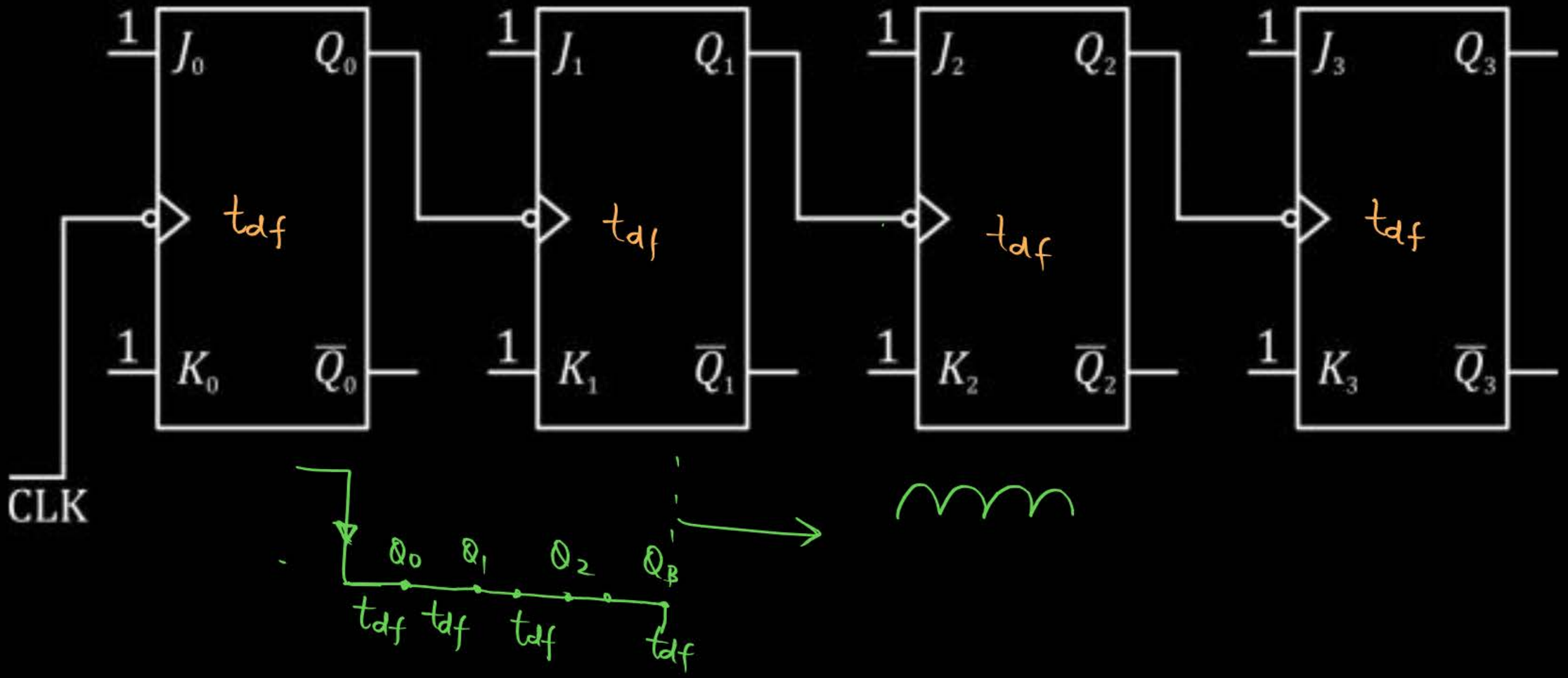


If starting state of the counter $Q_zQ_yQ_x$ is $(101)_2$ then after 251 CLK pulses output $Q_zQ_yQ_x$ is (6)$_{10}$.


Qz Qy Qx
0 0 0
1st 0 1 1
2nd 0 1 0
3rd 1 0 1
4th 1 0 0
5th 1 1 1
6th 1 1 0
7th 0 0 1
8th 0 0 0
MOD-8
0 – 3 – 2 – 5 – 4 – 7 – 6 – 1

Max. Clock Frequency:

Lets take a 4-bit asynchronous counter : Ripple Counter



Lets understand the worst case delay and max clock frequency :

$$(T_d)_{worst} = n\,t_{df}$$

for proper working $T_{clk} \geq n\,t_{df}$

$$\frac{1}{f_{clk}} \geq n\,t_{df}$$

$$f_{clk} \leq \frac{1}{n\,t_{df}}$$

$$(f_{clk})_{max} = \frac{1}{n\,t_{df}}$$

Topic : 2 Min Summary

- Question Discussion on Asynchronous counter
- fmax calculation and its significance

Thank you

GW

Soldiers !