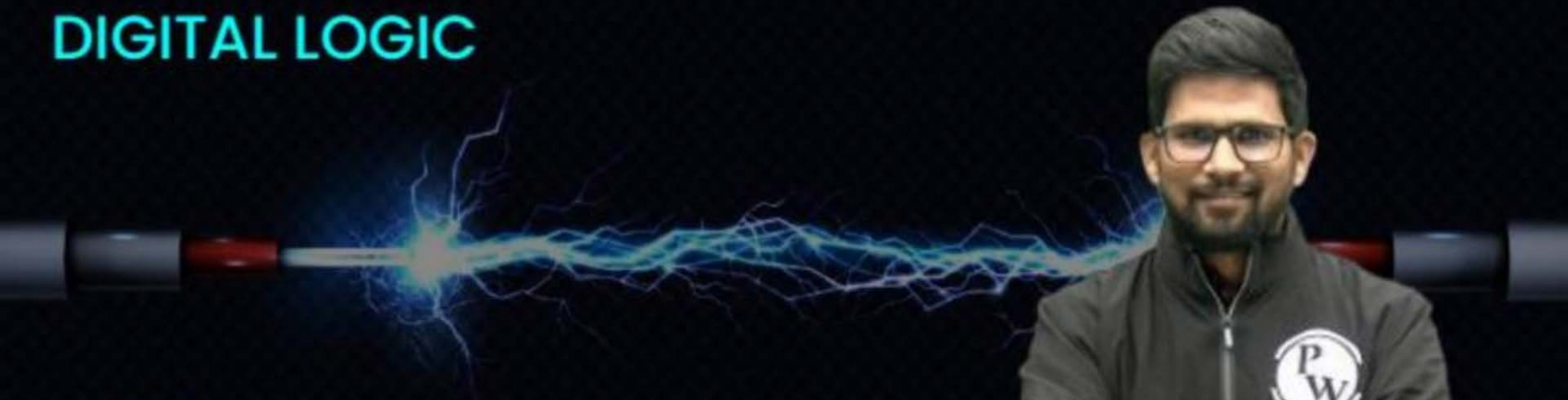
# COMPUTER SCIENCE & IT

## DIGITAL LOGIC



Lecture No: 06

Sequential Circuit



By- Chandan Gupta Sir

# Recap of Previous Lecture

- Synchronous Counter
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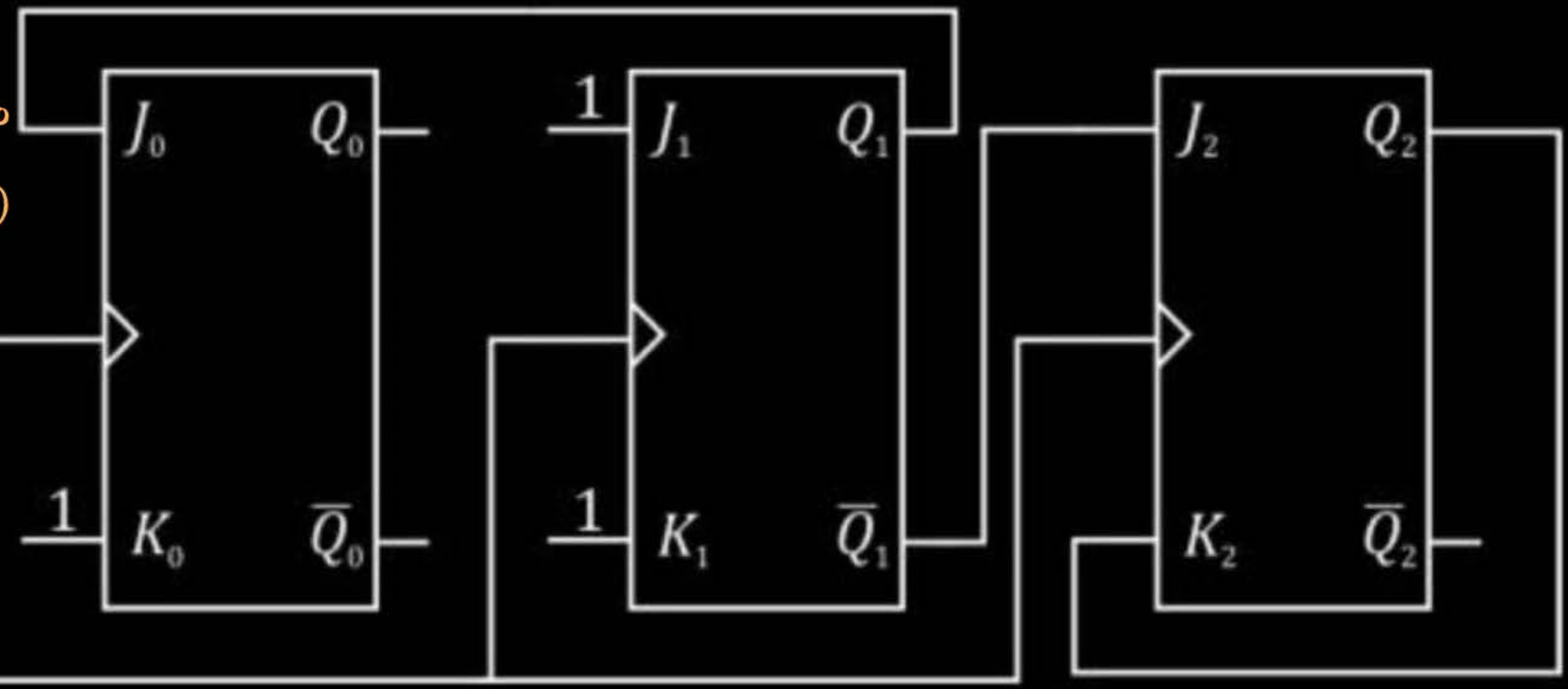
Synchronous Counter

## Question

A sequential circuit is as given below :




$Q_0(n+1)$
$= J_0\overline{Q}_0 + \overline{K}_0 Q_0$
$= Q_1(n) \cdot \overline{Q}_0(n)$

$Q_1(n+1)$
$= \overline{Q}_1(n)$

$Q_2(n+1)$
$= \overline{Q}_1\overline{Q}_2$
$+ \overline{Q}_2 \cdot Q_2$
$= \overline{Q_1(n)+Q_2(n)}$

If initial state of counter is $Q_2Q_1Q_0 = (001)_2$, then after 8th clock pulse, counter will be in state ( 1 )$_{10}$.

| | fclk/2 $Q_2$ | fclk/2 $Q_1$ | fclk/2 $Q_0$ | |
|---|---|---|---|---|
| | 0 | 0 | 1 | ↑ MOD-2 counter |
| 1st | 1 | 1 | 0 | ↓ |
| 2nd | 0 | 0 | 1 | |

$(001)_2 \xrightarrow{2 \times 4} (001)_2$

## Question

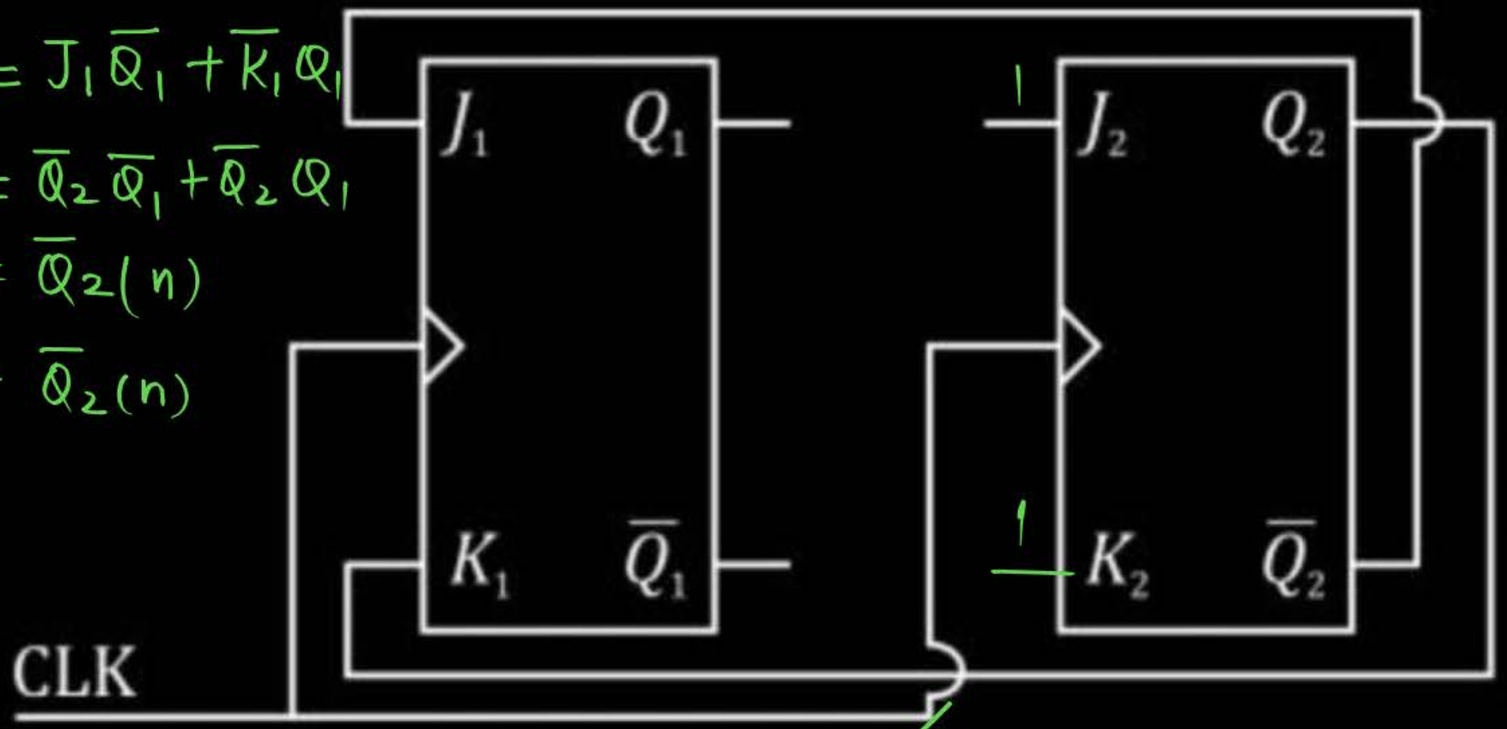
The output of the two FFs, $Q_1$ and $Q_2$ are initially at '0'. The sequence generated at $Q_1$ after application of clock pulses :

$Q_1(n+1) = J_1\overline{Q}_1 + \overline{K}_1 Q_1$

$= \overline{Q}_2\overline{Q}_1 + \overline{Q}_2 Q_1$

$= \overline{Q}_2(n)$

$Q_2(n+1) = \overline{Q}_2(n)$




| | $Q_1$ | $Q_2$ |
|---|---|---|
| | 0 | 0 |
| 1st | 1 | 1 |
| 2nd | 0 | 0 |
| 3rd | 1 | 1 |

(a) 01110.....

(b) 01010.....

(c) 00110.....

(d) 01100.....

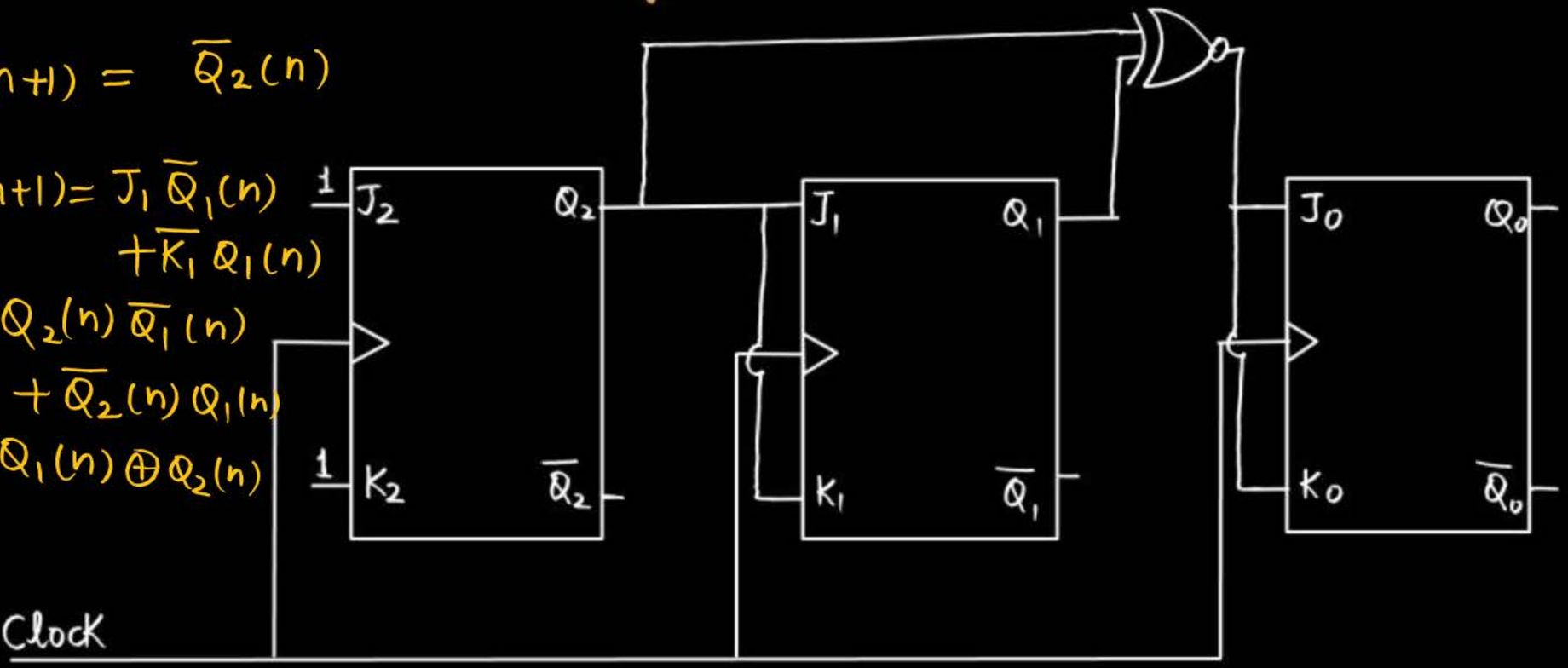
#Q. A sequential ckt is as given below:

$Q_2(n+1) = \overline{Q_2}(n)$

$Q_1(n+1) = J_1\overline{Q_1}(n) + \overline{K_1}Q_1(n)$

$= Q_2(n)\overline{Q_1}(n) + \overline{Q_2}(n)Q_1(n)$

$= Q_1(n) \oplus Q_2(n)$




$Q_0(n+1) = T_0\overline{Q_0} + \overline{K_0}Q_0$

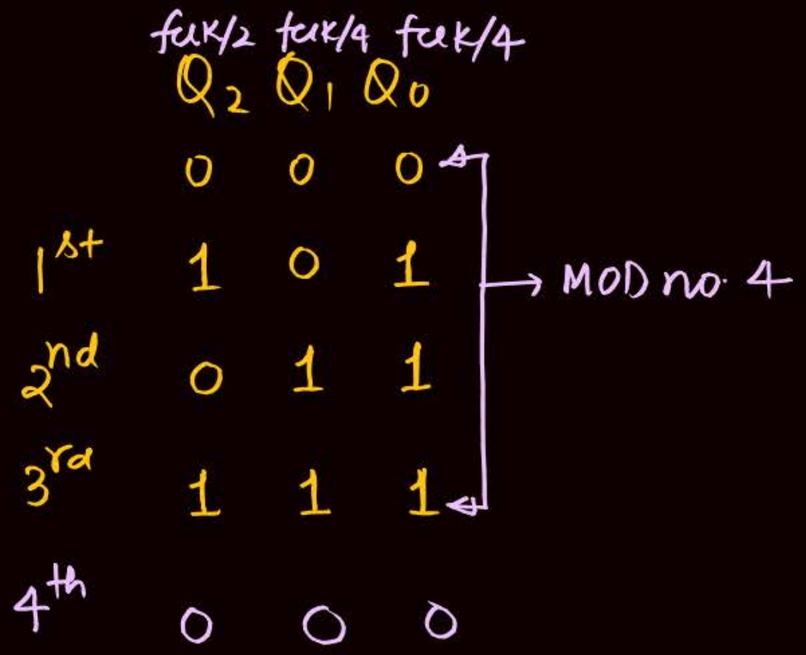
$= (Q_2 \odot Q_1)\overline{Q_0} + \overline{Q_2 \odot Q_1}\,Q_0$

$= Q_2 \odot Q_1 \oplus Q_0$

$= \overline{Q_2(n) \oplus Q_1(n) \oplus Q_0(n)}$

The ckt starts with $Q_2Q_1Q_0 = (000)_2$ then next three state of the counter will be

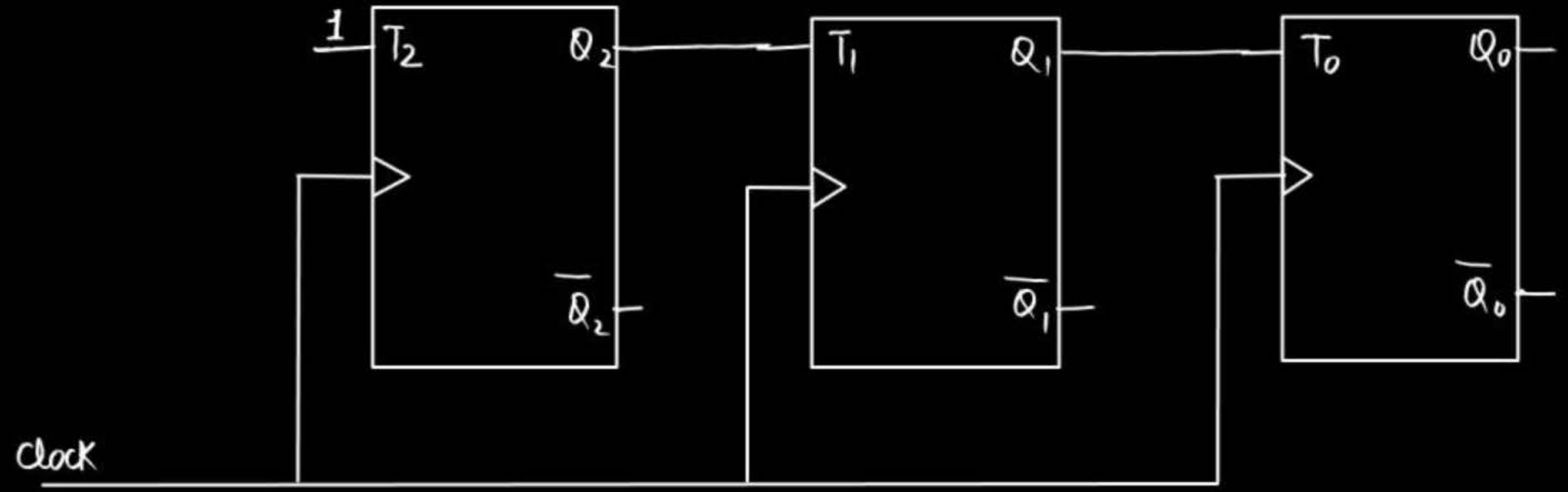
a. 101, 111, 011 b. 101, 010, 111 c. 101, 011, 111 d. 111, 011, 101


fclk/2 fclk/4 fclk/4
Q2 Q1 Q0
0 0 0
1st 1 0 1
2nd 0 1 1
3rd 1 1 1
4th 0 0 0
MOD no 4

#Q. A sequential ckt is as given below:

$Q_2(n+1) = T_2 \oplus Q_2(n) = 1 \oplus Q_2(n) = \overline{Q_2}(n)$ , $Q_1(n+1) = T_1 \oplus Q_1(n) = Q_2(n) \oplus Q_1(n)$

$Q_0(n+1) = T_0 \oplus Q_0(n) = Q_1(n) \oplus Q_0(n)$




| | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|
| | 1 | 0 | 0 |
| 1st | 0 | 1 | 0 |
| 2nd | 1 | 1 | 1 |
| 3rd | 0 | 0 | 0 |
| 4th | 1 | 0 | 0 |

This circuit starts with $Q_2Q_1Q_0 = (100)_2$ then state of the counter after 3rd clock edge will be

a. $(010)_2$ b. $(111)_2$ c. $(100)_2$ d. $(000)_2$

#Q. A sequential ckt is as given below:

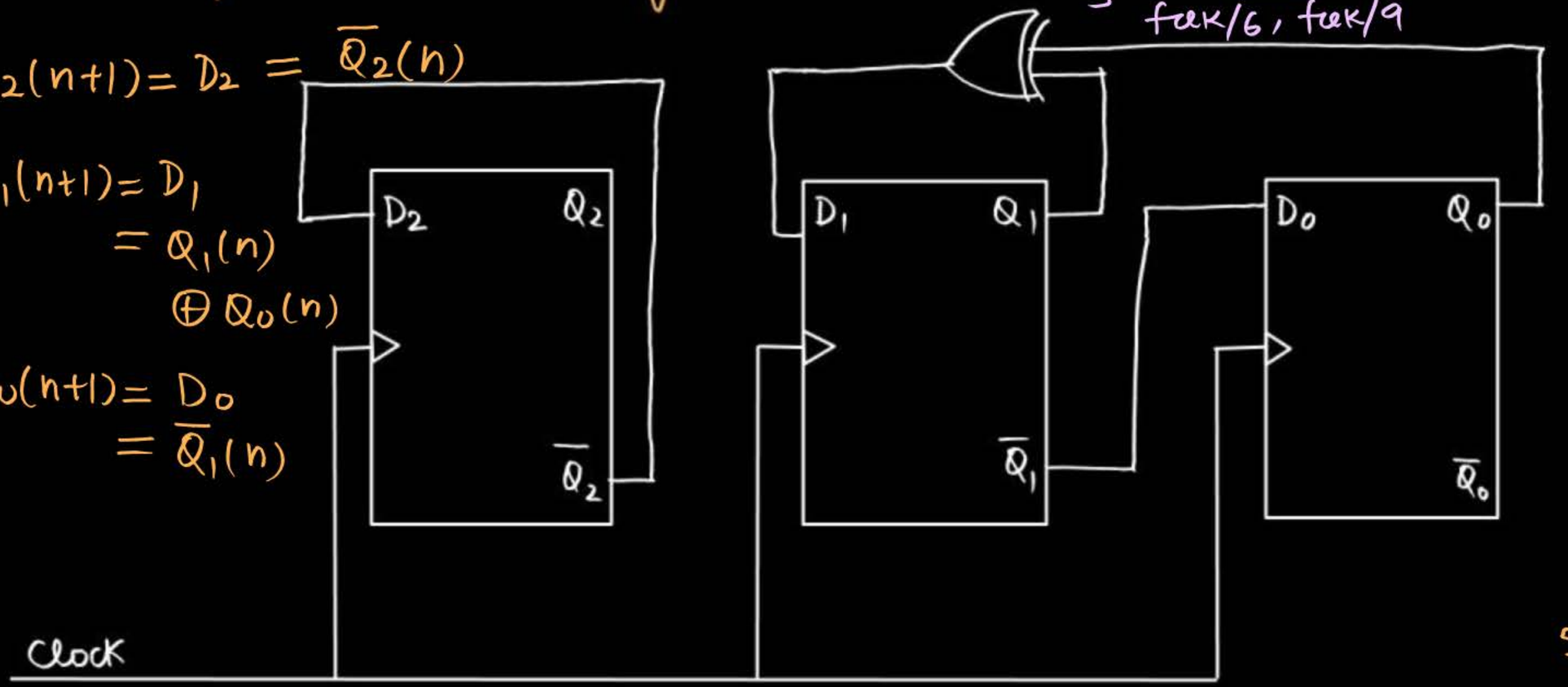
$\checkmark \frac{f_{clk}}{3}$, $\frac{3T_{clk}}{f_{clk}/6, f_{clk}/9} = T_{Q_0}$, $T_1 = 2T_{Q_0}$, $T_2 = 3T_{Q_0}$

$f_{clk}/2$ $f_{clk}/3$ $f_{clk}/3$

$Q_2(n+1) = D_2 = \overline{Q_2(n)}$

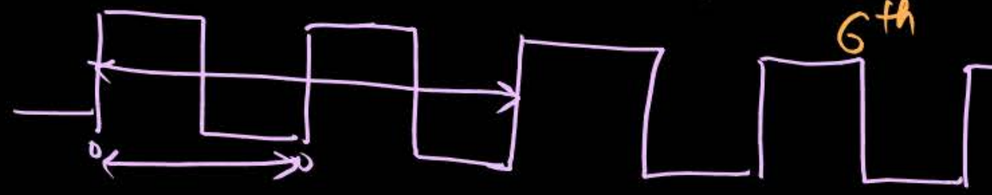
$Q_1(n+1) = D_1 = Q_1(n) \oplus Q_0(n)$

$Q_0(n+1) = D_0 = \overline{Q_1(n)}$




| | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|
| | 1 | 0 | 1 |
| 1st | 0 | 1 | 1 |
| 2nd | 1 | 0 | 0 |
| 3rd | 0 | 0 | 1 |
| 4th | 1 | 1 | 1 |
| 5th | 0 | 0 | 0 |

a. If starting state of the counter is $Q_2Q_1Q_0 = (101)_2$ then what is the state of the counter after 4th clock edge $(7)_{10}$.

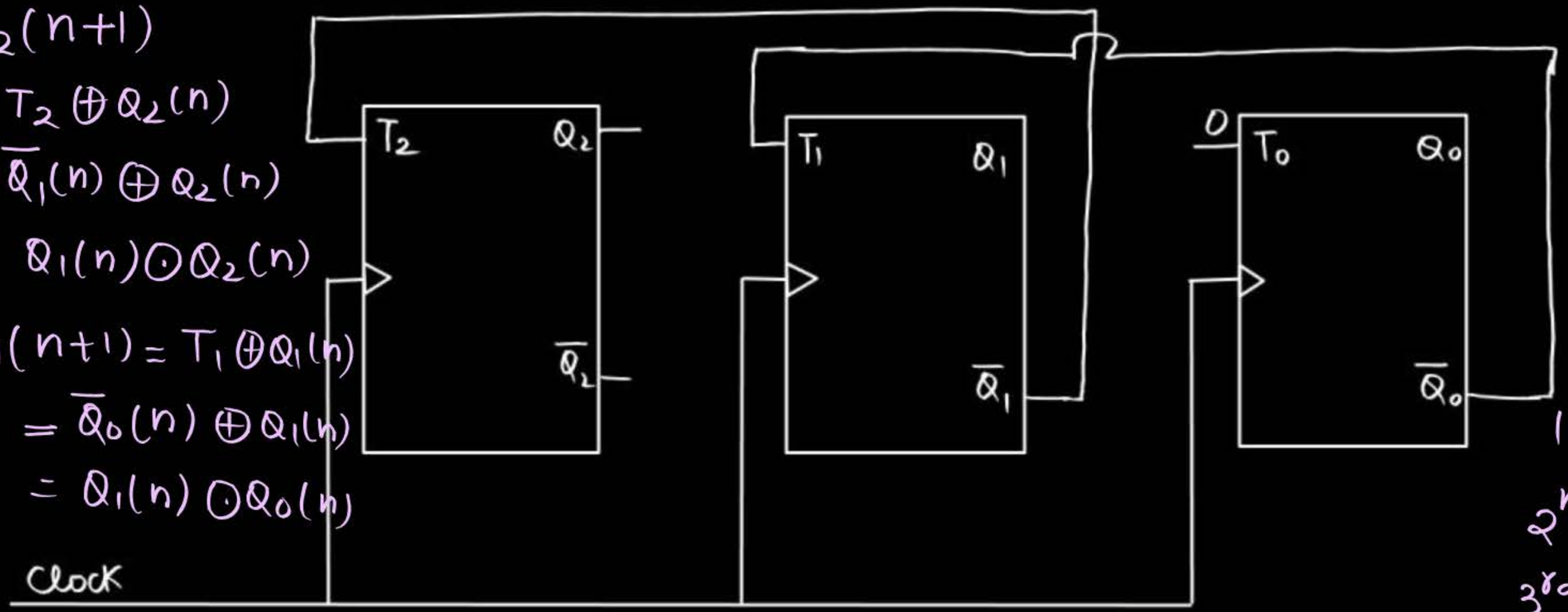



b. MOD no. of the counter is 6.

#Q. A sequential ckt is as given below:

$Q_2(n+1)$
$= T_2 \oplus Q_2(n)$
$= \overline{Q_1}(n) \oplus Q_2(n)$
$= Q_1(n) \odot Q_2(n)$

$Q_1(n+1) = T_1 \oplus Q_1(n)$
$= \overline{Q_0}(n) \oplus Q_1(n)$
$= Q_1(n) \odot Q_0(n)$




$Q_0(n+1) = T_0 \oplus Q_0(n)$
$= 0 \oplus Q_0(n)$
$Q_0(n+1) = Q_0(n)$

fast/4 fast/2

| $Q_2$ | $Q_1$ | $Q_0$ | |
|---|---|---|---|
| 0 | 0 | 0 | ← |
| 1st 1 | 1 | 0 | → MOD 4 |
| 2nd 1 | 0 | 0 | |
| 3rd 0 | 1 | 0 | ← |
| 4th 0 | 0 | 0 | |

a. If input clock frequency is 10MHz, then O/P frequency at O/P $Q_1$ will be $\frac{5}{}$ MHz.

b. If counter starts with $(110)_2$ then summation of next three states will be $(6)_{10}$.

$Q_2Q_1Q_0 =$

# #Q. A sequential ckt is as given below: 0—2-3—1—1

$Q_1(n+1)$

$= J_1\overline{Q}_1 + \overline{K}_1 Q_1$

$= \overline{Q}_0\overline{Q}_1 + \overline{Q}_0 Q_1$

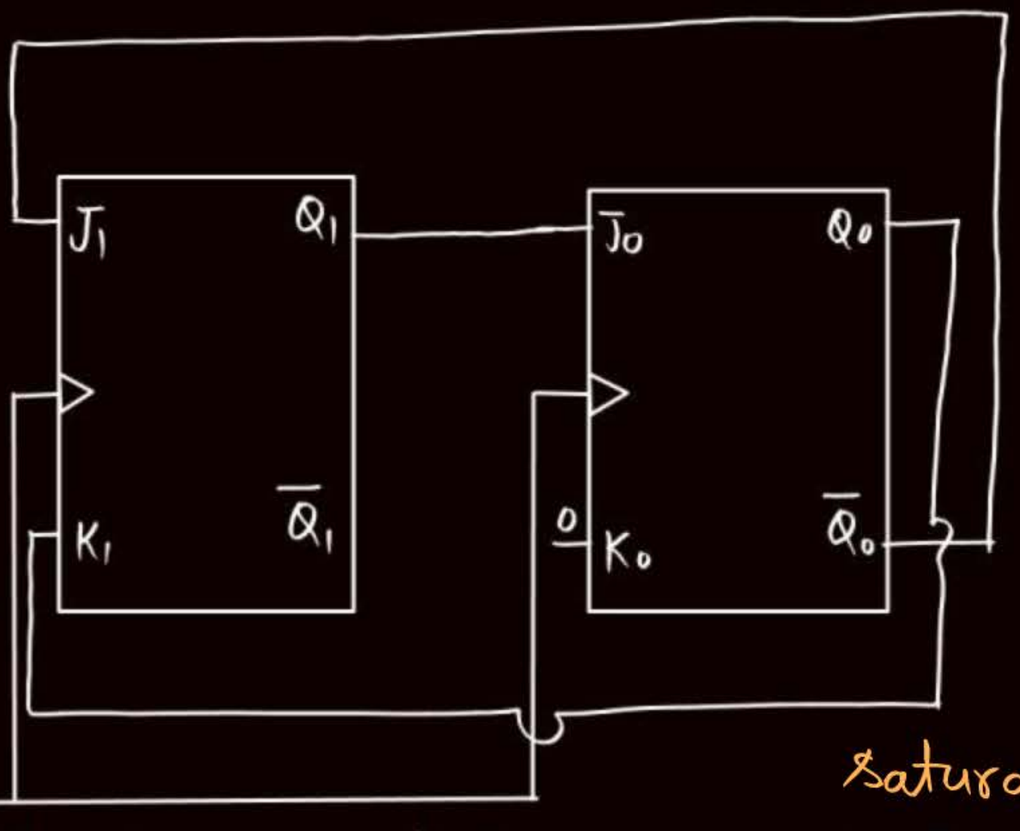
$= \overline{Q}_0(n)$

$Q_0(n+1) = J_0\overline{Q}_0 + \overline{K}_0 Q_0$

$= Q_1\overline{Q}_0 + 1 \cdot Q_0$

$= (Q_1 + Q_0)$

$= Q_1(n) + Q_0(n)$




| | $Q_1$ | $Q_0$ |
|---|---|---|
| | 0 | 0 |
| 1st | 1 | 0 |
| 2nd | 1 | 1 |
| 3rd | 0 | 1 |
| 4th | 0 | 1 |
| 5th | 0 | 1 |

Saturated counter

Given counter started with $Q_1Q_0 = (00)_2$ then next four states of the counter will be

a. 10, 11, 01, 00 b. 10, 11, 00, 10 c. 10, 11, 01, 01 d. 01, 11, 10, 10

# Q. Design a counter (saturated counter) with transition as given below:

HW $(00 - 11 - 01 - 10 - 10)$ → using (a) JK FFs
(b) T FFs

# Synchronous Series Carry Counter

4-bit synchronous series carry counter :

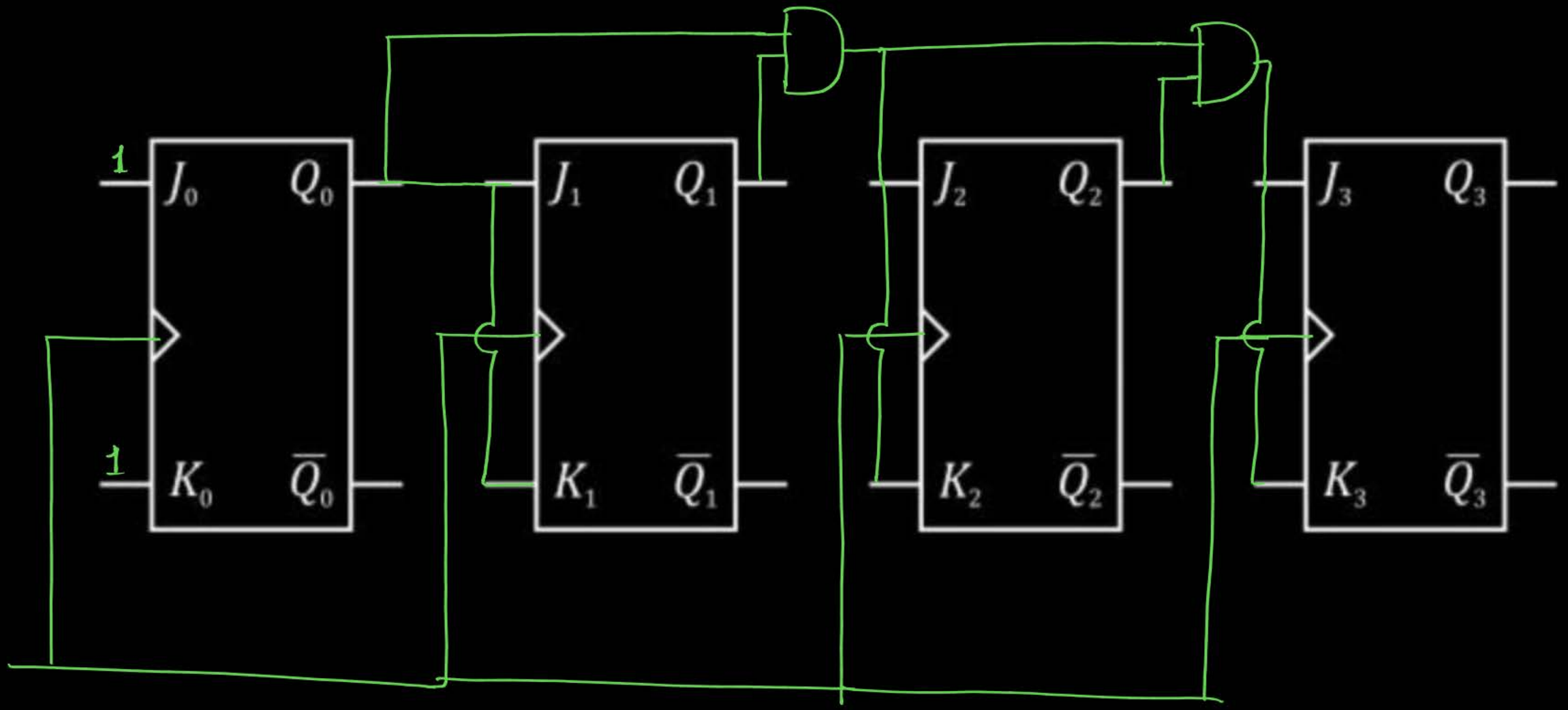
Lest analyze the sequence and design it :

| $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |

1st
2nd
3rd

| $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

Design using J-K FF : →

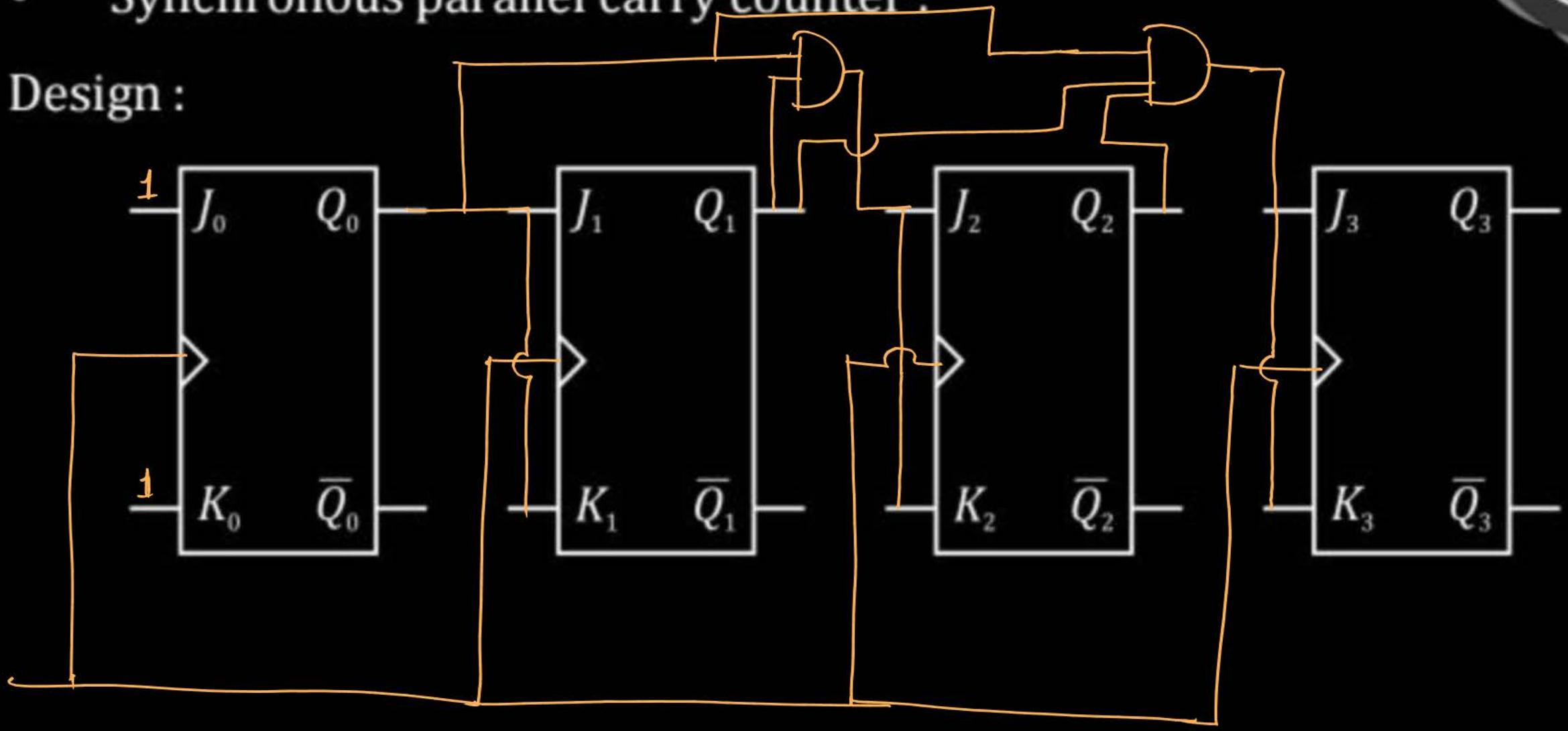


No. of AND gate require is : For n-bit synchronous series carry counter, $(n-2)$

2-i/p AND gate will be required

- Synchronous parallel carry counter :

Design :



- No. of AND gates required for n-bit synchronous parallel carry counter $= (n-2)$
  - The highest multi i/p AND gate $= (n-1)$ i/p AND gate

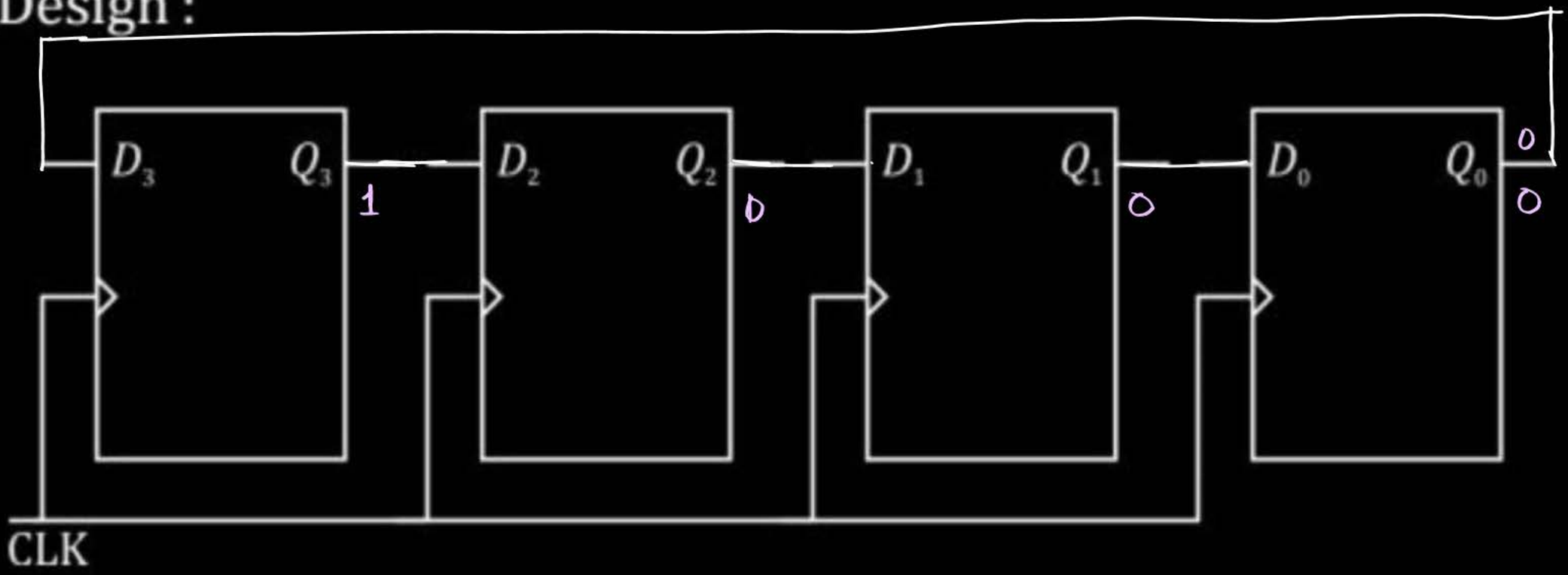
# Ring Counter

$Q_3(n+1) = D_3 = Q_0(n)$ , $Q_2(n+1) = D_2 = Q_3(n)$

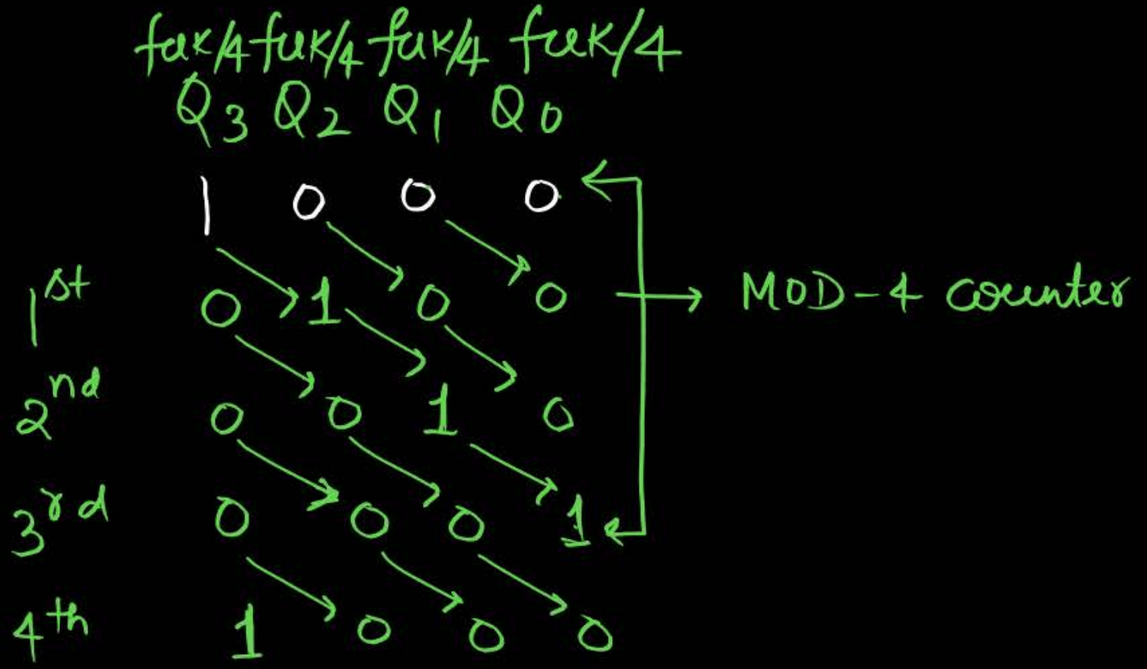
$Q_1(n+1) = D_1 = Q_2(n)$ , $Q_0(n+1) = D_0 = Q_1(n)$

4-bit Ring Counter :

Circuit Design :



Working :


fck/4 fck/4 fck/4 fck/4
Q3 Q2 Q1 Q0
1 0 0 0
1st 0 1 0 0
2nd 0 0 1 0
3rd 0 0 0 1
4th 1 0 0 0
MOD-4 counter

## Imp points of Ring Counter : →

- In a n-bit ring counter no. of used states = $n$ as MOD no. = $n$ always.
- No. of unused states = $(2^n - n)$
- Frequency at the o/p of each ff will be $f_Q = \frac{f_{CLK}}{n}$ i.e. divided by MOD no. at each o/p.

# A 4-bit ring counter started with state $(1010)_2$, then its MOD no ——.

H.W. and the next three states ( )$_{10}$, ( )$_{10}$, ( )$_{10}$.

# Topic : 2 Min Summary

→ Synchronous Counter

Thank you

GW

*Soldiers !*