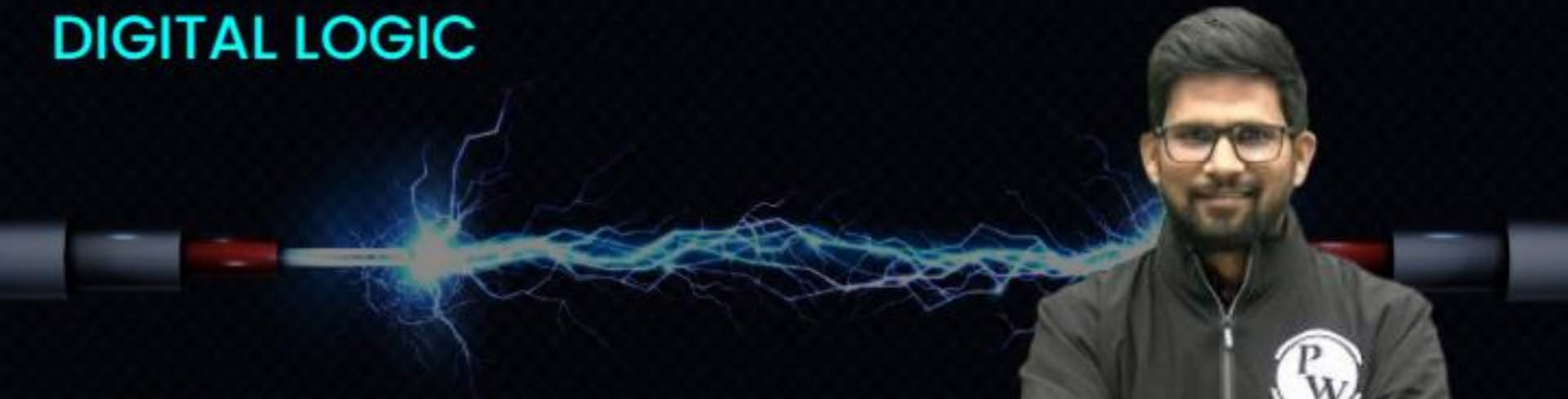
COMPUTER SCIENCE & IT

DIGITAL LOGIC



Lecture No: 06

Miscellaneous Topics

By- Chandan Gupta Sir

Recap of Previous Lecture

- Question Practice

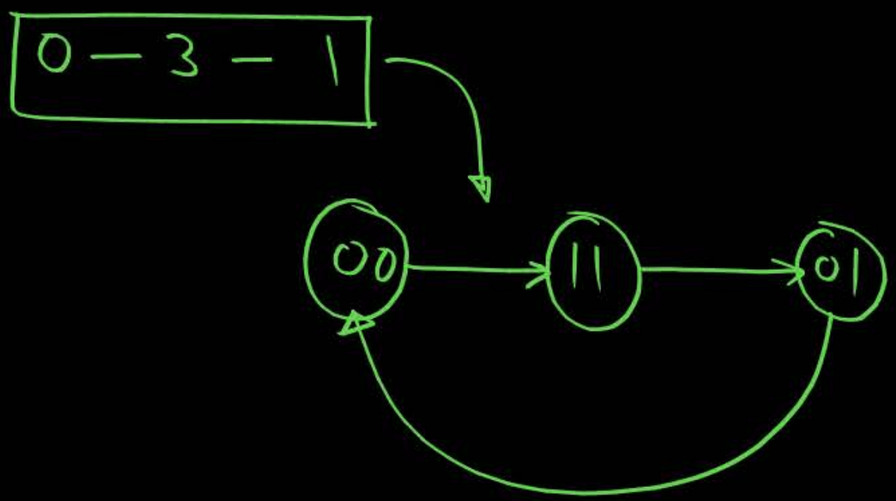
State transition Diagram

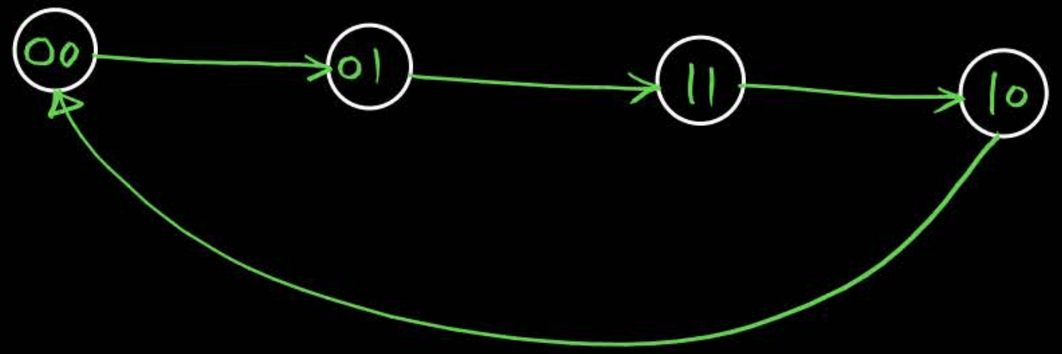
State Transition Diagram

What is state transition diagram ?

- A diagram that represents all the possible transitions of a sequential CKt.

0 – 1 – 3 – 2 ⟶ Counter

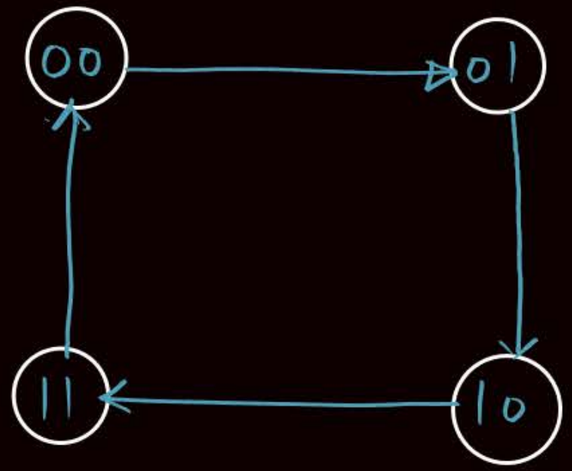




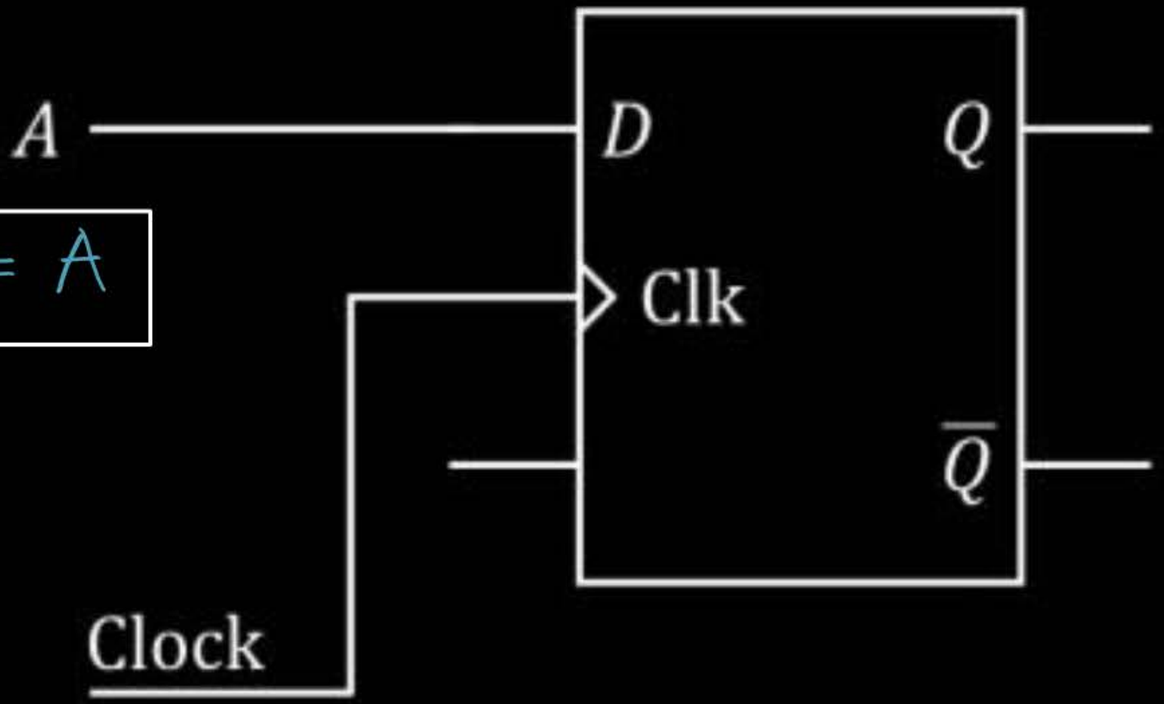
$00 - 01 - 10 - 11$

$Q_1(n+1) = \overline{Q_1}(n)$

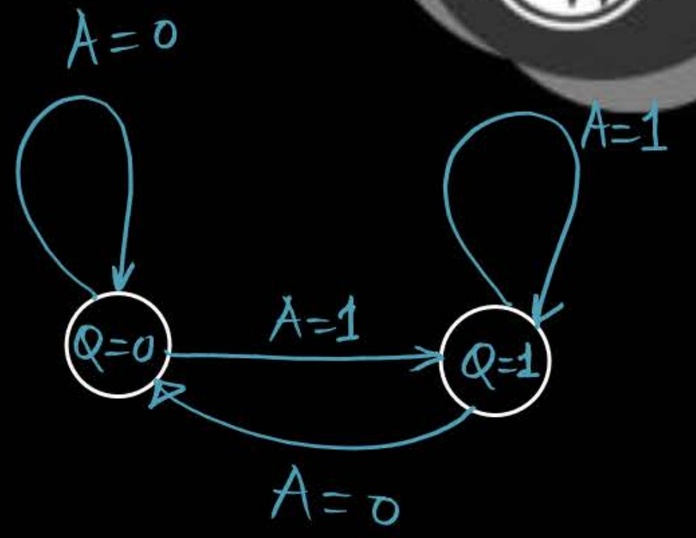
$Q_0(n+1) = \overline{Q_0}(n)$



- Lets understand it with an example :

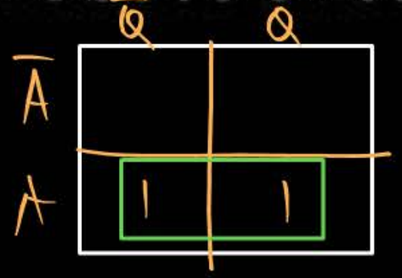


$Q(n+1) = D = A$



A	Q(n)	Q(n+1)
0	0	0
0	1	0
1	0	1
1	1	1

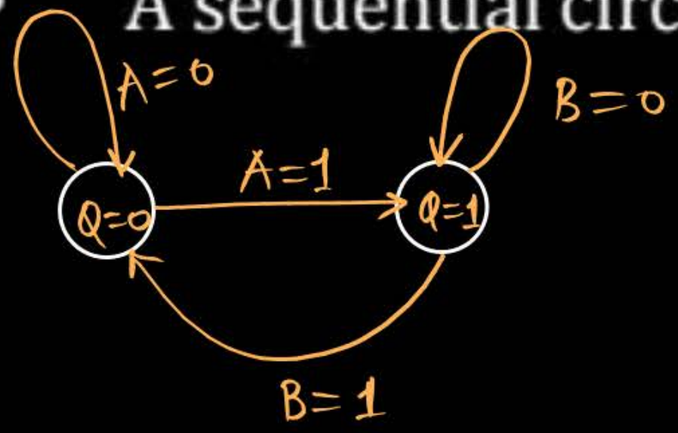
State transition diagram for above circuit will be :

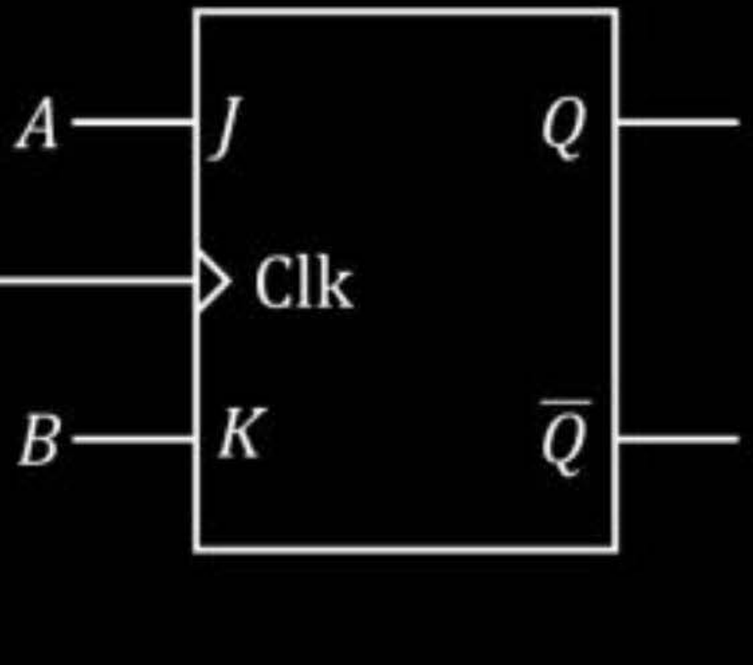


$Q(n+1) = A$

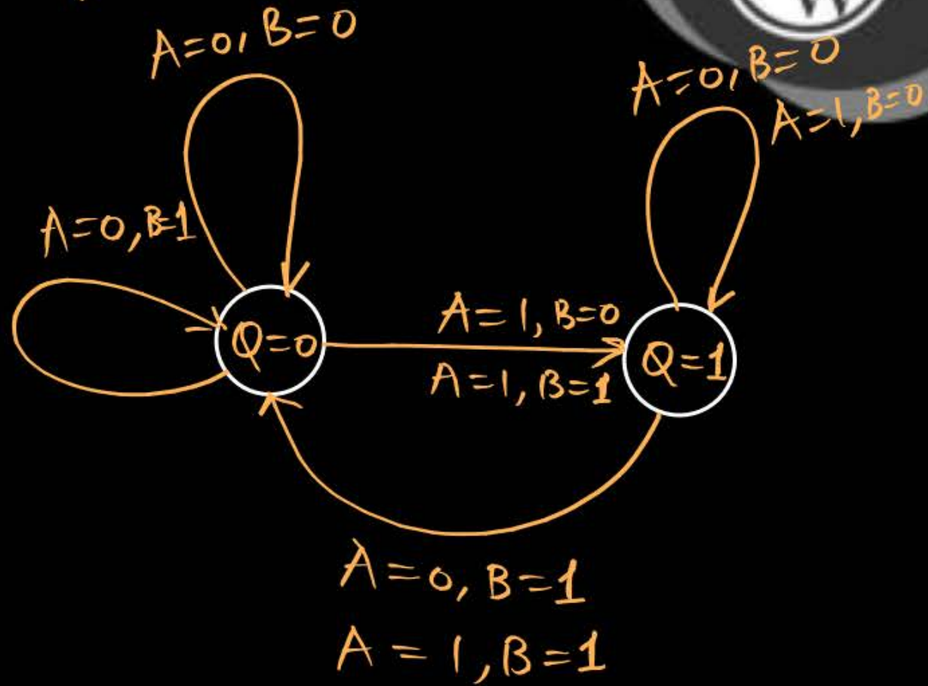
$Q(n+1) = \{2, 3$

- A sequential circuit is as given below :





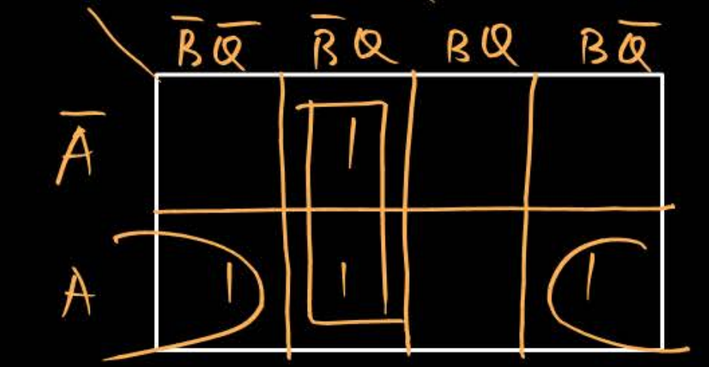
$Q(n+1) = A\bar{Q}(n) + \bar{B}Q(n)$



State transition diagram of above circuit will be :

A	B	Q(n)	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$Q(n+1) = \Sigma(1, 4, 5, 6)$



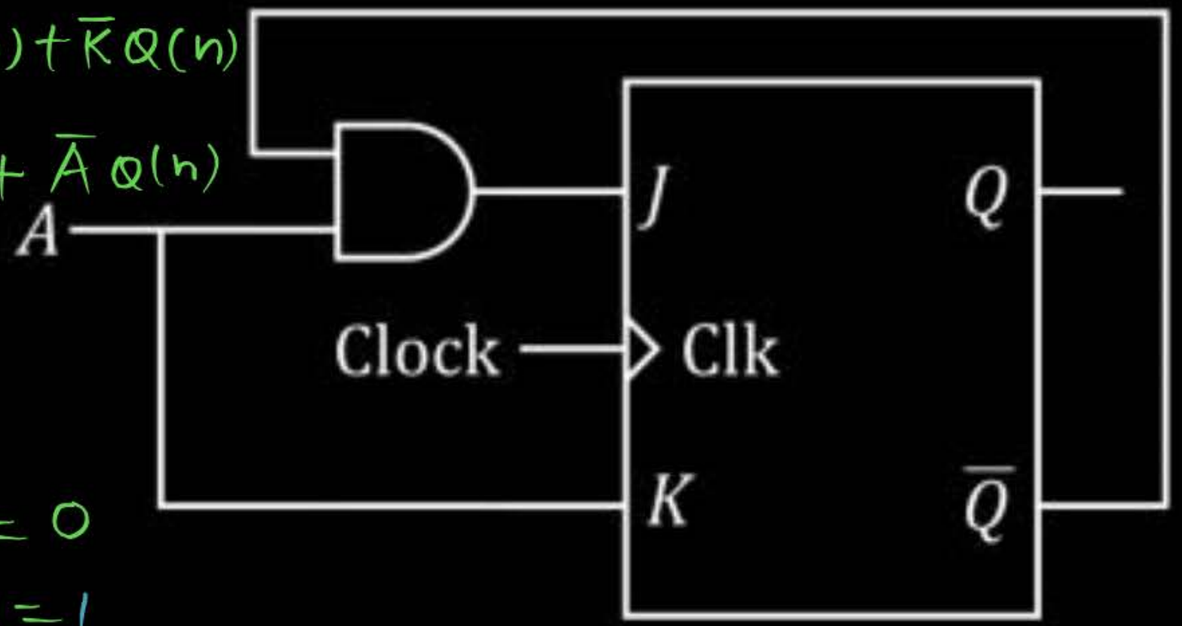
$$Q(n+1) = A\bar{Q} + \bar{B}Q$$

$J = A$

$K = B$

Question

A sequential circuit is as given below :



$Q(n+1) = J\overline{Q}(n) + \overline{K}Q(n)$

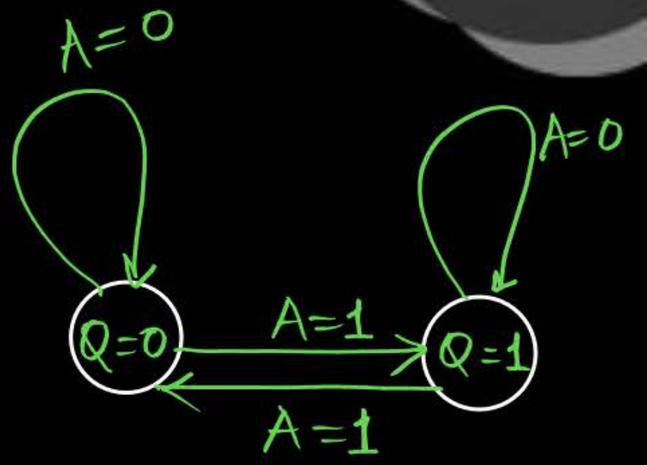
$= A\overline{Q}(n)\,\overline{Q}(n) + \overline{A}\,Q(n)$

$Q(n+1) = A \oplus Q(n)$

$Q(n) = 0$

$A = 0 \longrightarrow Q(n+1) = 0$

$A = 1 \longrightarrow Q(n+1) = 1$

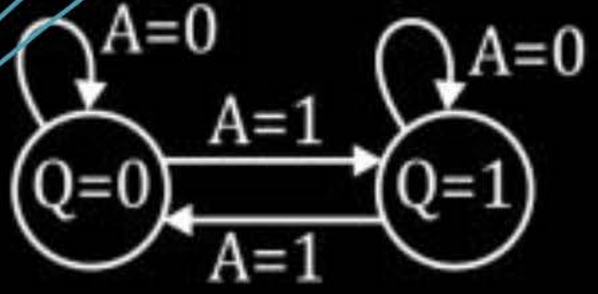


State transition diagram of above sequential circuit is

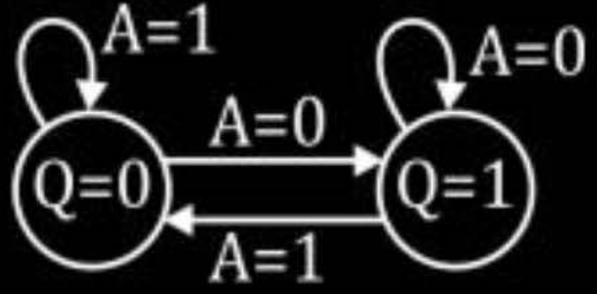
$Q(n) = 1, \quad A = 0 \longrightarrow Q(n+1) = 1$

$A = 1 \longrightarrow Q(n+1) = 0$

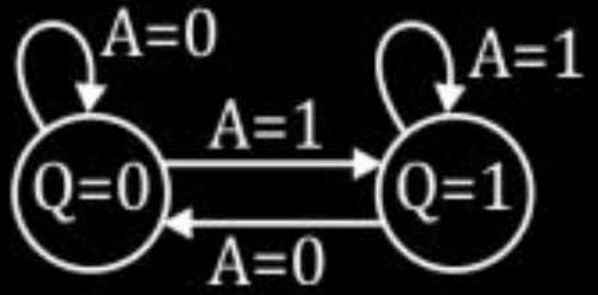
(a)



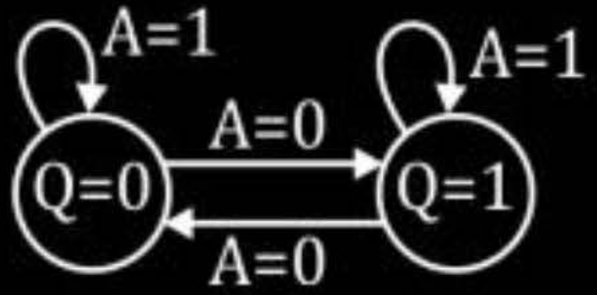
(b)



(c)

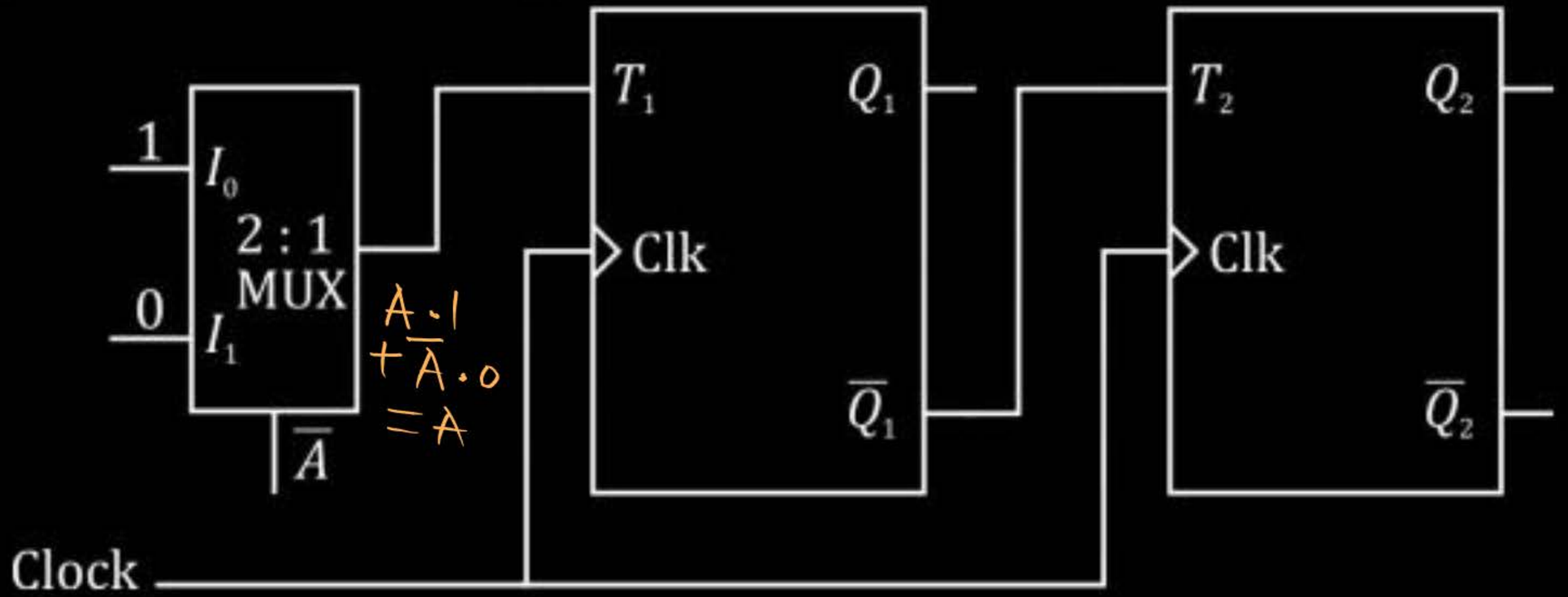


(d)



Question

A sequential circuit is as given below :



State transition diagram of above circuit will be :

$$Q_1(n+1) = T_1 \oplus Q_1(n) = A \oplus Q_1(n)$$

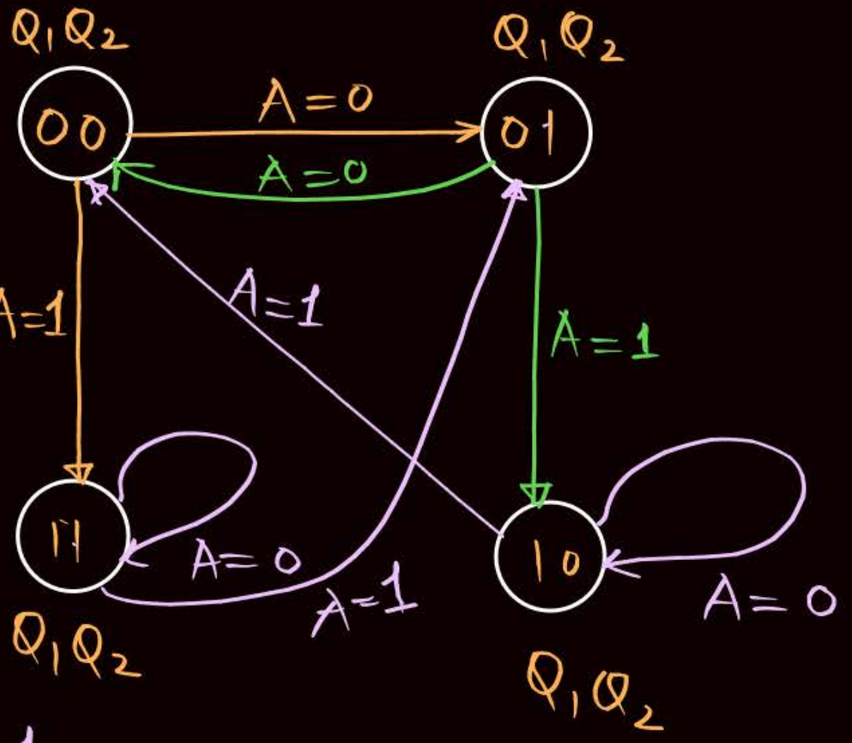
$$Q_2(n+1) = T_2 \oplus Q_2(n) = \bar{Q}_1(n) \oplus Q_2(n) = Q_1(n) \odot Q_2(n)$$

$Q_1(n)=1$, $Q_2(n)=0$:
- $A=0 \rightarrow Q_1(n+1) = 1$
- $Q_2(n+1)=0$

$\Rightarrow A=1, Q_1(n+1)=0$, $Q_2(n+1)=0$

$Q_1(n)=1$, $Q_2(n)=1$:
- $A=0$, $Q_1(n+1)=1$
- $Q_2(n+1)=1$

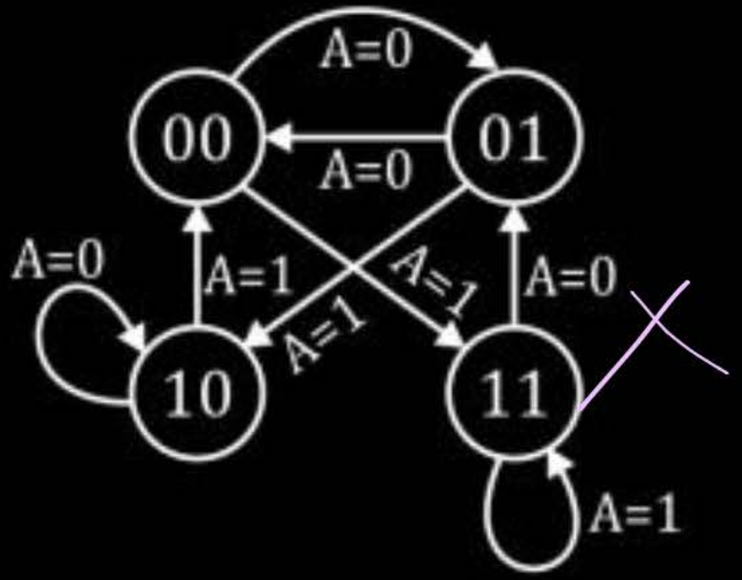
$A=1 \rightarrow Q_1(n+1)=0$, $Q_2(n+1)=1$



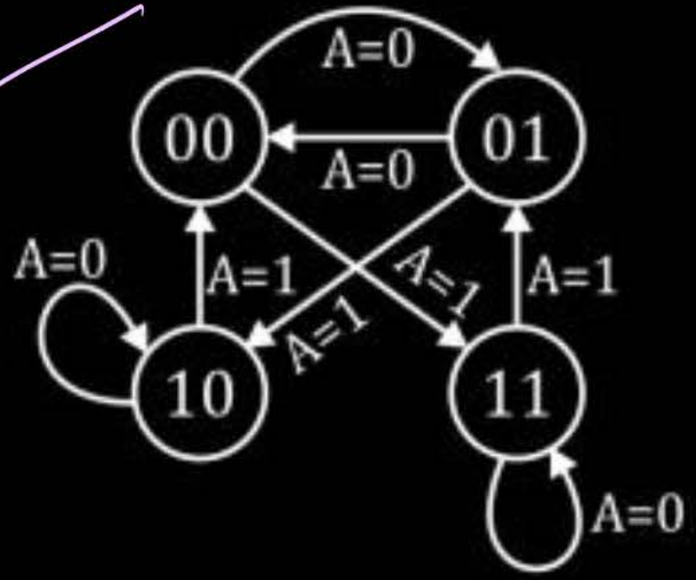
$Q_1(n)=0$, $Q_2(n)=0$:
- $A=0 \rightarrow Q_1(n+1) = 0$, $Q_2(n+1)=1$
- $A=1 \rightarrow Q_1(n+1) = 1$, $Q_2(n+1)=1$

$Q_1(n)=0$, $Q_2(n)=1$:
- $A=0 \rightarrow Q_1(n+1)=0$, $Q_2(n+1)=0$
- $A=1, Q_1(n+1)=1$, $Q_2(n+1)=0$

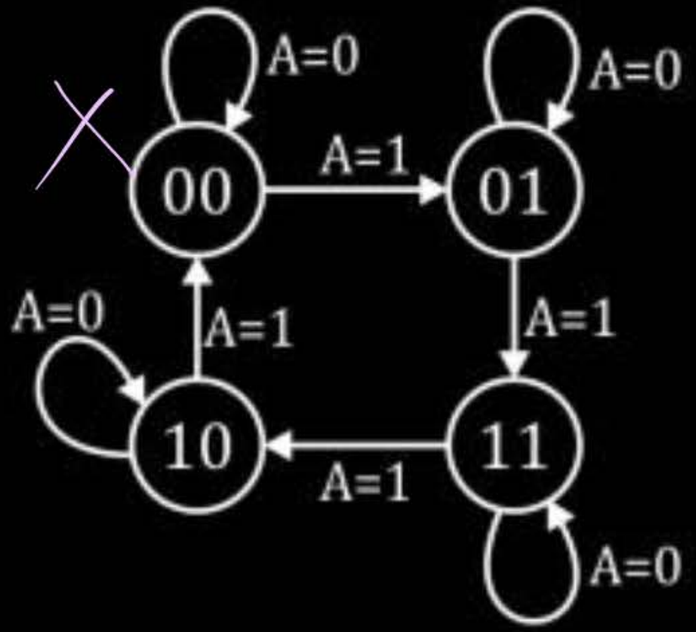
(a)


A=0
00
01
A=0
A=0
A=1
A=1
A=1
A=0
10
11
A=1

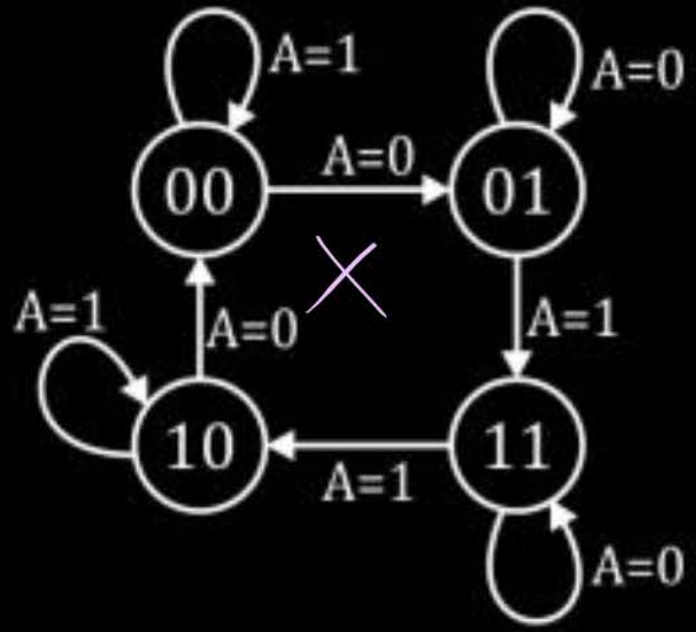
(b)


A=0
00
01
A=0
A=0
A=1
A=1
A=1
10
11
A=0

(c)

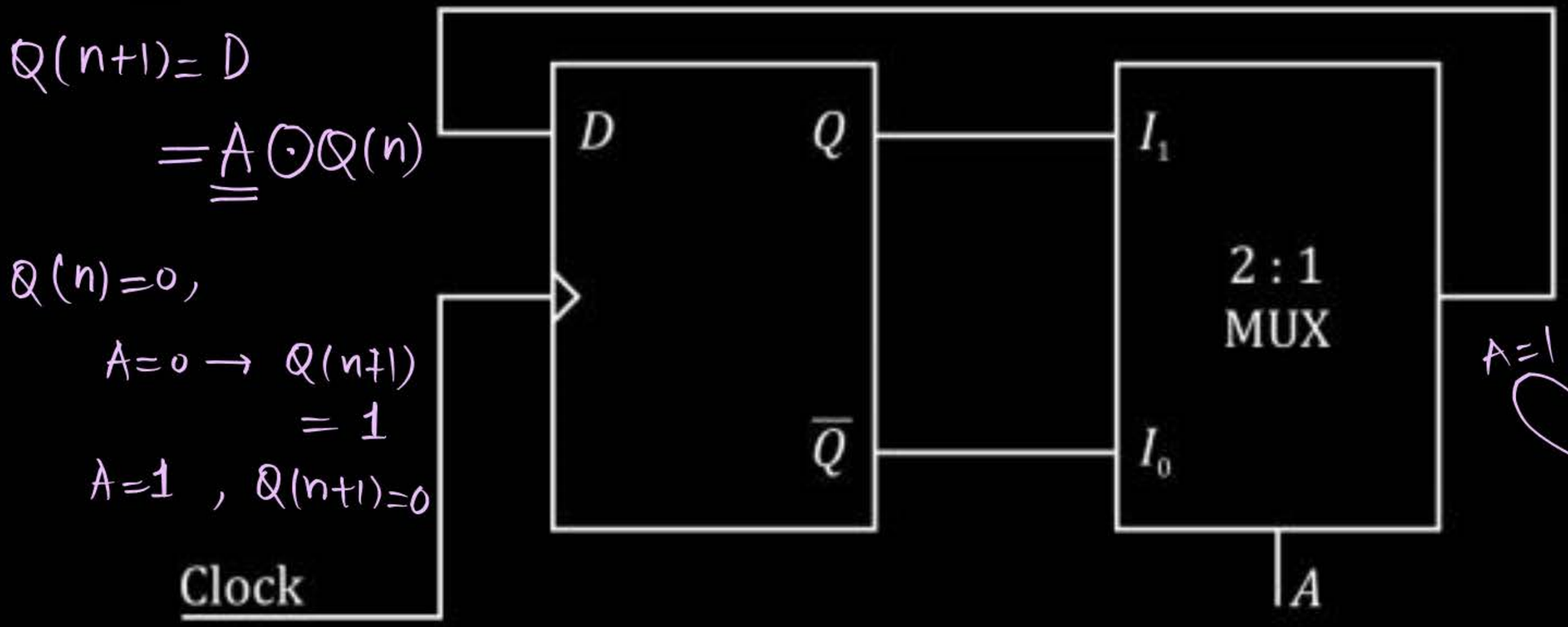

A=0
A=0
00
A=1
01
A=0
A=1
A=1
10
11
A=1
A=0

(d)

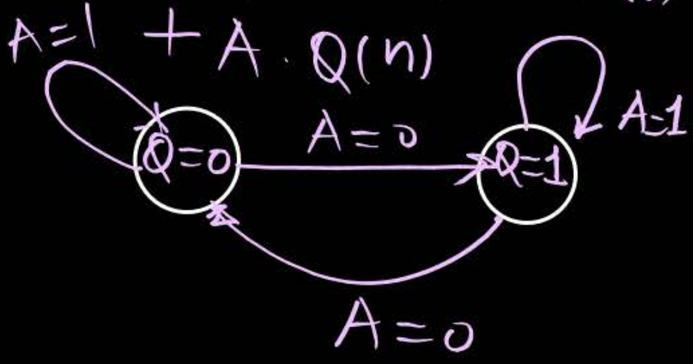

A=1
A=0
00
A=0
01
A=1
A=0
A=1
10
11
A=1
A=0

Question

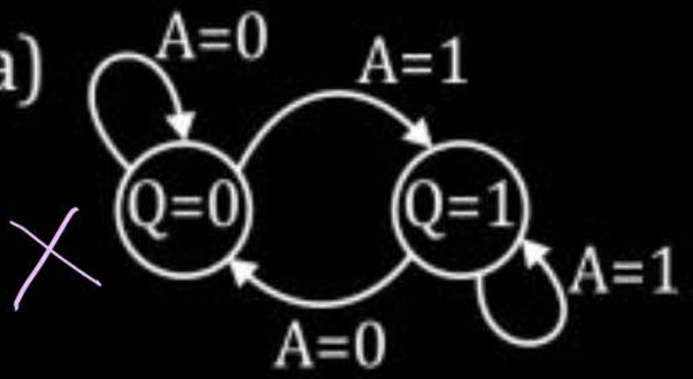
A sequential circuit is as given below :



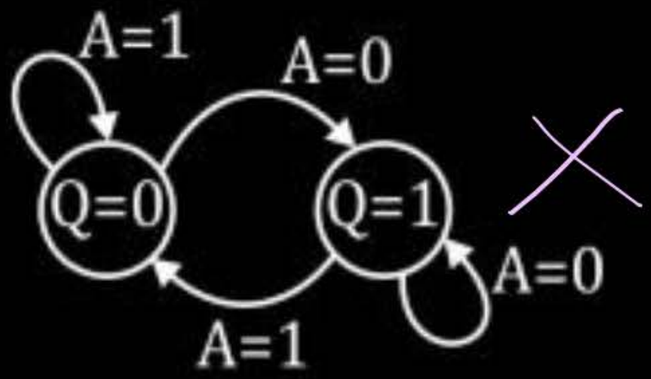
State transition diagram of above circuit will be :



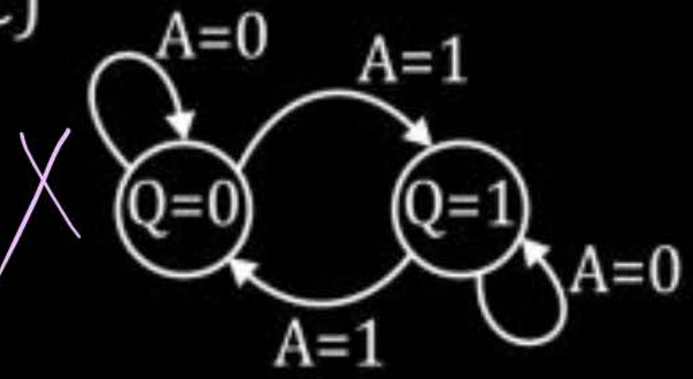
(a)



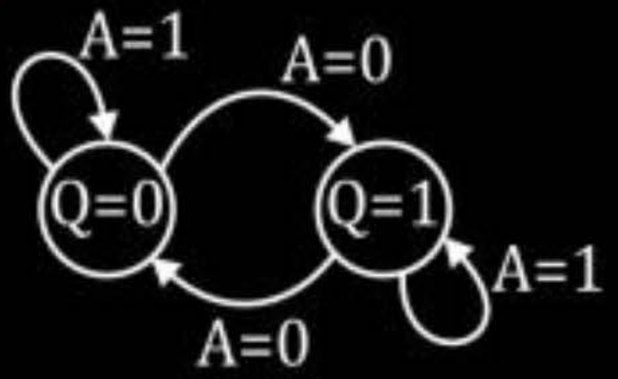
(b)



(c)

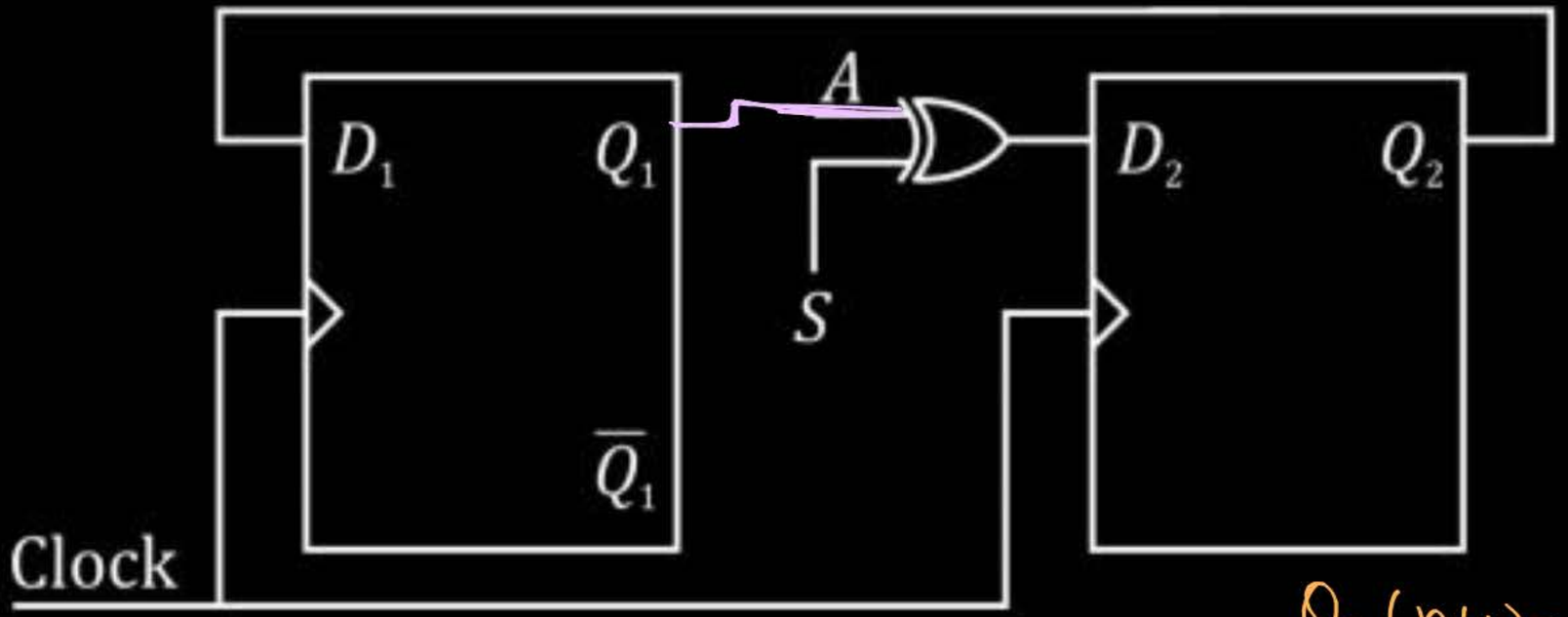


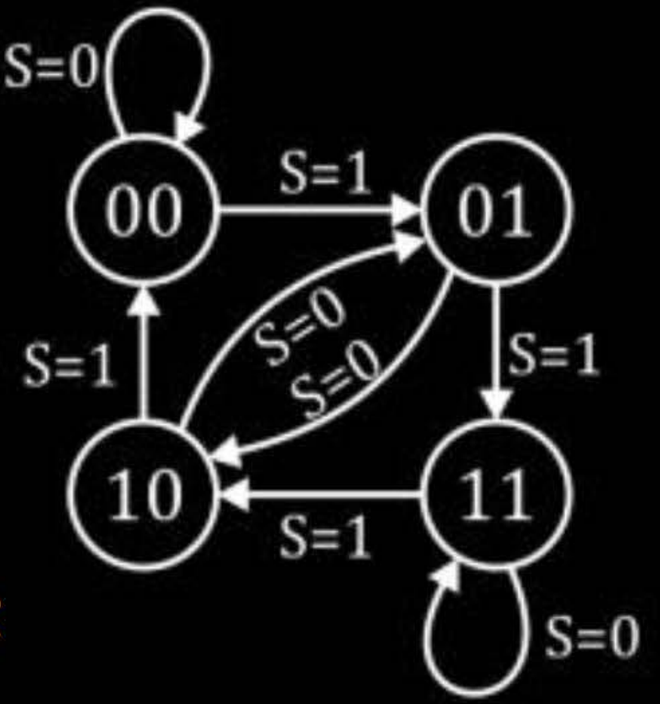
(d)



Question

The digital logic shown in the figure satisfies the given state diagram when Q_1 is connected to input A of the XOR gate :





$Q_1(n+1) = D_1 = Q_2(n)$

$Q_2(n+1) = D_2 = Q_1(n) \oplus S = A \oplus S$

$Q_2(n+1) = A \odot S$

$A = \overline{Q}_1(n) \Rightarrow Q_2(n+1) = Q_1(n) \oplus S$

$S \Rightarrow \overline{S} \rightarrow Q_2(n+1) = Q_1(n) \oplus S$

Suppose XOR gate is replaced by XNOR gate then which of the option preserves the state diagram :

(a) Input A is connected to $\bar{Q}_2$

(b) Input A is connected to Q_2

(c) Input A is connected to $\bar{Q}_1$ and S is complimented.

(d) Input A is connected to $\bar{Q}_1$

Parity generator :

A	B	C	P_e	P_o
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

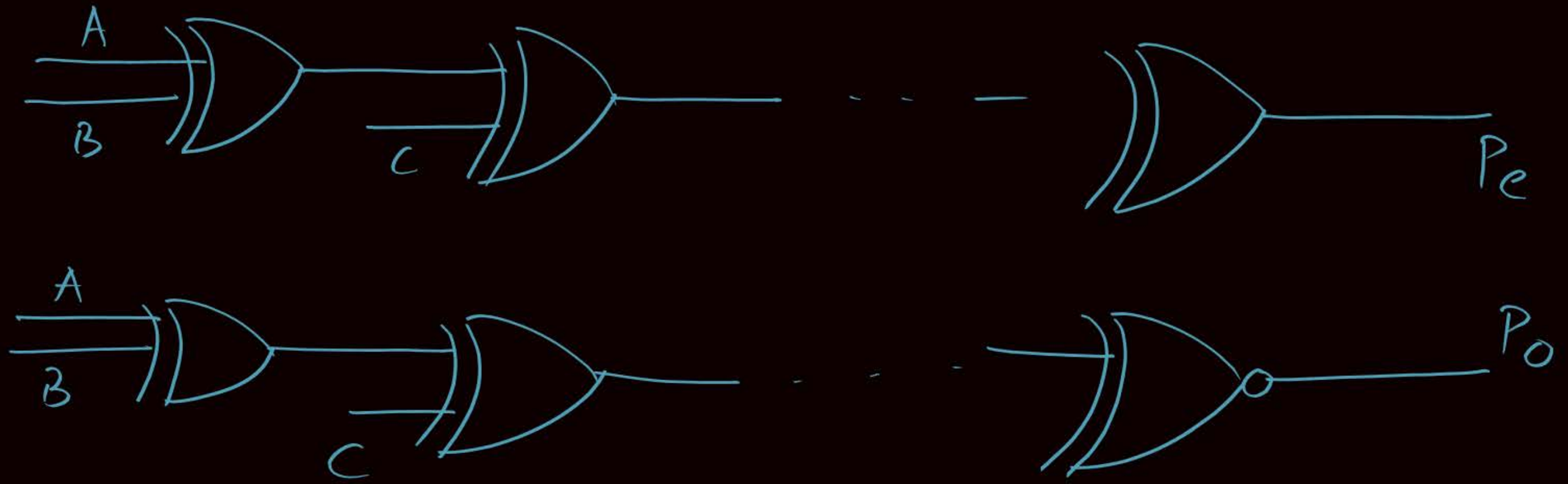
$$P_e(A,B,C) = A \oplus B \oplus C$$

$$P_o(A,B,C) = \overline{A \oplus B \oplus C}$$

$$= A \oplus B \odot C$$

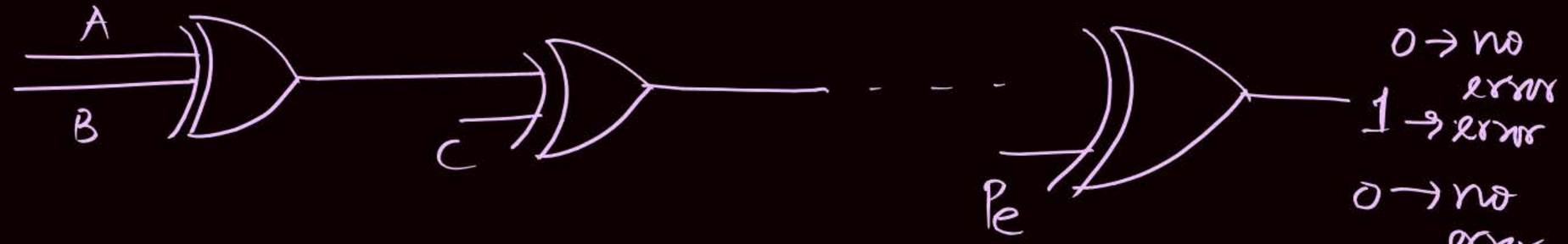
$$P_e(A,B,C,D) = A \oplus B \oplus C \oplus D$$

$$P_o(A,B,C,D) = \overline{A \oplus B \oplus C \oplus D}$$


A
B
C
Pe
A
B
C
Po

Parity Checker :

even Parity checker $\longrightarrow$ $E_{even} = A \oplus B \oplus C \oplus D \cdots \oplus P_e$ $\Rightarrow$ 1 $\rightarrow$ error



odd parity checker

$E_{odd} \Rightarrow \overline{A \oplus B \oplus C \oplus D \cdots \oplus P_o}$

Topic : 2 Min Summary

- State transition diagram
- Parity generator/checker

Thank you

GW

Soldiers !