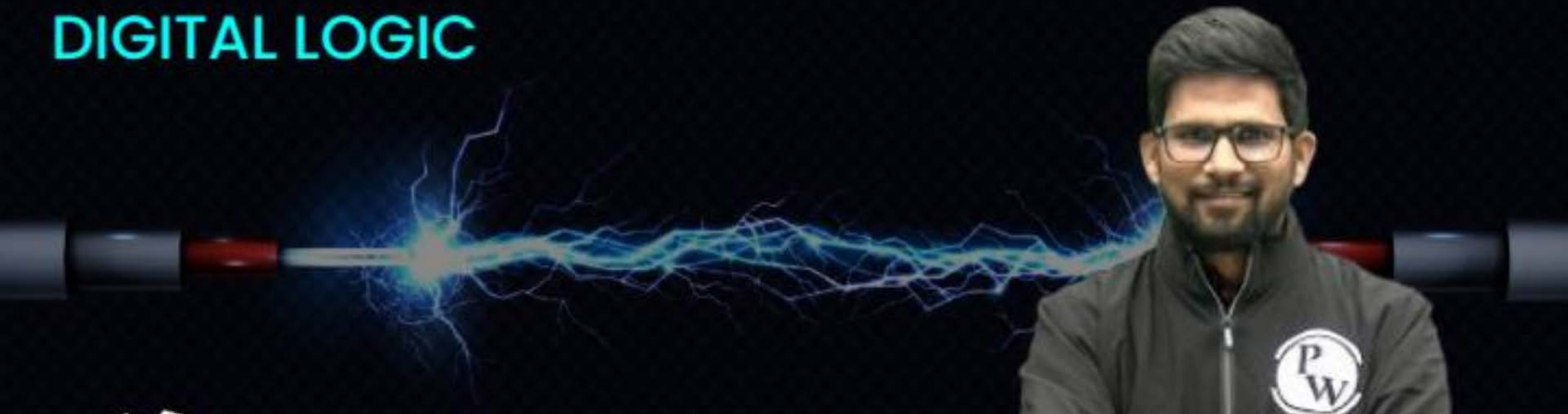
COMPUTER SCIENCE & IT

DIGITAL LOGIC



Lecture No: 03

Sequential Circuit

By- Chandan Gupta Sir

Recap of Previous Lecture

- J-K FF
- Race around condition

Counter

Counters

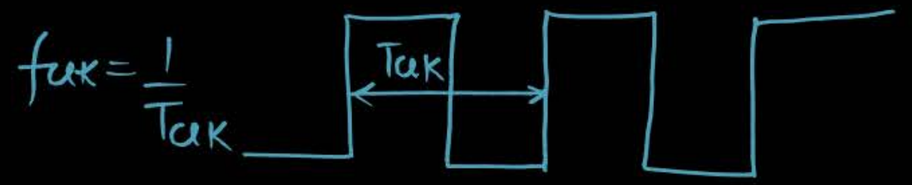
- What is counter and for what it is used for ?

$\Rightarrow$ To count clock pulses applied.

\# Frequency division

\# Pulse width stretching

$\frac{10\,MHz}{2} = 5\,MHz$



$f_1 = \frac{1}{2T_{clk}}$

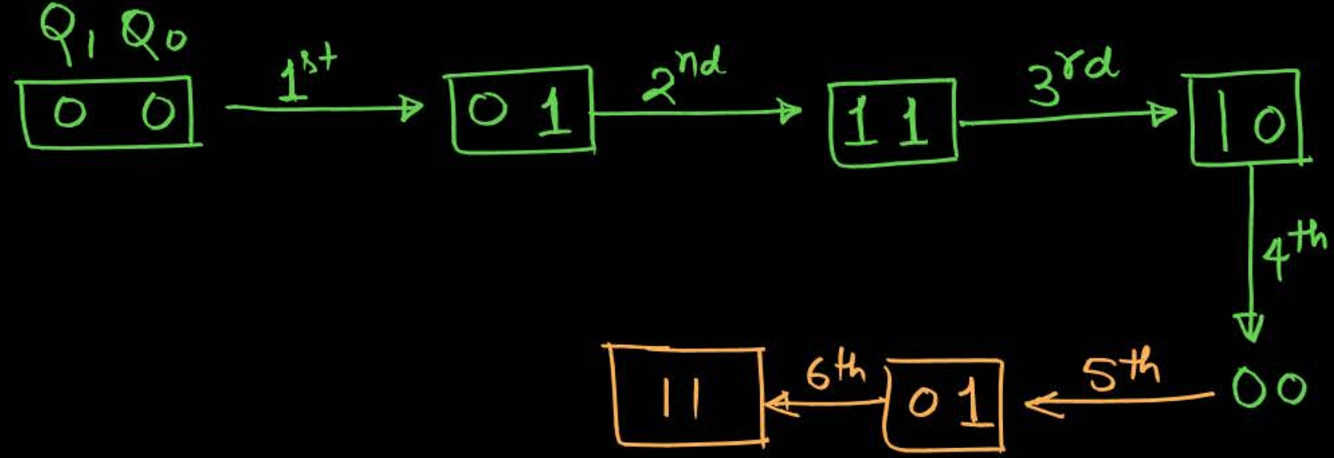
$= \frac{f_{clk}}{2}$

- MOD No. of the counter :

Total no. of different states in counter is called as MOD no. of the counter.

0 — 1 — 3 — 2

MOD no. = 4



0 - 2 - 4 - 5 - 7 - 8

↳ MOD no. = 6

0 - 3 - 6 - 9 - 12 - 15 - 18 - 21

↳ MOD no. = 8

0-1-2-1-3-1-4

→ MOD no. = 7

0-1-2-0-1-3-1-2-3

→ MOD no = 9

- Properties related to MOD No. :

After MOD no. of clock pulses counter will reach to its starting state

0 – 2 – 3 – 5 – 1 – 6 – 7 → MOD no. 7

If this counter started with starting state $(11)_2$ then what will be its state after 24 clock pulses $(6)_{10}$.

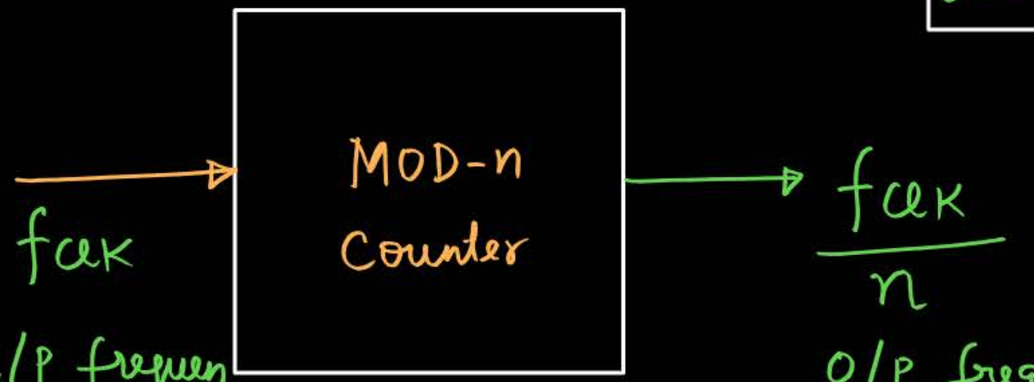
$(3)_{10} \xrightarrow{7\,CLK} (3)_{10} \xrightarrow{7\,CLK} (3)_{10} \xrightarrow{7\,CLK} (3)_{10} \xrightarrow{22^{nd}} (5)_{10}$

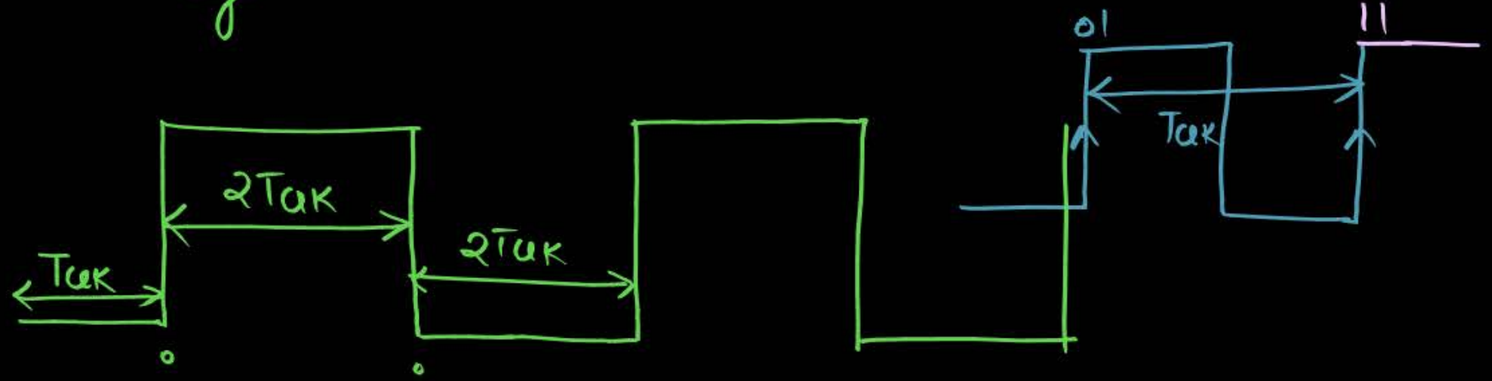
$(5)_{10} \xrightarrow{23^{rd}} (1)_{10} \xrightarrow{24^{th}} (6)_{10}$

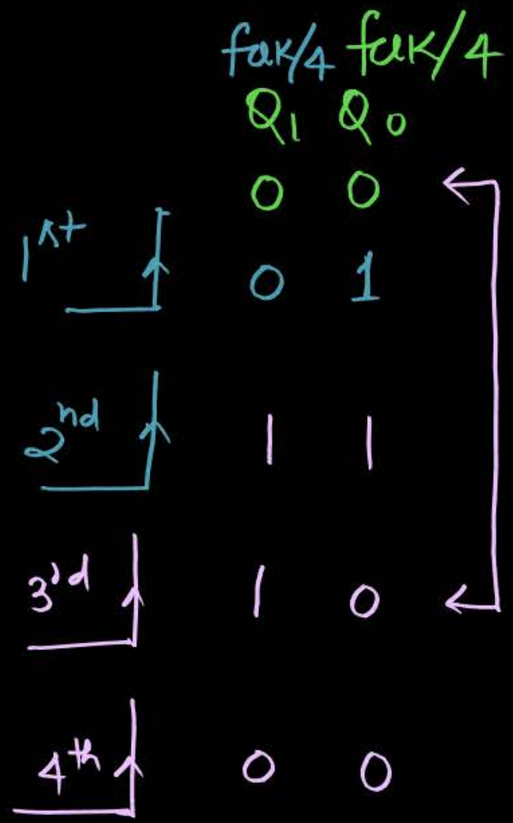
After application of integer multiple of MOD no. clock pulses counter will reach to its starting state.

#

0 – 1 – 3 – 2





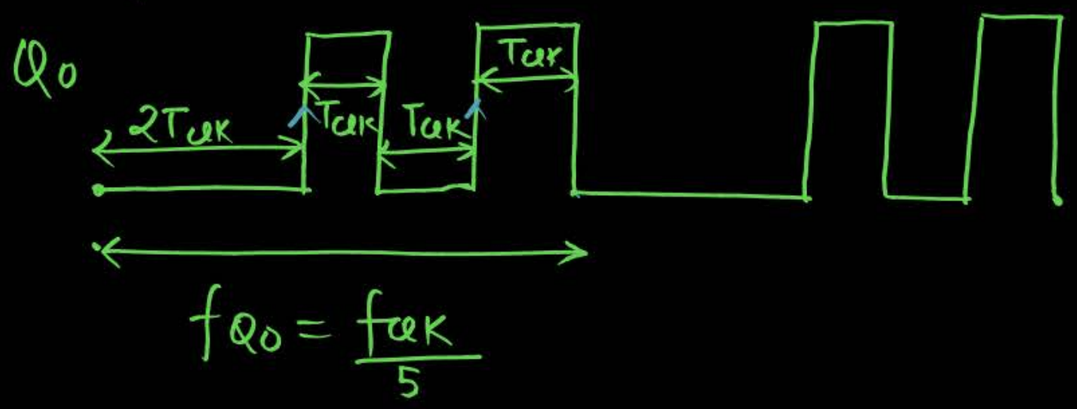


$T_{Q_0} = 4T_{clk}$

$f_{Q_0} = f_{clk}/4$

$Q_1 \rightarrow T_{off} = 2T_{clk}$, $T_{ON} = 2T_{clk}$ $\rightarrow f_{Q_1} = f_{clk}/4$

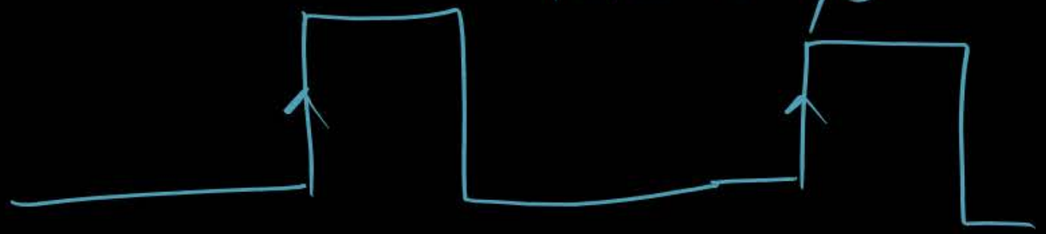
(0-3-6-9-12) → MOD-5 Counter



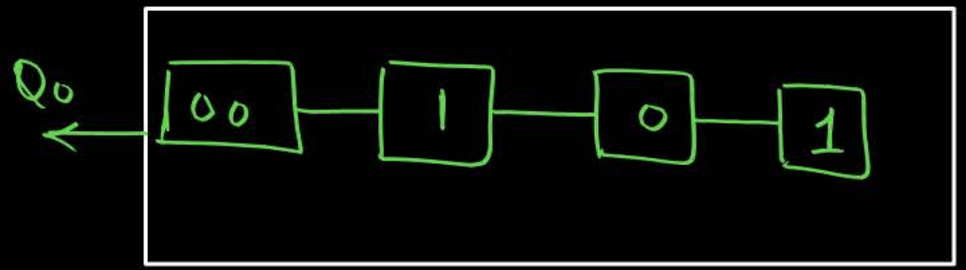
Q_1, $T_{OFF} = 3T_{CLK}$

$T_{ON} = 2T_{CLK}$ → $T_{Q_1} = 5T_{CLK}$

$f_{Q_1} = f_{CLK}/5$



$f_{CLK}/5$	$f_{CLK}/5$	$f_{CLK}/5$	$f_{CLK}/5$
Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0



Types of Counter

Asynchronous Counter

⇒ Different FFs are driven by different clocks.

Only fixed sequence is possible

- up sequence
- down sequence

It's delay is more and that's why it is relatively slow.

⇒ Eg. BCD Counter, and any fixed sequence

Synchronous Counter

⇒ All the FFs are driven by same external clock.

Any sequence is possible.

Its delay is less and that's why it is relatively faster.

Eg. Johnson Counter, Ring Counter etc., any fixed or random sequence.

- No. of ffs required for designing a counter

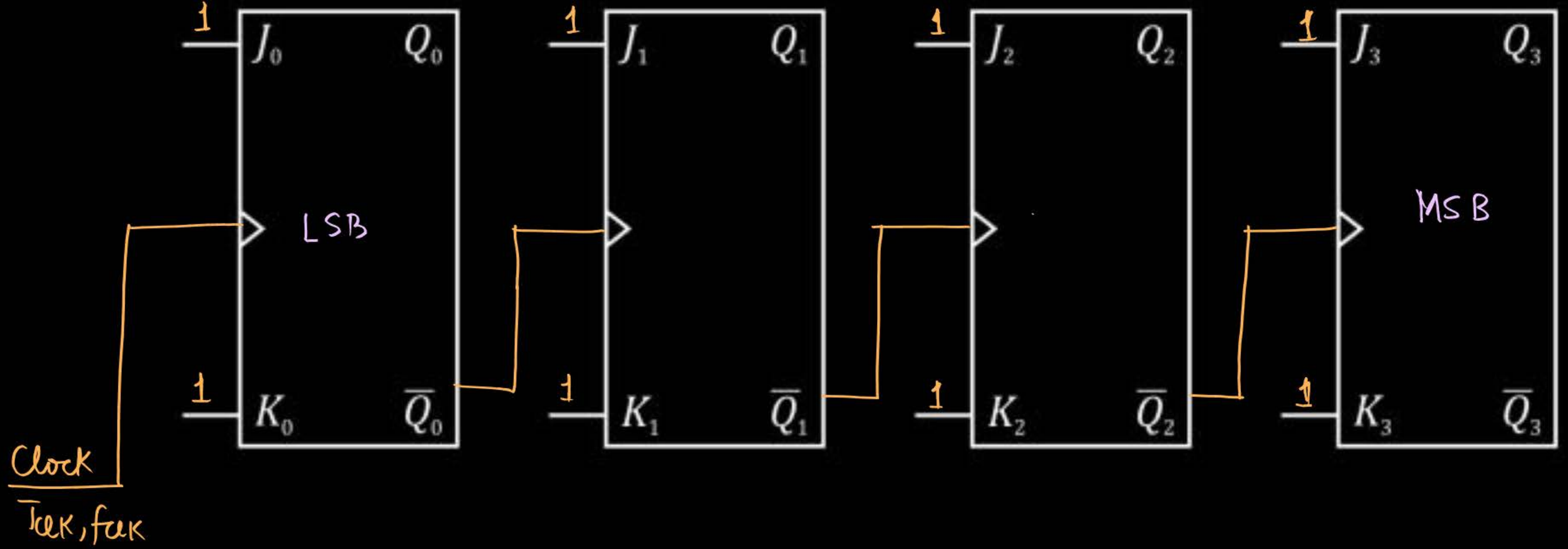
MOD no = M

$\Rightarrow$

$\Rightarrow$ if n-ff's are required then $\boxed{2^n \geq M}$ → should be satisfied.

4-bit Asynchronous Counter

- Circuit :



- Working :

⇒ Q_0 will toggle at every clock pulse

⇒ Q_1 will toggle when $\overline{Q_0}$ will take transition $(0 \to 1)$ or Q_0 will take transition from $(1 \to 0)$

Q_2 will toggle when Q_1 will take transition from $(1 \to 0)$.

Q_3 will toggle when Q_2 will take transition from $(1 \to 0)$

	$f_{CLK}/16$ Q_3	$f_{CLK}/8$ Q_2	$f_{CLK}/4$ Q_1	$f_{CLK}/2$ Q_0
Starting state	0	0	0	0
1st clock	0	0	0	1
2nd clock	0	0	1	0
3rd clock	0	0	1	1
4th Clock	0	1	0	0
5th Clock	0	1	0	1
6th Clock	0	1	1	0
7th Clock	0	1	1	1
8th Clock	1	0	0	0

$Q_0 \rightarrow T_{off} = 1T_{CLK}$
$T_{ON} = 1T_{CLK}$
$T_{Q_0} = 2T_{CLK}$
$f_{Q_0} = f_{CLK}/2$

$Q_1 \rightarrow T_{off} = 2T_{CLK}$
$T_{ON} = 2T_{CLK}$
$T_{Q_1} = 4T_{CLK}$
$f_{Q_1} = f_{CLK}/4$

$Q_2 \rightarrow T_{off} = 4T_{CLK}$
$T_{ON} = 4T_{CLK}$
$T_{Q_2} = 8T_{CLK}$
$f_{Q_2} = f_{CLK}/8$

9th clock	1 0 0 1
10th clock	1 0 1 0
11th clock	1 0 1 1
12th clock	1 1 0 0
13th clock	1 1 0 1 →
14th clock	1 1 1 0
15th clock	1 1 1 1
16th clock	0 0 0 0

MOD no. = 16

$Q_3 \rightarrow$

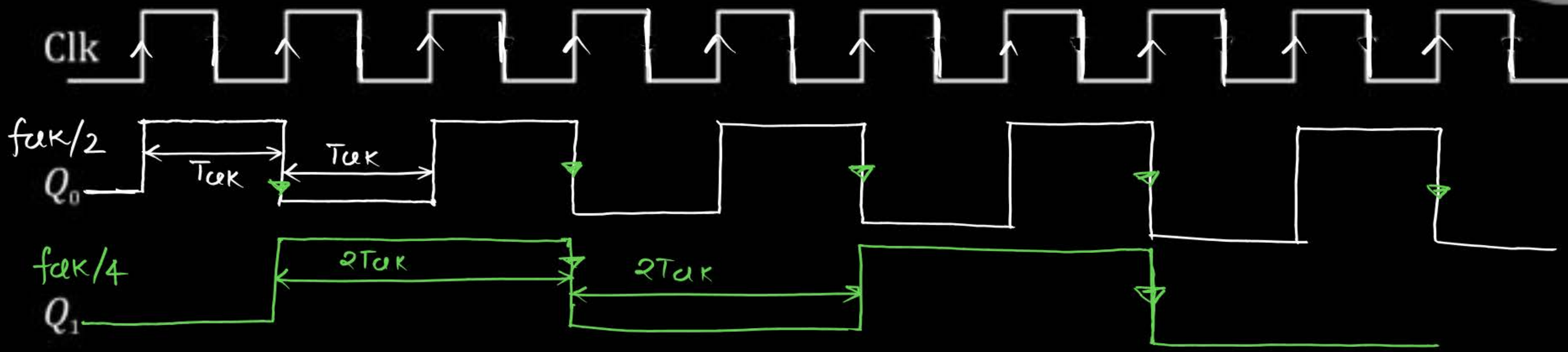
$T_{OFF} = 8T_{CLK}$

$T_{ON} = 8T_{CLK}$

$T_{Q_3} = 16T_{CLK}$

$f_{Q_3} = f_{CLK}/16$

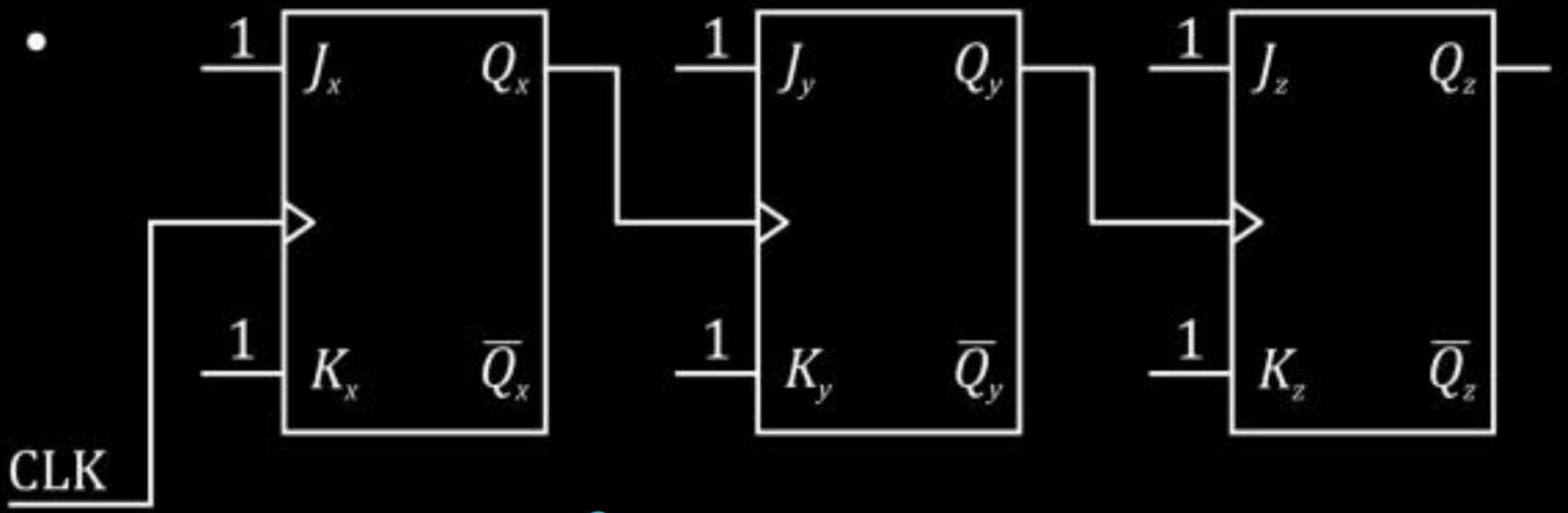
- Clock Diagram :



Q_2 H.W.

Q_3 H.W.

How to identify LSB bit and type (up or down) of Asynch. Counter

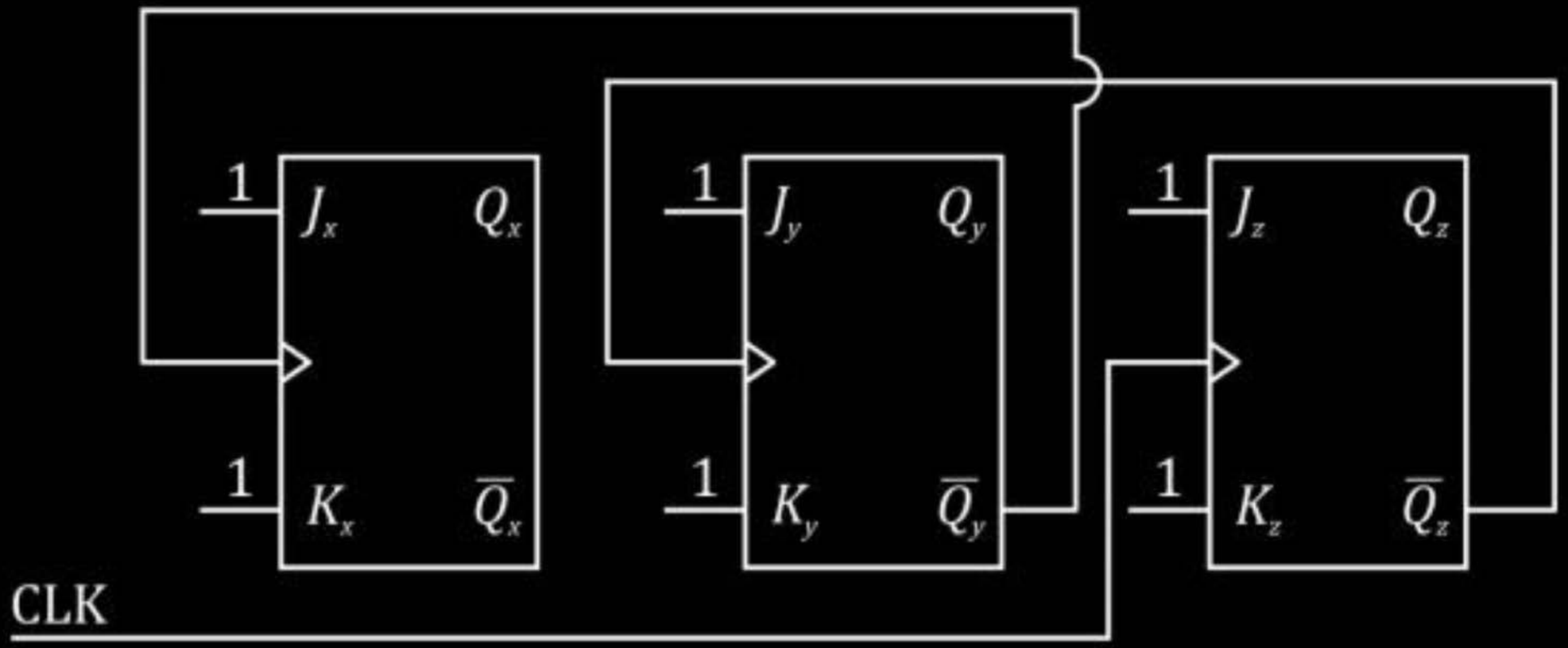


$Q_z\ Q_y\ Q_x$

LSB Bit → Q_x

MSB Bit → Q_z

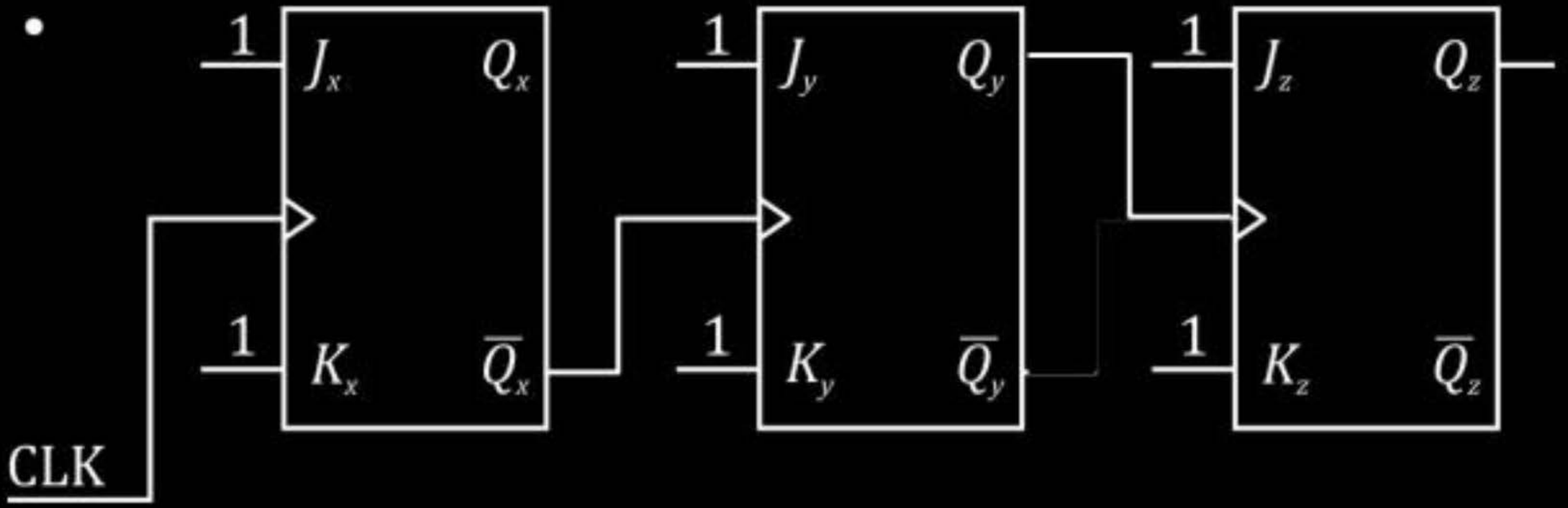
Up counter or down counter ? → down counter MOD-8



LSB Bit → Q_z

MSB Bit → Q_x

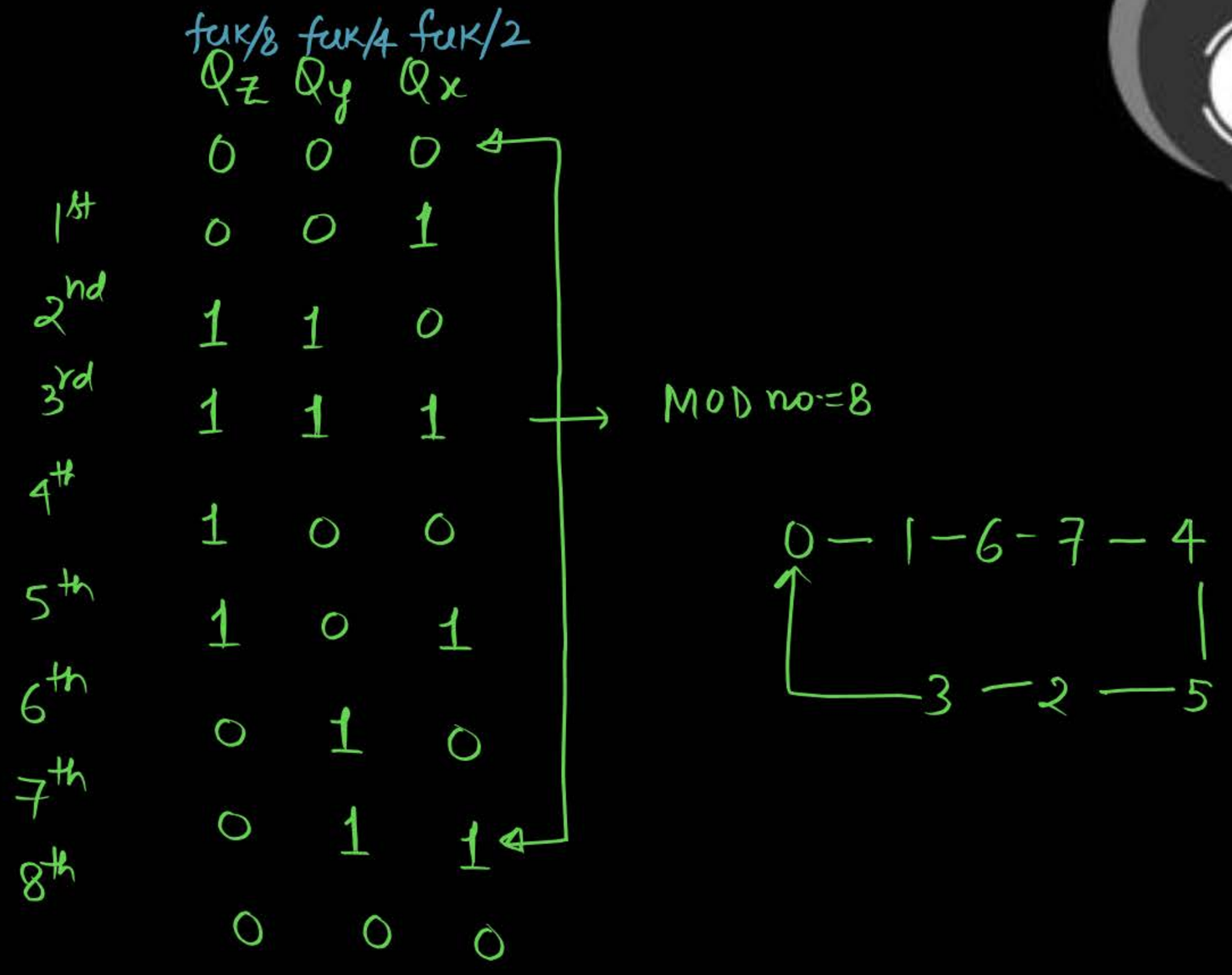
Up counter or down counter ? → Upcounter – MOD-8



What is the MOD no. of above counter ?

Starting state $= (101)_2$ $\xrightarrow{3\,CLK}$

Sequence generated is ?

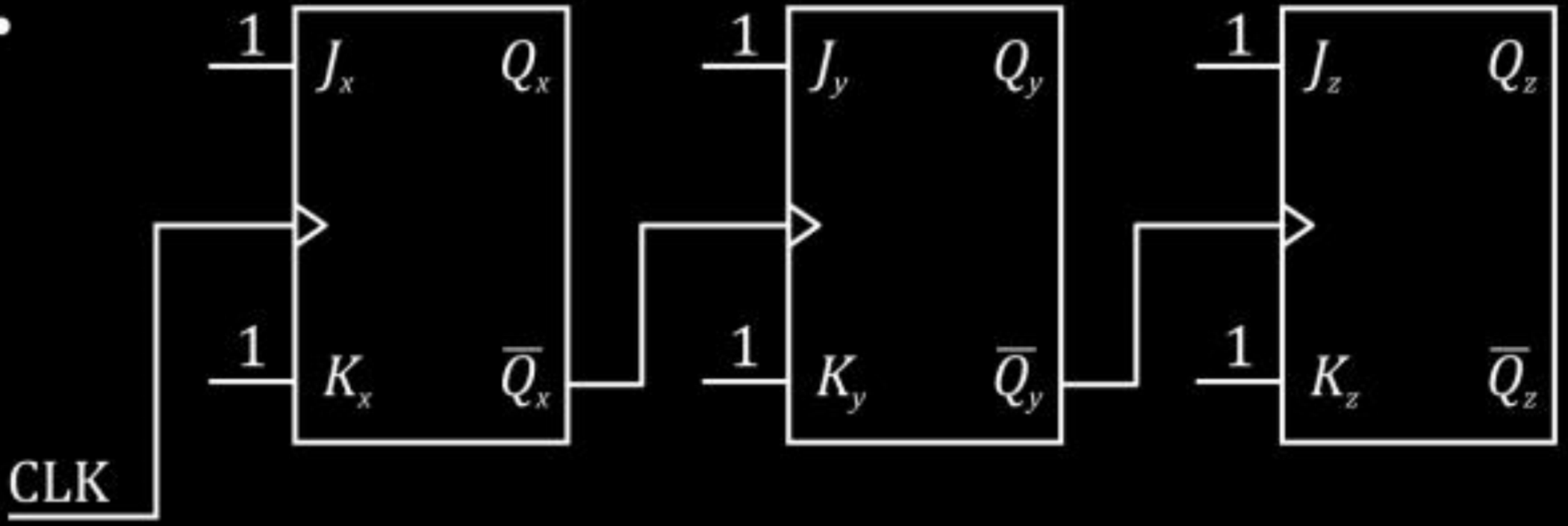


$f_x = ?$ $f_{clk}/2$ $f_y = ?$ $= f_{clk}/4$

$f_z = ?$ $f_{clk}/8$

- If starting state is $Q_zQ_yQ_x = (100)_2$ then after 11 CLK pulses counter will be at state – $(3)_{10}$.

$(100)_2 \xrightarrow{8^{th}\ CLK} (100)_2 \xrightarrow{9^{th}} (5)_{10} \xrightarrow{10^{th}} (2)_{10} \xrightarrow{11^{th}} (3)_{10}$

- 

LSB Bit $\rightarrow$

MSB Bit $\rightarrow$

- Final Conclusion :

Trigger type	Clock i/p from previous o/p	Counter type
+ve edge triggered	Q	down counter
+ve edge triggered	$\overline{Q}$	up counter
−ve edge triggered	Q	up counter
− ve edge triggered	$\overline{Q}$	down counter

Topic : 2 Min Summary

→ Asynchronous Counter

Thank you

GW

Soldiers !