

# CS & IT ENGINEERING



## Operating System

### Memory Management

Lecture – 5

By– Vishvadeep Gothi sir



# Recap of Previous Lecture



Topic

Performance of Paging

Topic

TLB





# Topics to be Covered



Topic

TLB Mapping

Topic

Segmentation



## Topic : Paging

### How TLB Stores Entries?

TLB (4 entries)



P.T. (8 entries)

000	
001	
010	
011	
100	
101	
110	
111	



## Topic : Paging-2



**TLB Mapping** → which p.T. entries is stored where in TLB

1. Fully Associative
2. Direct
3. Set-Associative

# Fully associative mapping :-

TLB

Tag ←

Page no.	P.T. entry
0100	✓
0010	✓
1010	✓
1001	✓
⋮	

L.A.

P	d
Tag	





## Topic : Paging-2

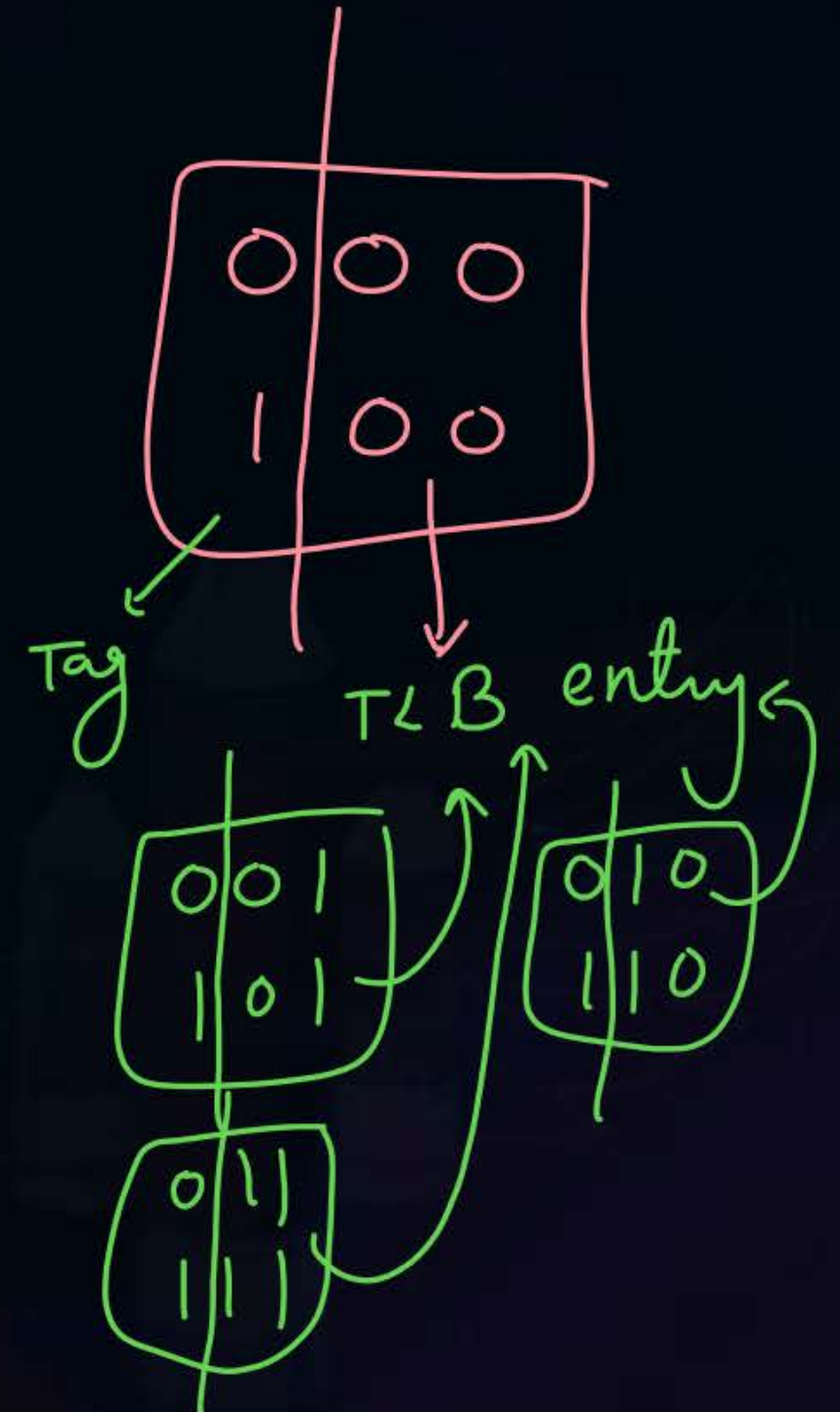
### TLB Mapping: Direct

TLB (4 entries)

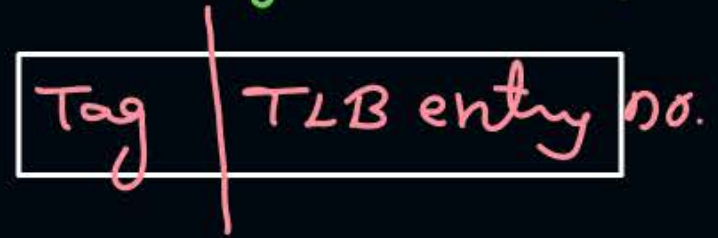
Tag		
00	<input checked="" type="checkbox"/>	f, 10 0, 4
01	<input type="checkbox"/>	1, 5
10	<input type="checkbox"/>	2, 6
11	<input type="checkbox"/>	3, 7

P.T. (8 - entries)

000	<input checked="" type="checkbox"/>
001	
010	
011	
100	
101	
110	
111	



← Page no. (P) →



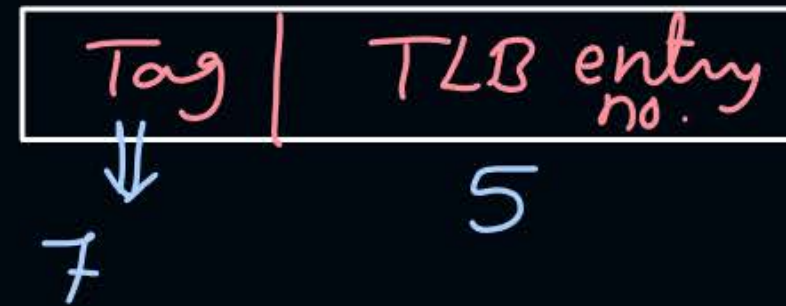
$$\text{No. of bits in TLB entry no.} = \log_2(\text{no. of entries in TLB})$$

Ex:- no. of pages =  $2^{12} \Rightarrow P = 12 \text{ bits}$

TLB can store 32 entries  
Direct mapping.  $\rightarrow 2^5$

Tag = 7 bits

← 12 →  
← P →

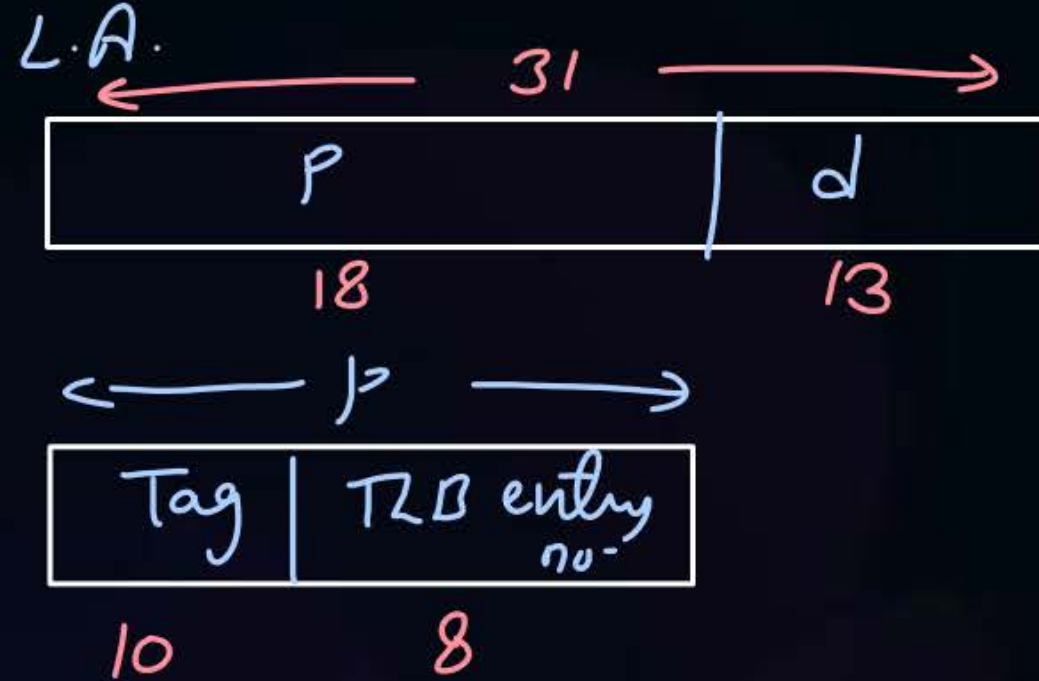






## Topic : Question

#Q. A computer system implements a 31-bit <sup>logical</sup>~~virtual~~ address, page size of 8 kilobytes, and a 256-entry translation look-aside buffer (TLB) organized as direct mapped. The minimum length of the TLB tag in bits is \_\_\_\_\_?



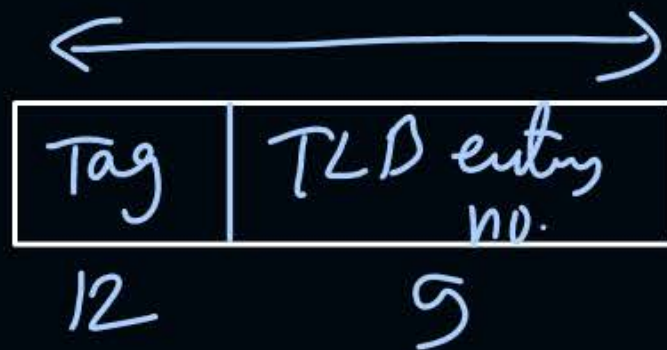
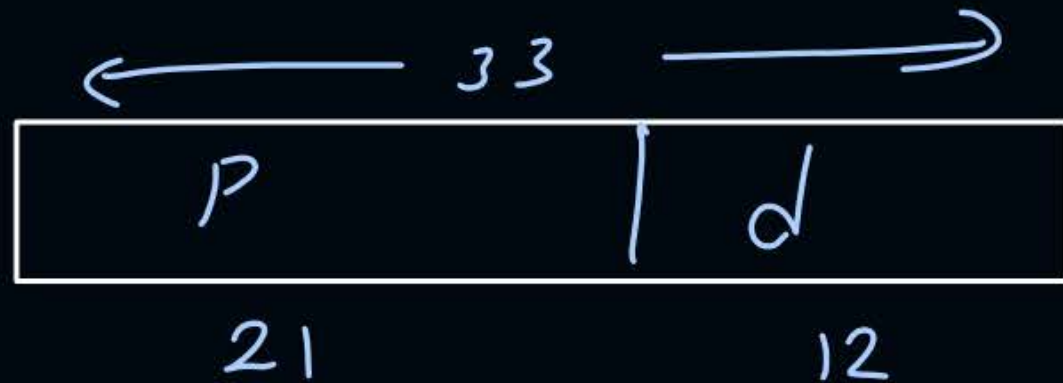
$$\begin{aligned}\text{no. of entries in TLB} &= 256 = 2^8 \\ \text{entry no.} &= \log_2 256 = 8 \text{ bits}\end{aligned}$$

#Q. L.A.S. = 8GB =  $2^{33} B \Rightarrow LA = 33$  bits

Direct mapped TLB has 512 entries

Page = 4KBytes =  $2^{12} B$

Tag = 12 bits



ex:- TLB size = 64 bytes

1 P.T. entry = 2 bytes

$$\begin{aligned}\text{no. of entries in TLB} &= \frac{64\text{B}}{2\text{B}} \\ &= 32\end{aligned}$$

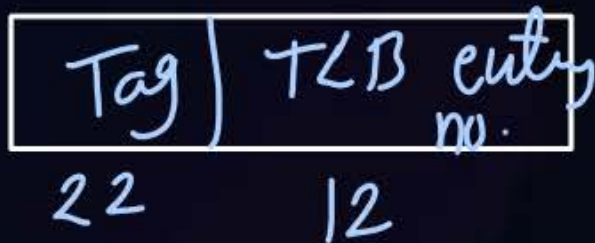
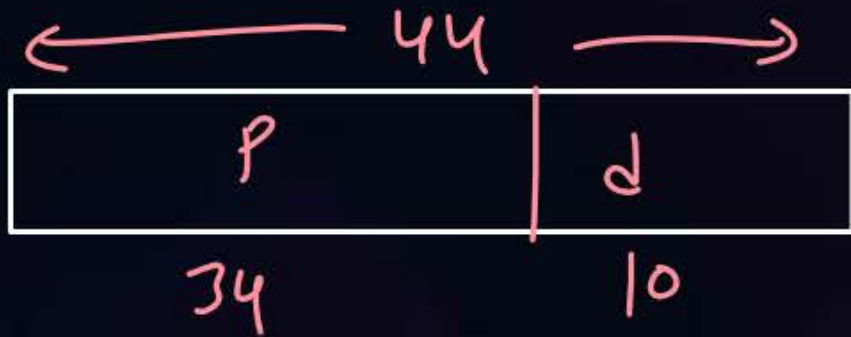




## Topic : Question

#Q. A computer system implements a 44- bit virtual address, page size of  $2^{10}$  kilobytes, and a 16KB look-aside buffer (TLB) organized as direct mapped. Each page table entry is of 4bytes. The minimum length of the TLB tag in bits is 22?

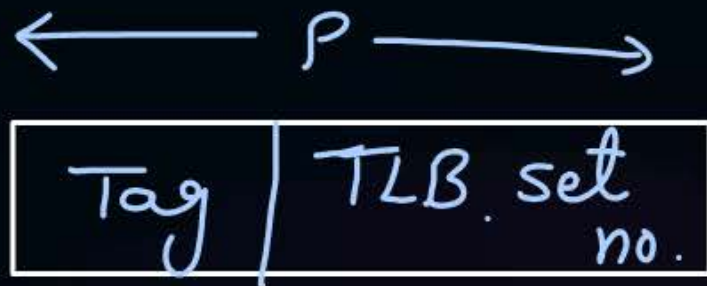
Sol<sup>n</sup> no. of entries in TLB =  $\frac{16KB}{4B} = 4k = 2^{12}$





## Topic : Paging-2

### TLB Mapping: Set Associative



2-way set associative TLB



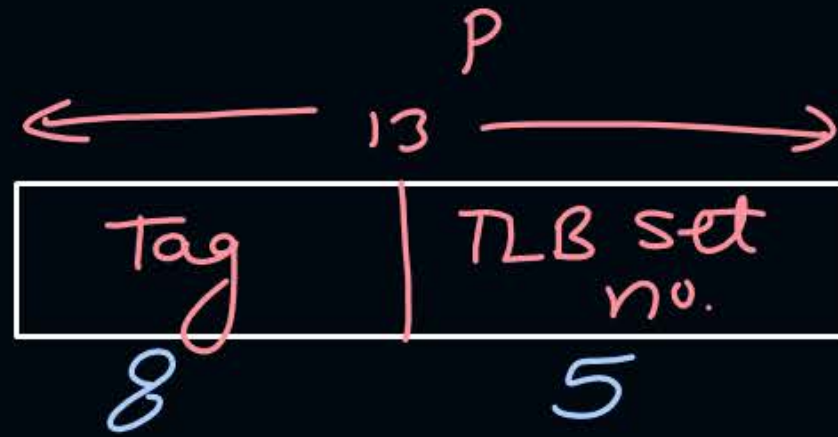
$$\text{no. of bits in TLB set no.} = \log_2 \left( \begin{array}{c} \text{no. of sets} \\ \text{in TLB} \end{array} \right)$$

$$\text{no. of sets in TLB} = \frac{\text{no. of entries in TLB}}{\text{associativity}}$$

ex:-

TLB  $\Rightarrow$  64 entries  
2-way set associative

P  $\Rightarrow$  13 bits



$$\text{no. of sets in TLB} = \frac{64}{2}$$

$$= 32$$

$$= 2^5 \Rightarrow \text{TLB set no.} = 5 \text{ bits}$$

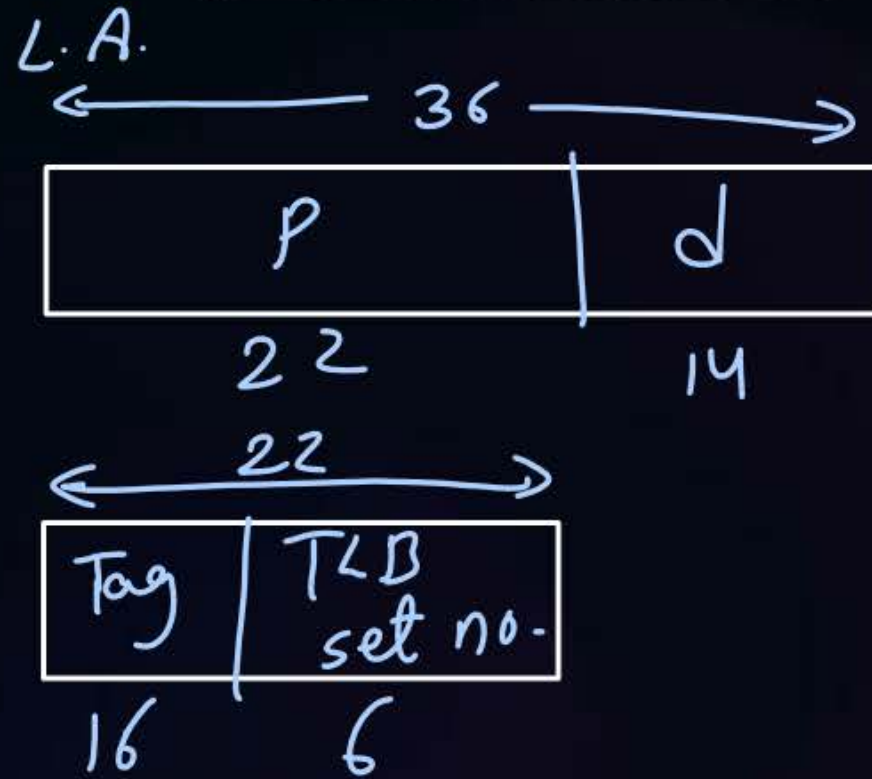




## Topic : Question

$$2^{14}$$

#Q. A Computer system implements a 36-bit virtual address, page size of 16 Kbytes and a 256 – entry translation look-aside buffer (TLB) organized into 64 sets each having four ways. Assume that the TLB tag does not store any process id. The minimum length of the TLb tag in bits is \_\_\_\_\_.



$$\text{no. of sets} = 64 = 2^6 \Rightarrow \text{set no.} = 6 \text{ bits}$$



## Topic : Paging

Paging suffers from internal fragmentation

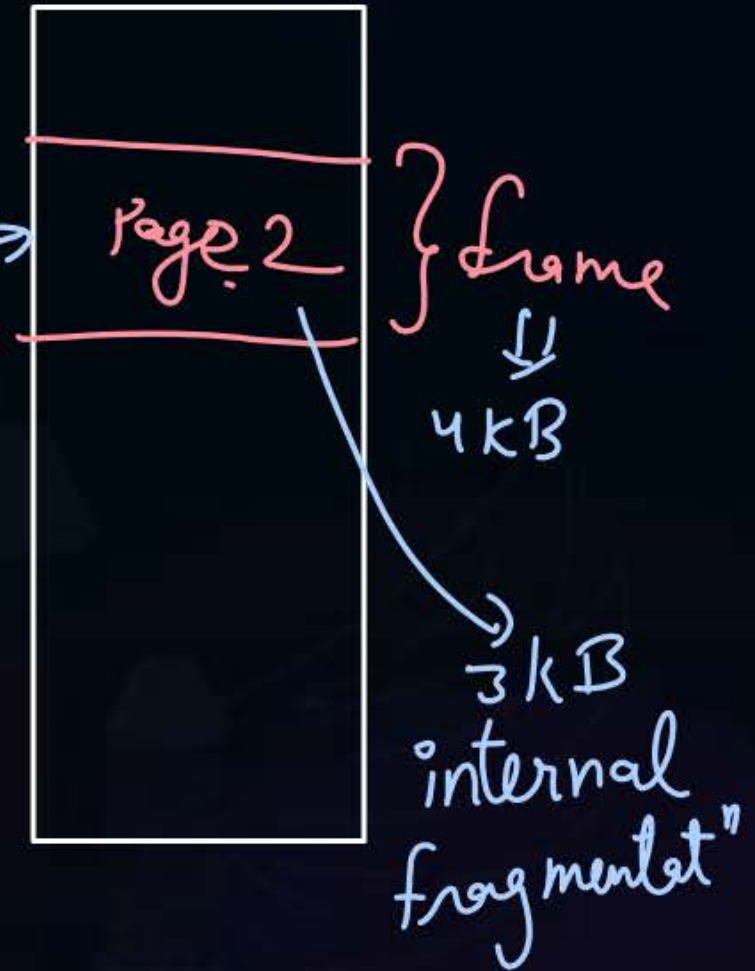
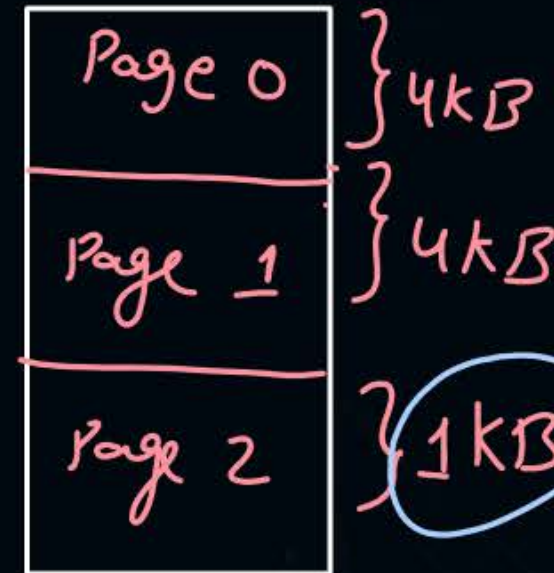
Assume a process 9 kbytes  
Page size = 4 kbytes



if Page size = 2 kbytes



internal fragmentat<sup>n</sup> ⇒ 1KB



Reducing page size can reduce internal fragmentation.

---

Homework:-

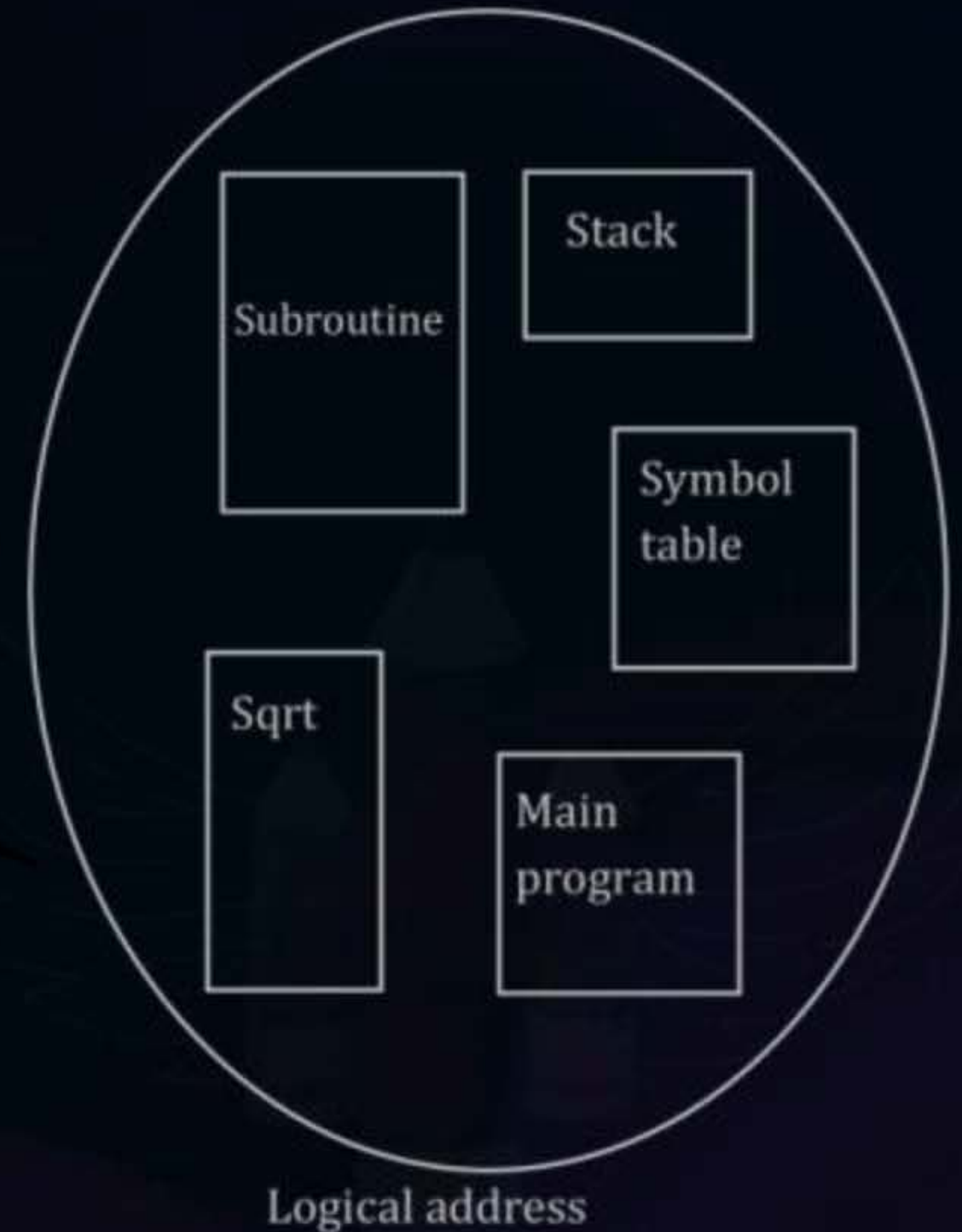
If page size is reduced or increased, then what impact it causes on page table size?





## Topic : Segmentation

- Divide Process in logically related partitions (Segments) Segments are scattered in physical memory





# Topic : Segmentation

Process

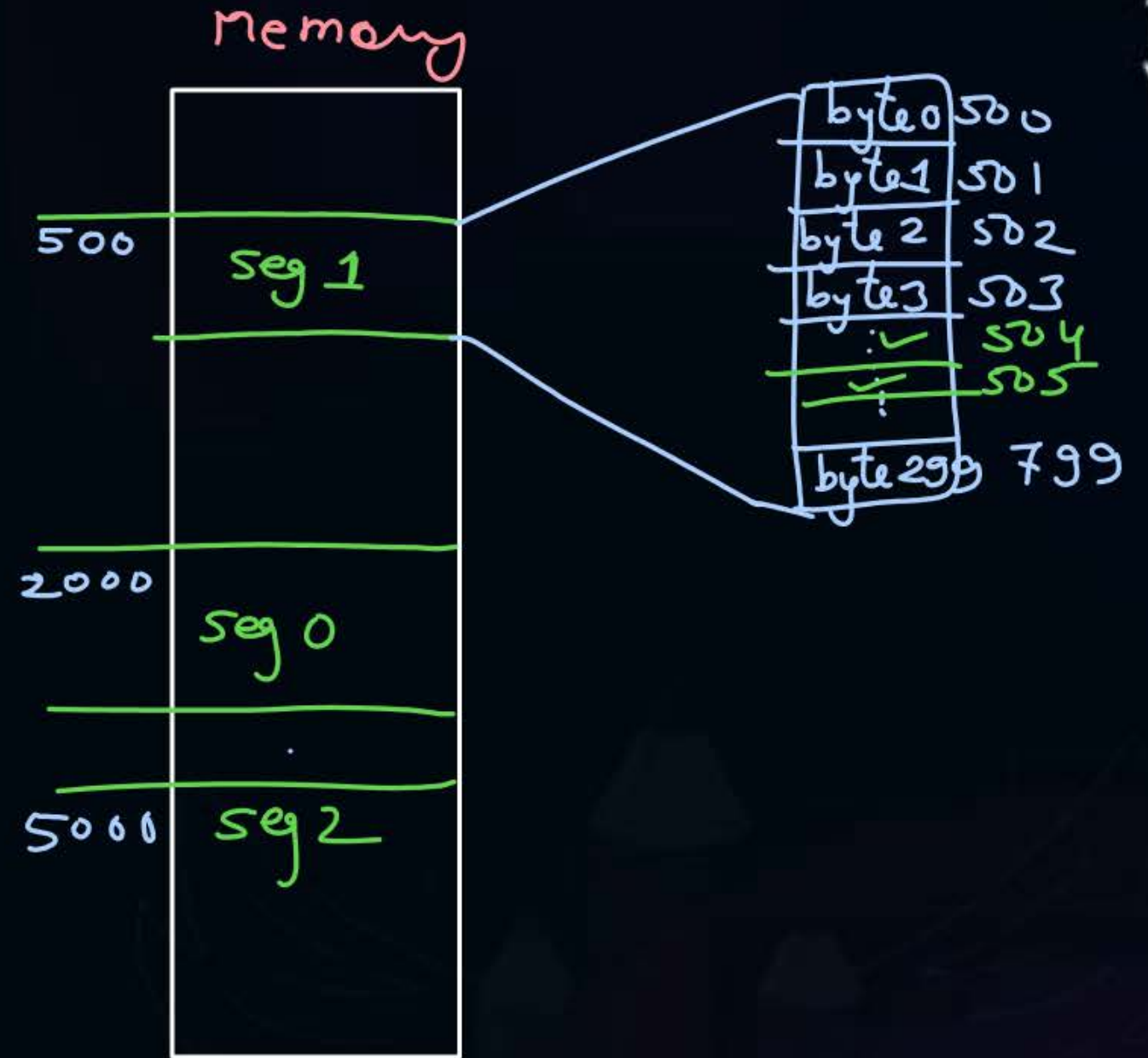


seg.no.

segment table

0	2000	500
1	500	300
2	5000	900

base limit  
size of each segment





## Topic : Segmentation

- Size of segment can vary, so along with base, keep limit information also
- Limit defines max number of *bytes* within the segment

CPU generates logical add.



segment no.

offset (byte no. of the segment)

offset is calculated based on largest allowed segment size.



Ex:- CPU wants L.A.  $\Rightarrow S = 1$   
byte = 5

S	d
1	5

search in seg. table  $\Rightarrow$  Base add. = 500

+

500 + 5

505

$\Downarrow$

Physical add.

CPU generates L.A. = 

S=1	d=400
-----	-------

seg. = base = 500  $\oplus$  900

#Q. Find physical address for the following requests?

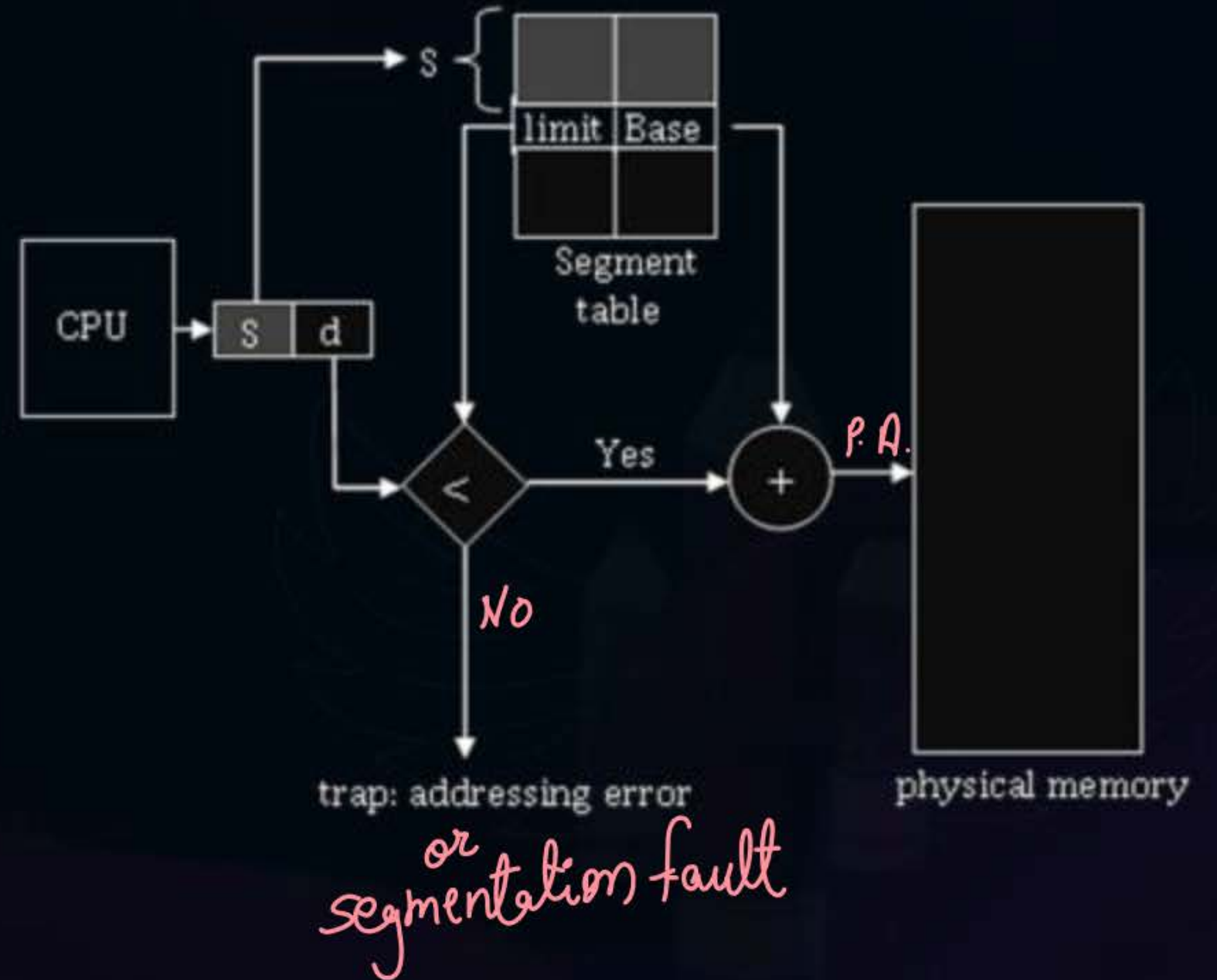
S	d	Physical Address
2	856	$5000 + 856 = 5856$
<u>1</u>	256	$500 + 256 = 756$
0	480	$2000 + 480 = 2480$
2	952	seg. fault

Seg. Table

0	2000	500
1	500	300
2	5000	900
	base	limit



# Topic : Segmentation







## Topic : Segmentation

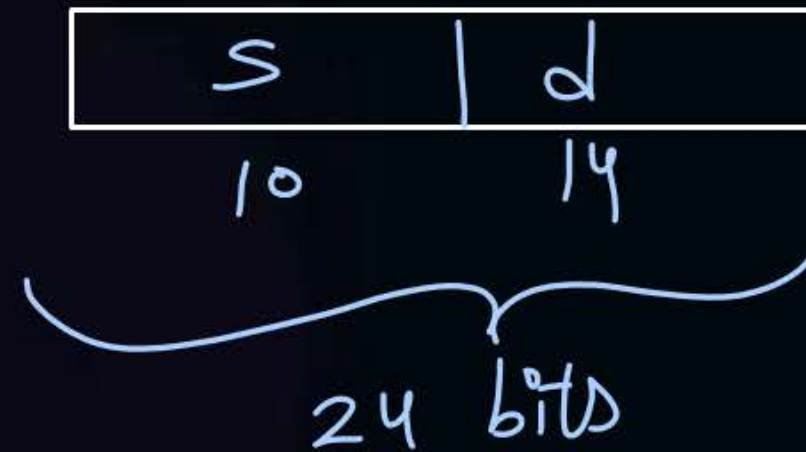


- Size of segment can vary, so along with base, keep limit information also
- Limit defines max number of words within the segment

[NAT]



#Q. Maximum segment size = 16KB =  $2^{14}$  B  $\Rightarrow$  d = 14 bits  
Number of segments in process =  $2^{10}$   $\Rightarrow$  s = 10 bits  
Logical address = 24 bits ??





## Topic : Segmentation



- Segmentation suffers from external fragmentation





## 2 mins Summary

**Topic**

**TLB Mapping**

**Topic**

**Segmentation**



**Happy Learning**

**THANK - YOU**