COMPUTER SCIENCE & IT

DIGITAL LOGIC

Lecture No: 05

Sequential Circuit

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Recap of Previous Lecture

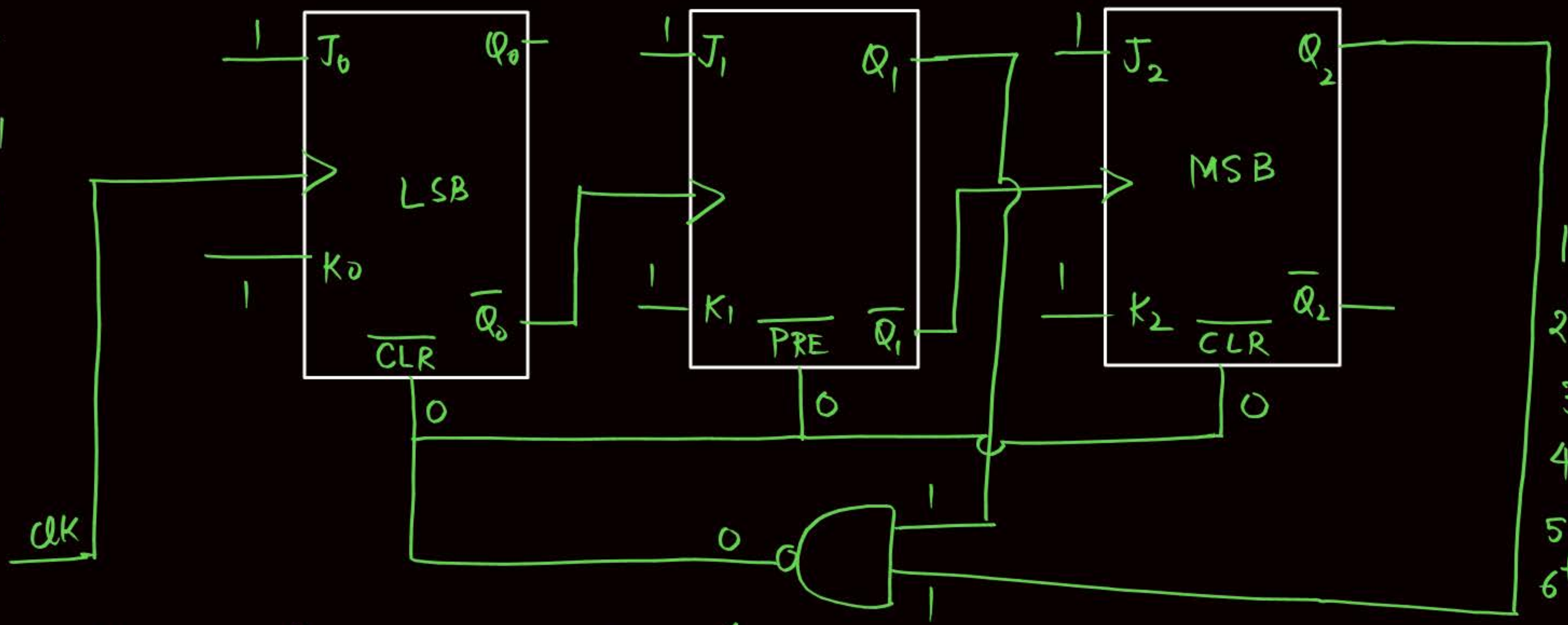
Asynchronous Counter

- Synchronous Counter

Q.

$Q_2 = 1$

$Q_1 = 1$

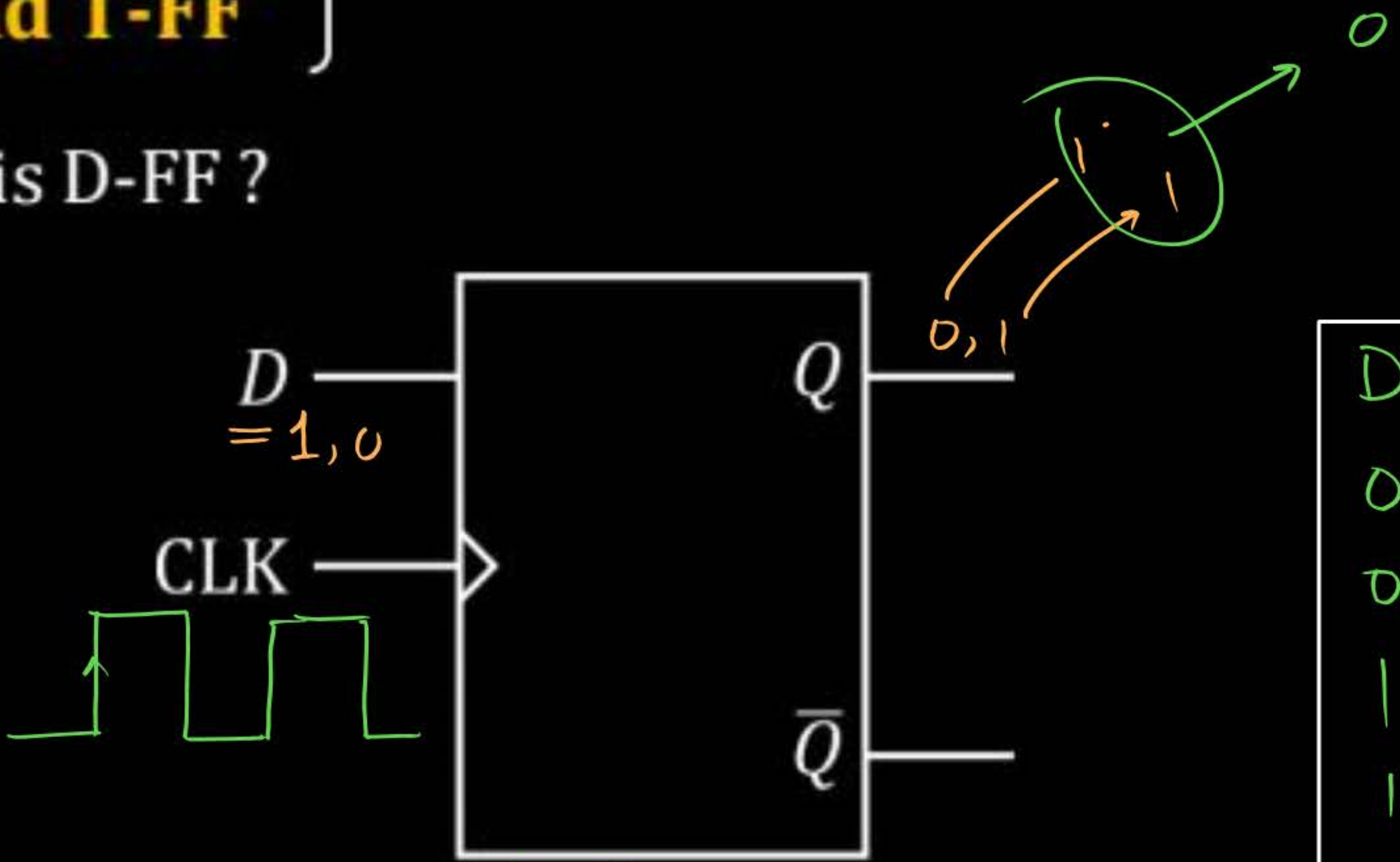


	Q_2	Q_1	Q_0
	0	0	0
1^{st}	0	0	1
2^{nd}	0	1	0
3^{rd}	0	1	1
4^{th}	1	0	0
5^{th}	1	0	1
6^{th}	1	1	0

MOD no. of the above counter $\underline{\quad 4 \quad}$.

[D-FF and T-FF]

- What is D-FF ?



$\boxed{Q(n+1) = D}$

Characteristic table

D	Q(n)	Q(n+1)
0	0	0
0	1	0
1	0	1
1	1	1

	$\overline{Q}(n)$	Q(n)
$\overline{D}$		
D	1	1

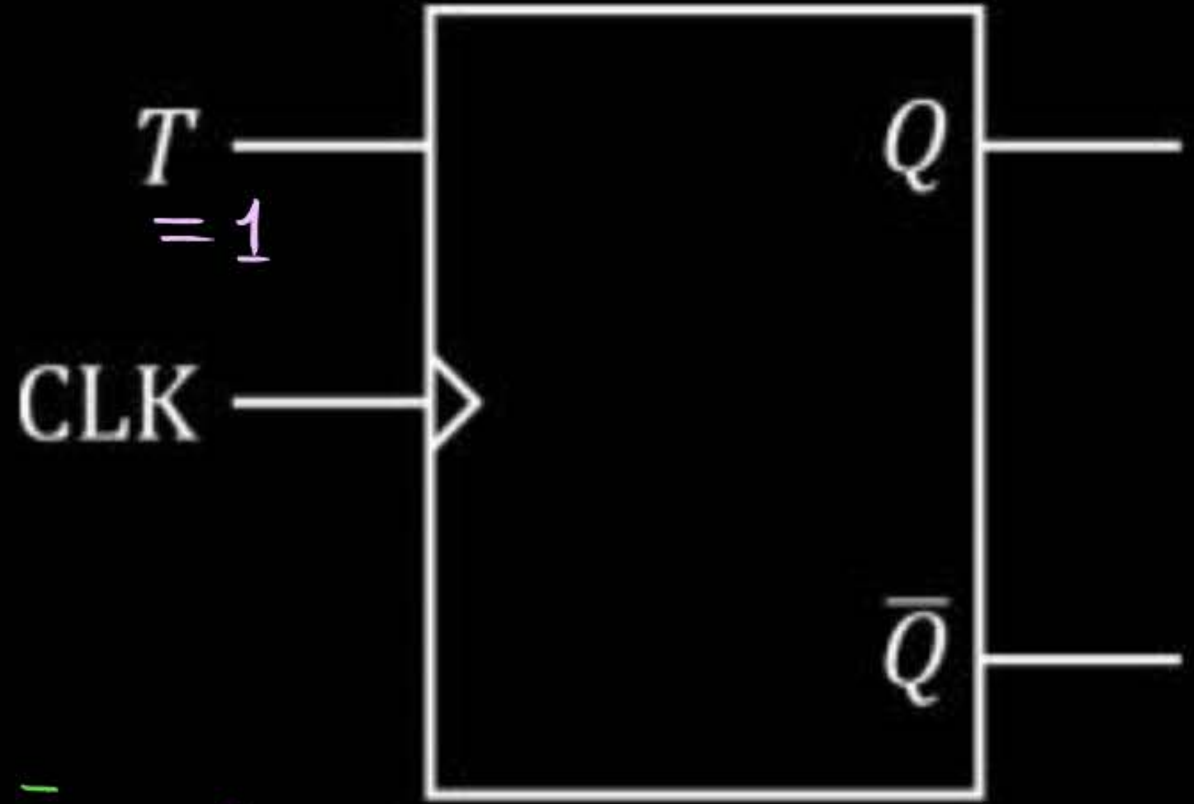
$$Q(n+1)[D, Q(n)] = \Sigma(2, 3) = D$$

- Excitation table :

$Q(n)$	$Q(n+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

[T-FF]

- What is T-FF ?



$$Q(n+1) = T \oplus Q(n)$$

$$Q(n+1) = 1 \oplus Q(n)$$

$$= \overline{Q(n)}$$

Characteristic table

T	Q(n)	Q(n+1)
0	0	0
0	1	1
1	0	1
1	1	0

Hold state

toggle state

	$\overline{Q}(n)$	$Q(n)$
$\overline{T}$		1
T	1	

$$Q(n+1)\left[T, Q(n)\right]$$

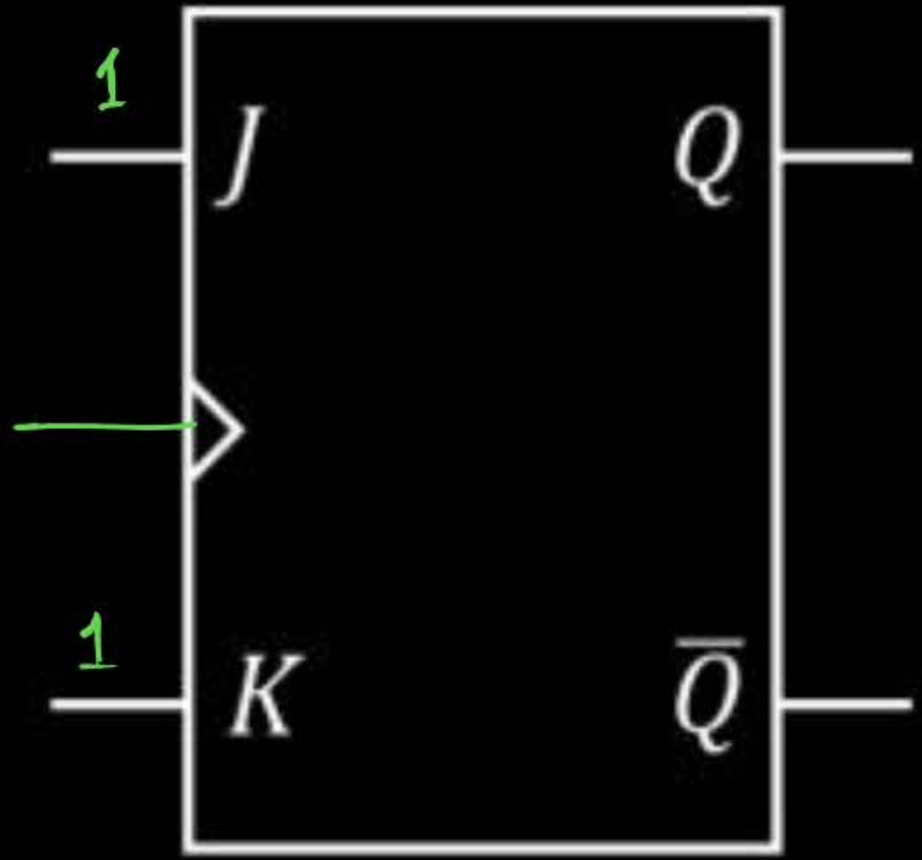
$$= \Sigma(1,2) = \overline{T}Q(n) + T\overline{Q}(n) = T \oplus Q(n)$$

- Excitation table :

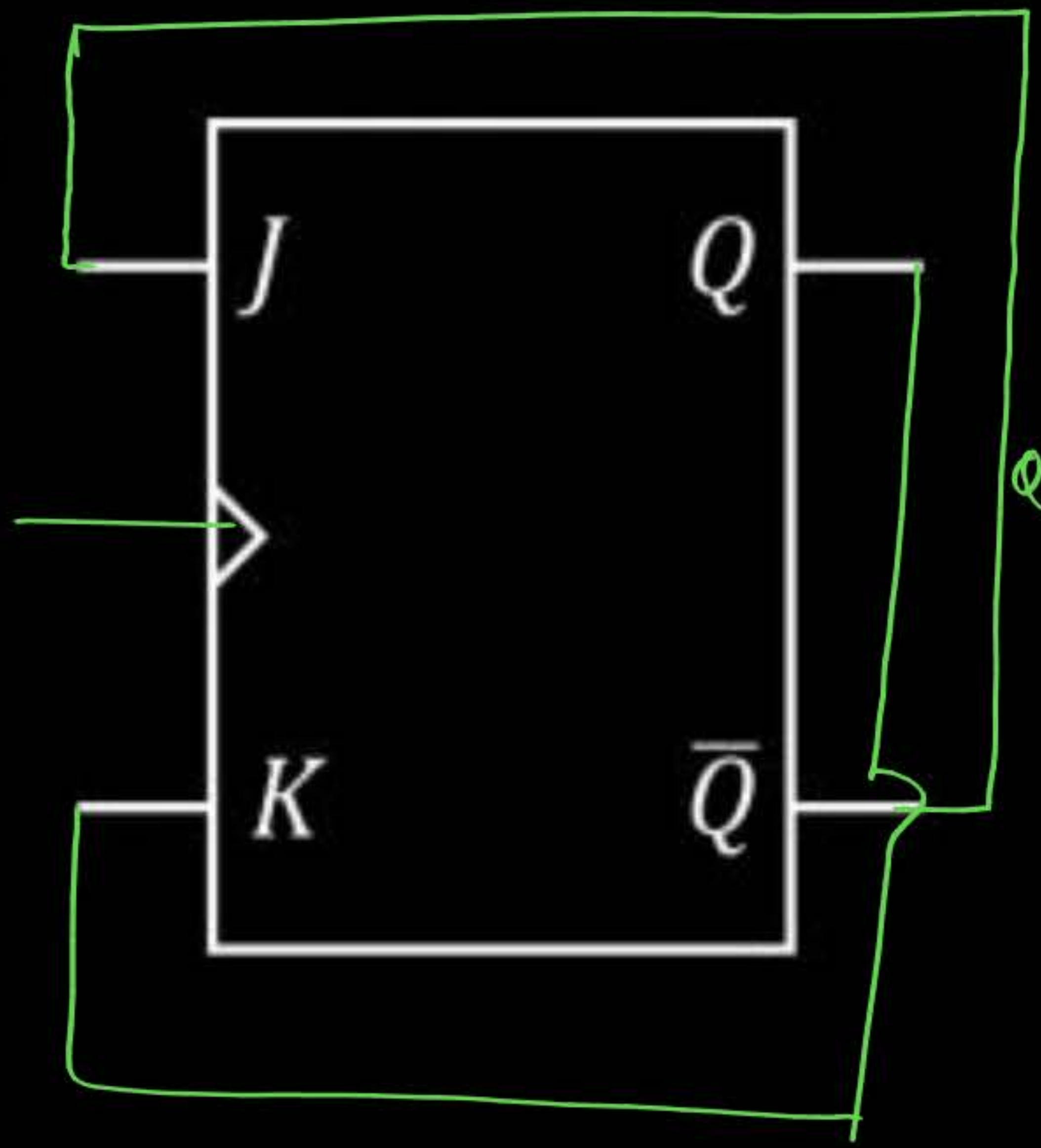
$Q(n)$	$Q(n+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

[Toggle mode of operation]

(i)



(ii)



$$Q(n+1) = J\bar{Q}(n) + \bar{K}Q(n) = \bar{Q}(n) + 0 = \bar{Q}(n)$$

$$Q(n+1) = J\bar{Q}(n) + \bar{K}Q(n) = \bar{Q}(n)\bar{Q}(n) + \bar{Q}(n)\cdot Q(n)$$

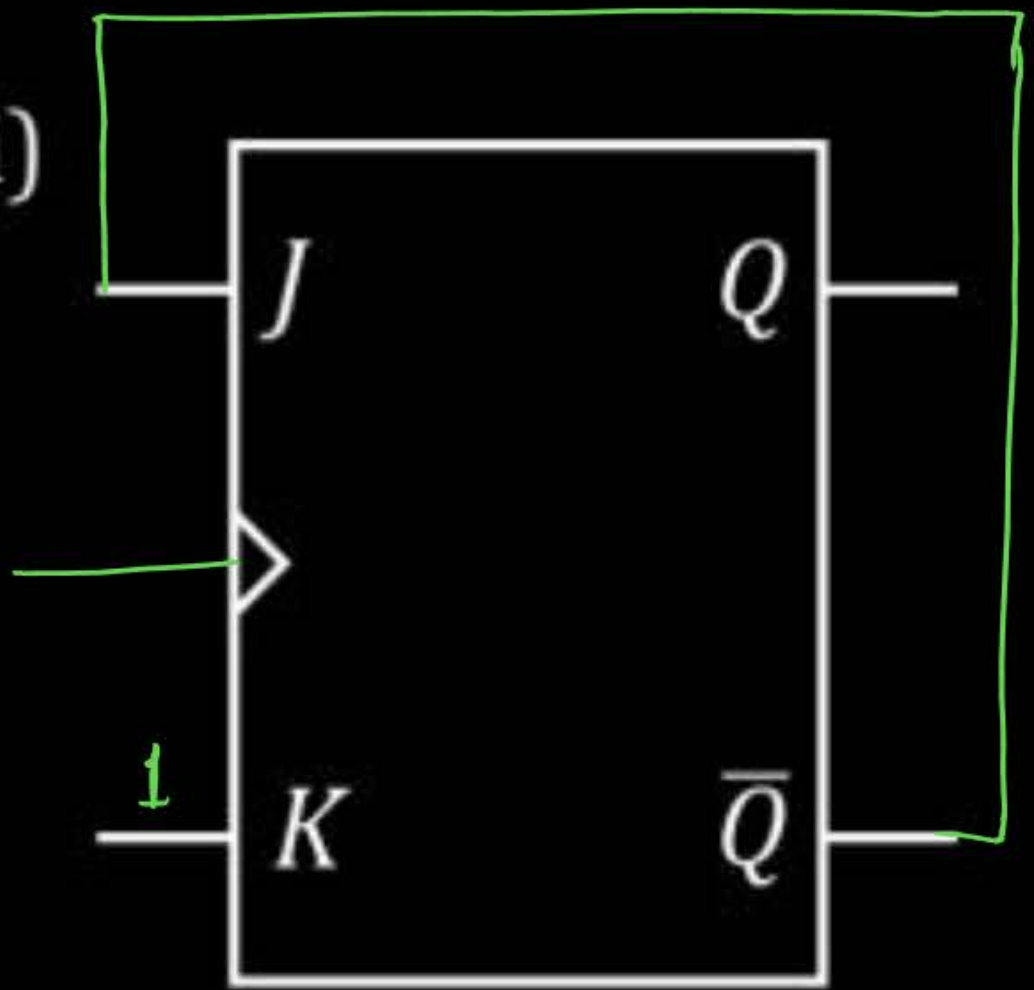
$$Q(n+1) = \bar{Q}(n)$$

$$\boxed{Q(n+1) = \bar{Q}(n)}$$

$\downarrow$

toggle mode of operation

(iii)

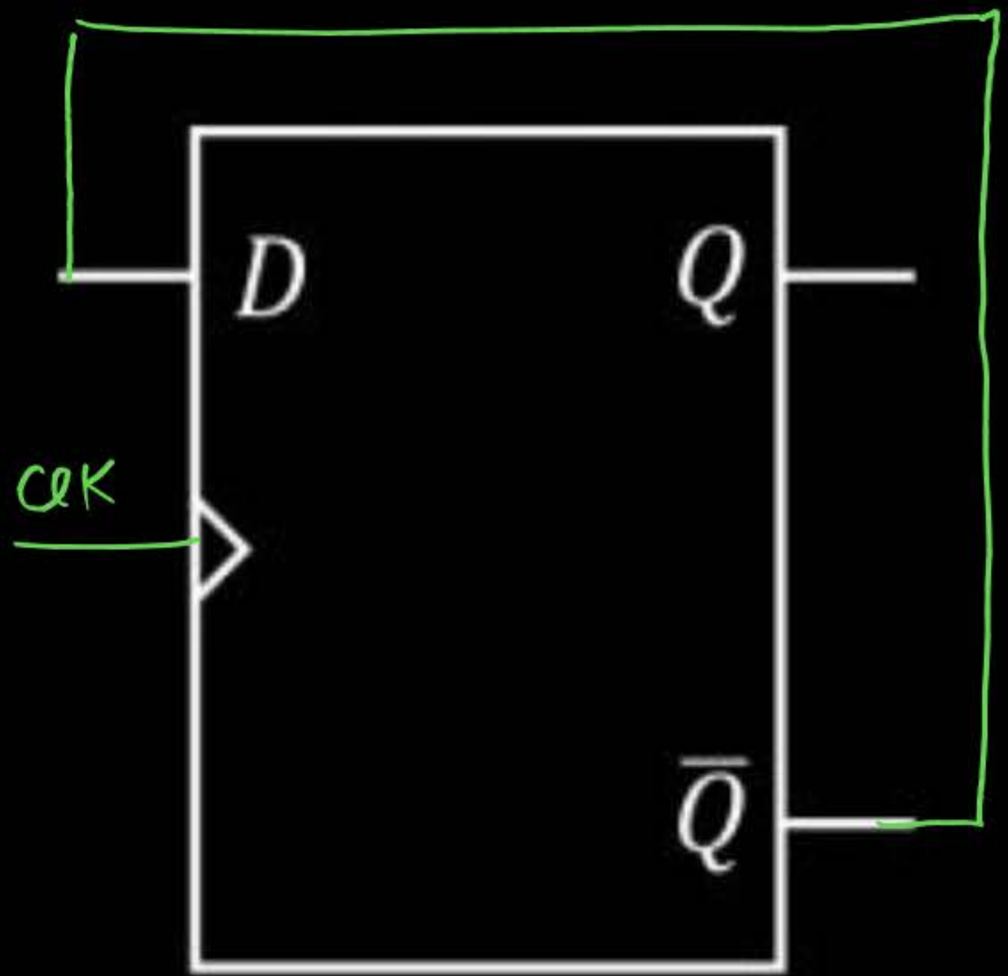


$$Q(n+1) = J\overline{Q}(n) + \overline{K}Q(n)$$

$$= \overline{Q}(n)\,\overline{Q}(n) + \overline{1}\,Q(n)$$

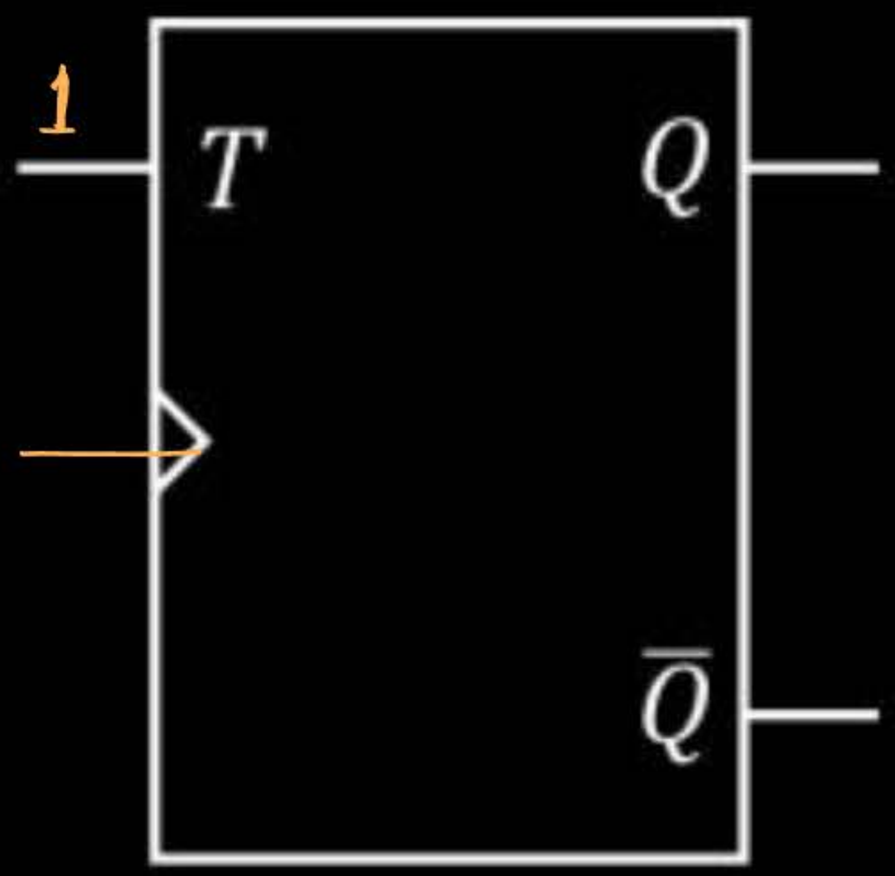
$$Q(n+1) = \overline{Q}(n)$$

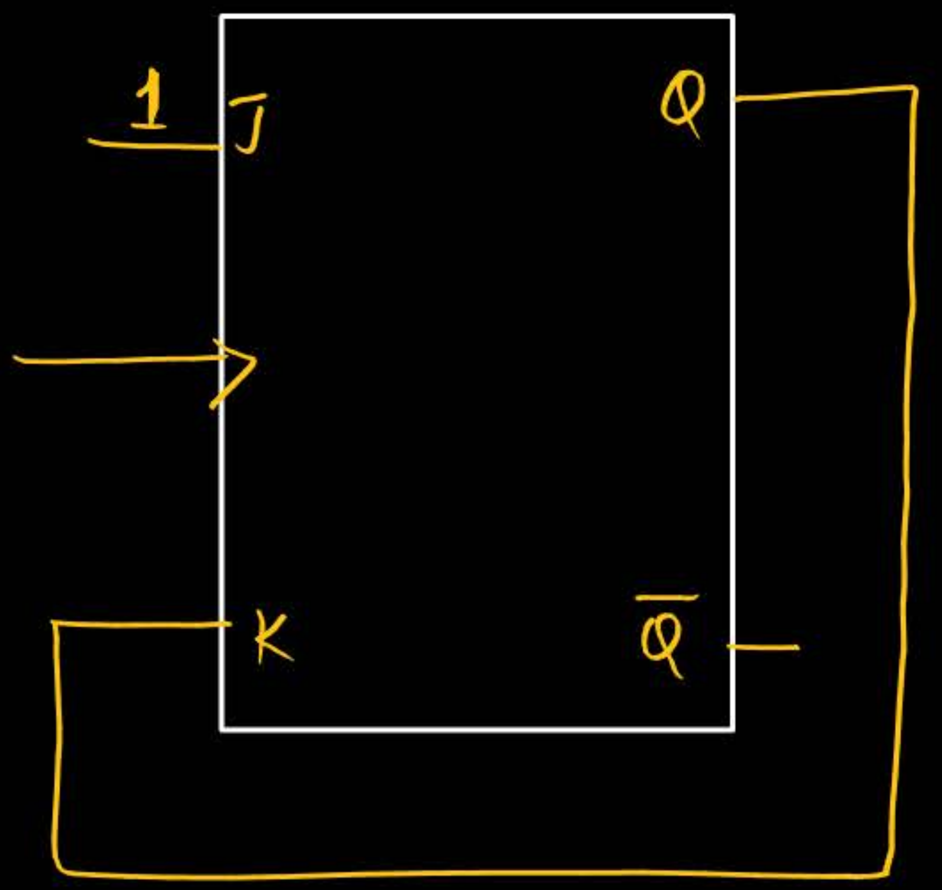
(iv)



$$\boxed{Q(n+1) = D = \overline{Q}(n)}$$

(v)





$$\boxed{\begin{aligned} Q(n+1) = T \oplus Q(n) &= 1 \oplus Q(n) \\ &= \overline{Q}(n) \end{aligned}}$$

$$Q(n+1) = J\overline{Q}(n) + \overline{K}Q(n)$$

$$= 1\,\overline{Q}(n) + \overline{Q(n)}\;Q(n)$$

$$Q(n+1) = \overline{Q}(n)$$

$f_{clk}/2$

Q

$$\left.\begin{array}{ll} & 0 \\ 1^{st} & 1 \end{array}\right] \rightarrow \text{MOD-2 Counter}$$

2^{nd} 0

3^{rd} 1

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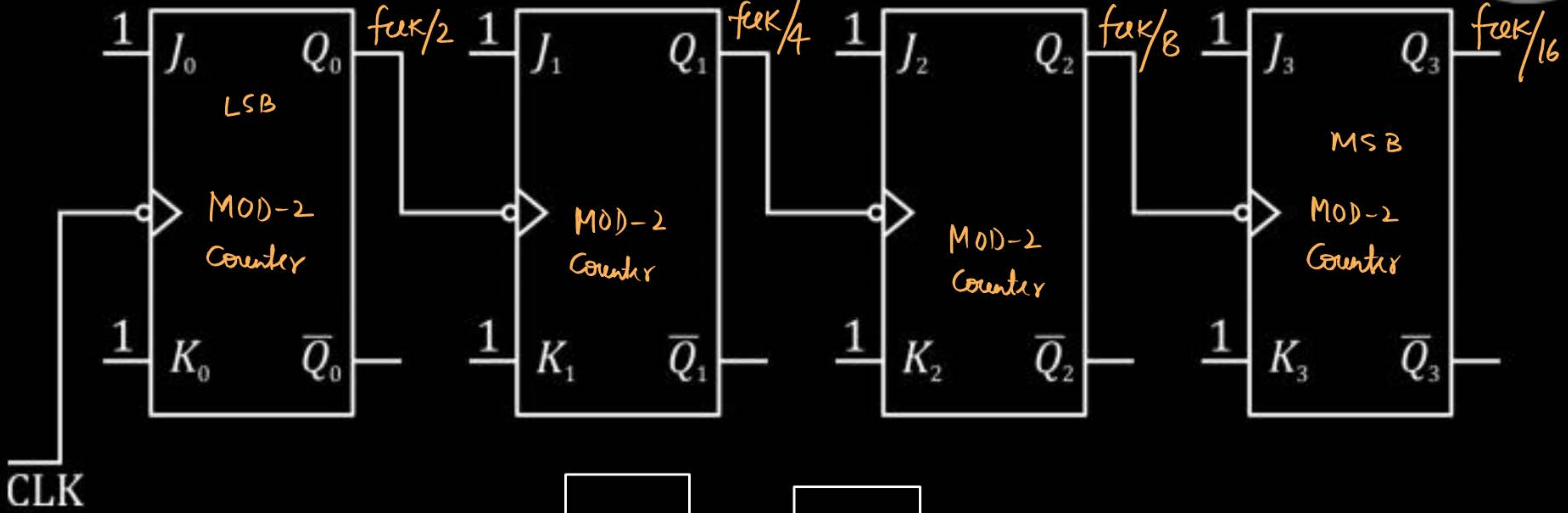
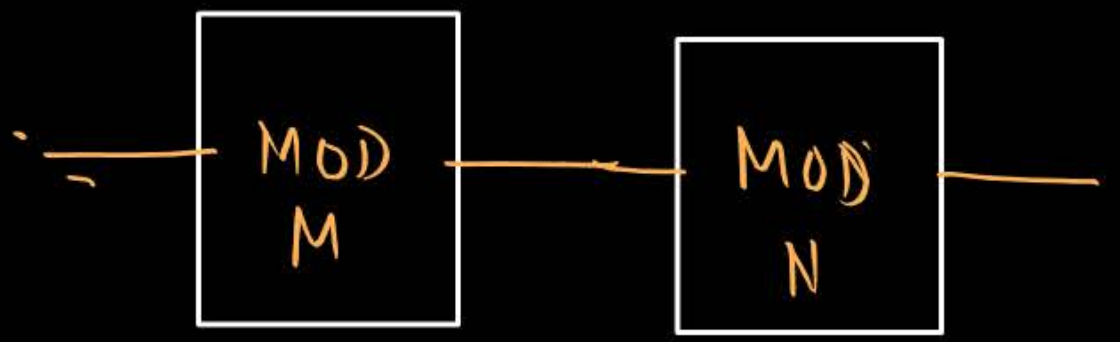
$\boxed{\text{Toggle mode of operation is the smallest counter possible i.e. MOD-2 Counter.}}$

Lets analyze asynchronous counter :

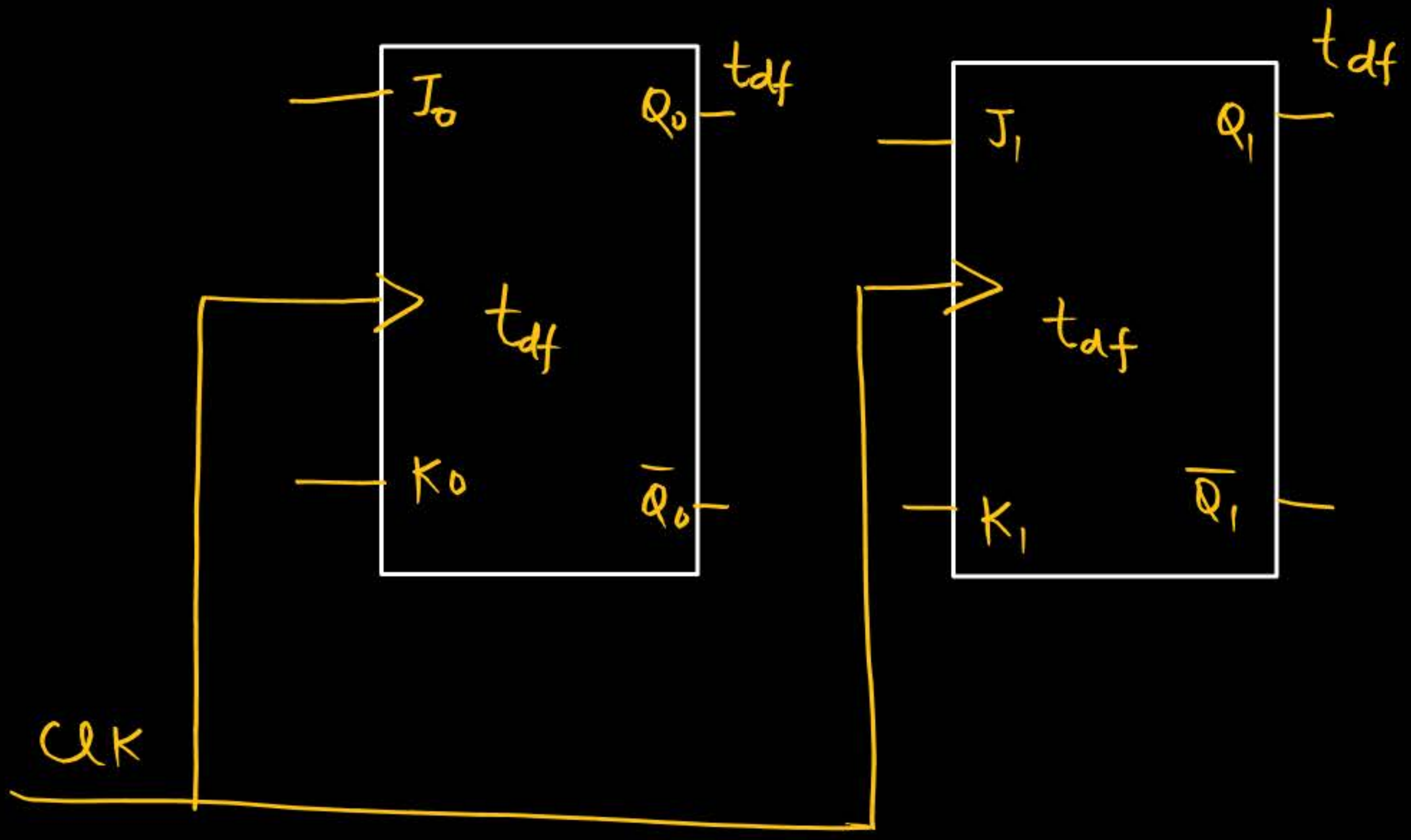


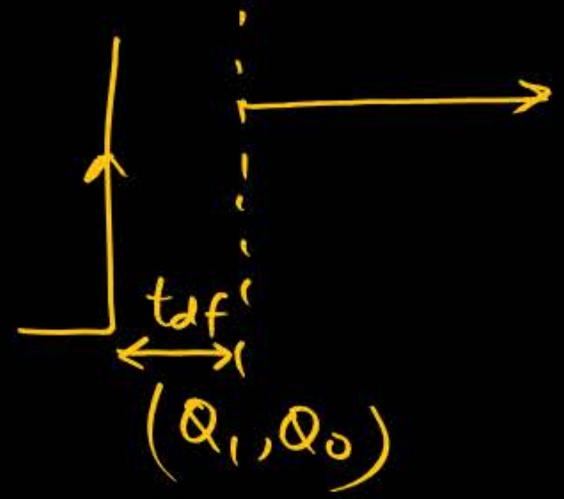


$\equiv$ MOD $\underline{\underline{M \cdot N}}$

Synchronous Counter

- What is synchronous counter ?





$T_{clk} \geq t_{df}$

$$\boxed{f_{clk} \leq 1/t_{df}}$$

$$\boxed{(f_{clk})_{max} = \frac{1}{t_{df}}}$$

How to design a Synchronous Counter

- 0 – 3 – 2 – 1 $\longrightarrow$ MOD no. = 4 $\longrightarrow$ 2FF $\longrightarrow$

Design above counter using JK-FF

$Q_1(n)$	$Q_0(n)$	$Q_1(n+1)$	$Q_0(n+1)$	J_1	K_1	J_0	K_0
0	0	1	1	1	X	1	X
0	1	0	0	0	X	X	1
1	0	0	1	X	1	1	X
1	1	1	0	X	0	X	1

	Q_1	Q_0
	0	0
1st	1	1
2nd	1	0
3rd	0	1
4th	0	0

$$J_1[Q_1(n), Q_0(n)] = \Sigma(0) + d\Sigma(2,3), \quad K_1 = \Sigma 2 + d\Sigma(0,1)$$

$$J_0 = \Sigma(0,2) + d\Sigma(1,3), \quad K_0 = \Sigma(1,3) + d\Sigma(0,2)$$

J_1	$\overline{Q_0}(n)$	$Q_0(n)$
$\overline{Q_1}(n)$	1	
$Q_1(n)$	X	X

$J_1 = \overline{Q_0}(n)$

K_1	$\overline{Q_0}(n)$	$Q_0(n)$
$\overline{Q_0}(n)$	X	X
$Q_1(n)$	1	

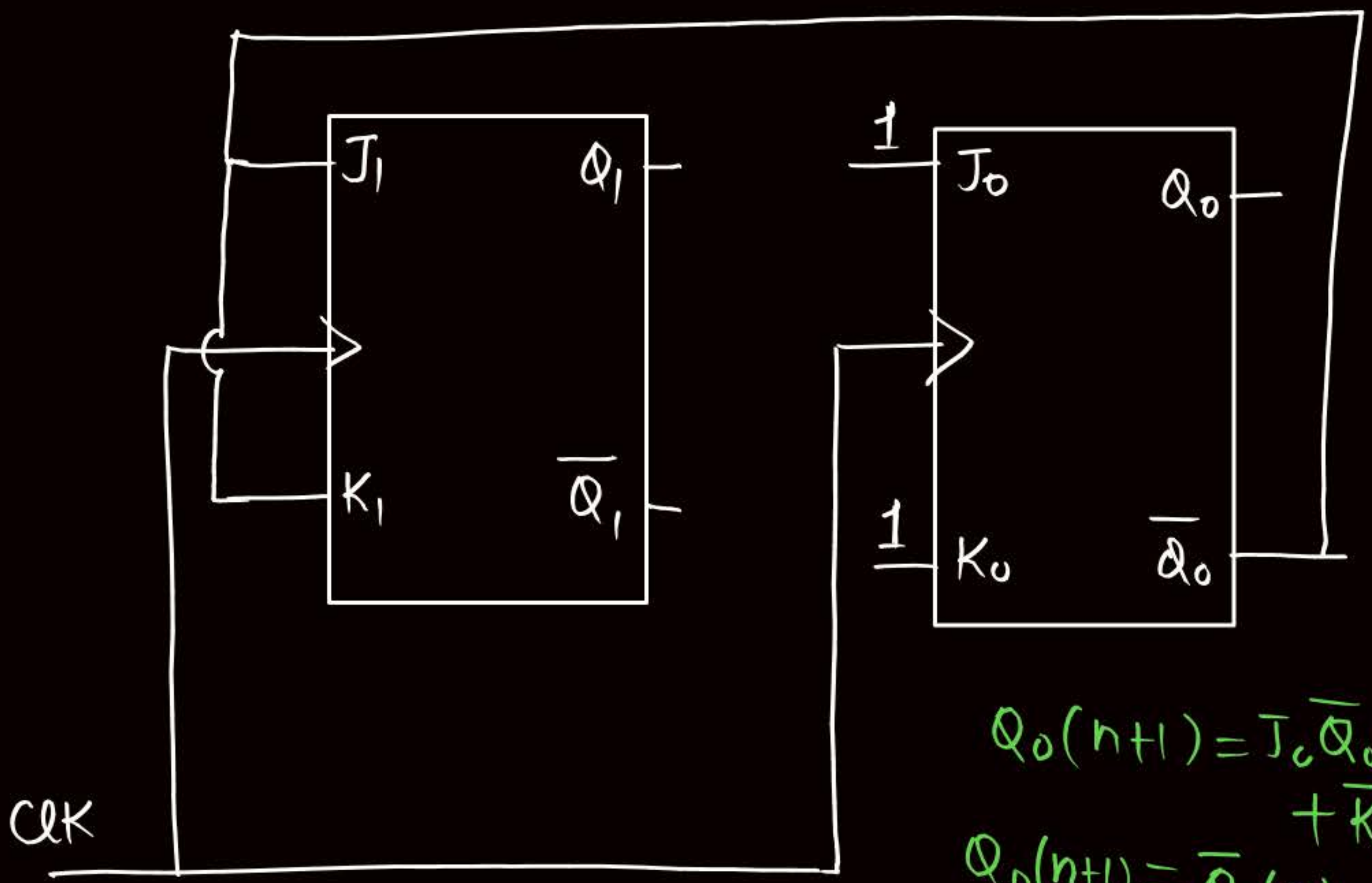
$K_1 = \overline{Q_0}(n)$

J_0	$\overline{Q_0}(n)$	$Q_0(n)$
$\overline{Q_1}(n)$	1	X
$Q_1(n)$	1	X

$J_0 = 1$

K_0	$Q_0(n)$	$Q_0(n)$
$\overline{Q_1}(n)$	X	1
$Q_1(n)$	X	1

$K_0 = 1$



$Q_1 = 0, \quad Q_0 = 0$

$Q_1 Q_0 = (00)$

	Q_1	Q_0
	0	0
1st	1	1
2nd	1	0
3rd	0	1
4th	0	0

MOD no. 4

$$Q_0(n+1) = J_0\overline{Q}_0(n) + \overline{K}_0 Q_0(n)$$

$$Q_0(n+1) = \overline{Q}_0(n)$$

Q_0	Q_1
0	0
1	1
0	1
1	0

$Q_0 Q_1 = (00)$

$$Q_1(n+1) = J_1\overline{Q}_1(n) + \overline{K}_1 Q_1(n)$$

$$= \overline{Q}_0(n)\,\overline{Q}_1(n) + Q_0(n)\,Q_1(n)$$

$$= Q_1(n) \odot Q_0(n)$$

- Design counter 0 – 1 – 2 – 4 – 6 using T-FF → MOD no. 5 → 3FF

$Q_2(n)$	$Q_1(n)$	$Q_0(n)$	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	1	0	0	1	1	0
0	1	1	X	X	X	X	X	X
1	0	0	1	1	0	0	1	0
1	0	1	X	X	X	X	X	X
1	1	0	0	0	0	1	1	0
1	1	1	X	X	X	X	X	X

$$T_2 = \Sigma(2,6) + d\,\Sigma(3,5,7)$$

$$T_1 = \Sigma(1,2,4,6) + d\,\Sigma(3,5,7)$$

$$T_0 = \Sigma(0,1) + d\,\Sigma 3,5,7)$$

T_2

	$\overline{Q}_1\overline{Q}_0$	$\overline{Q}_1 Q_0$	$Q_1 Q_0$	$Q_1\overline{Q}_0$
$\overline{Q}_2(n)$			X	1
$Q_2(n)$		X	X	1

$\rightarrow Q_1$

$T_2 = Q_1(n)$

T_1

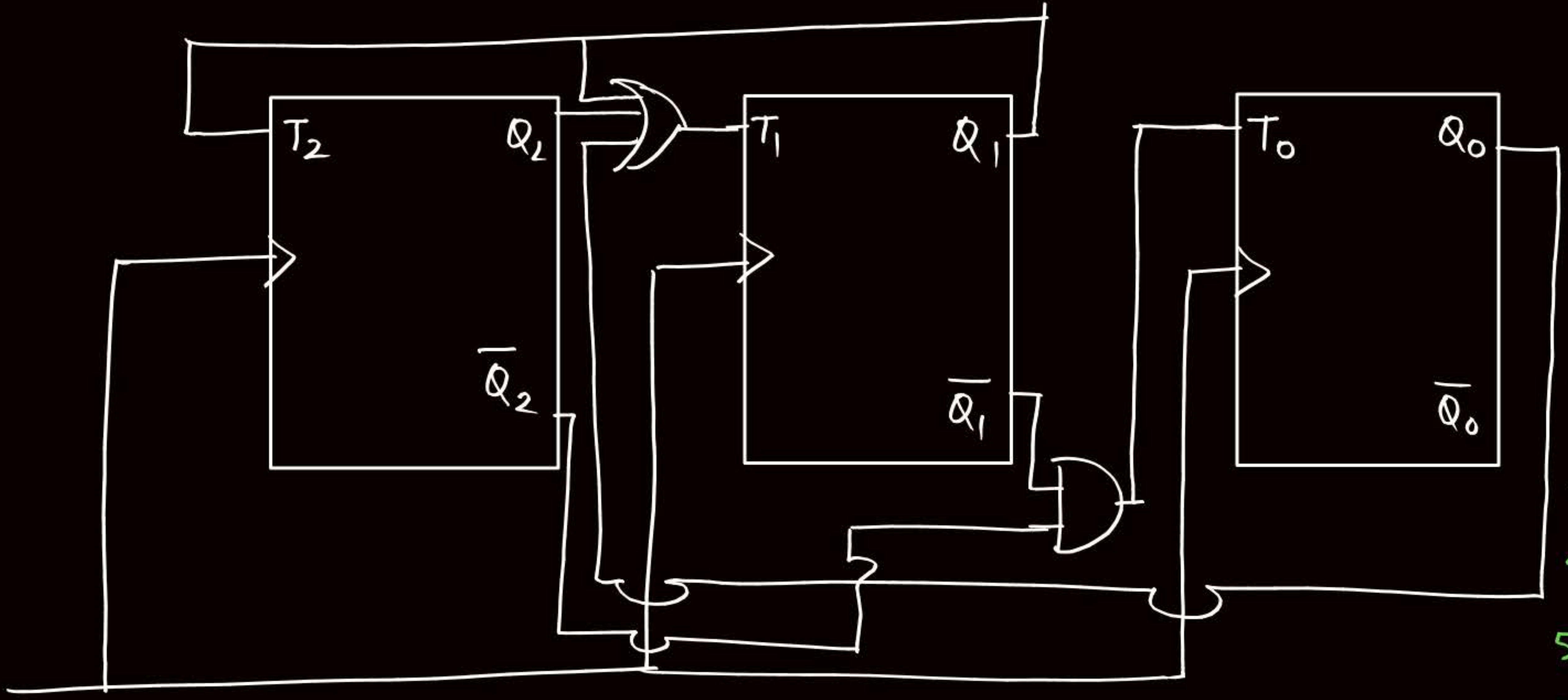
	$\overline{Q}_1\overline{Q}_0$	$\overline{Q}_1 Q_0$	$Q_1 Q_0$	$Q_1\overline{Q}_0$
$\overline{Q}_2$		1	X	1
Q_2	1	X	X	1

$T_1 = Q_2 + Q_1 + Q_0$

T_0

	$\overline{Q}_1\overline{Q}_0$	$\overline{Q}_1 Q_0$	$Q_1 Q_0$	$Q_1\overline{Q}_0$
$\overline{Q}_2$	1	1	X	
Q_2		X	X	

$$T_0 = \overline{Q}_2(n)\,\overline{Q}_1(n) = \overline{Q_2(n) + Q_1(n)}$$



	Q_2	Q_1	Q_0
	0	1	0
1^{st}	1	0	0
2^{nd}	1	1	0
3^{rd}	0	0	0
4^{th}	0	0	1
5^{th}	0	1	0
6^{th}			

$$Q_2(n+1) = T_2 \oplus Q_2(n)$$
$$= Q_1(n) \oplus Q_2(n)$$

$$Q_0(n+1) = T_0 \oplus Q_0(n)$$
$$= \overline{Q}_1(n)\,\overline{Q}_2(n) \oplus Q_0(n)$$
$$= \overline{Q_2(n)+Q_1(n)} \oplus Q_0(n)$$

$$Q_1(n+1) = T_1 \oplus Q_1(n)$$
$$= \left[Q_2(n)+Q_1(n)+Q_0(n)\right] \oplus Q_1(n)$$
$$= \overline{Q}_2(n)\cdot\overline{Q}_1(n)\cdot\overline{Q}_0(n)\cdot Q_1(n) + \left[Q_2(n)+Q_1(n)+Q_0(n)\right]\cdot\overline{Q}_1(n)$$

$$Q_1(n+1) = \left[Q_2(n)+Q_0(n)\right]\overline{Q}_1(n)$$

- Design counter 0 – 3 – 2 – 6 – 7 – 9 – 5 using D-FF $\boxed{\text{H.W}}$

Question

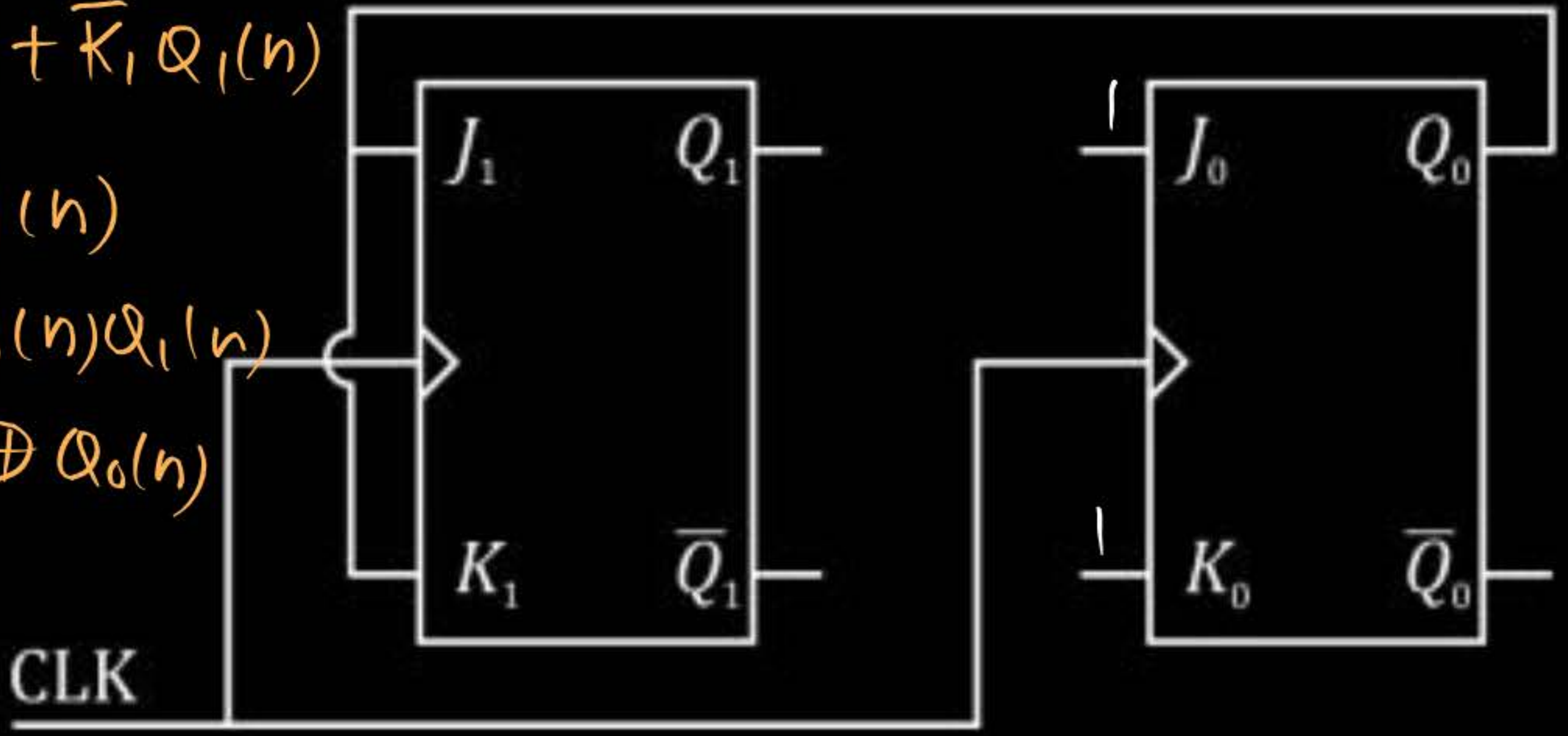
A sequential circuit is as given below :

$(n+1) = J_1 \bar{Q}_1(n) + \bar{K}_1 Q_1(n)$

$= Q_0(n)\bar{Q}_1(n) + \bar{Q}_0(n) Q_1(n)$

$Q_1(n+1) = Q_1(n) \oplus Q_0(n)$

$(n+1) = \bar{Q}_0(n)$



	Q_0	Q_1
	0	0
1st	1	0
2nd	0	1
3rd	1	1
4th	0	0

Initial state of the synchronous counter is given as $\boxed{Q_0Q_1 = (00)_2}$ what will be states of counter after applying clock pulses.

(a) 00 – 10 – 01 – 11 – 00 (b) 00 – 10 – 11 – 01 – 00

(c) 00 – 11 – 10 – 01 – 00 (d) 00 – 01 – 10 – 11 – 00

Question

The initial state of the given counter is $\boxed{Q_1Q_0 = (00)_2}$. What will be states of counter after applying clock pulses :

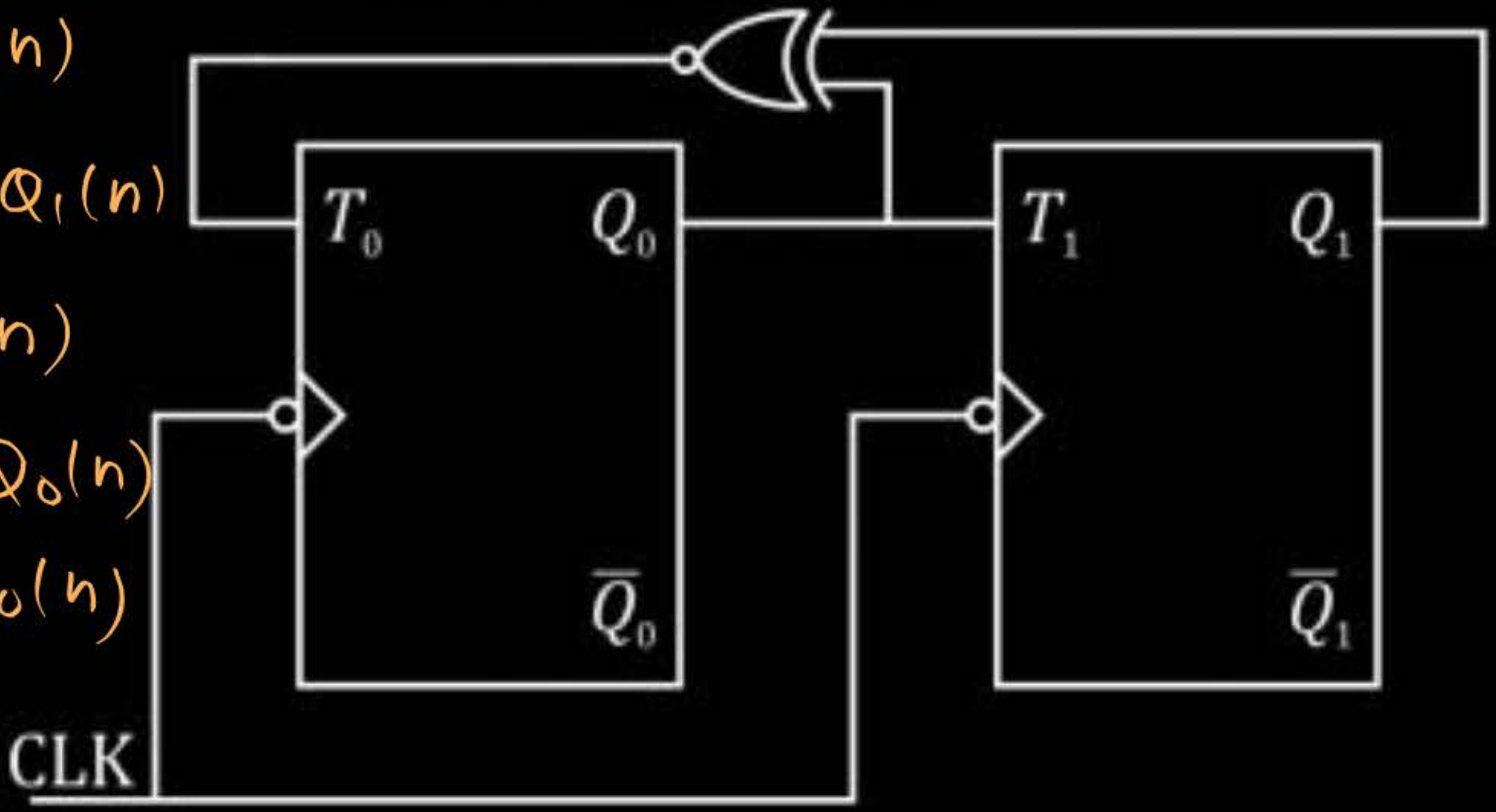
$(n+1) = T_1 \oplus Q_1(n)$

$= Q_0(n) \oplus Q_1(n)$

$(n+1) = T_0 \oplus Q_0(n)$

$= Q_1(n) \odot Q_0(n)$

$(n+1) = \overline{Q_1(n)} \oplus Q_0(n)$



	Q_1	Q_0
	0	0
1st	0	1
2nd	1	1
3rd	0	0

MOD =

(a) 00 – 10 – 11 – 01 – 00

(b) 00 – 01 – 11 – 00

(c) 00 – 11 – 01 – 10 – 00

(d) 00 – 01 – 10 – 00

[Question]

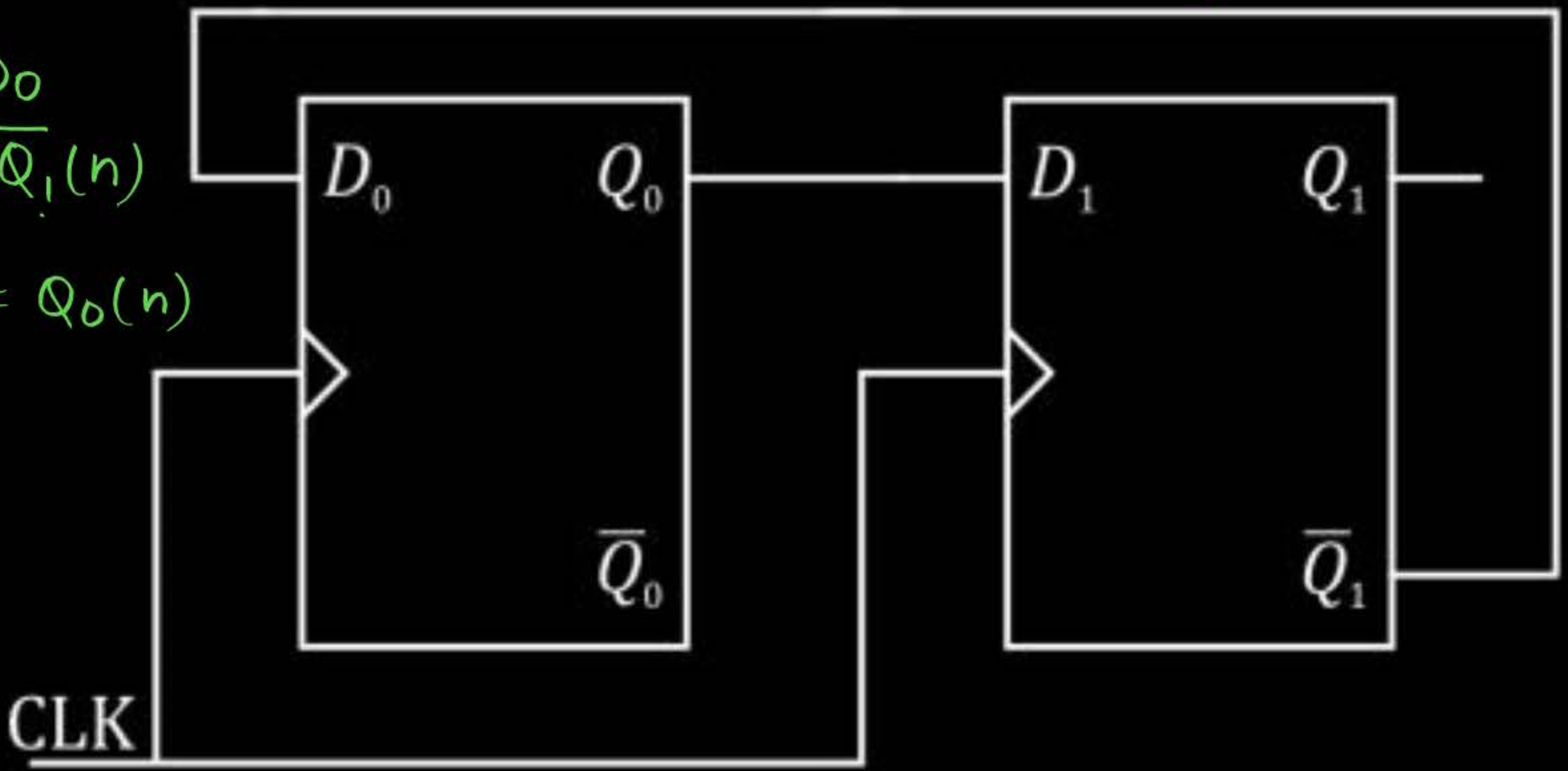
A sequential circuit is as given below :

$(0 - 2 - 3 - 1)$

$(0)_{10} \xrightarrow{4\times55} (0)_{10} \xrightarrow{221^{th}} (2)_{10} \xrightarrow{222^{th}} (3)_{10}$

$Q_0(n+1) = D_0$
$= \overline{Q_1}(n)$

$Q_1(n+1) = D_1 = Q_0(n)$



	Q_0	Q_1
	0	0
1st	1	0
2nd	1	1
3rd	0	1
4th	0	0

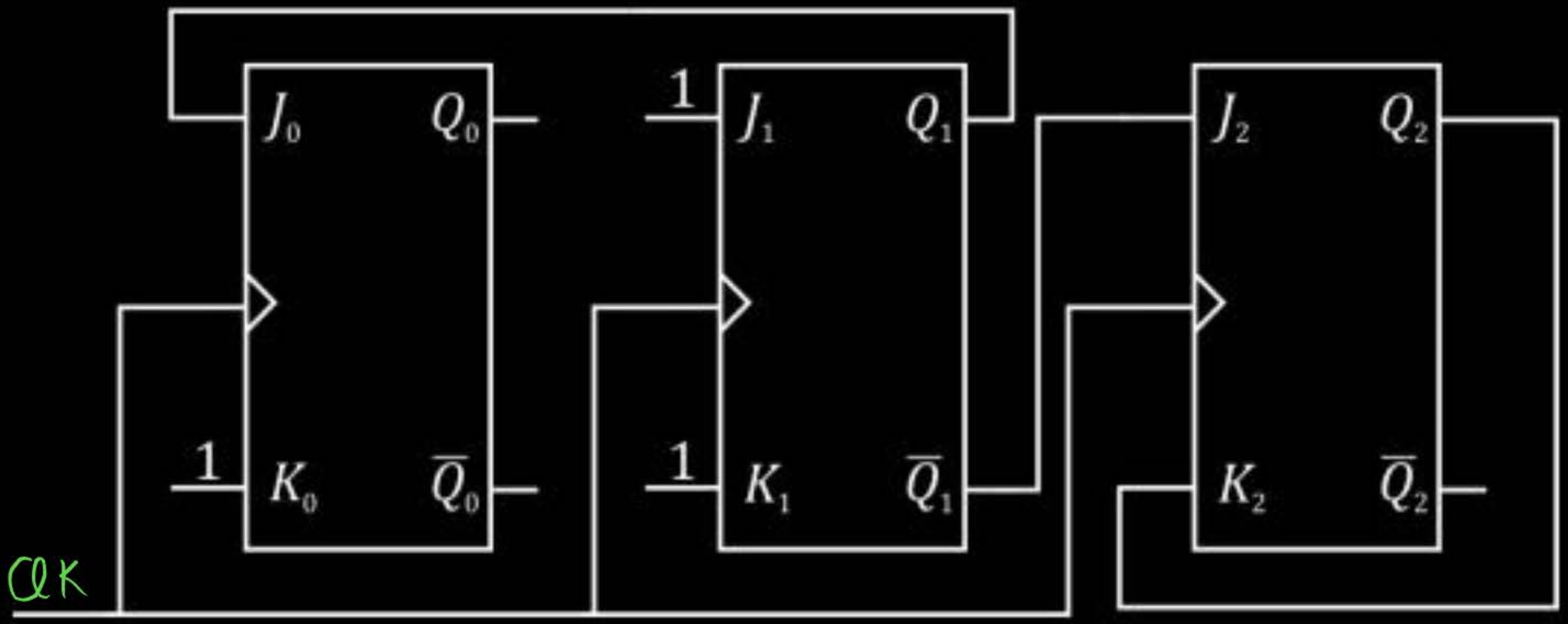
→ MOD no. 4

Initial state of the counter is $Q_0Q_1 = (00)_2$. What will the state of counter after application of 222 clock pulses $(3)_{10}$.

Question

A sequential circuit is as given below :

H.W.

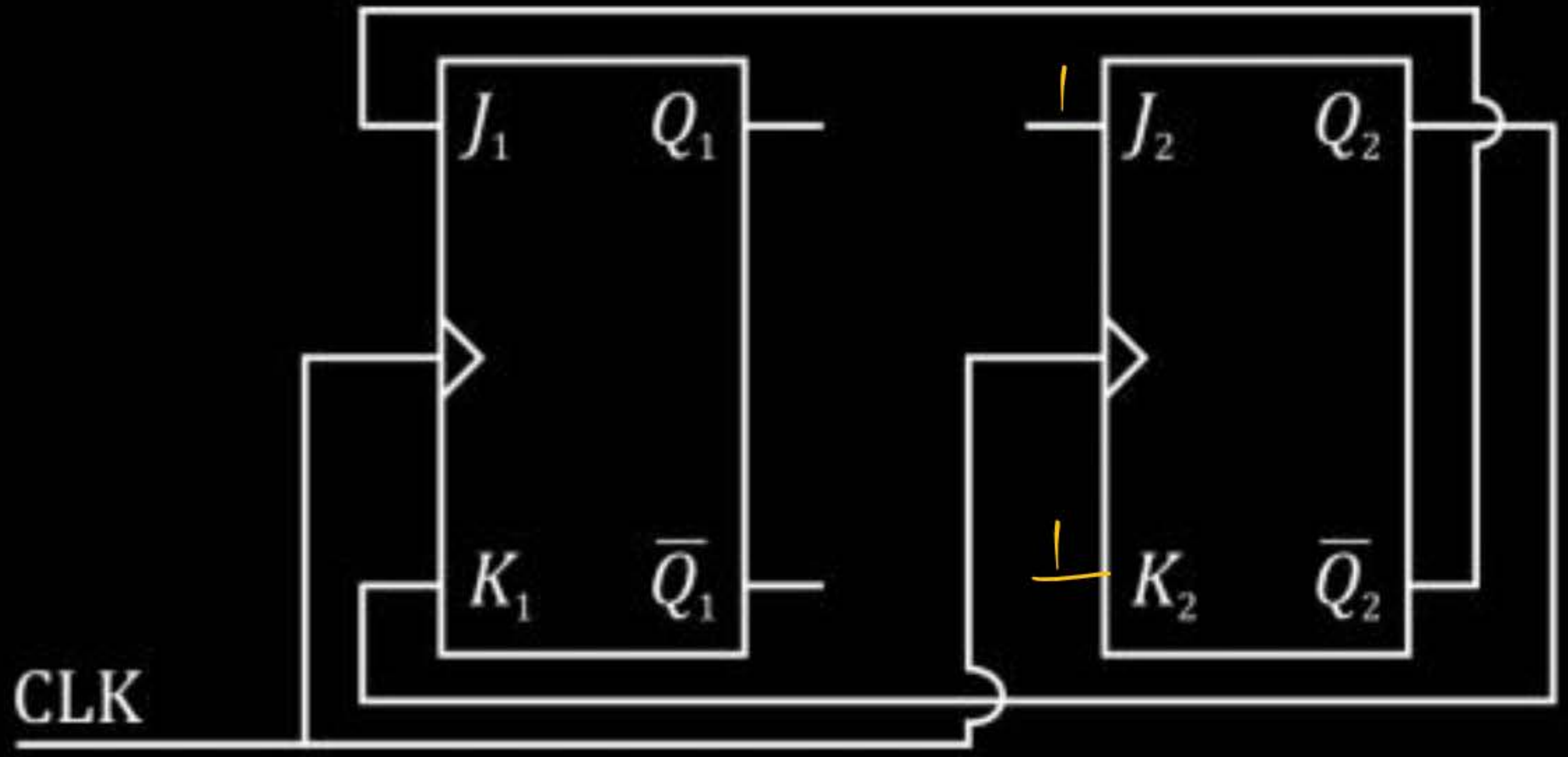


If initial state of counter is $Q_2Q_1Q_0 = (001)_2$, then after 8^{th} clock pulse, counter will be in state $(\quad)_{10}$.

Question

The output of the two FFs, Q_1 and Q_2 are initially at '0'. The sequence generated at Q_1 after application of clock pulses :

H.W.



(a) 01110.....

(b) 01010.....

(c) 00110.....

(d) 01100.....

Topic : 2 Min Summary

→ synchronous Counter

Thank you

GW Soldiers !