PRACTICE SHEET-1

CS & IT

DIGITAL LOGIC

SEQUENTIAL CIRCUIT

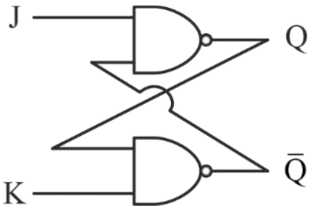
Q1 In a S-R flip-flop, the present output is Q = 1. Then after applying input S = 0, R = 1 and then S = 0, R = 0, output will be:
(A) Q = 0
(B) Q = 1
(C) Q = → invalid state
(D) None of these

Q2 In a JK flip-flop output Q = 0. To change it to Q = 1, the inputs J and K will be:
(A) J = 1, K = 1 (B) J = 1, K = X
(C) J = 0, K = 0 (D) J = 0, K = 1

Q3 Which of the following is true?
(A) S = 1, R = 1, is a valid state input for S-R ff
(B) J = 1, K = 1 is an invalid state input for J-K ff
(C) Input (0, 0) is hold state input for both S-R as well as JK ff
(D) None of these

Q4 A flip flop has characteristic equation $Q(n+1) = \overline{A}\,\overline{Q} + \overline{B}Q$
Then it will be in toggle mode of operation if
(A) A = 1, B = 1 (B) A = 0, B = 1
(C) A = 1, B = 0 (D) A = 0, B = 0

Q5 A logic circuit is as given below:
Then which of the following is true about above circuit?



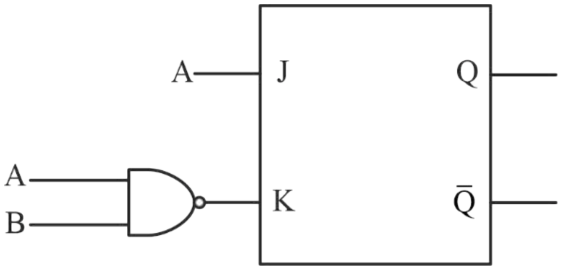
(A) Race around condition at J = 1, K = 1
(B) Race around condition at J = 0, K = 0
(C) J = 1, K = 1 is invalid state input
(D) None of these

Q6 In J-K FF, to change output from 0 to 1 input is changed from
(A) J = 0, K = 0 to J = 0, K = 1
(B) J = 0, K = 1 to J = 1, K = 0
(C) J = 0, K = 1 to J = 0, K = 0
(D) J = 1, K = 0 to J = 0, K = 1

Q7 Which of the following statement is true?
(A) Master-Slave ff is used to avoid race-around condition.
(B) Edge triggered J-K FF has problem of race-around condition when J = 1, K = 1
(C) Race-around condition occurs in S-R ff with S = 1, R = 1
(D) None of these

Q8 To solve the problem of invalid state at input S = 1 and R = 1 in S-R ff, S and R are replaced by
(A) $S = J\overline{Q}, R = \overline{K}Q$
(B) $S = J\overline{Q}, R = KQ$
(C) $S = JQ, R = \overline{K}Q$
(D) S = JQ, R = KQ

Q9 In J-K FF, J and K inputs are given as:



Then which of the following is true?

(A) $Q(n+1) = A\overline{Q} + AB$

(B) $Q(n+1) = A\overline{Q} + \overline{B}Q$

(C) $Q(n+1) = A \oplus B \oplus Q$

(D) $Q(n+1) = A \oplus B$

Q10 Which of the following is true?

(A) $Q(n+1) = S + \overline{R}Q$ is valid for all S and R values

(B) $Q(n+1) = J\overline{Q} + \overline{K}Q$ is valid only when J. K = 1

(C) $Q(n+1) = S + \overline{R}Q$ is valid when S.R = 1

(D) $Q(n+1) = S + \overline{R}Q$ is valid when S.R = 0

Q11 A counter sequence is given as:

2 – 3 – 1 – 0 – 4 – 7, then MOD no. of the counter is

(A) 7 (B) 6

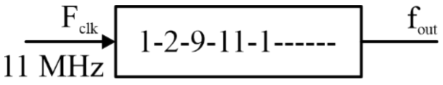
(C) 5 (D) 4

Q12 A counter sequence is given as:

3 – 2 – 1 – 4 – 6 – 3 – - - - - -

If its starting state is $(100)_2$ then after application of 1049 clock pulses, counter will be at __(__)$_{10}$.

Q13 A sequential circuit is as given below:



The value of f_{out} will be _____ MHz.

Q14 Which of the following is not true?

(A) In asynchronous different FFs are driven by different clock

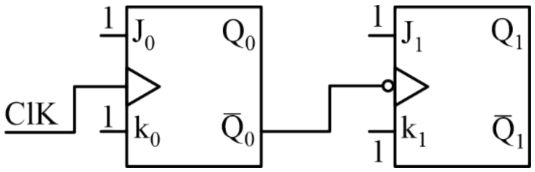
(B) In asynchronous counter at output of each FF input frequency is divided by 2

(C) The sequence 0 – 1 – 3 -2 require 2 FFs to design it with asynchronous counter

(D) Fixed up sequence and fixed down sequence is possible to design with asynchronous counter

Q15 A sequential circuit is as given below:

The above circuit is



(A) MOD -4 up counter

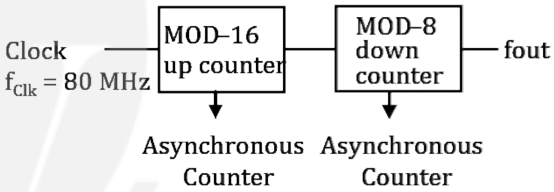
(B) MOD-4 down counter

(C) MOD-4 neither up nor down counter

(D) MOD-2 counter

Q16 A sequential circuit as given below:

Value of f_{out} will be



(A) Can not be calculated as one block is up-counter and other is down counte

(B) 5 MHz

(C) 0.625 MHz

(D) 3.33 MHz

Q17 MOD-12 counter can be designed

(A) cascading two MOD-6 counter

(B) cascading MOD-4 counter and MOD-8 counter

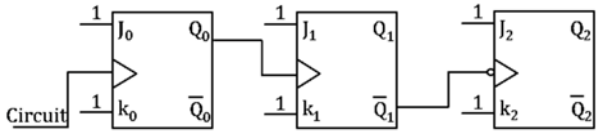
(C) cascading MOD-4 & mod-3 counter

(D) cascading MOD-3 & MOD-9 counter

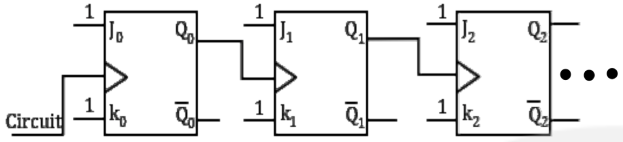
Q18 A sequential circuit is as given below:

Initially the counter is at $Q_0Q_1Q_2 = (100)_2$ then

after 2 clock pulses, output will be ____(___)$_{10}$____.



Q19 A sequential circuit is as given below has total 20 FFs connected. If input clock frequency is 128 MHz then, at output of 16th FF frequency of the waveform will be:

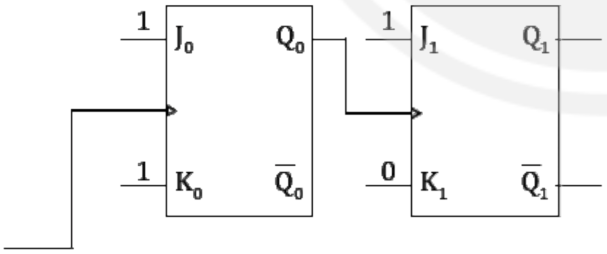


(A) 8 MHz (B) 12.8 MHz
(C) 1.95 KHz (D) 4 MHz

Q20 Sequential circuit A is designed with 5 FFs and sequential circuit –B is designed with 6-FFs, then maximum MOD no. possible combinedly using sequential circuit-A & sequential circuit-B is _____.

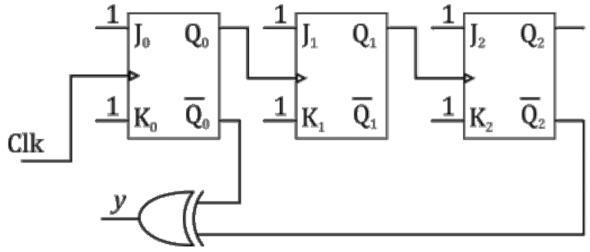
Q21 To design a MOD-224 counter, minimum no. of FFs required is_____.

Q22 A sequential circuit is as given below:



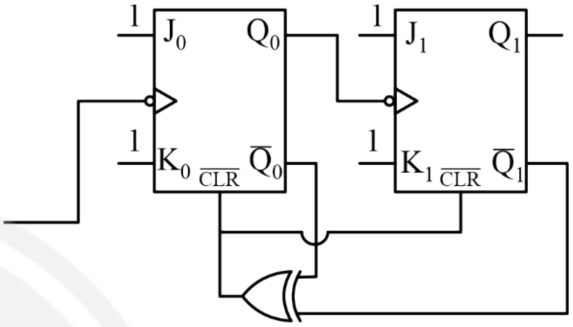
Both the ffs are at reset state initially, then MOD-no. of the counter is
(A) MOD-4 counter (B) MOD-3 counter
(C) MOD-2 counter (D) None of these

Q23 A sequential circuit is as given below:



We have applied 32 clock pulses then number of times output y toggles is_____.

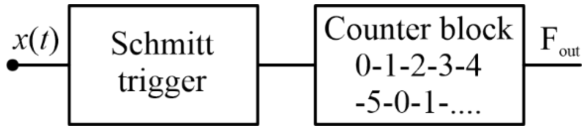
Q24 A sequential circuit is as given below:



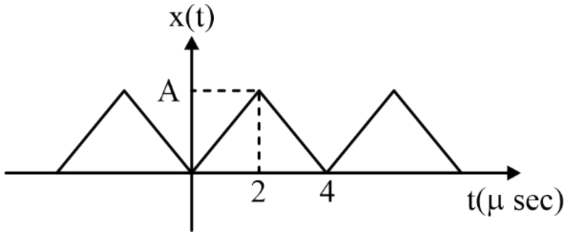
The counter is _____.
(A) MOD-4 UP counter
(B) MOD-3 Down counter
(C) MOD-3 UP counter
(D) MOD-4 Down counter

Q25 Asynchronous counter designed suing 4-FFs has Mod number M. By adding FFs in cascade, we changed the MOD number to 6M, then the minimum number of additional FFs used is_____.

Q26 A sequential circuit is designed as shown:

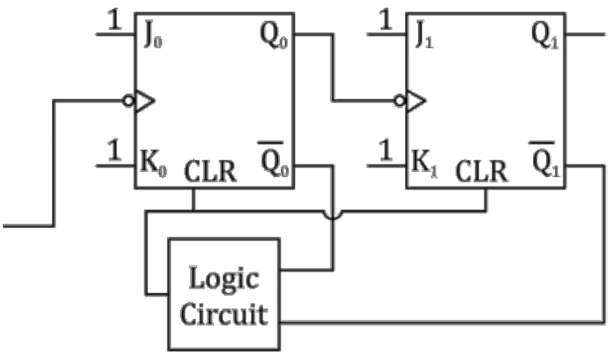


x(t) is given as



The value of F_{out} _____kHz.

Q27 A sequential circuit is as given below:



If above sequential circuit has to work as MOD-3 counter then logic circuit will be:

(A) Two input OR gate

(B) Two input AND gate

(C) Two input NAND gate

(D) Two input NOR gate

Q28 Which of the following is true:

(A) Asynchronous counters are faster compared to synchronous counters.

(B) For same MOD-number, synchronous counters require fewer FFs compared to asynchronous counter

(C) Sequence 0-1-2-3-0 can be designed only in asynchronous counter.

(D) Sequence 0-1-3-2-0 can be designed only in synchronous counter.

Q29 We have two sequential circuits:

Circuit-A → MOD number M.

Circuit-B → MOD number N.

To design a counter of MOD no. MN, we can

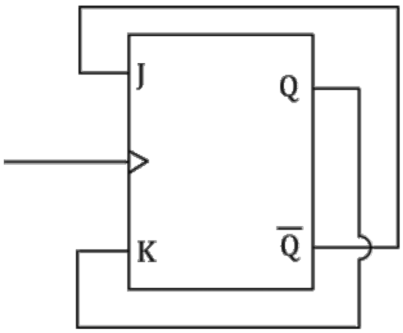
(A) Cascade Circuit-A and Circuit-B

(B) Cascade N Blocks of circuit-A

(C) Cascade M blocks of circuit-B

(D) Cascade circuit A with M blocks of circuit-B.

Q30 Let's consider the circuit given below:



Counter is at Q = 0 initially, then after applying clock pulses the sequence generated at $\overline{Q}$ will be

(A) 1010101010.....

(B) 110011001100.....

(C) 0110001010011...

(D) 01011011101....

Q31 MOD-10 & MOD-20 counters are cascaded to design MOD-200 counter, then minimum number of ffs required is_____.

Q32 An asynchronous counter is designed using 10 FFs having MOD No. 1000. Delay of each FF used is 8 n sec, then for which clock frequencies, counter will work properly.

(A) 12.5 MHz (B) 1.25 MHz

(C) 125 MHz (D) 25 MHz

Q33 We have MOD-8 asynchronous counter, counting in up-sequence. Delay of each FF is t_d. Initially it is at $(011)_2$ and 1-clock is applied then decoding errors that will appear →

(A) $(010)_2$ & $(000)_2$

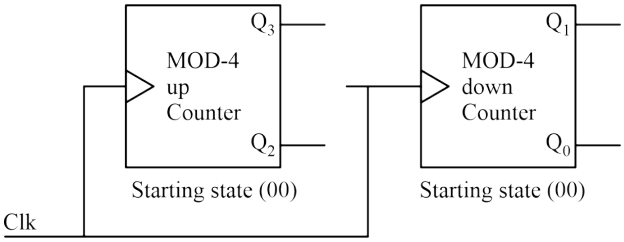
(B) $(000)_2$ & $(101)_2$

(C) $(101)_2$ & $(010)_2$

(D) $(010)_2$& $(110)_2$

Q34 We have a MOD-128 down counter starting with state $(111)_{10}$. After application of 370 clock pulses, counter will be at __$(___)_{10}$___.

Q35 A sequential circuit is as given below:

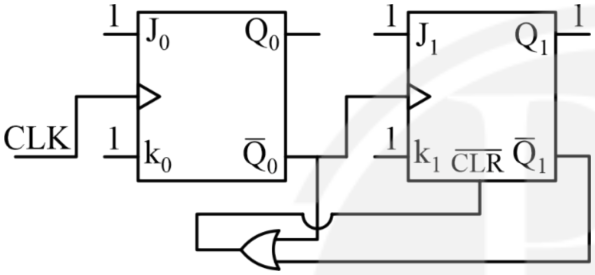


After applying clock pulses, which count sequence will not appear at output $Q_3Q_2\ Q_1Q_0$ is

(A) $(0)_{10}$ (B) $(7)_{10}$

(C) $(10)_{10}$ (D) $(11)_{10}$

Q36 We have sequential circuit as given below:



The above circuit is

(A) MOD-3 counter (B) MOD-2 counter

(C) MOD-4 counter (D) None of these

Q37 MOD-32 up counter has starting state $(00110)_2$ and MOD-16 down counter has starting state $(0110)_2$. Application of 75 clock pulses up counter is in state M and down counter is in state N then value of M + N is ____(__)$_{10}$___.

Q38 Which of the following is true about decoding error in asynchronous counter?

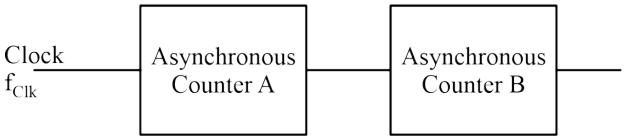
(A) It is removed by using additional signaling

(B) It can be avoided using strobe signal

(C) Decoding error is present in asynchronous as well as in synchronous counter

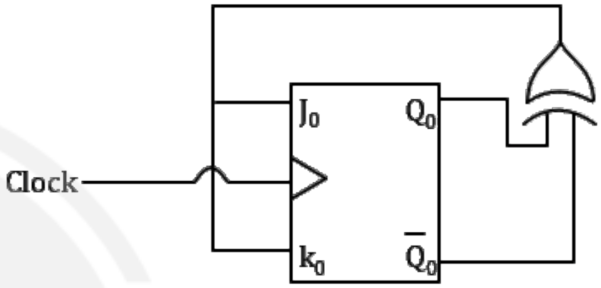
(D) None of these

Q39 A sequential circuit is as given below:



Counter A is MOD-10 up counter and counter B is MOD-24 down counter. FF used in designing has equal delay of t_d = 10 nsec. Then maximum clock frequency value of f_{clk} that can be used to have proper operation of the circuit is ____MHz.

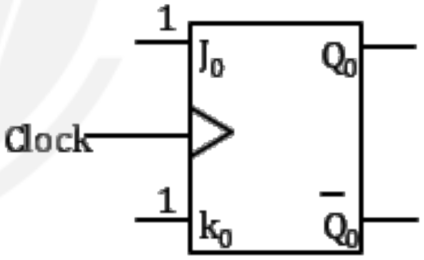
Q40 A sequential circuit is as given below:



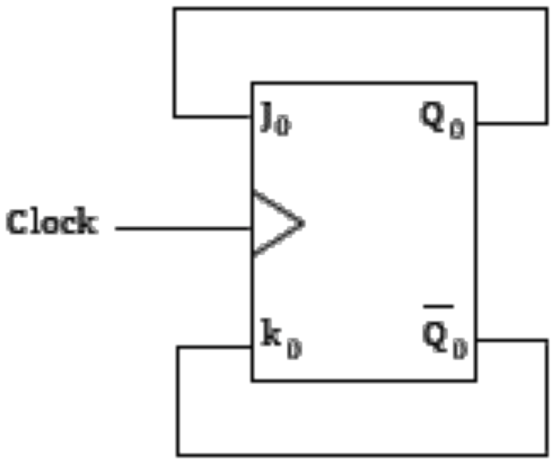
If input clock frequency is 5 MHz, the frequency of output waveform at output Q_0 is _____MHz.

Q41 Which of the following circuit represents toggle mode of operation.

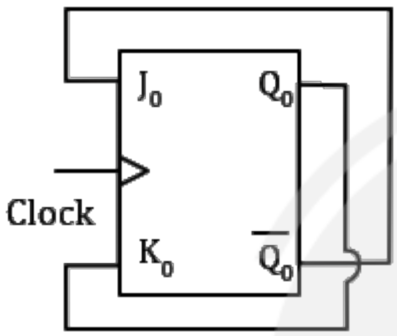
(A)



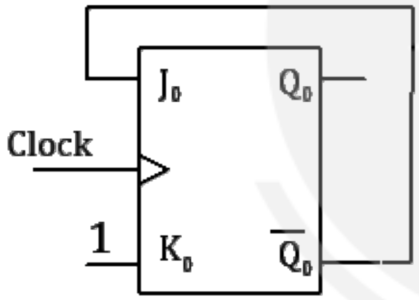
(B)



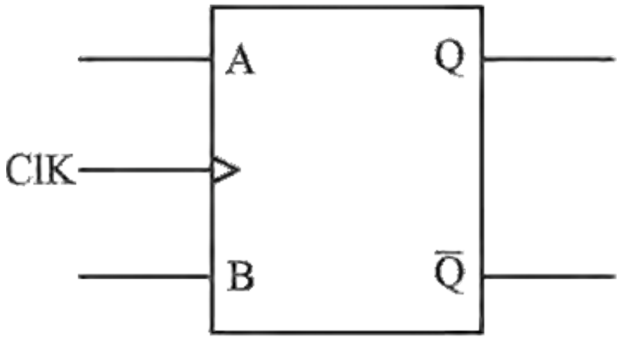
(C)



(D)



Q42 A FF is given as:



Characteristic equation of above FF is $Q(n+1) = A \odot B \oplus Q(n)$

To convert this FF into T-FF, A & B will be:

(A) A = T, B = 1

(B) A = $\overline{T}$, B =1

(C) A = $\overline{T}$, B =0

(D) A =0 B = $\overline{T}$

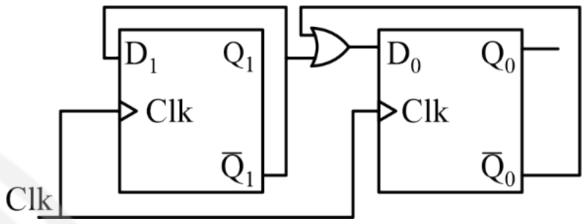
Q43 To convert J-K FF into D-FF, J-K input will be

(A) $J = \overline{D}, K = D$ (B) J = K = D

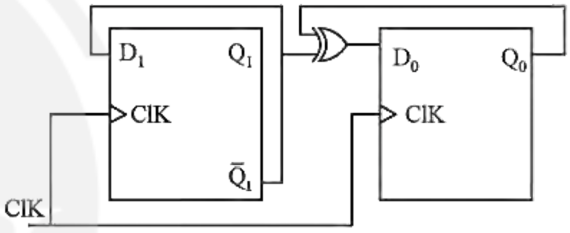
(C) $J = D, K = \overline{D}$ (D) $J = K = \overline{D}$

Q44 To design a counter with counting sequence 0 – 3 – 1 – 2 – 0 the circuit will be

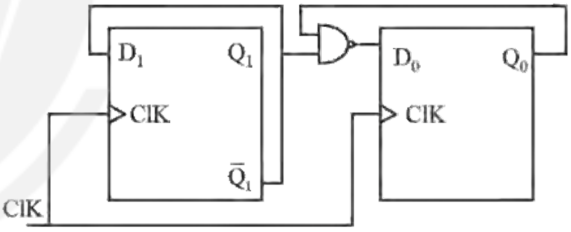
(A)



(B)

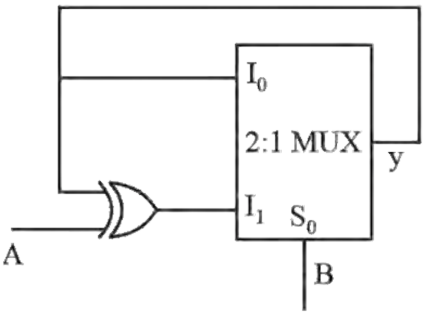


(C)



(D) None of these

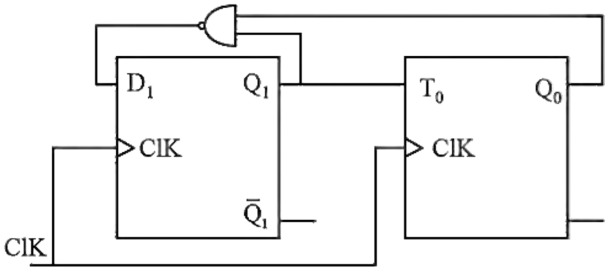
Q45 A circuit is as given below:



Above circuit can work as

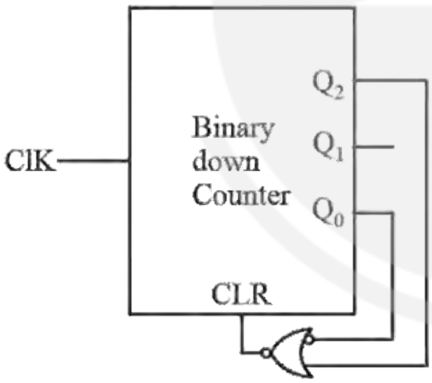
(A) Positive level triggered T-FF.
(B) Negative level triggered T-FF.
(C) Level triggered D-FF.
(D) Edge triggered T-FF

Q46 A circuit is as given below:



Initially FFs are at rest $Q_0Q_1 = (00)_2$, then sequence that will be generated after application of clock pulses:
(A) 00 – 10 – 11 – 00
(B) 00 – 01 – 10 – 11 – 00
(C) 00 – 01 – 11 – 00
(D) 00 – 01 – 11 – 10 – 00

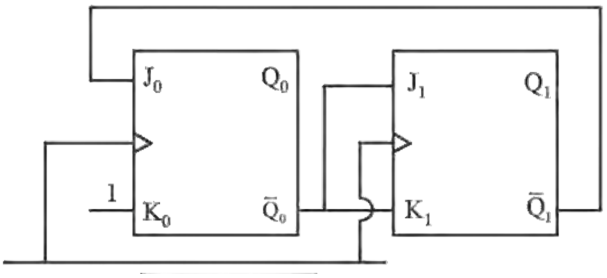
Q47 A sequential circuit is as given below:



Above counter will be
(A) MOD-4 Counter (B) MOD-5 Counter
(C) MOD-2 Counter (D) MOD-6 Counter

Q48 A synchronous counter is designed using D-FFs that generate sequence 0 – 3 – 1 – 2 – 0. FFs used have delay of t_d = 45 nsec and logic gates used has zero delay, then maximum clock frequency that can be used to have proper operation of the circuit is _____ MHz.

Q49 A sequential circuit is as given below:



Initially counter is at $Q_1Q_0 = (11)_2$ then after applying clock next state will be
(A) $(01)_2$ (B) $(10)_2$
(C) $(00)_2$ (D) None of these

Q50 We have a T-FF, to convert it into D-FF, input T must be
(A) $D \odot Q$ (B) $D \oplus Q$
(C) D (D) $\overline{D}$

Q51 We want to design a counter with counting sequence 0 – 1 – 2 – 3 – 0, using
Circuit-A → Asynchronous counter
Circuit-B → Synchronous counter
The used FFs in circuit-A and circuit-B are of same logic family and used logic gates has 0 delay while FFs have delay of 25 nsec. Then which of the following is true?
(A) Maximum clock frequency is same in both the circuits.
(B) Maximum clock frequency is double in circuit-B compared to circuit-A.
(C) Maximum clock frequency is half in circuit-B compared to circuit-A
(D) None of these

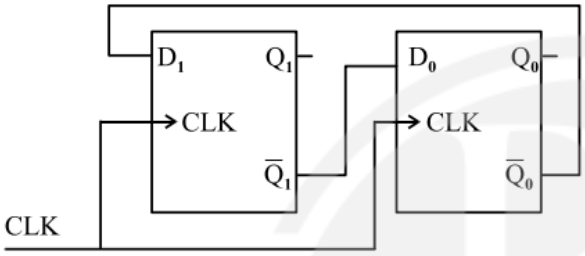
Q52 A counter has to be designed to generate a sequence
$0 - 2 - 2^2 - 2^3 - 2^4 - 2^5 - 2^6$
To design the counter appropriate number of FFs needed is_____.

Q53 Which of the following is true?

(A) Johnson counter has more unused states compared to ring counter
(B) Duty cycle in case of ring counter is 1/2n.
(C) Duty cycle in case of Johnson counter is 1/2n.
(D) MOD no. of Johnson counter = 2 MOD no. of ring counter.

Q54 A 3 – bit ring counter has starting state of $(110)_2$. Duty cycle of the waveform at LSB bit of the counter is _____%

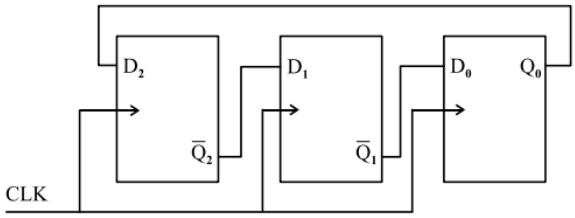
Q55 A sequential CKT is as given below:



Starting state of the counter is $Q_1Q_0 = (10)_2$. Its clock frequency is 5 MHz, then at o/p of Q0 the frequency of the waveform is _____ MHz.

Q56 2-bit Johnson counter generate the sequence: Q_1Q_0[Q_1–MSB, Q_0 – LSB]:
(A) 00–10–11–01–00
(B) 00–11–10–01–00
(C) 00–01–11–00
(D) 00–11–01–10–00

Q57 In a 3-bit Johnson counter, connections are interchanges as given below:

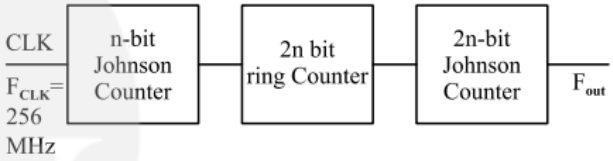


If starting state is $Q_2Q_1Q_0 = (100)_2$, the next state after applying clock will be:
(A) $(110)_2$ (B) $(001)_2$
(C) $(101)_2$ (D) $(000)_2$

Q58 We have a 4-bit ring counter and a 4-bit Johnson counter. No. of unused states in ring counter is m and in Johnson counter is n then the value of (m – n) is _____.

Q59 Which of the following is true?
(A) Decoding circuit of ring counter is more complex compared to ring counter.
(B) Decoding circuit of Johnson counter is more complex compared to asynchronous counter.
(C) Decoding circuit of asynchronous counter is more complex compared to ring counter
(D) None of these

Q60 A sequential CKT is as given below:

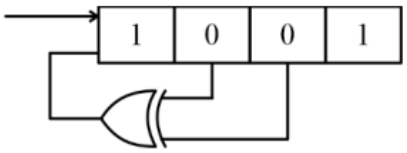


If value of f_{out} = 0.25 MHz, the value of n is __.

Q61 A 2-bit ring counter is cascaded with 3-bit Johnson counter then no. of unused states in cascaded counter will be _____.

Q62 Which of the following is 'not true'?
(A) Johnson counter and asynchronous counter has duty cycle of 50% at each o/p.
(B) Duty cycle in ring counter is always $\leq$ 50%
(C) In Johnson counter, duty cycle is $\geq$ 50%
(D) The synchronous counter with random sequence has duty cycle < 50% or = 50% or > 50%.

Q63 A 4-bit serial-in parallel-out register is connected as shown:



After _____ clock pulses output will be again $(1001)_2$.

Q64 For 8-bit SISO register, to serially out the data from register, number of clock pulses required is

(A) 8 (B) 7

(C) 6 (D) 0

Q65 The order of the speed of registers based on time taken to store the data and time taken to retrieve the stored data is:

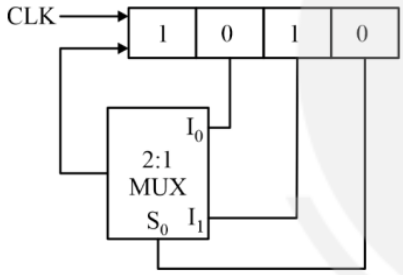
(A) SIPO > SISO > PISO > PIPO

(B) PIPO > SIPO = PISO > SISO

(C) SISO > SIPO = PISO > PIPO

(D) PIPO > PISO > SIPO > SISO

Q66 A SIPO register is connected as shown:

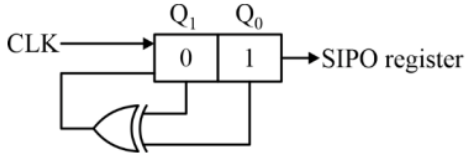


After three clock pulses output of register will be:

(A) $(0010)_2$ (B) $(0101)_2$

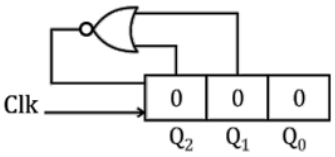
(C) $(0001)_2$ (D) $(1010)_2$

Q67 A sequential circuit is as given below:



Clock pulses are applied to this SIPO register, then duty cycle of the waveform generated at output Q1 is _____ %.

Q68 A 3-bit serial-in parallel-out register is as given below:



Initially the content of SIPO register is asshown above. Then which of the following is true?

(A) After 6-clock pulses output will be again $(000)_2$

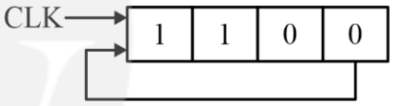
(B) After 3-clock pulses output will be again $(000)_2$

(C) Output will be never $(000)_2$ again

(D) After 8-block pulses output will be again $(000)_2$

Q69 For 8-bit PISO register design, the number of 2 : 1 MUXs required are____.

Q70 A 4-bit SIPO register has starting content of (1100)2 as shown:



All the used FFs are replaced by T-FF then after 2 clock pulses the content of the register will be:

(A) $(1010)_2$ (B) $(1111)_2$

(C) $(0000)_2$ (D) None of these

Q71 SISO register is an example of

(A) Asynchronous circuit (counter)

(B) Synchronous circuit (counter)

(C) Asynchronous circuit as well assynchronous circuit

(D) None of these

Q72 Johnson counter is an example of

(A) Asynchronous counter

(B) Synchronous counter

(C) Asynchronous circuit as well assynchronous circuit

(D) None of these

Answer Key

Q1	(A)
Q2	(A, B)
Q3	(C)
Q4	(B)
Q5	(D)
Q6	(B)
Q7	(A)
Q8	(B)
Q9	(A)
Q10	(D)
Q11	(B)
Q12	1
Q13	2.75
Q14	(C)
Q15	(B)
Q16	(C)
Q17	(C)
Q18	7
Q19	(C)
Q20	2048
Q21	8
Q22	(C)
Q23	24
Q24	(C)
Q25	3
Q26	41.67
Q27	(D)
Q28	(D)
Q29	(B)
Q30	(A)
Q31	9
Q32	(A, B)
Q33	(A)
Q34	125
Q35	(D)
Q36	(B)
Q37	28
Q38	(B)
Q39	11.11
Q40	2.5
Q41	(A, C, D)
Q42	(A, C, D)
Q43	(C)
Q44	(B)
Q45	(A)
Q46	(C)
Q47	(B)
Q48	22.22
Q49	(B)
Q50	(B)
Q51	(B)
Q52	7
Q53	(D)
Q54	(66.67)

Q55 0

Q56 (A)

Q57 (B)

Q58 4

Q59 (C)

Q60 4

Q61 20

Q62 (C)

Q63 7

Q64 (B)

Q65 (B)

Q66 (C)

Q67 (66.67)

Q68 (C)

Q69 7

Q70 (B)

Q71 (B)

Q72 (B)

Hints & Solutions

Q1 Text Solution:
(A)

Q2 Text Solution:
(A, B)

Q3 Text Solution:
(C)

Q4 Text Solution:
(B)

Q5 Text Solution:
(D)

Q6 Text Solution:
(B)

Q7 Text Solution:
(A)

Q8 Text Solution:
(B)

Q9 Text Solution:
(A)

Q10 Text Solution:
(D)

Q11 Text Solution:
(B)

Q12 Text Solution:
(1)

Q13 Text Solution:
(2.75)

Q14 Text Solution:
(C)

Q15 Text Solution:
(B)

Q16 Text Solution:
(C)

Q17 Text Solution:
(C)

Q18 Text Solution:
(7)

Q19 Text Solution:
(C)

Q20 Text Solution:
(2048)

Q21 Text Solution:
(8)

Q22 Text Solution:
(C)

Q23 Text Solution:
(24)

Q24 Text Solution:
(C)

Q25 Text Solution:
(3)

Q26 Text Solution:
(41.67)

Q27 Text Solution:
(D)

Q28 Text Solution:
(D)

Q29 Text Solution:
(B)

Q30 Text Solution:
(A)

Q31 Text Solution:
(9)

Q32 Text Solution:

(A, B)

Q33 Text Solution:
(A)

Q34 Text Solution:
(125)

Q35 Text Solution:
(D)

Q36 Text Solution:
(B)

Q37 Text Solution:
(28)

Q38 Text Solution:
(B)

Q39 Text Solution:
(11.11)

Q40 Text Solution:
(2.5)

Q41 Text Solution:
(A, C, D)

Q42 Text Solution:
(A, C, D)

Q43 Text Solution:
(C)

Q44 Text Solution:
(B)

Q45 Text Solution:
(A)

Q46 Text Solution:
(C)

Q47 Text Solution:
(B)

Q48 Text Solution:
(22.22)

Q49 Text Solution:
(B)

Q50 Text Solution:
(B)

Q51 Text Solution:
(b)

Q52 Text Solution:
7

Q53 Text Solution:
(d)

Q54 Text Solution:
(66.67)

Q55 Text Solution:
0

Q56 Text Solution:
(a)

Q57 Text Solution:
(b)

Q58 Text Solution:
4

Q59 Text Solution:
(c)

Q60 Text Solution:
4

Q61 Text Solution:
20

Q62 Text Solution:
(c)

Q63 Text Solution:
7

Q64 Text Solution:
(b)

Q65 Text Solution:
(b)

Q66 Text Solution:

(c)

Q67 Text Solution:
(66.67)

Q68 Text Solution:
(c)

Q69 Text Solution:
7

Q70 Text Solution:
(b)

Q71 Text Solution:
(b)

Q72 Text Solution:
(b)