PRACTICE SHEET-1

Computer Science & Information Technology
Digital Logic
Combinational Circuit

Q1 Which of the following is true?

(A) All gates follow commutative as well as associative law.

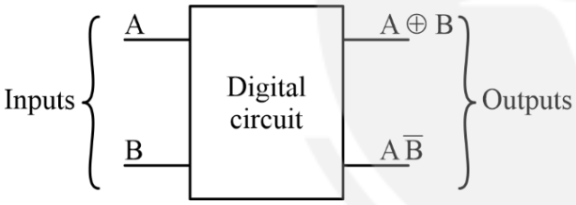
(B) NOR & XNOR do not follow associative law

(C) NAND & XOR do not follow associative law

(D) All gates follow commutative law, but some gates do not follow associative law.

Q2 We have to implement half adder as well as half subtractor. The minimum number of 2-i/P NAND gate required is _____.

Q3 A digital circuit is as given below:

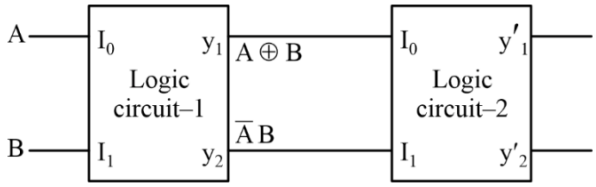


This circuit implements:

(A) A + B (B) A – B

(C) B – A (D) None of these

Q4 A logical circuit is as given below:



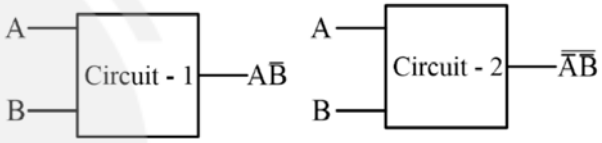
Function of logic circuit – 1 & logic circuit – 2 is same. The output y'_1 will be

(A) $A \oplus B$ (B) $A\overline{B}$

(C) $\overline{A}B$ (D) $A - B$

Q5 We have two numbers A and B and both are 4-bit numbers. To perform complete addition of these two numbers, total number of H.A.s + OR gate required is _____.

Q6 Which of the following circuits can be used as universal circuit:



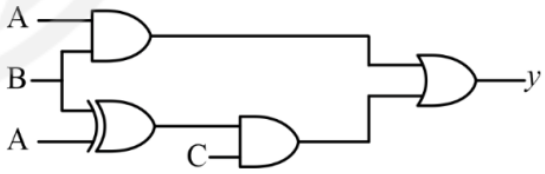
(A) circuit – 1 and circuit – 2 both

(B) circuit – 1 only

(C) circuit – 2 only

(D) Neither circuit – 1 nor circuit – 2

Q7 A logical circuit is implemented as:



Output y is

(A) '1' when majority of the i/P_s A, B, C are at '1'

(B) '0' when minority of the i/P_s A, B, C are at '1'

(C) '1' when minority of the i/P_s A, B, C are at '1'

(D) '0' when majority of the i/P_s A, B, C are at '1'

Q8 x, y, z are i/P_s of a full adder then, sum output of full adder will be '1' if

(A) $\bar{x}\,\bar{y} + \bar{y}\,\bar{z} + \bar{z}\,\bar{x} = 1$

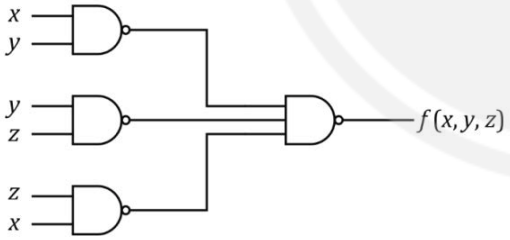
(B) xyz = 1
(C) (x + y) (y + z) (z + x) = 0
(D) None of these

Q9 Which of the following is/are true?
(A) NOR gate is equivalent to NAND gate with bubbled i/P_s
(B) OR gate is equivalent to NAND gate with bubbled i/P_s
(C) AND gate is equivalent to NOR gate with bubbled i/P_s
(D) NAND gate is equivalent to NOR gate with bubbled i/P_s

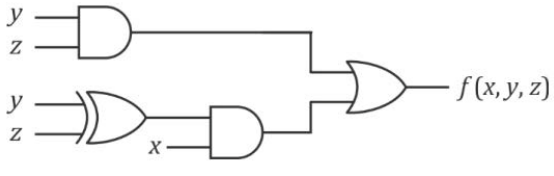
Q10 We have to implement H.A circuit & full adder circuit together. I/P lines for H.A. is x, y and i/P lines for full adder is x, y, z then minimum number of 2 – i/P NAND gate required is _____.

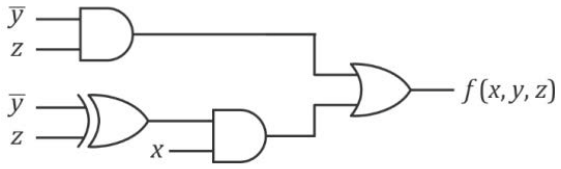
Q11 We have a 4-bit adder in which each full adder has sum delay of t_s = 4 nsec and carry delay of 2 nsec. In one minute number of additions completed by this full adder is _____ × 10^9.

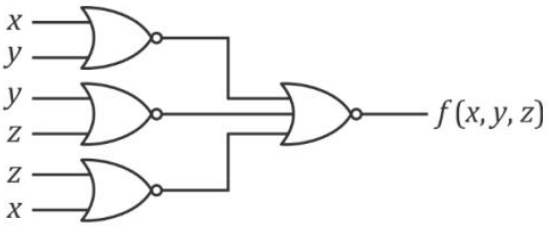
Q12 A logical circuit is as given below:

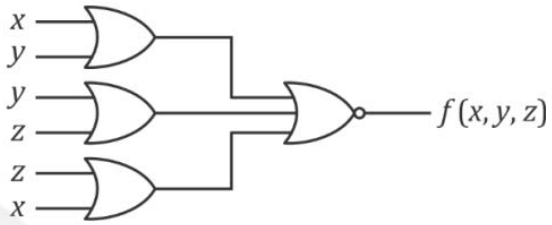


Which of the following circuit is/are equivalent to the above circuit:

(A)


(B)


(C)


(D)


Q13 A K-map is as given below:

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{x}$	1	1		1
x		1	1	

In minimized solution of above K-map, there are terms x y, x z and one term is missing. The missing term is
(A) $\bar{y}z$
(B) xz
(C) $\bar{x}z$
(D) $\bar{x}\,\bar{z}$

Q14 A K-Map is as given below:

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{x}$	1	1		X
x	X		1	1

Its minimized solution will be
(A) $x \odot y$

(B) $x \oplus y$
(C) $\bar{z} + \bar{x}\,\bar{y}$
(D) $\bar{z} + xy + \bar{x}\,\bar{y}$

Q15 $F(x, y, z) = \overline{\overline{x\bar{y}} + \overline{\bar{x}y}} + x\bar{y}z + x\,\overline{yz}$
Then the minimized solution of f(x,y,z) will be
(A) $x + \bar{y}$ (B) $\bar{x}y$
(C) $xy\,\bar{z}$ (D) $x + \bar{y} + z$

Q16 In a 4-bit parallel adder, sum delay and carry delay of each full adder is t_s = 1 nsec and t_c = 5 nsec respectively. No. of additions performed per sec by adder is N_1. If delays are interchanged then no. of additions performed per sec is N_2, then N_2/N_1 _____.

Q17 A K-map is as given below:
Then minimized solution of K-map is:

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	
$\bar{A}B$	1	1	1	X
$A\bar{B}$			1	
AB		X	X	

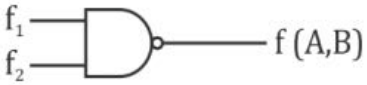
(A) $\bar{A}\bar{C} + \bar{A}D + CD$
(B) $\bar{A}\bar{C} + CD$
(C) $\bar{A}B + CD + \bar{A}\bar{C}$
(D) None of these

Q18 K-map of two logical functions f_1 (A, B) and f_2 (A, B) is as given below:

f_1	$\bar{B}$	B
$\bar{A}$	1	
A		1

f_1	$\bar{B}$	B
$\bar{A}$	1	1
A		

Then K-map of f (A, B) will be



(A)

f	$\bar{B}$	B
$\bar{A}$	1	1
A		1

(B)

f	$\bar{B}$	B
$\bar{A}$		1
A	1	1

(C)

f	$\bar{B}$	B
$\bar{A}$	1	1
A		

(D)

f	$\bar{B}$	B
$\bar{A}$		1
A	1	

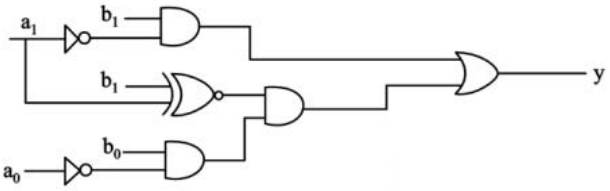
Q19 f (A, B, C, D) is as given below:
$f(A, B, C, D) = \overline{\bar{B}D + AC + \bar{A}B} + ABCD + \bar{A}BC + ABC$
Then no. of entries in K-map of f (A, B, C, D) that are filled with '1' are_____.

Q20 f (x, y, z) is given as: $f(x,y,z) = \bar{x}\bar{y} + \bar{x}z + zy$, The equivalent f (x, y, z) can also be
(A) $(\bar{x} + y + \bar{z})(x + \bar{y} + \bar{z})(x + \bar{y} + z)$
(B) $(x + \bar{y} + z)(\bar{x} + y + z)(\bar{x} + y + \bar{z})$
(C) $(\bar{x} + \bar{y})(\bar{x} + z)(x + y)$
(D) None of these

Q21 Which of the following is true?
(A) K-map has more than one solution.
(B) K-map always has unique solution.
(C) K-map can have more than one solution.
(D) None of these

Q22 A & B are two-bit numbers as
$A = a_1a_0$ and $B = b_1b_0$
Then no. of combination in which A > 2B are _____.

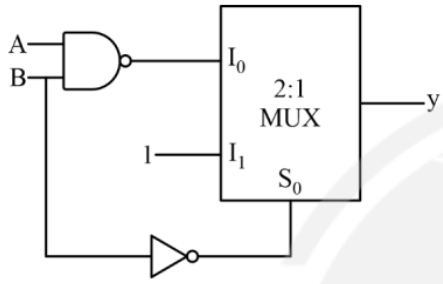
Q23 A digital circuit is as given below:



Input lines of the circuit are a_1, b_1, a_0, b_0 and output line is y.

Then no. of combinations of input lines in which output y will be '1'are _____.

Q24 A MUX circuit is as given below:



Output y is

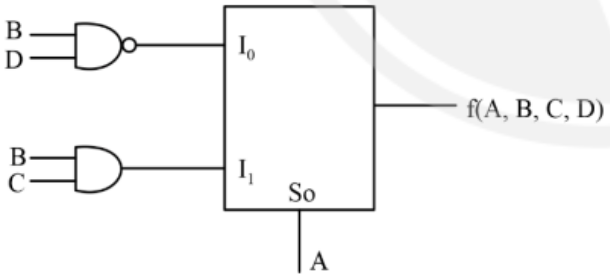
(A) $\overline{A} + \overline{B}$

(B) $\overline{A + B}$

(C) $A \oplus B$

(D) $A\overline{B}$

Q25 A MUX circuit is as given below:



f(A, B, C, D) is:

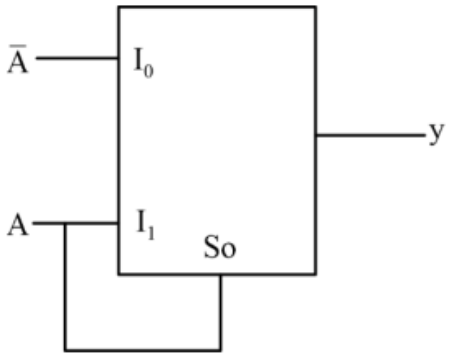
(A) Σ (0, 1, 2, 3, 4, 5, 6, 14, 15)

(B) Σ (0, 1, 2, 3, 4, 6, 13, 15)

(C) Σ (0, 1, 2, 3, 4, 6, 14, 15)

(D) Σ (1, 2, 3, 4, 5, 6, 7, 13, 14, 15)

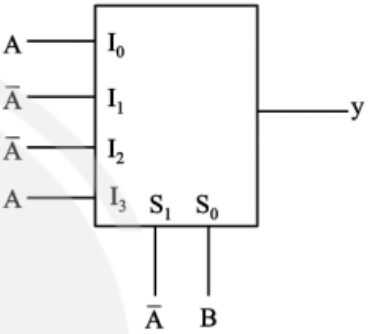
Q26 A MUX circuit is as given below, output y is



(A) $\overline{A}$ (B) A

(C) 0 (D) 1

Q27 A 4:1 MUX is given as:

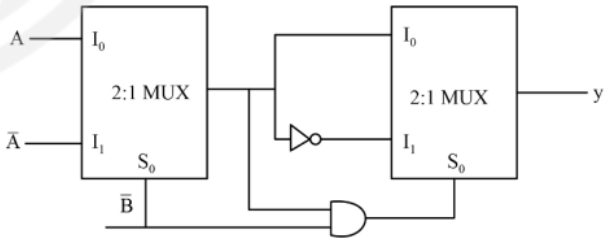


Output y is

(A) $\overline{B}$ (B) B

(C) $A \oplus B$ (D) $A \odot B$

Q28 A combinational circuit is designed using MUX as shown below: -

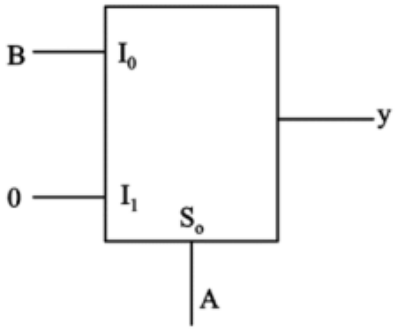


output y is

(A) $\overline{A + B}$ (B) $A.B$

(C) $A \oplus B$ (D) $A \odot B$

Q29 A MUX circuit is implemented as shown:



output y represents

(A) Comparator output when B < A

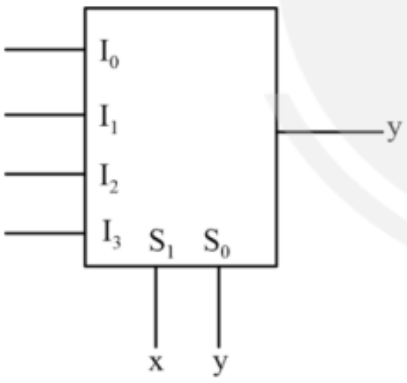
(B) Comparator output when B = A

(C) Comparator output when B > A

(D) Comparator output when B < 2A

Q30 In a full subtractor the corresponding input bits of two numbers are x & y [x – y] and input borrow is z and output borrow is B. Output borrow is implemented as shown.

The values of I_0, I_1, I_2 & I_3 are:



(A) $I_0 = z$, $I_1 = 1$, $I_2 = 0$, $I_3 = z$

(B) $I_0 = z$, $I_1 = 0$, $I_2 = 1$, $I_3 = \overline{z}$

(C) $I_0 = 1$, $I_1 = z$, $I_2 = 0$, $I_3 = z$

(D) $I_0 = \bar{z}$, $I_1 = 1$, $I_2 = 0$, $I_3 = z$

Q31 To implement 1024 : 1, the required 4 : 1 MUXs are _____.

Q32 Which of the following is true:

(A) MUX is non-universal circuit.

(B) MUX can be used to implement half adder as well as full adder.

(C) 2:1 MUX has 1–input line, 1–output line and 2-select line

(D) If in a MUX input lines are 24 then minimum 4-select lines are required for proper functioning.

Q33 Which of the following is true:

(A) Decoder and MUX have same internal circuitry

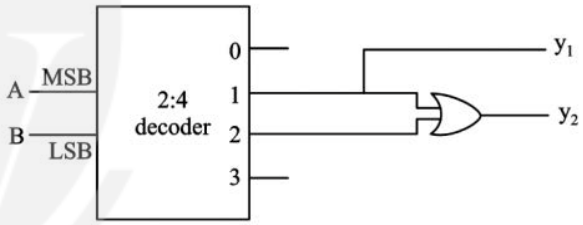
(B) MUX & De MUX have same internal circuitry

(C) De MUX and decoder have same internal circuitry

(D) None of these

Q34 A combinational circuit using decoder and OR gate is as given below:

o/p y_1 & y_2 combinedly represents:



(A) Half adder

(B) Half subtractor with subtraction (B–A)

(C) Half subtractor with subtraction (A–B)

(D) Comparator o/p with (A > B)

Q35 To implement 1 : 512 De MUX, we require N, 1:8 De MUX, then the value of N is _____.

Q36 To implement 1:128 De MUX, we require

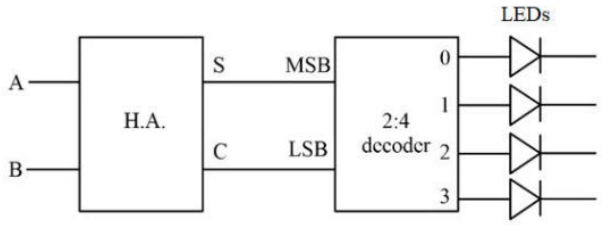
(A) 127 – 1:4 DeMUX

(B) 127 – 1:2 DeMUX

(C) 18 – 1:8 DeMUX & 1 – 1:2 DeMUX

(D) 40 – 1:8 DeMUX & 1 – 1:2 DeMUX

Q37 A combinational circuit is as given below. When input is A = 0 & B = 1, then LED no. that glows will be_____.

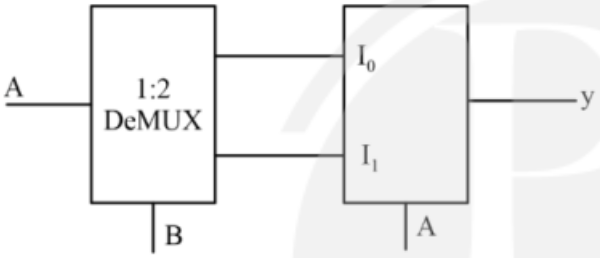


Q38 For a decoder having 4 input lines, no. of output lines are

(A) 1 (B) 2

(C) 16 (D) 4

Q39 A digital circuit is as given below:



Output y is

(A) A (B) B

(C) A.B (D) (A + B)

Q40 Which of the following is 'not true'?

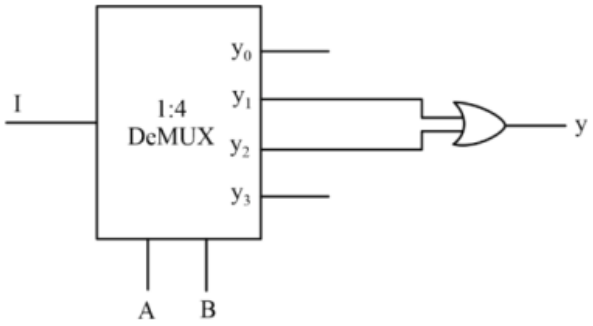
(A) DeMUX is not a universal circuit

(B) For 52 output lines, no. of select lines must be atleast 6 for DeMUX.

(C) DeMUX is parallel to serial converter.

(D) DeMUX is serial to parallel converter

Q41 A circuit is as shown below:



(A) $A \oplus B$ if $I = 1$

(B) $A \odot B$ if $I = 0$

(C) $A.B$ if $I = 1$

(D) A + B if I = 0

Q42 For implementing full adder and full subtractor we require a decoder of the order n : M, where n is no. of input lines & M is no. of output lines, then value of M is _____.

Q43 It is given that:

$x_1 \odot x_2 \odot x_3 \odot x_4 = 0$

Then which of the following is true?

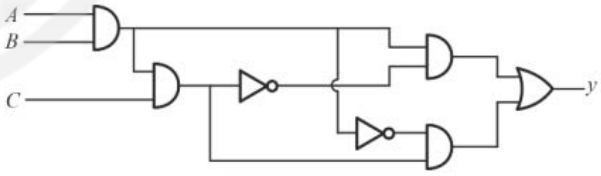
(A) $x_1 x_2 + x_3 x_4 = 1$

(B) $x_1 \oplus x_2 + x_2 \oplus x_3 + x_3 \oplus x_4 = 1$

(C) $x_1x_2\ x_3x_4 = 0$

(D) $\overline{x_1 x_2} + x_2 x_3 + \overline{x_3 x_4} = 1$

Q44 A digital circuit is as given below:



Output y is

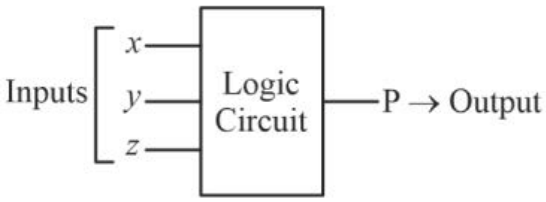
(A) $AB\overline{C}$

(B) $A \oplus B \oplus C$

(C) $A \odot B \oplus C$

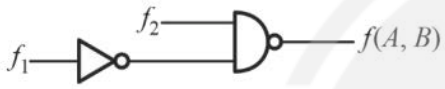
(D) $\overline{A + B + C}$

Q45 A circuit is designed as shown:



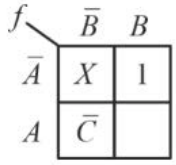
Output P is 1 when majority of input lines are '0'.
Output is
(A) xy + yz + zx
(B) $\bar{x}\,\bar{y} + \bar{y}\;\bar{z} + \bar{z}\,\bar{x}$
(C) $\overline{x + y + z}$
(D) $\overline{xy + yz}$

Q46 Two logical functions:
f_1 (A, B) = Σ (1, 2)
f_2(A, B) = Σ (0, 1, 3)
then output f(A, B) will be



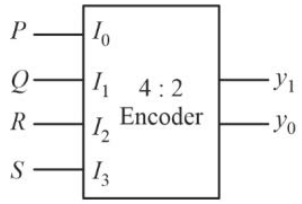
(A) Σ (1, 2)
(B) Σ (0, 1, 3)
(C) Σ (0, 1, 2, 3)
(D) Σ (1)

Q47 A K-Map is as given below:



Its simplified solution will be
(A) $(\overline{A} + \overline{B})\overline{C}$
(B) $(\overline{A} + \overline{B})(\overline{A} + \overline{C})$
(C) $\overline{AB} + \overline{BC}$
(D) None of these

Q48 A 4 : 2 Encoder is as given below:



Output y_1 will be
(A) (P + Q)
(B) (Q + R)
(C) (R + S)
(D) (P + S)

Q49 Which of the following is not true?
(A) $\overline{A} + \overline{B}C = (A + \overline{B})(\overline{B} + C)$
(B) $\overline{A} + \overline{B}C = \overline{AB} \cdot (\overline{A} + C)$
(C) $AB + AC + \overline{B}C = AB + \overline{B}C$
(D) AB + BC + AC = (A + B) (B + C) (C + A)

Q50 For n-variable, the number of self dual functions are found to be 256, then the value of n is_____.

Q51 To add two 5-bit numbers, we required m H.A.s and n-OR gates then minimum value of (m + n) is _____.

Q52 Two stage SOP circuit can directly be implemented
(A) Using NAND gates at first stage & AND gate at second stage.
(B) Using NAND gates only at both first & second stage.
(C) Using AND gates only at both first & second stage.
(D) Using NOR gates only at both stages.

Answer Key

Q1	(D)
Q2	6
Q3	(C)
Q4	(B)
Q5	(10)
Q6	(B)
Q7	(A, B)
Q8	(D)
Q9	(B, C)
Q10	10
Q11	6
Q12	(A, C)
Q13	(B)
Q14	(A)
Q15	(A)
Q16	2.5
Q17	(B)
Q18	(B)
Q19	8
Q20	(B)
Q21	(C)
Q22	4
Q23	6
Q24	(A)
Q25	(C)
Q26	(D)
Q27	(A)
Q28	(B)
Q29	(C)
Q30	(A)
Q31	341
Q32	(B)
Q33	(C)
Q34	(C)
Q35	73
Q36	(B, C)
Q37	2
Q38	(C)
Q39	(C)
Q40	(C)
Q41	(A)
Q42	8
Q43	(C)
Q44	(A)
Q45	(B)
Q46	(B)
Q47	(B)
Q48	(C)
Q49	(A)
Q50	4
Q51	13
Q52	(B)

Hints & Solutions

Q1 Text Solution:
(d)

Q2 Text Solution:
6

Q3 Text Solution:
(c)

Q4 Text Solution:
(b)

Q5 Text Solution:
(10)

Q6 Text Solution:
(b)

Q7 Text Solution:
(a, b)

Q8 Text Solution:
(d)

Q9 Text Solution:
(b, c)

Q10 Text Solution:
10

Q11 Text Solution:
6

Q13 Text Solution:
(b)

Q14 Text Solution:
(a)

Q15 Text Solution:
(a)

Q16 Text Solution:
2.5

Q17 Text Solution:
(b)

Q18 Text Solution:
(b)

Q19 Text Solution:
8

Q20 Text Solution:
(b)

Q21 Text Solution:
(c)

Q22 Text Solution:
4

Q23 Text Solution:
6

Q24 Text Solution:
(a)

Q25 Text Solution:
(c)

Q26 Text Solution:
(d)

Q27 Text Solution:
(a)

Q28 Text Solution:
(b)

Q29 Text Solution:
(c)

Q30 Text Solution:
(a)

Q31 Text Solution:
341

Q32 Text Solution:
(b)

Q33 Text Solution:

(c)

Q34 Text Solution:
(c)

Q35 Text Solution:
73

Q36 Text Solution:
(b, c)

Q37 Text Solution:
2

Q38 Text Solution:
(c)

Q39 Text Solution:
(c)

Q40 Text Solution:
(c)

Q41 Text Solution:
(a)

Q42 Text Solution:
8

Q43 Text Solution:
(c)

Q44 Text Solution:
(a)

Q45 Text Solution:
(b)

Q46 Text Solution:
(a)

Q47 Text Solution:
(b)

Q48 Text Solution:
(c)

Q49 Text Solution:
(a)

Q50 Text Solution:
4

Q51 Text Solution:
13

Q52 Text Solution:
(b)