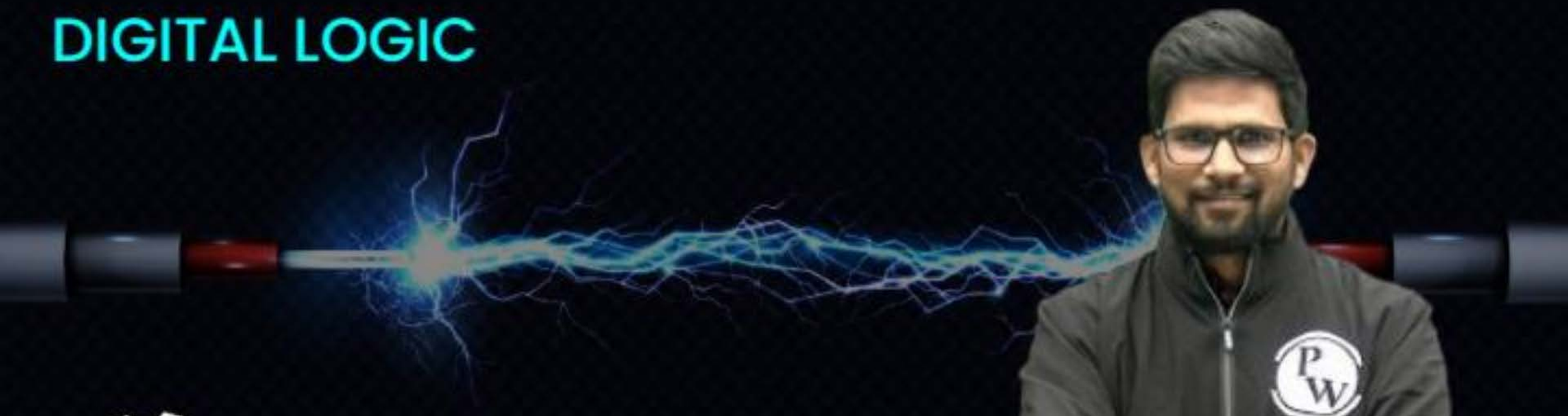
COMPUTER SCIENCE & IT

DIGITAL LOGIC



Lecture No: 01

Sequential Circuit

By- Chandan Gupta Sir

Recap of Previous Lecture

- Decoder & Encoder
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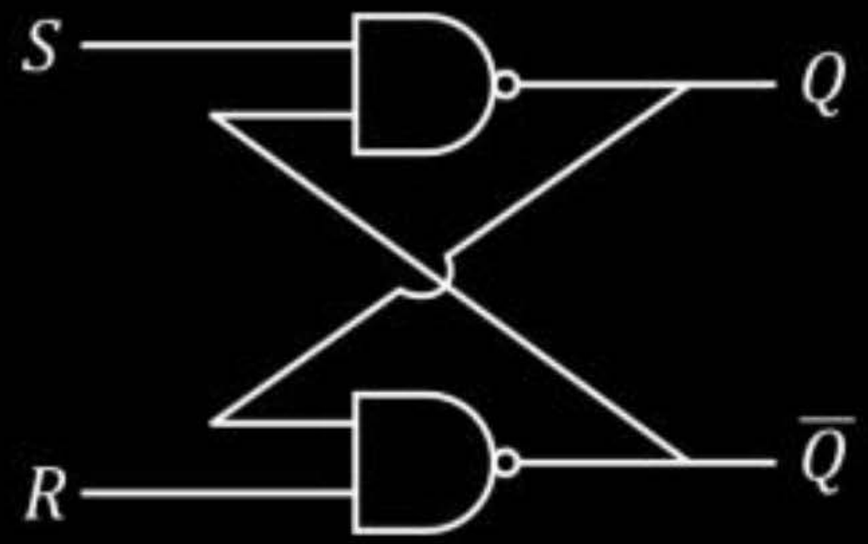
S-R latch

Sequential Circuit → O/P depends on present and past i/p values.

- Basic element of sequential circuit ?
  - → SR latch

S-R Latch :

SR latch using NAND gate :



S	R	Q(n+1)
0	0	invalid state
0	1	1
1	0	0
1	1	Q(n) → hold state

→ Working :

$S=0,\ R=1 \qquad Q(n)=?\ \longrightarrow\ Q(n+1)=1$

$S=1,\ R=1 \qquad Q(n)=1\ \longrightarrow\ Q(n+1)=1$

$S=1,\ R=0, \qquad Q(n)=1\ \longrightarrow\ Q(n+1)=0$

$S=1,\ R=1 \qquad Q(n)=0\ \longrightarrow\ Q(n+1)=0$

$S=0,\ R=1, \qquad Q(n)=0\ \longrightarrow\ Q(n+1)=1$

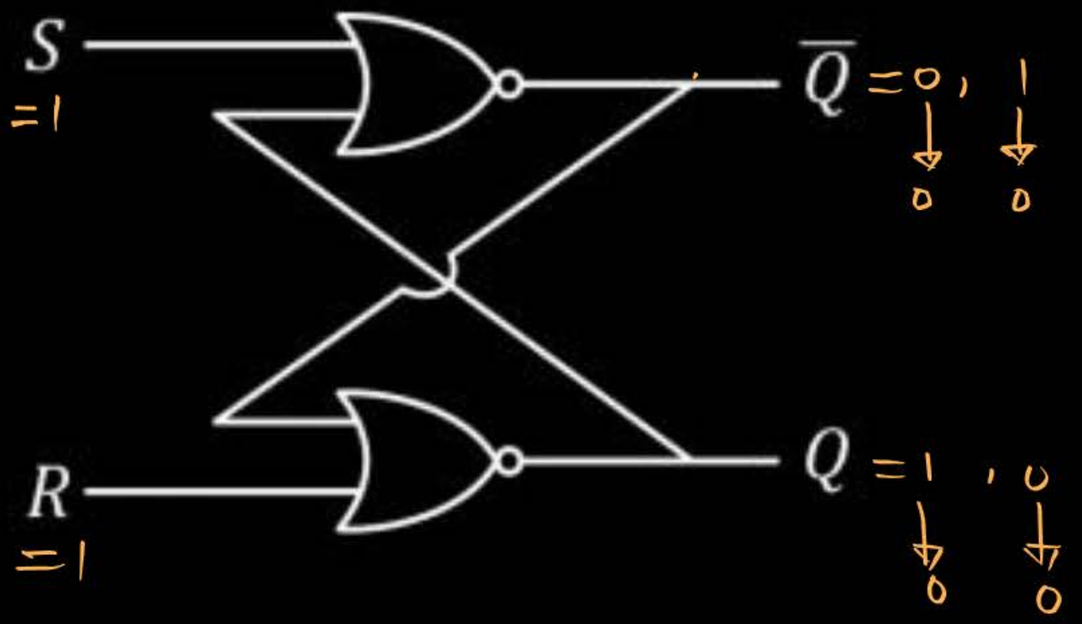
- Concept of present state and next state :

S	R	$Q(n+1)$
0	0	invalid
0	1	1
1	0	0
1	1	$Q(n)$

- Invalid inputs :

$S=0$, $R=0$ generates same value of Q & $\bar{Q}$ and therefore they are invalid input state and will be never used on input side

SR latch using NOR gate :



S	R	Q(n+1)
0	0	Q(n) → hold state
0	1	0
1	0	1
1	1	invalid state

→ Working :

- Truth Table :

S	R	$Q(n+1)$
0	0	$Q(n)$
0	1	0
1	0	1
1	1	invalid state

$S=0, R=1, Q(n)=?$ $Q(n+1)=0$

$S=0, R=0, Q(n)=0, Q(n+1)=0$

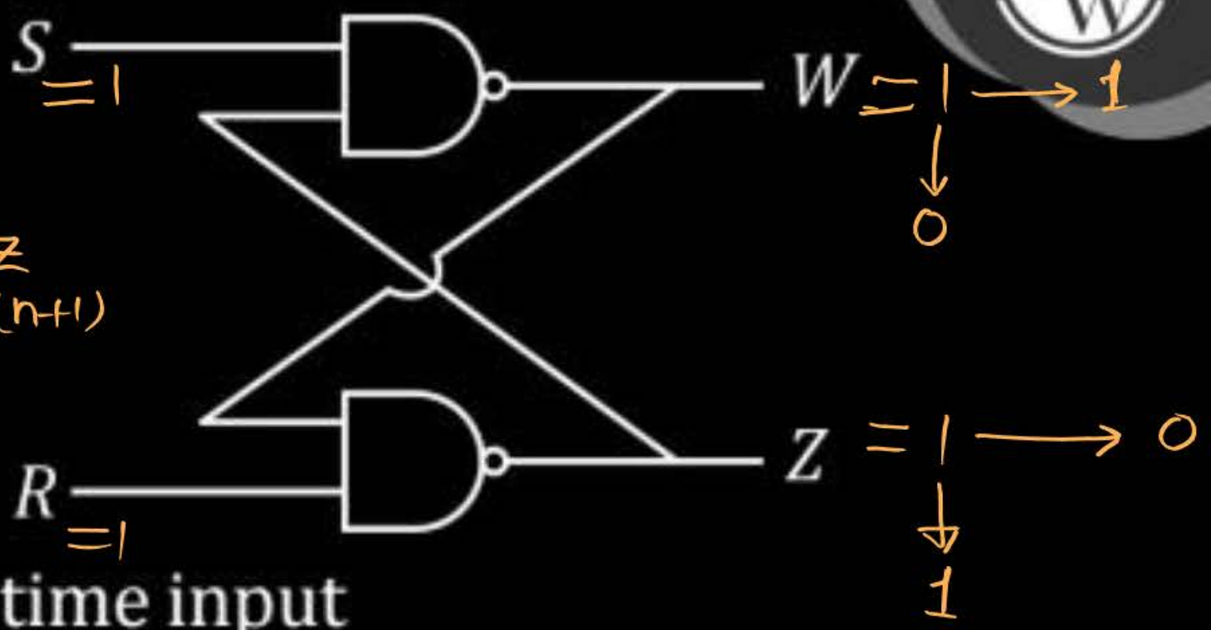
$S=1, R=0, Q(n)=0, Q(n+1)=1$

$S=0, R=0, Q(n)=1, Q(n+1)=1$

- Invalid states : $S=1, R=1$ is invalid state input because it generates output such that Q & $\bar{Q}$ becomes same which is contradictory to design of latch.

Question

A NAND latch circuit is given below :



$S=0, R=0, Q(n)=?, Q(n+1)=1, \overline{Q}(n+1)=1$

$S=1, R=1, Q(n)=1, \overline{Q}(n)=1 \longrightarrow Q(n+1), \overline{Q}(n+1)$ (W, Z)

Initially input $S = R = 0$ and after sometime input changes from $S = R = 0$ to $S = R = 1$ then

(a) Output changes from $W = Z = 1$ to $W = Z = 1$.

(b) Output changes from $W = Z = 1$ to either W = 1 and Z = 0 or W = 0 and Z = 1

(c) Output changes from $W = Z = 1$ to $W = Z = 0$

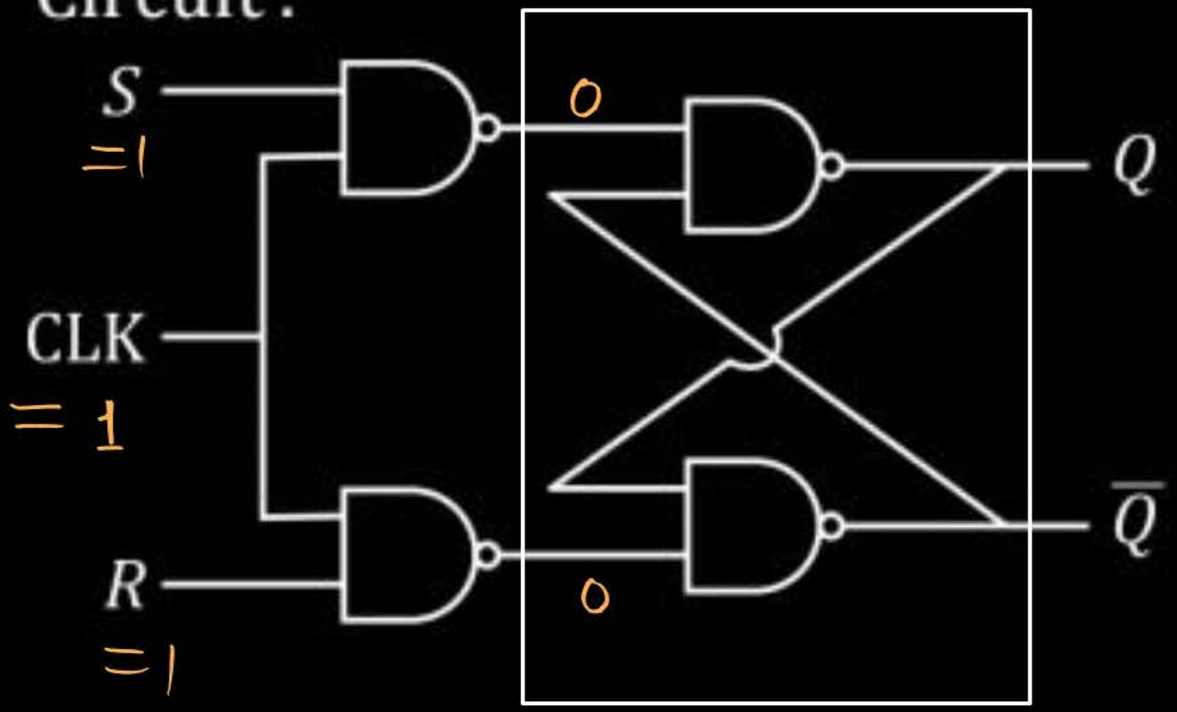
(d) None of these

- IMP Points :

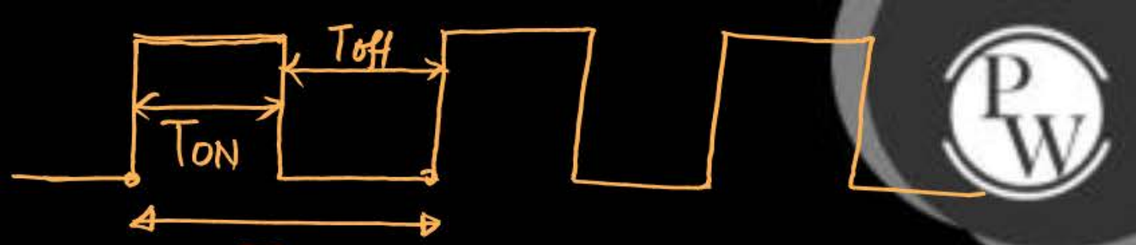
Hold state i/p [NAND or NOR latch] will hold the present o/p in the next o/p if only if present output is a valid state [Q & $\overline{Q}$ should be complement each other]. If present o/p state will be invalid o/p state [Q & $\overline{Q}$ are same] then in next o/p, o/p will go to any of the valid state (1, 0) or (0, 1).

S-R Flip-Flop

- Circuit :



+ve level triggered FF



$T_{clk} = T_{ON} + T_{off}$

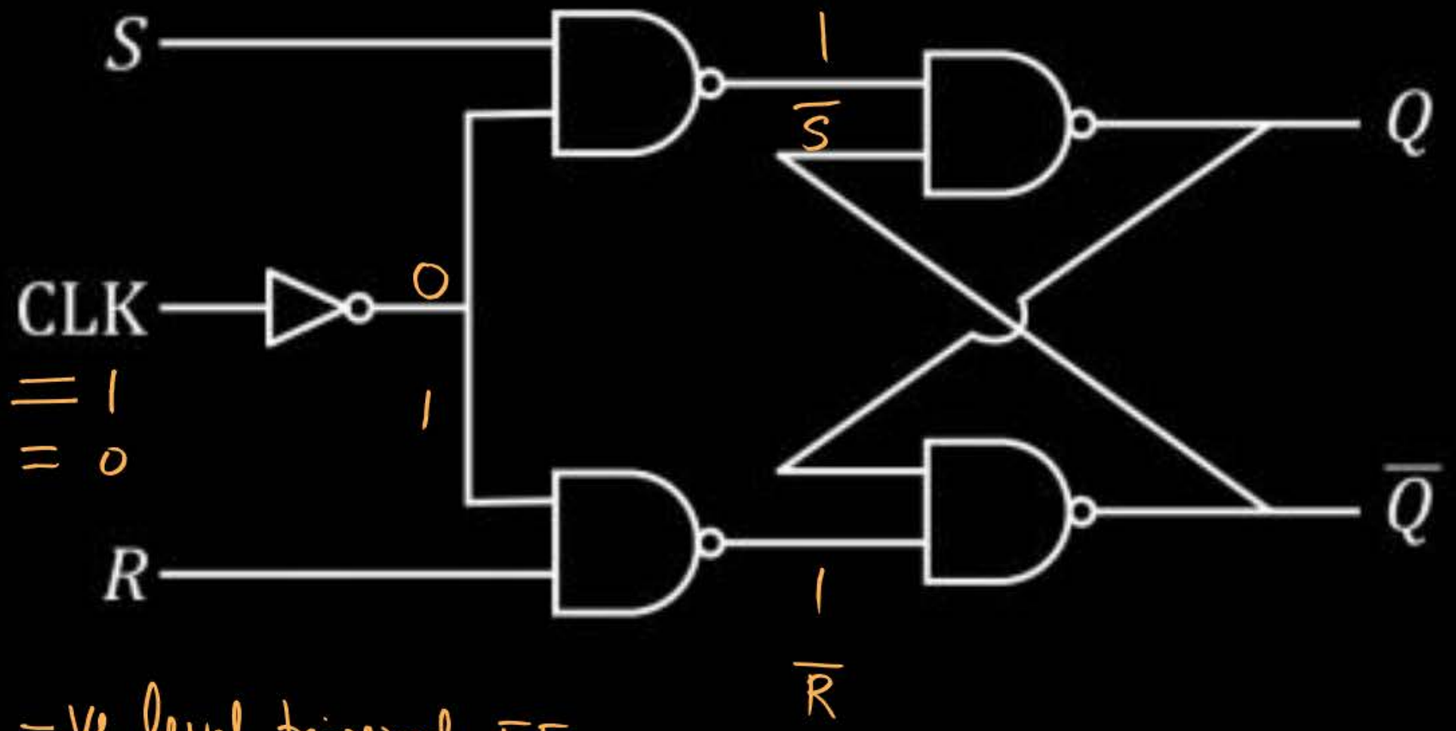
$\%\ \text{duty cycle} = \frac{T_{ON}}{T_{ON}+T_{off}} \times 100\%$

$= \frac{T_{ON}}{T_{clk}} \times 100\%$

- Truth Table :

CLK	S	R	$Q(n+1)$
0	X	X	Q(n)
1	0	0	Q(n)
1	0	1	0
1	1	0	1
1	1	1	invalid state

If circuit is changed to :



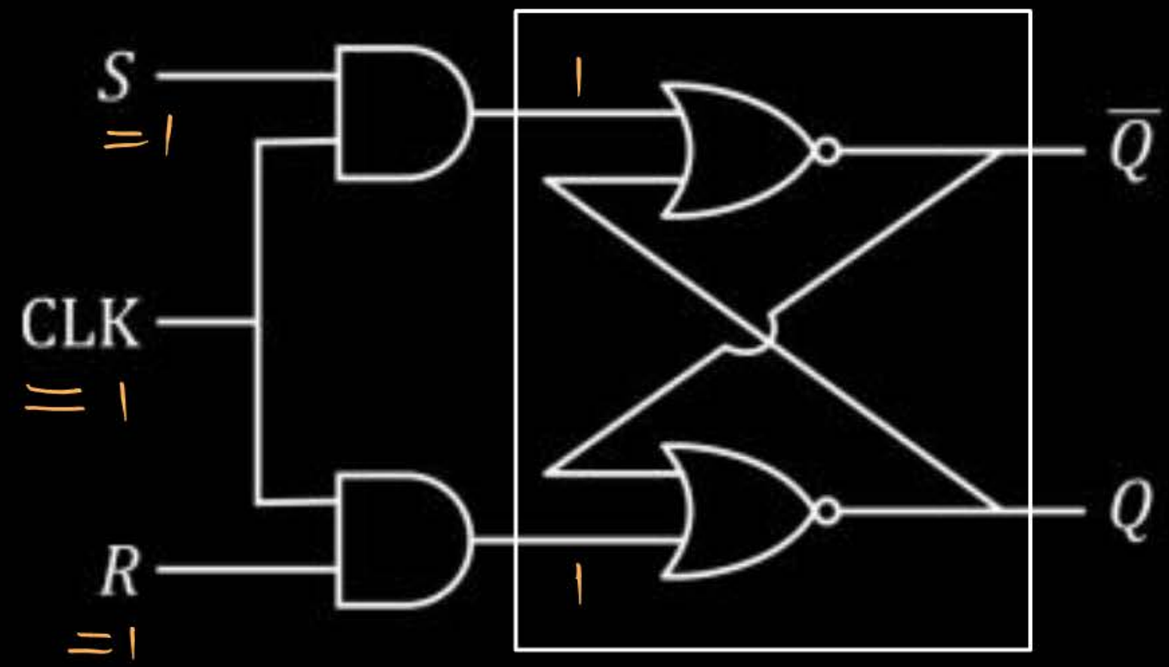
CLK = 1
= 0

-ve level triggered FF

Then truth table will be :

CLK	S	R	$Q(n+1)$
CLK=1	X	X	Q(n)
CLK=0	0	0	Q(n)
CLK=0	0	1	0
CLK=0	1	0	1
CLK=0	1	1	invalid state

S-R FF – using NOR latch + Clock



+Ve level triggered FF.

Truth Table :

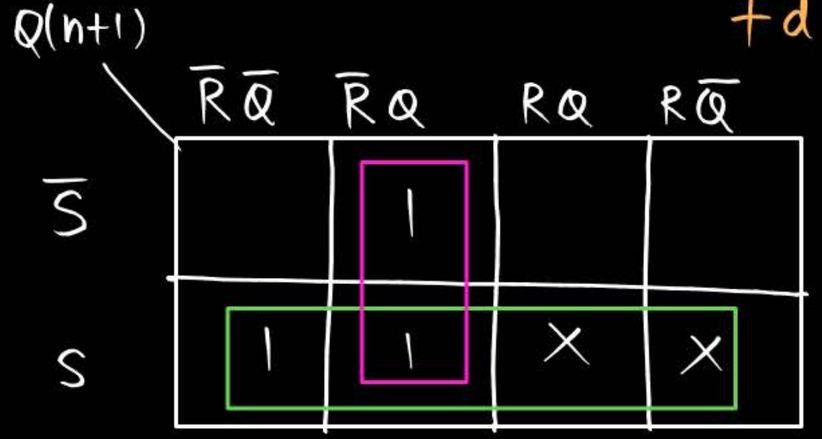
CLK	S	R	$Q(n+1)$
0	X	X	$Q(n)$
1	0	0	$Q(n)$
1	0	1	0
1	1	0	1
1	1	1	invalid state

Characteristic Table of SR Flip-Flop

When CKt is triggered

S	R	$Q(n)$	$Q(n+1)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

$Q(n+1)[S, R, Q(n)] = \sum(1,4,5) + d\sum(6,7)$

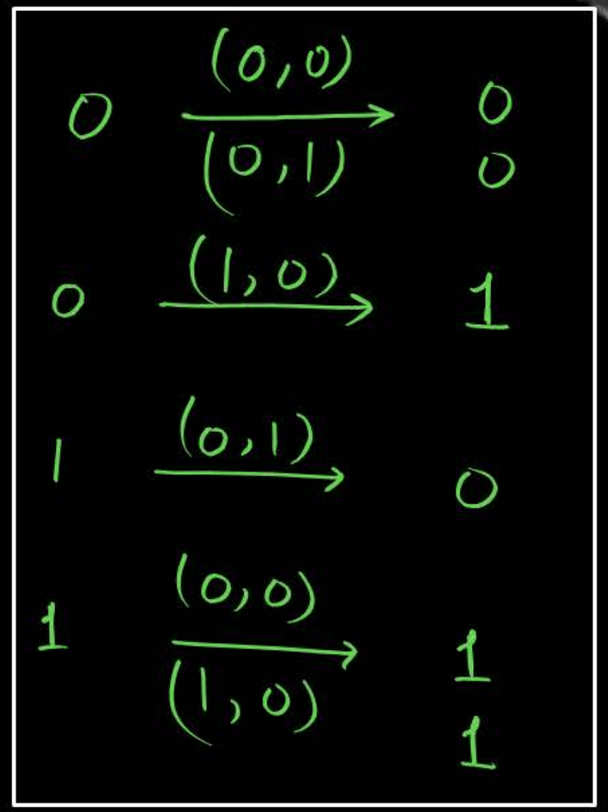


$Q(n+1) = S + \bar{R}Q(n)$

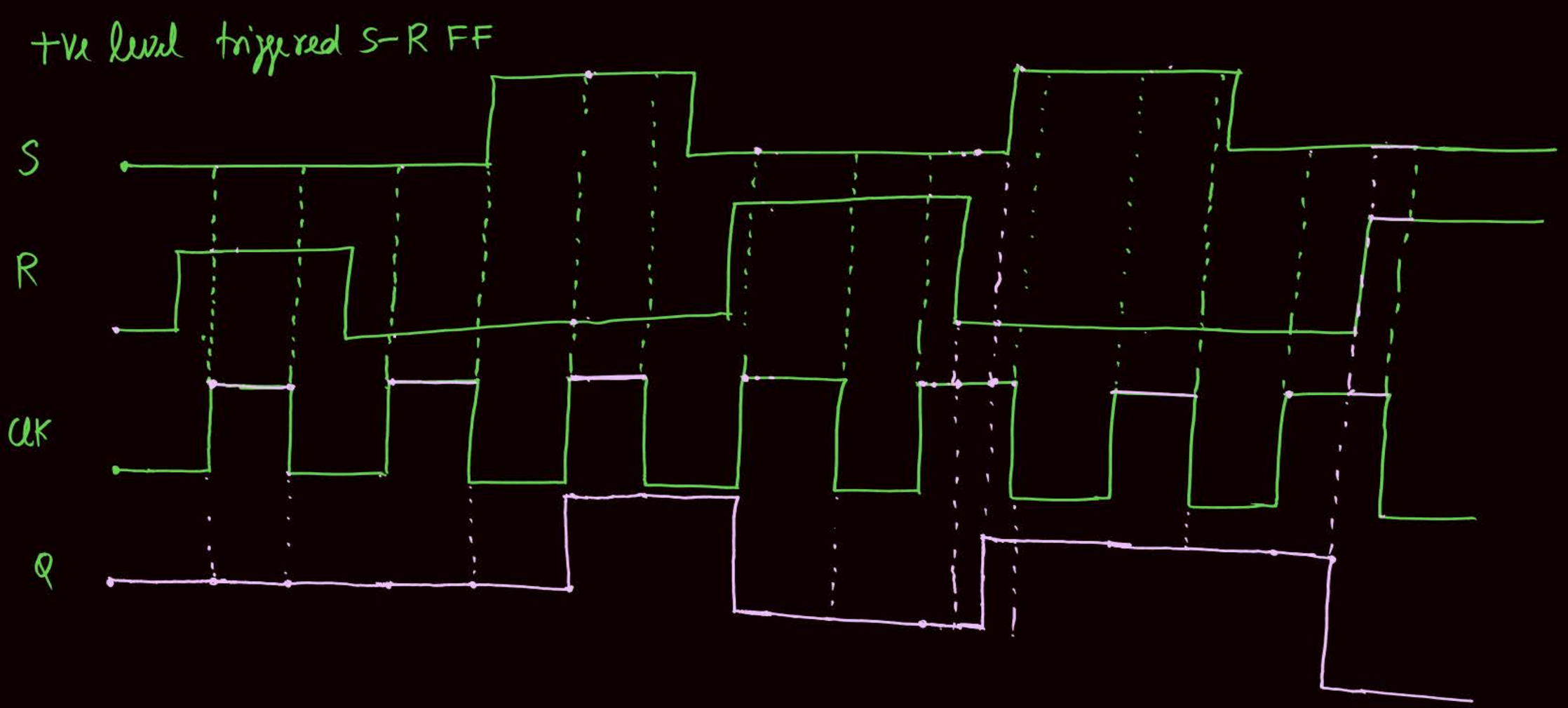
→ Valid only if $S \cdot R = 0$

Excitation Table

$Q(n)$	$Q(n+1)$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



+ve level triggered S-R FF



Topic : 2 Min Summary

- S-R latch
- SR FF

Thank you

GW

Soldiers !