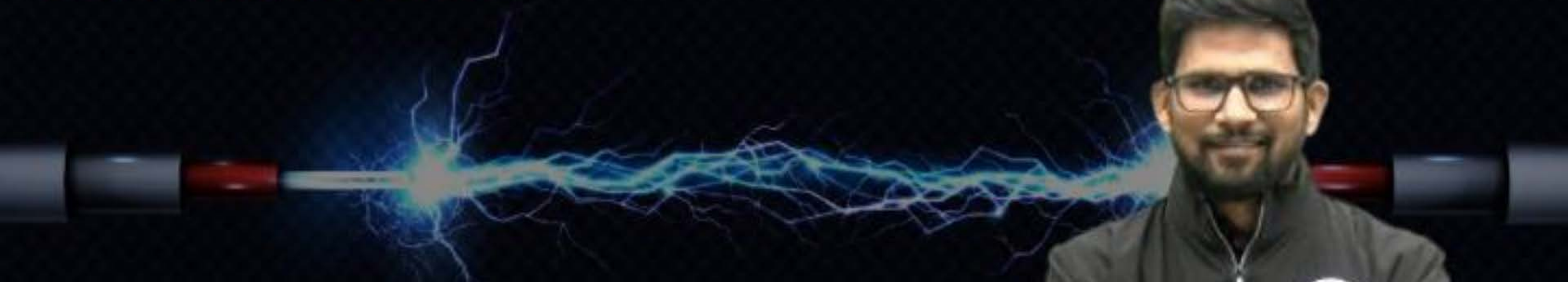


COMPUTER SCIENCE & IT

DIGITAL LOGIC




Lecture No. 07

**BOOLEAN THEOREMS AND
GATES**

By- Chandan Gupta Sir





Recap of Previous Lecture

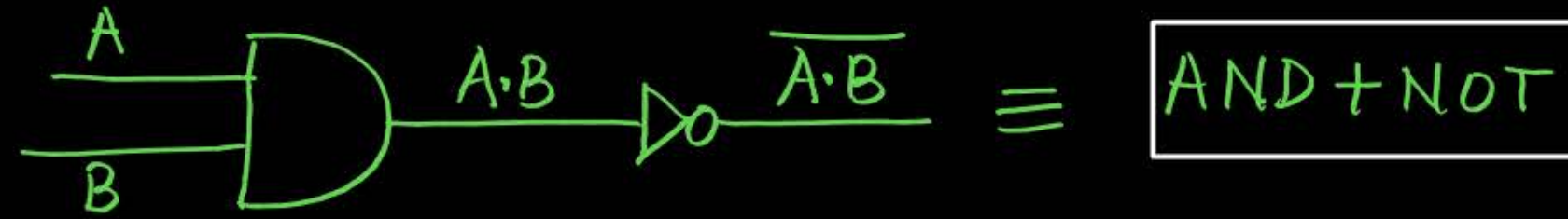
Arithmetic gates



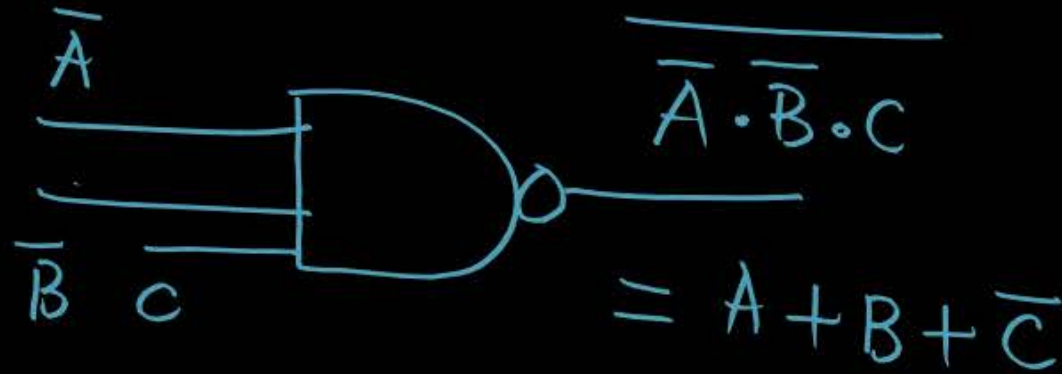
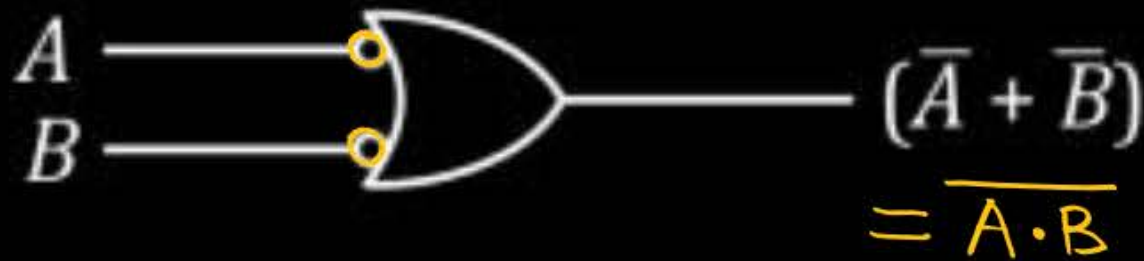
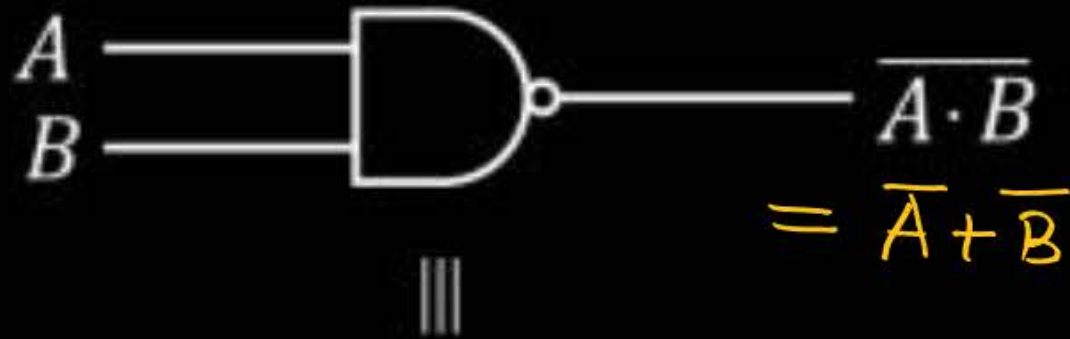
Topics to be Covered

Universal gates

[NAND GATE]



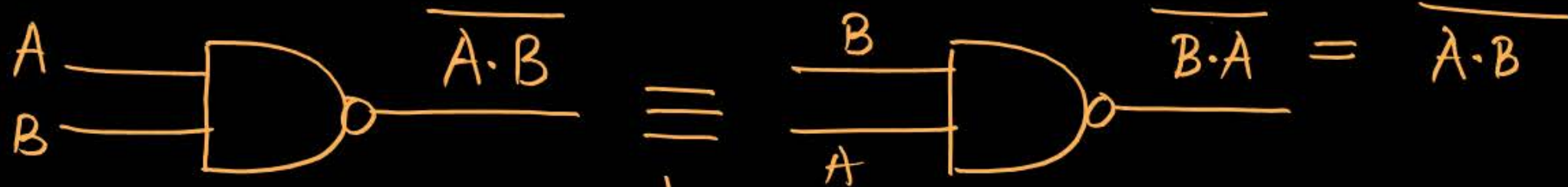
Representation :



	A	B	$y = \overline{A \cdot B}$
0	0	0	1
1	0	1	1
2	1	0	1
3	1	1	0

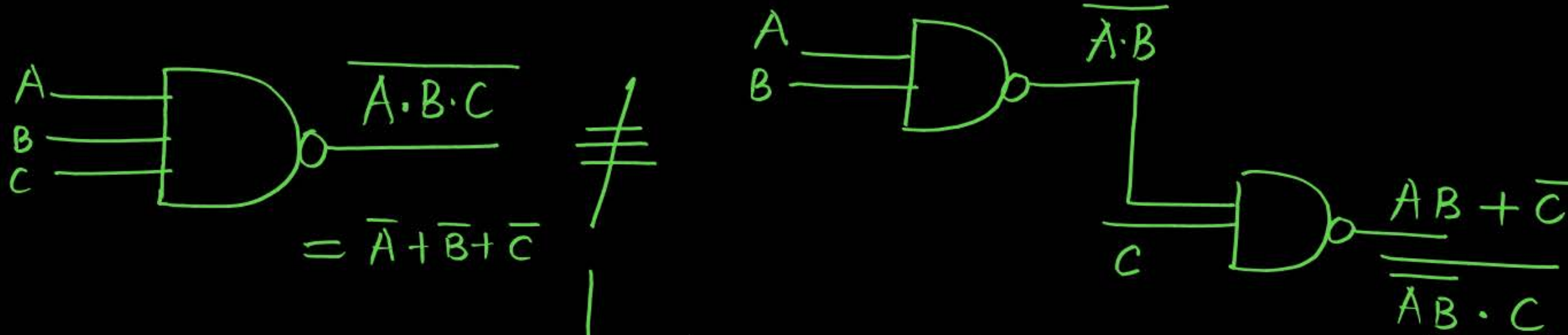
$$\begin{aligned}
 y(A, B) &= \Sigma(0, 1, 2) \\
 &= \Pi(3) \\
 &= (\overline{A} + \overline{B}) \\
 &= \overline{A \cdot B}
 \end{aligned}$$

- Commutative Law :



It holds commutative law \rightarrow position of variables is irrelevant.

- Associative Law :



It does not hold associative law.

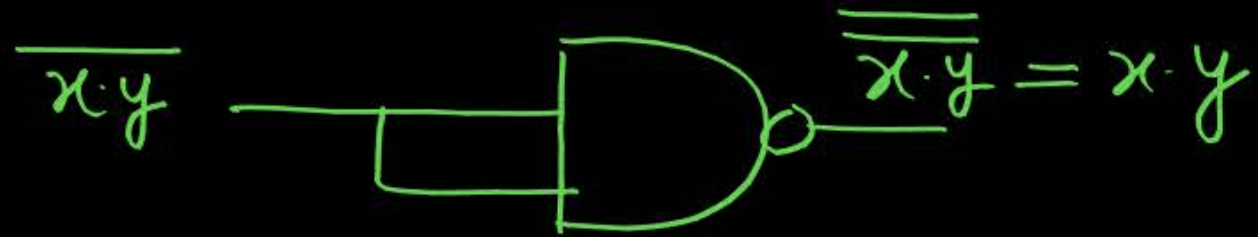
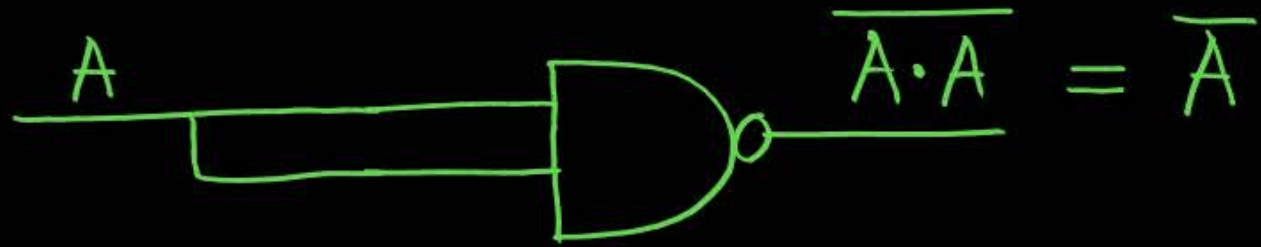
- IMP Points :

- If any one of the i/p line is at logic '0' then irrespective of other i/p lines, o/p will be at logic '1' for sure.
- O/P will be logic '0' only in one case when all the i/p lines will be at logic '1'.

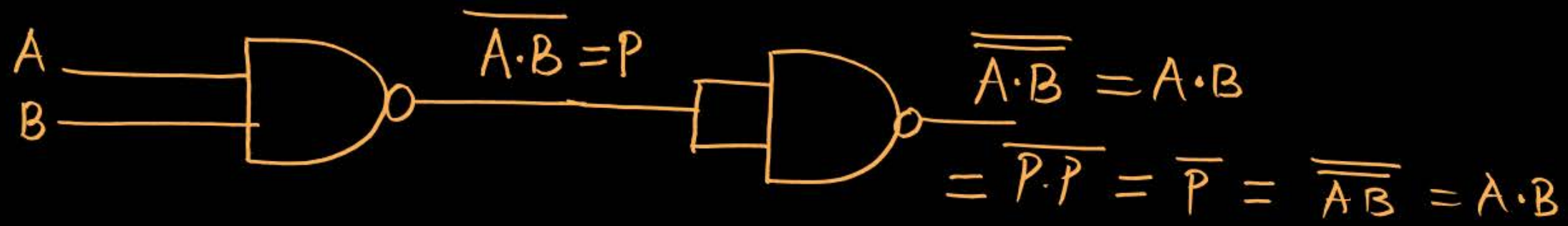
[NAND As an Universal Gate]



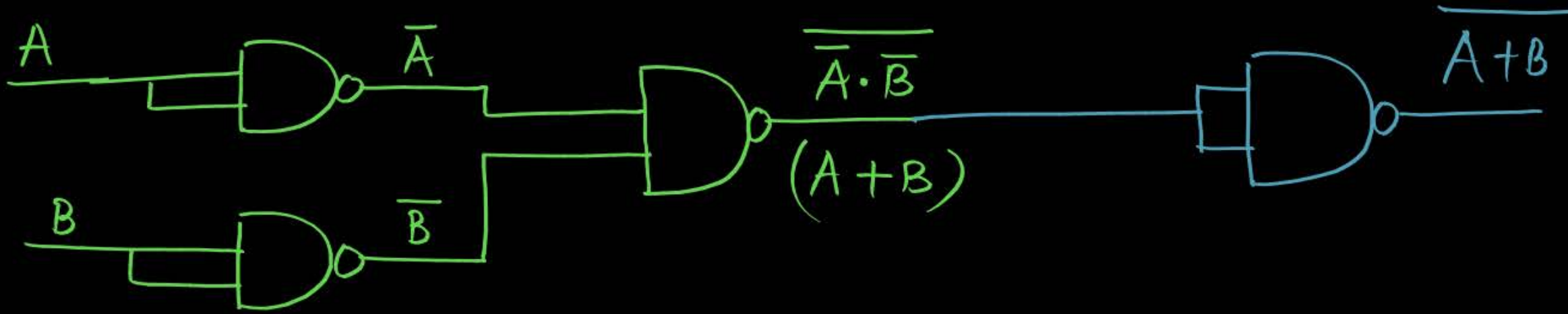
- NOT GATE :



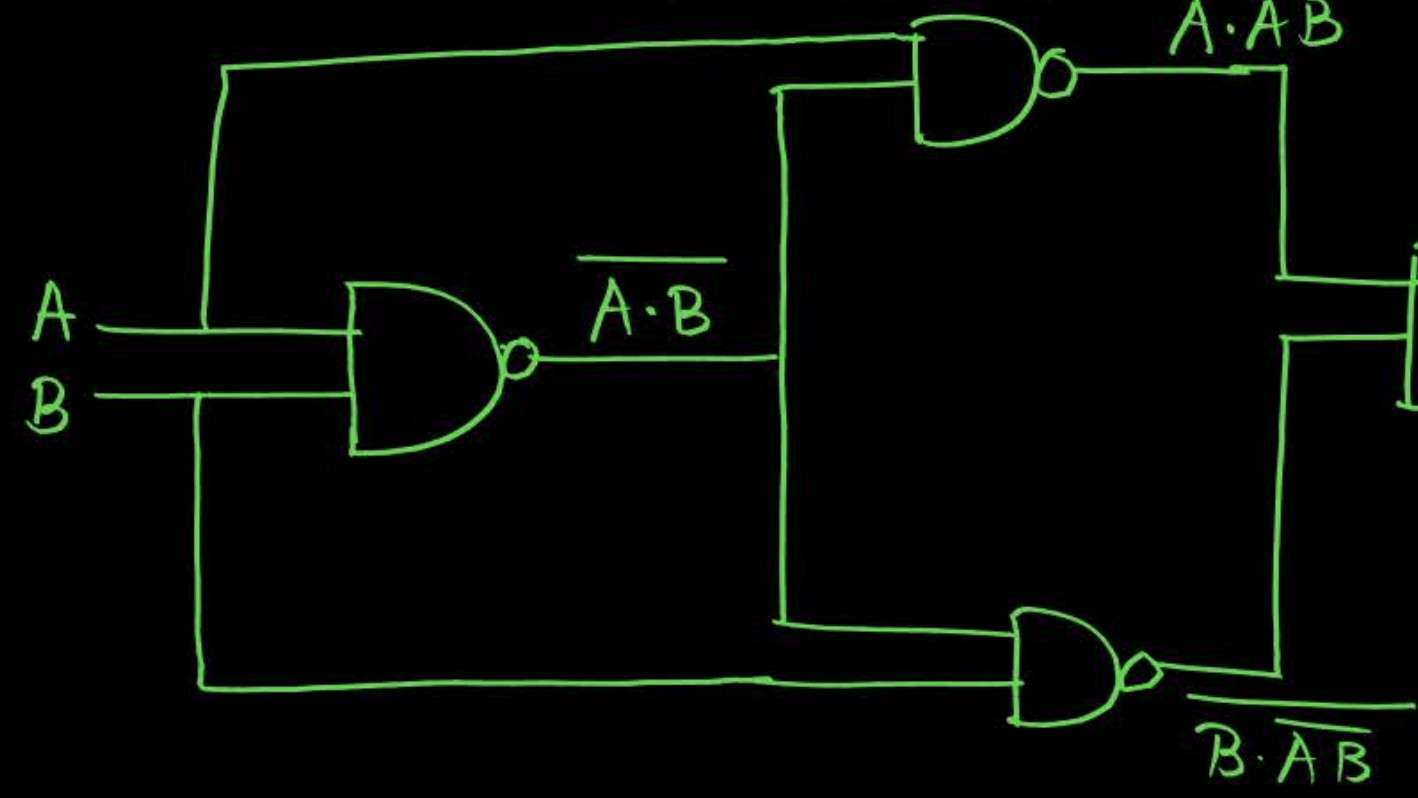
- AND GATE :



- OR GATE :



• XOR GATE and XNOR GATE:



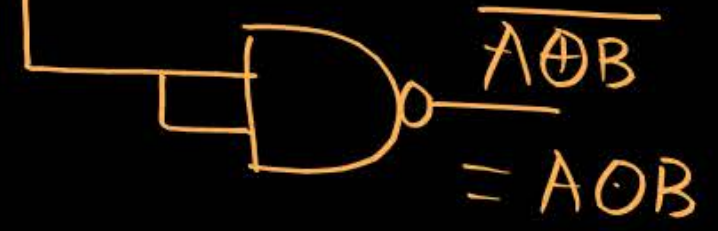
$$\begin{aligned}
 &= \bar{B} + AB \\
 &= (\bar{B} + A)(\bar{B} + B) \\
 &= (A + \bar{B})
 \end{aligned}$$

$$A \cdot \bar{A}B = \bar{A} + AB = (\bar{A} + A)(\bar{A} + B) = (\bar{A} + B)$$

$$A \oplus B = (\bar{A} + B) \cdot (A + \bar{B}) = \overline{A \odot B} = (A \oplus B)$$

$$= A \cdot \bar{A}B + B \cdot \bar{A}B = A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$

$$\begin{aligned}
 &= A\bar{B} + \bar{A}B \\
 &= \bar{A}B + A\bar{B} = A \oplus B
 \end{aligned}$$

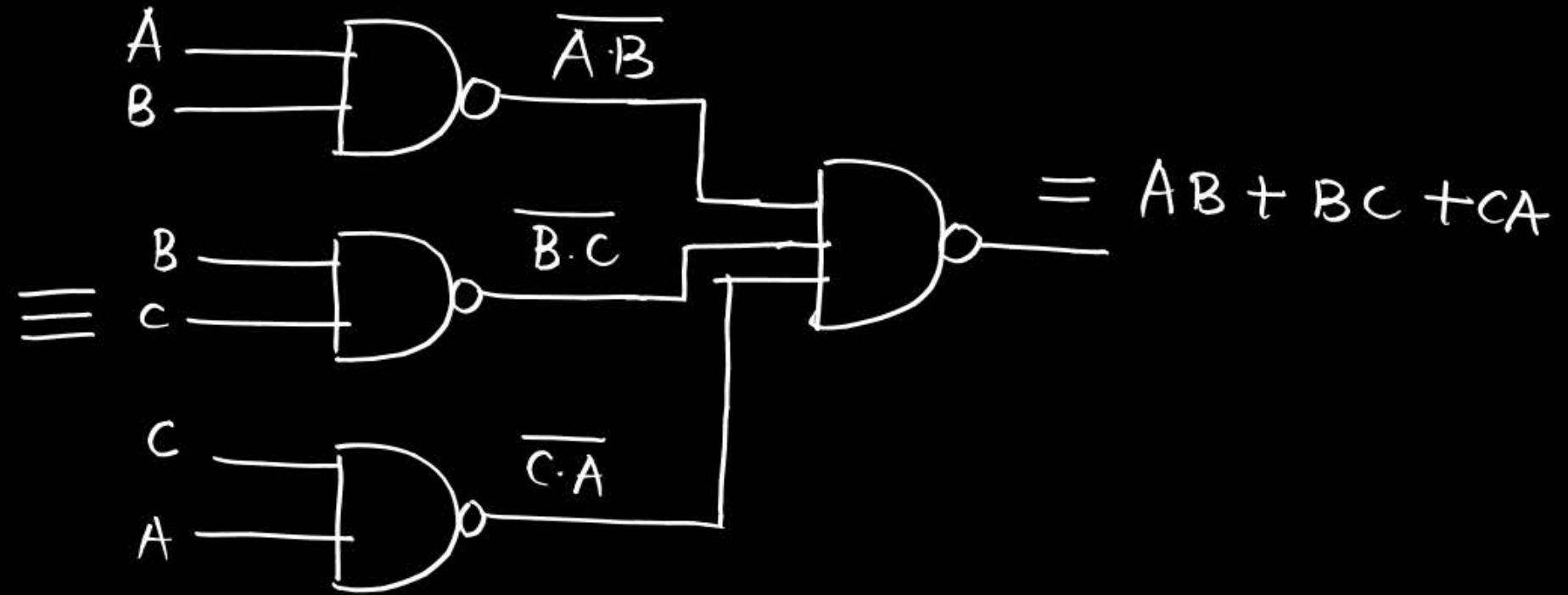
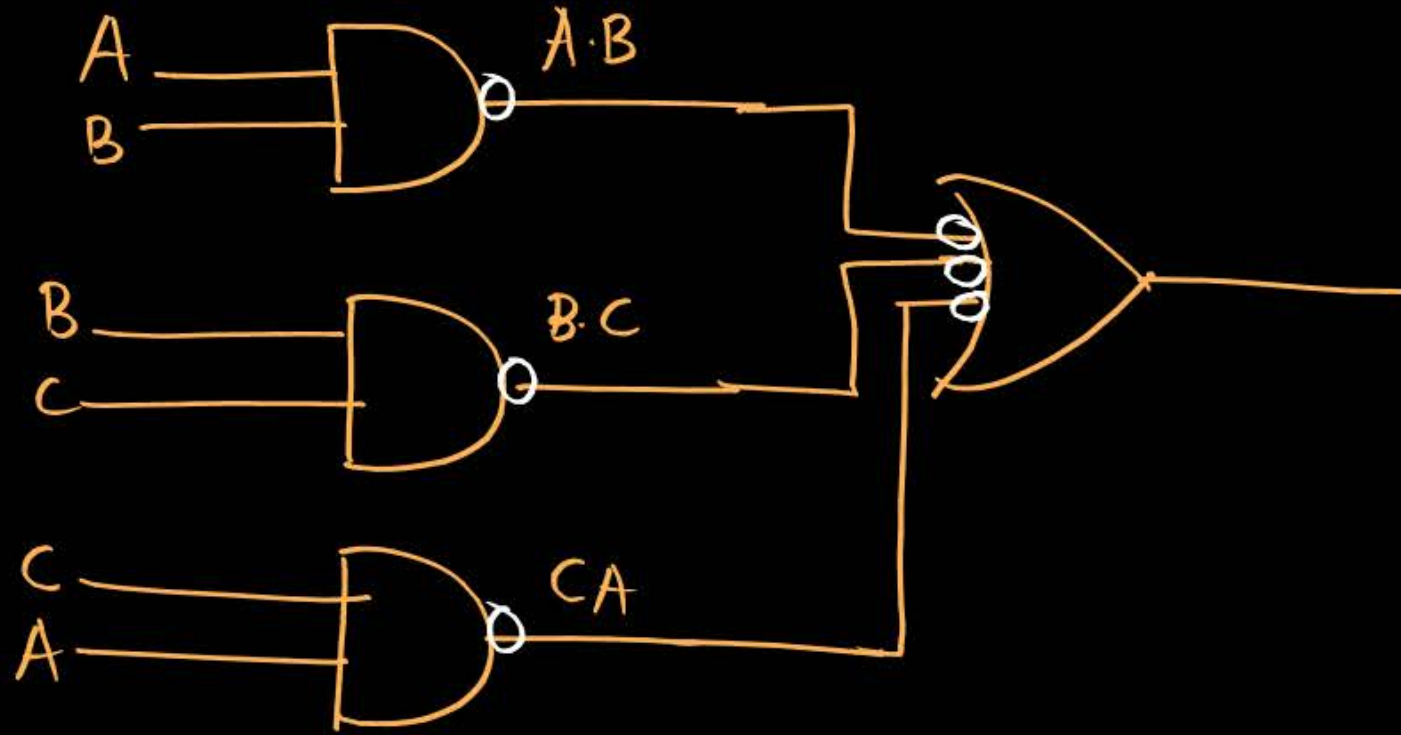


$$A \odot B = \overline{A \oplus B}$$

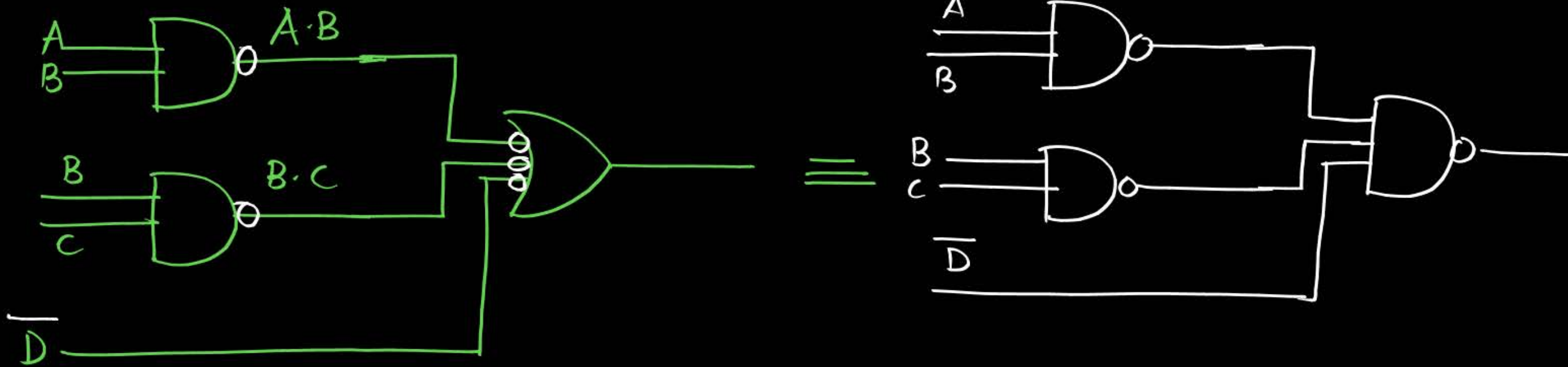
[2-Stage Implementation of SOP using NAND Gate]



- $y = AB + BC + CA$



- $y = AB + BC + D$

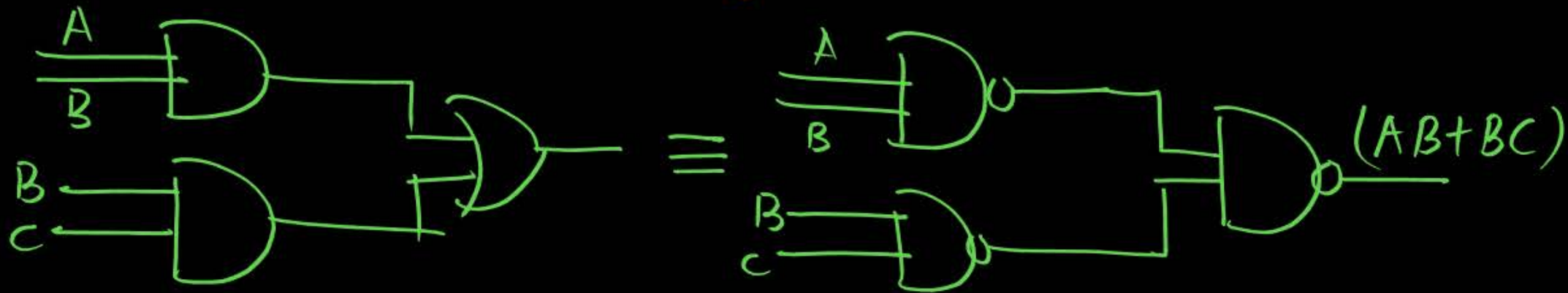


Question on minimum no. of NAND Gates

[Question]

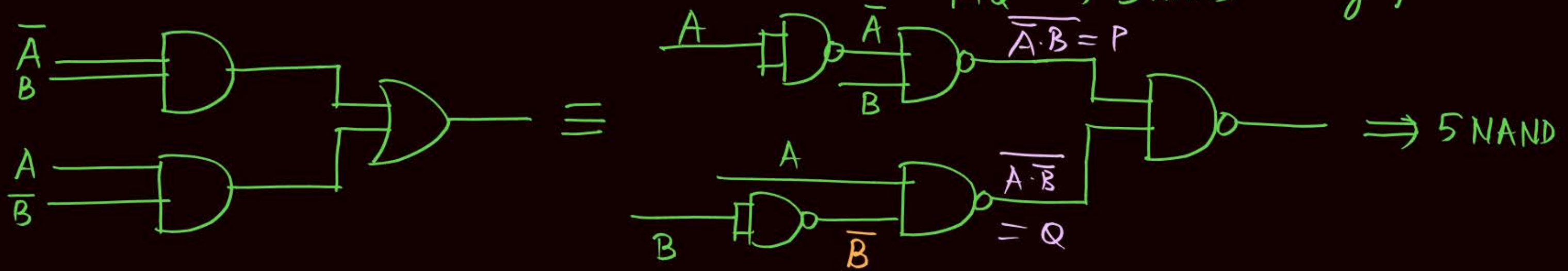
$y = AB + BC$, to implement y , minimum no. of 2-input NAND gate required is _____.

$$\left. \begin{array}{l} A \cdot B \longrightarrow 2 \text{ NAND} \longrightarrow P \\ B \cdot C \longrightarrow 2 \text{ NAND} \longrightarrow Q \\ P + Q \longrightarrow 3 \text{ NAND} \longrightarrow y \end{array} \right\} 7 \text{ NAND}$$



$$y(A, B) = \bar{A}B + A\bar{B} = A \oplus B,$$

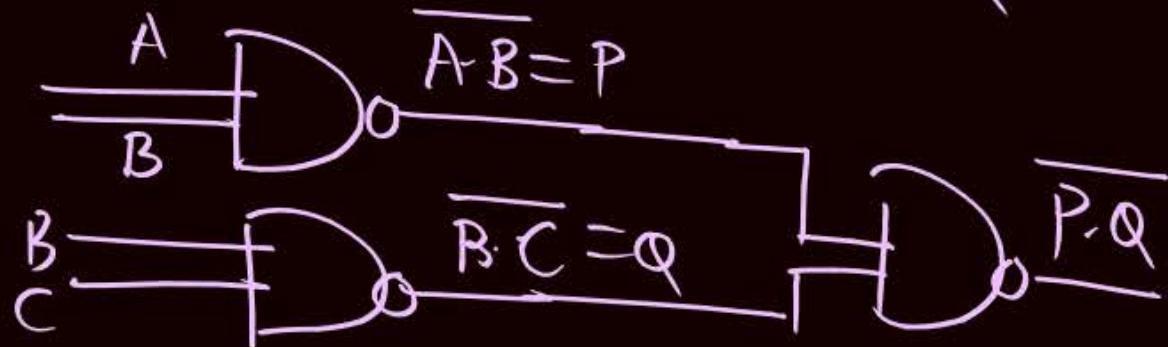
$$\left. \begin{array}{l} \bar{A} \cdot B \rightarrow 3 \text{ NAND} \rightarrow P \\ A \cdot \bar{B} \rightarrow 3 \text{ NAND} \rightarrow Q \\ P + Q \rightarrow 3 \text{ NAND} \rightarrow y \end{array} \right\} 9 \text{ NAND}$$



$$y = AB + BC$$

$$\bar{y} = \overline{AB + BC} = \overline{AB} \cdot \overline{BC}$$

$$y = \overline{\overline{AB} \cdot \overline{BC}} = \overline{P \cdot Q}$$



$$A \cdot B \rightarrow 2 \text{ NAND}$$

$$\overline{A \cdot B} \rightarrow 1 \text{ NAND}$$

$$A + B \rightarrow 3 \text{ NAND}$$

$$y = \bar{A}B + A\bar{B}$$

$$\bar{y} = \overline{\bar{A}B + A\bar{B}} = \overline{\bar{A}B} \cdot \overline{A\bar{B}}$$

$$y = \overline{\bar{A}B \cdot A\bar{B}} = \overline{P \cdot Q}$$

$$\left. \begin{array}{l} P = \underline{\bar{A}} \cdot \underline{B} \rightarrow 2 \text{ NAND} \\ Q = A \cdot \underline{\bar{B}} \rightarrow 2 \text{ NAND} \\ y \rightarrow \overline{P \cdot Q} \rightarrow 1 \text{ NAND} \end{array} \right\} \underline{5 \text{ NAND}}$$

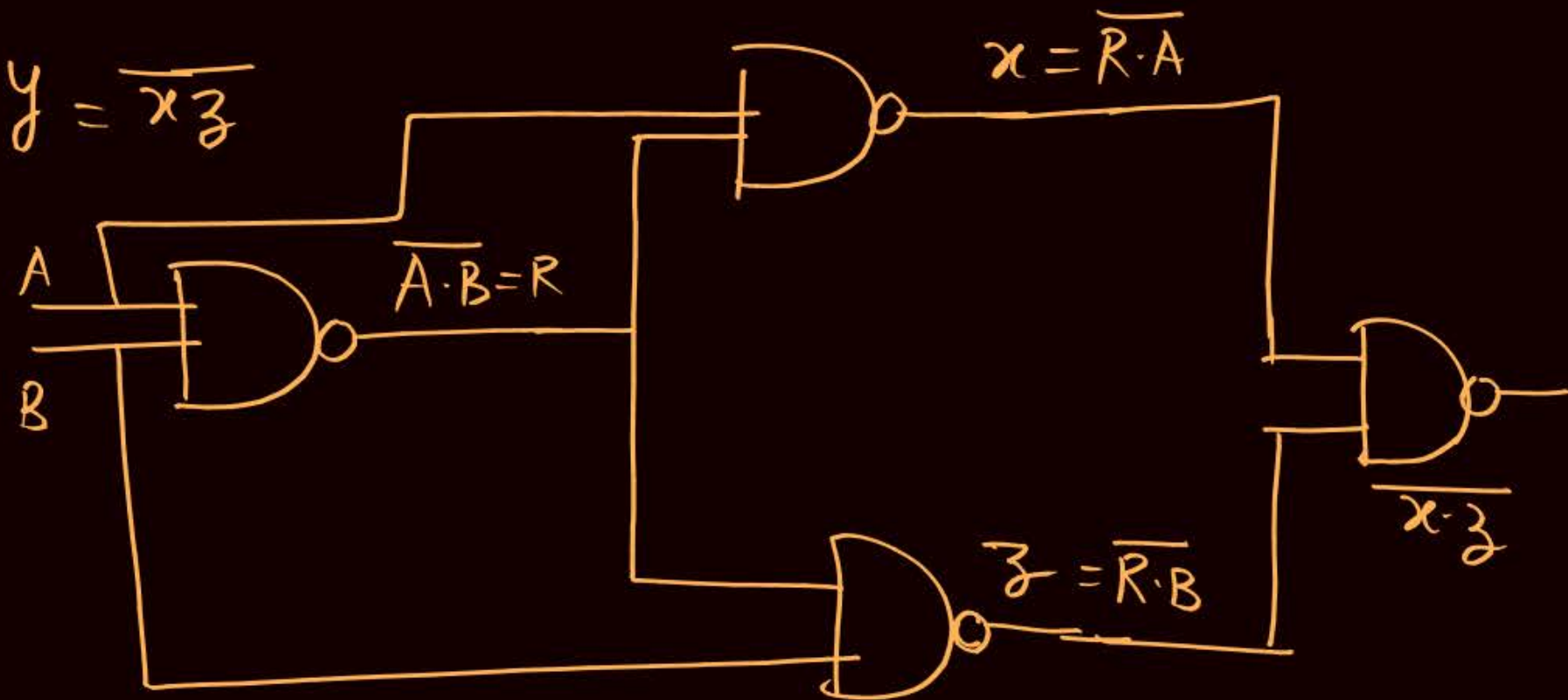
$$y = \bar{A}B + A\bar{B} = (\bar{A} + \bar{B})(A + B)$$

$$= \underline{\underline{\bar{A} \cdot B}} (A + B) = R(A + B)$$

$$y = R \cdot A + R \cdot B$$

$$\bar{y} = \overline{R \cdot A + R \cdot B} = \underline{\underline{\bar{R} \cdot \bar{A}}} \cdot \underline{\underline{\bar{R} \cdot \bar{B}}} = x \cdot z$$

$$y = \overline{x \cdot z}$$



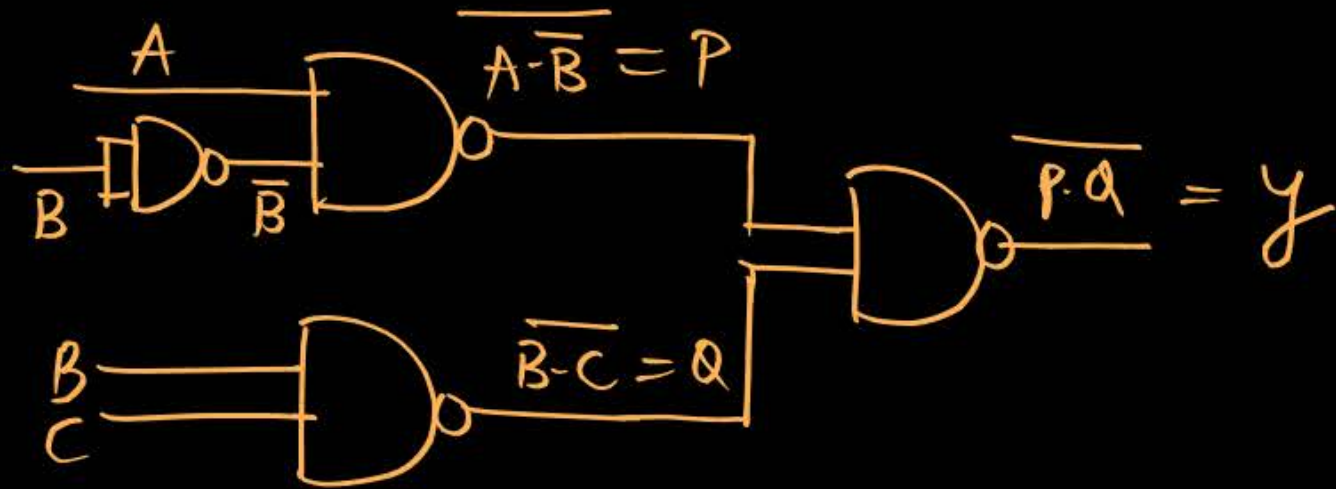
[Question]

$$y = A\bar{B} + BC$$

Minimum no. of 2-input NAND gates required to implement y 4

$$\bar{y} = \overline{A\bar{B} + BC} = \overline{A\bar{B}} \cdot \overline{BC} = P \cdot Q$$

$$y = \overline{P \cdot Q}$$



[Question]

$$f(A, B, C) = \bar{A} + \bar{A}B + \bar{A}B\bar{C} = \bar{A}(1 + B + B\bar{C}) = \bar{A} \cdot 1 = \bar{A} \longrightarrow 1 \text{ NAND}$$

Minimum no. of 2-input NAND gates required to implement y 1

#Q. $y = \overline{AB} + \overline{B.C} = \overline{A+B+B+C} = \overline{A+B+C} = \overline{A.B.C}$

Minimum no. of 2-i/p NAND gate required 3.

$$\left. \begin{array}{l} \overline{A.B} \rightarrow 1 \text{ NAND} \rightarrow P \\ \overline{B.C} \rightarrow 1 \text{ NAND} \rightarrow Q \\ P+Q \rightarrow 3 \text{ NAND} \rightarrow y \end{array} \right\} 5 \text{ NAND}$$

$$\overline{A.B.C} = \overline{R.C}$$

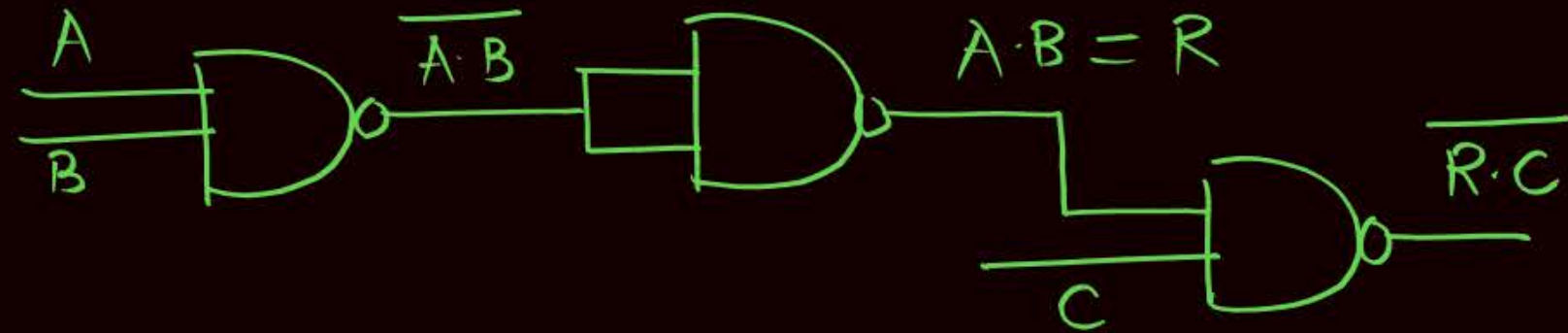
$$A.B \rightarrow 2 \text{ NAND} \rightarrow \underline{\underline{R}}$$

$$R.C \rightarrow 2 \text{ NAND}$$

$$\overline{R.C} \rightarrow 1 \text{ NAND}$$

$$\overline{y} = A.B.C = ABC$$

$$y = \overline{ABC}$$



Q. $y = \overline{AB} + \overline{CD} = \overline{A+B+C+D} = \overline{A \cdot B \cdot C \cdot D}$

Minimum no. of 2-i/p NAND gate required _____.

$$\left. \begin{array}{l} \overline{A \cdot B} \rightarrow 1 \text{ NAND} \Rightarrow P \\ \overline{C \cdot D} \rightarrow 1 \text{ NAND} \Rightarrow Q \end{array} \right\} 2 \text{ NAND}$$

$P + Q \rightarrow 1 \text{ NAND}$

$$\overline{y} = \overline{\overline{AB} + \overline{CD}} = AB \cdot CD$$

$$y = \overline{ABCD}$$

$$\overline{A \cdot B \cdot C \cdot D}$$

$$\left. \begin{array}{l} A \cdot B \rightarrow R \rightarrow 1 \text{ NAND} \\ R \cdot C \rightarrow S \rightarrow 1 \text{ NAND} \end{array} \right\} 2 \text{ NAND}$$

$\overline{S \cdot D} \rightarrow 1 \text{ NAND}$

[Question]



$$y = \bar{A}BC$$

To implement y , minimum no. of 2-input NAND gates required is 5

$$y = \bar{A} \underline{B} \underline{C}$$

$$B.C \longrightarrow 2 \text{ NAND} \longrightarrow P$$

$$\bar{A}.P \longrightarrow \bar{A} \longrightarrow 1 \text{ NAND} \longrightarrow \bar{A}.P \longrightarrow 2 \text{ NAND}$$

[Question]

$$f(A, B, C, D) = (\bar{A} + \bar{B})(C + D) = \overline{A \cdot B} (C + D) = P(C + D) = P \cdot C + P \cdot D$$

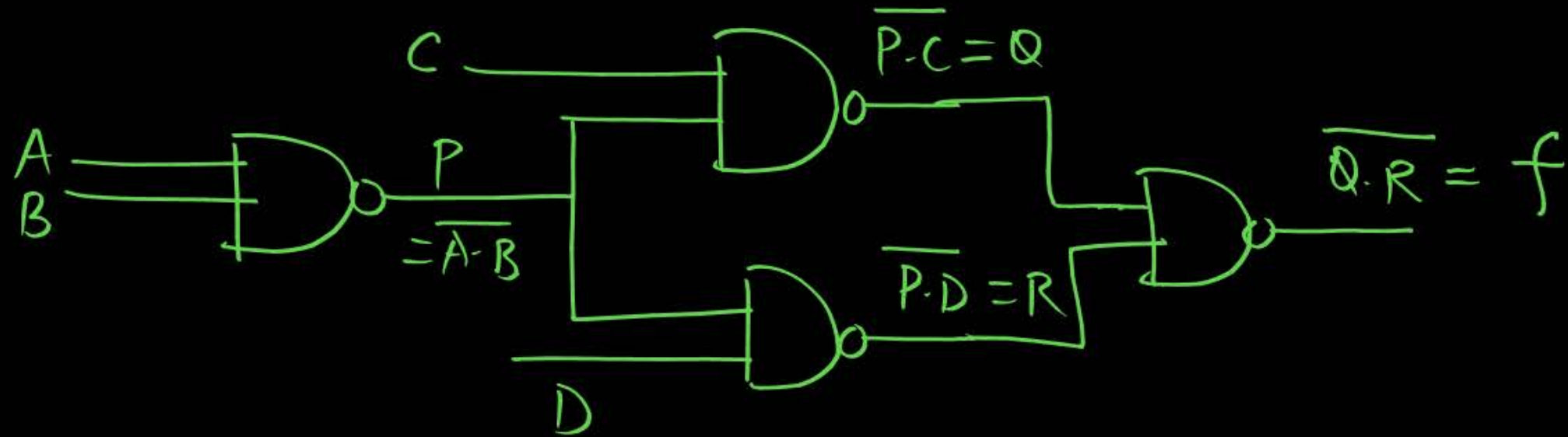
Minimum no. of 2-input NAND gates required to implement

$$f(A, B, C, D) \underline{4}$$

$$f = PC + PD$$

$$\bar{f} = \overline{PC + PD} = \overline{PC} \cdot \overline{PD} = Q \cdot R$$

$$f = \overline{Q \cdot R}$$



Implement following function with minimum no. of 2-i/p NAND gates:

Q. $Y = \bar{A}B + B\bar{C}$

Q. $Y = (\bar{A} + \bar{B})(\bar{C} + D)$

Q. $Y = \bar{A}B + \bar{C}D$

Q. $Y = \overline{\bar{A}BC}$

Q. $Y = AB + BC + CA$

Q. $Y = \Sigma(1, 2, 4, 7)$



2 Minute Summary

→ universal gates

Thank you

GW
Soldiers !

