COMPUTER SCIENCE & IT

DIGITAL LOGIC

Lecture No. 01

Combinational Circuit

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Duality & Imp basics related to boolean function

Combinational CKt

[Type of Digital Circuit]

- Combinational Circuit
- Sequential Circuit

Combinational ckt	Sequential ckt
1. O/P depends on present i/p only.	1. O/P depends on present i/p and past i/p values.
2. There is no memory.	2. There is memory.
3. There is no feedback.	3. There is feedback.
eg. H.A., F.A, H.S, F.S, MUX, DeMUX, Decoder, Encoder etc.	eg. ff, Counters, shift registers etc.

[How to Design Combinational Circuit]

1. Identify no. of i/p lines and no. of o/p lines.

2. Truth table b/w i/Ps (all the combinations of i/p) and o/Ps.

3. Write down o/Ps in SOP or POS format.

4. Now minimize your o/Ps using boolean theorems or K-Map.

5. Now implement the o/Ps using gates.

Standard Combinational Circuits

- Half Adder
- Half Subtractor
- Full Adder
- Full Subtractor

$A = a_3 a_2 a_1 a_0 = 1011$

$B = b_3 b_2 b_1 b_0 = 0111$

$$
\begin{array}{ccccc}
 & 1 & 0 & 1 & 1 \\
 & 0 & 1 & 1 & 1 \\
 & 1 & 1 & 1 & \\
\hline
1 & 0 & 0 & 1 & 0
\end{array}
$$

$$
\begin{array}{cccc}
 & 2 & 3 & 7 \\
 & 3 & 9 & 2 \\
 & 1 & 0 & \\
\hline
0 & 6 & 2 & 9
\end{array}
$$

$8^2 \, 8^1 \, 8^0$

$(147)_8 = (64 + 32 + 7)_{10}$

$(234)_8 + (128 + 24 + 4)_{10}$

$1 \; 1$

$(403)_8 = 256 + 0 + 3$

$= (259)_{10}$

$= (103)_{10}$

$(156)_{10}$

$(259)_{10}$

[Half Adder]

- What is half adder and what are input lines and what are output lines ?

⇒ 2-i/p lines ⟶ corresponding bits of the two no. being added ⟶ x, y

$\boxed{\begin{matrix} a_3 & b_3 \\ a_2 & b_2 \\ a_1 & b_1 \end{matrix}}$

⇒ 2-o/p lines ⟶ Sum o/p ⟶ S

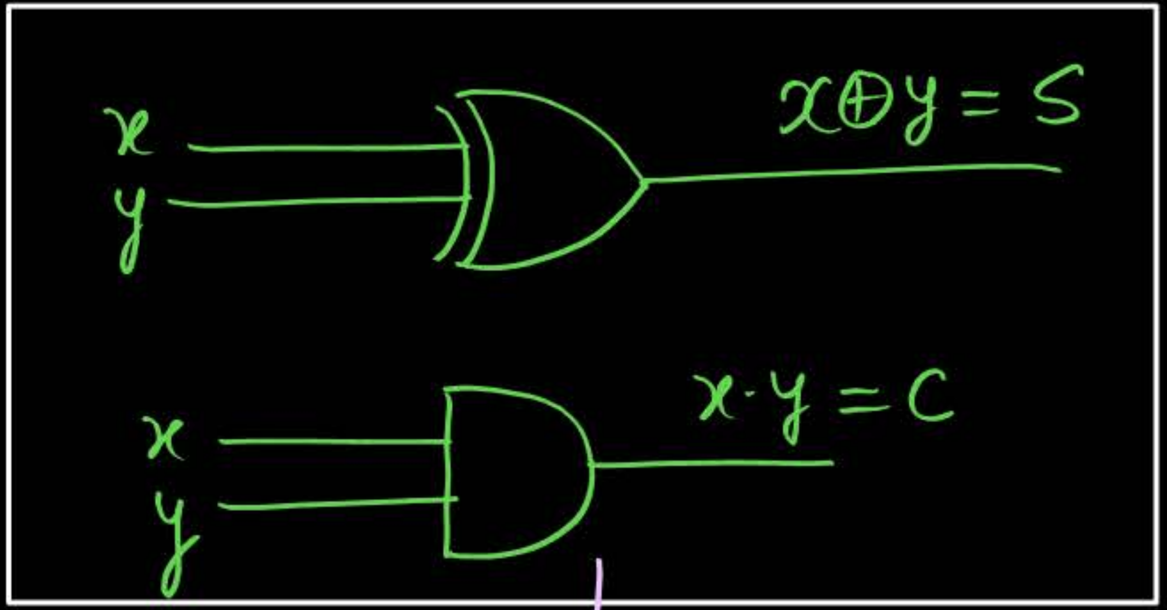
Carry o/p ⟶ C

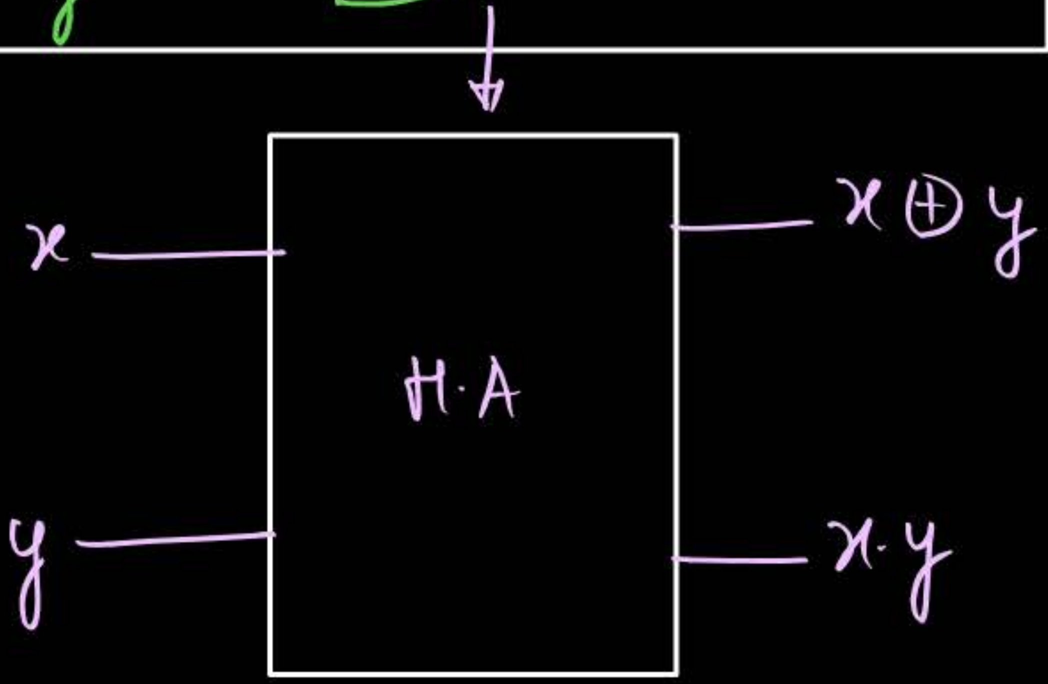
	Input lines		Output lines	
	x	y	S-o/p	C-o/p
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	0	1

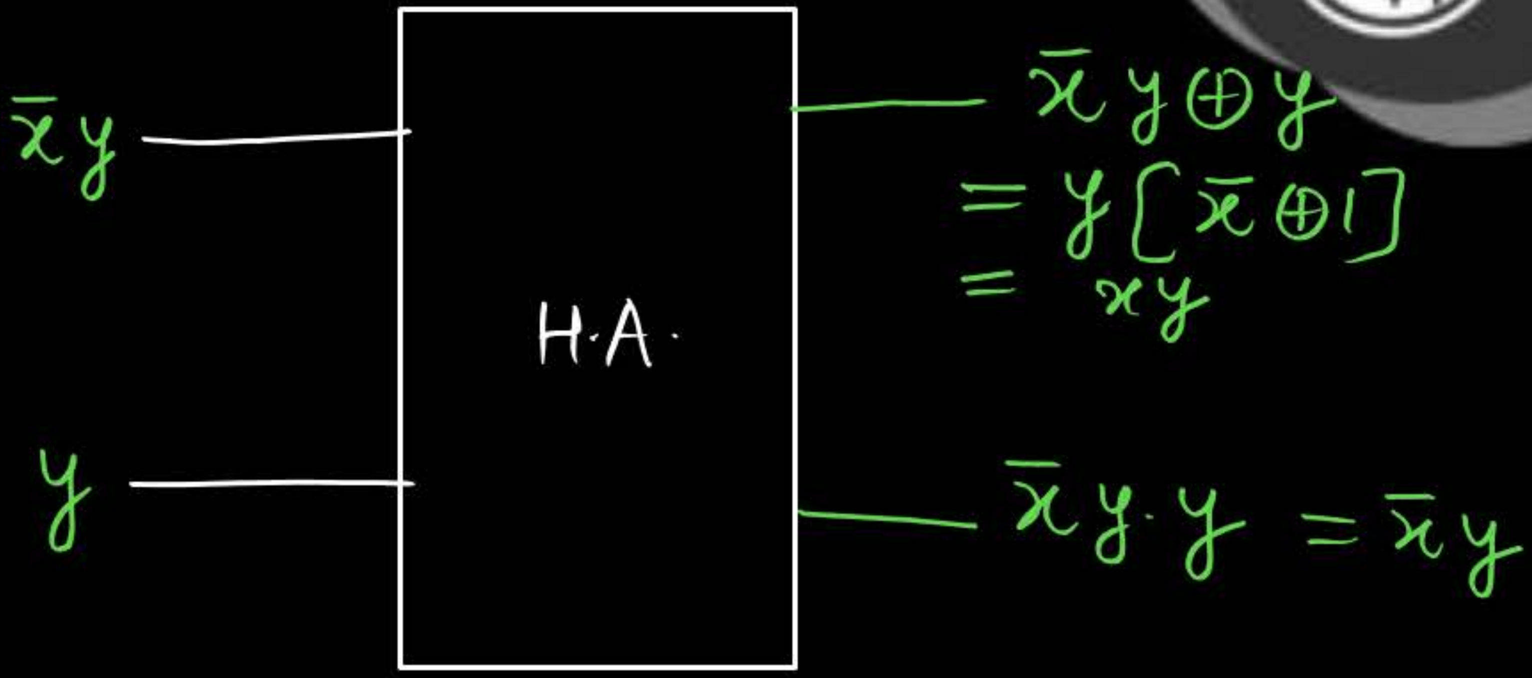
$$S(x,y) = \sum(1,2) = \prod(0,3)$$
$$= \bar{x}y + x\bar{y} = x \oplus y$$

$$C(x,y) = \sum 3 = \prod(0,1,2)$$
$$= x \cdot y$$

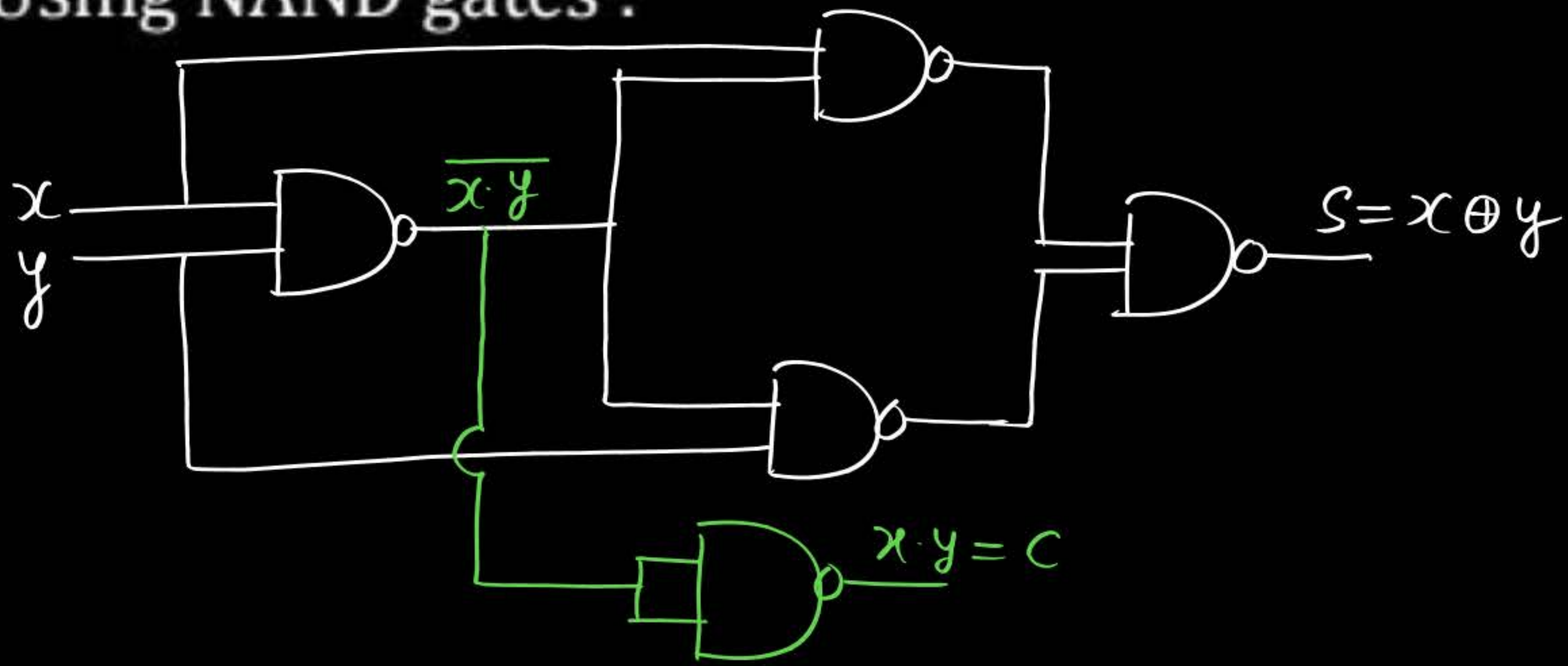
Implementation using gates :



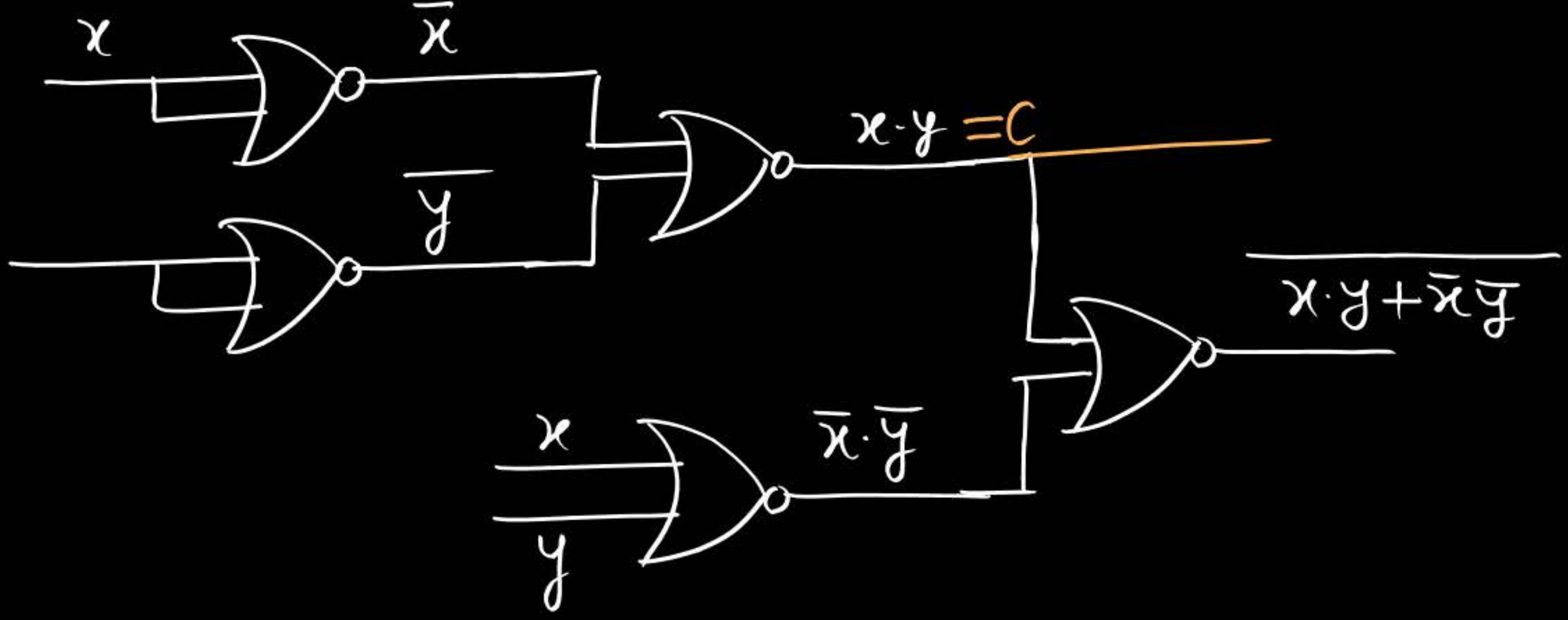




- Using NAND gates :



- Using NOR gates :



$\overline{x \cdot y + \bar{x}\bar{y}} = \overline{x \odot y} = x \oplus y$
$= S$

$\Rightarrow$ Note : To implement H.A. we require 5 (2-i/p NAND gates) or 5 (2-i/p NOR gates).

Full Adder

- What is full adder and what are input lines and what are output lines ?

⇒ 3-i/p lines ⟶ Corresponding bits of the two no.s (x, y) and carry generated from previous addition z.

2-o/p lines ⟶ sum o/p - S
Carry o/p - C

	Input lines			Output lines	
	x	y	z	S-o/p	C-o/p
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Carry o/p of a full adder is majority i/p circuit.

↳ when majority i/p will be at '1' o/p will 1 and when majority i/p will be '0' → o/p will be '0'.

$$S(x,y,z) = \sum(1,2,4,7)$$
$$= x \oplus y \oplus z$$

↓ self dual boolean function

✓ $$C(x,y,z) = \sum(3,5,6,7) = \pi(0,1,2,4)$$

self dual boolean f^n.

$$= \bar{x}yz + x\bar{y}z + xy\bar{z} + xyz$$

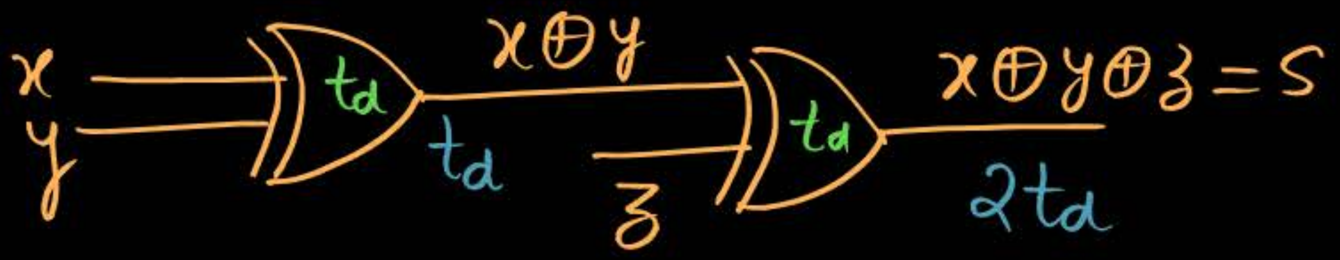
$$= xy + yz + xz$$

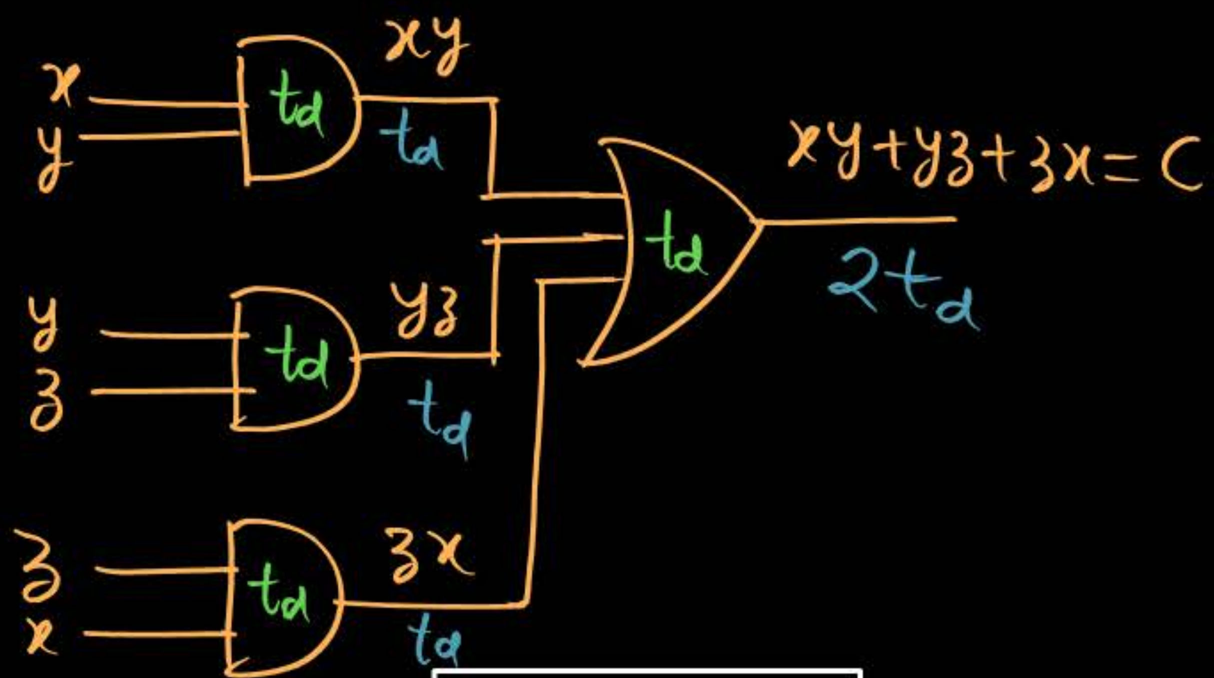
$$= xy + z(x \oplus y)$$

$$\bar{x}yz + x\bar{y}z + xy\bar{z} + xyz$$

$$= z(\bar{x}y + x\bar{y}) + xy$$

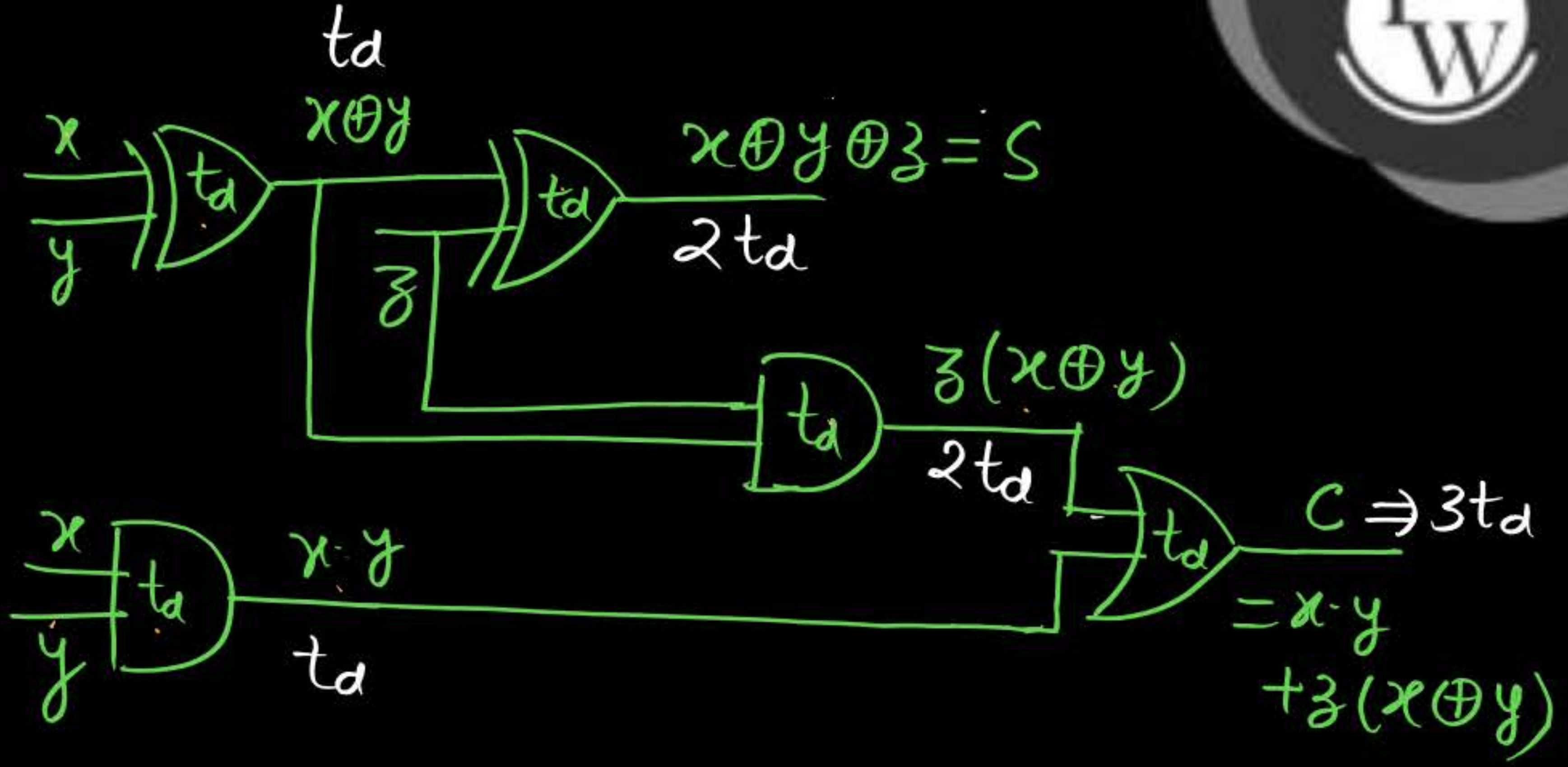
Implementation using gates :





Circuit – I

overall delay $= 2t_d$



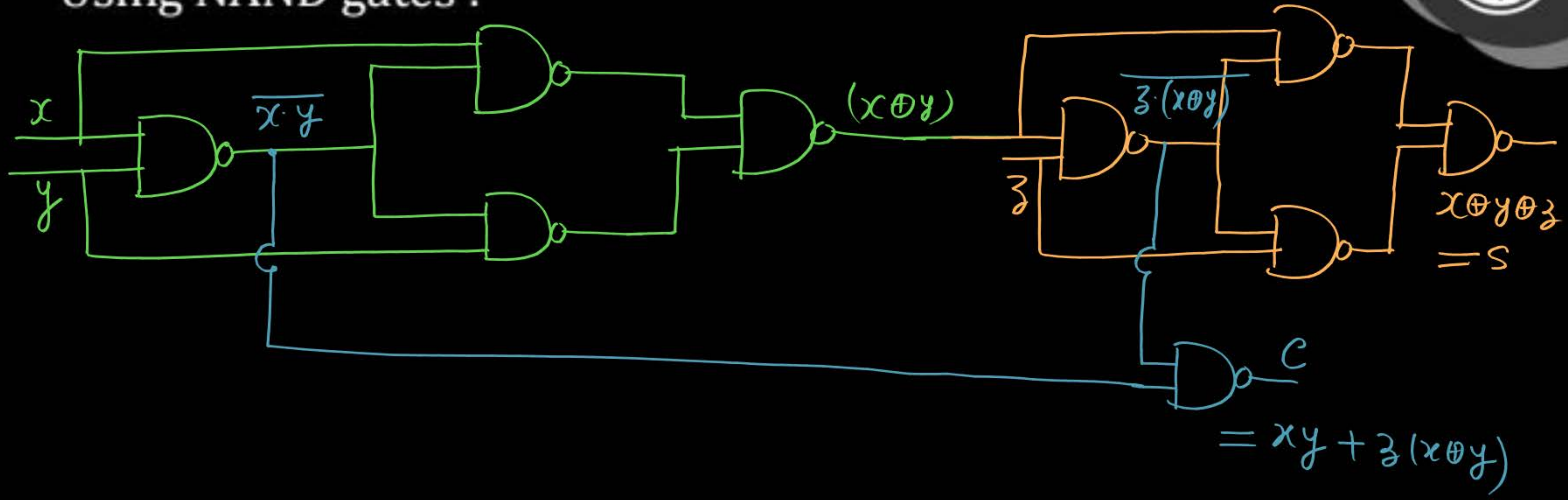
Circuit – II $\longrightarrow$ 2 H.A + 1 OR

overall delay $\rightarrow 3t_d$

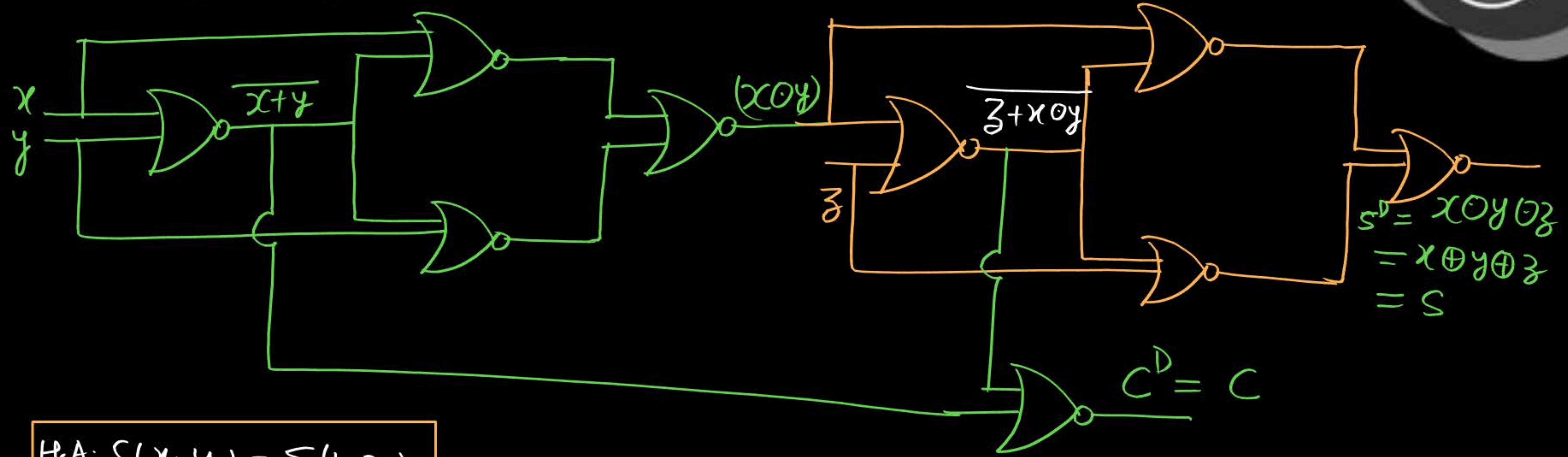
⇒ Circuit II is better compare to circuit-I w.r.t no of gates used for designing.

⇒ Circuit-I has less delay compare to circuit-II.

- Using NAND gates :



- Using NOR gates :



H.A. $S(x, y) = \Sigma(1,2)$

$\downarrow$

non self dual

$$C^D = (x+y)(z + x\odot y) = (x+y)[z + \bar{x}\bar{y} + xy]$$

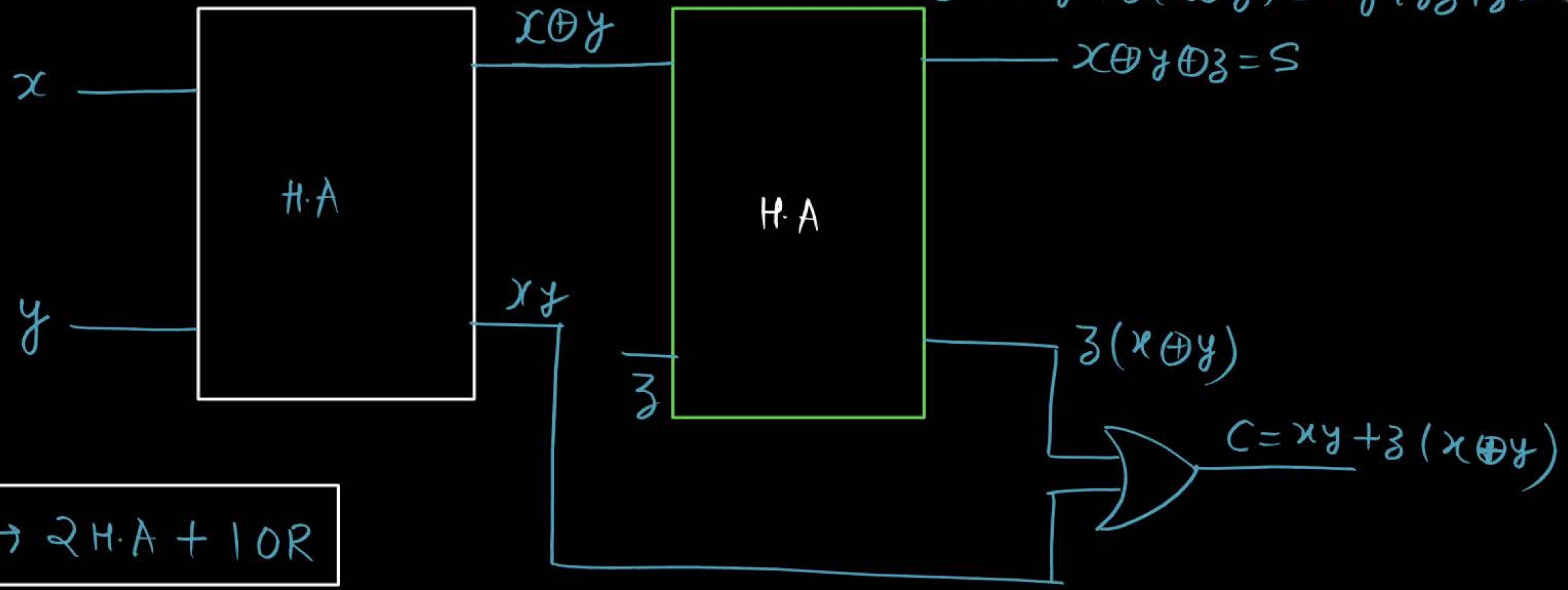
$$= xz + xy + yz + xy = xy + yz + xz$$

Note: To implement F.A., we require → 9 (2-i/p NAND gates) or 9 (2-i/p NOR gates).

- Full adder using H.A. and OR gate :

$S = x \oplus y \oplus z$

$C = xy + z(x \oplus y) = xy + yz + zx$



$\boxed{1\,F.A \longrightarrow 2\,H.A + 1\,OR}$

$\Rightarrow$ F.A $\rightarrow$ i/p $\rightarrow$ x, y, z $\longrightarrow$ $(x+y+z)$

$(x+z+y)$

$(y+z+x)$

$$C_{out} = xy + yz + zx$$

$$= \underline{\underline{xy}} + z(x \oplus y) \checkmark$$

$$= x \cdot z + y(x \oplus z)$$

$$= yz + x(y \oplus z)$$

Homework Questions

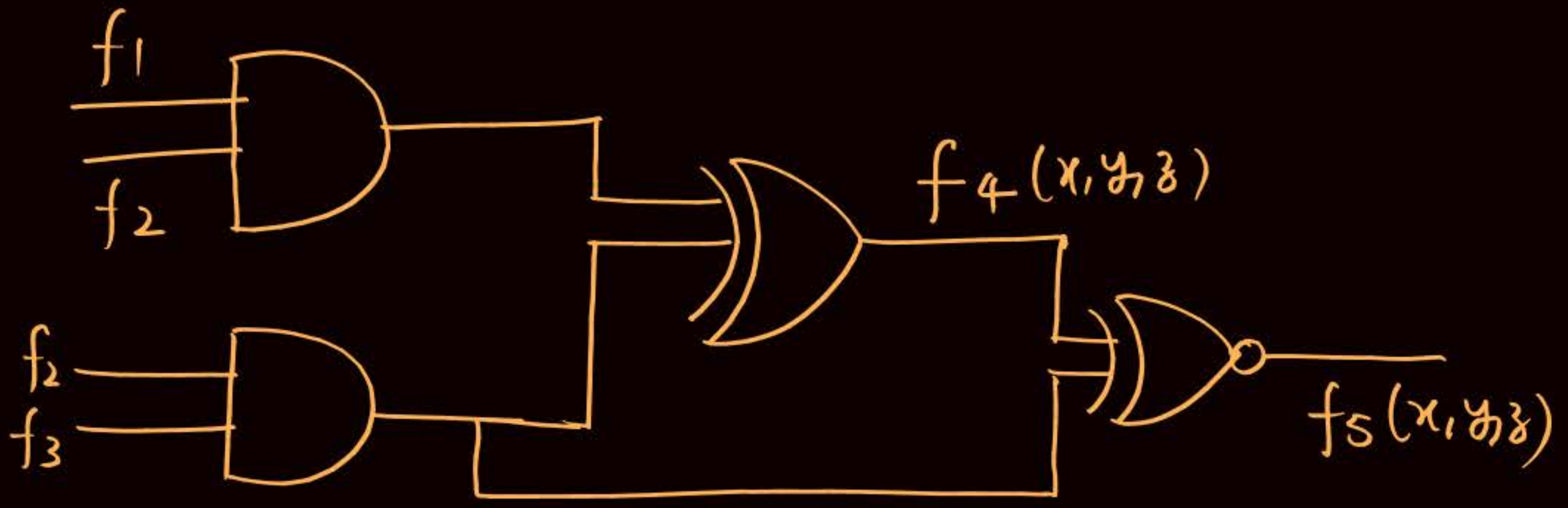
#Q. $f(x,y,z) = \bar{x}y + yz + \bar{x}z \longrightarrow$ self dual or not

#Q. $f(x,y,z) = \bar{x}\bar{y} + yz + \bar{x}z \longrightarrow$ self dual or not.

#Q. $f_1(x,y,z) = \Sigma(0,1,2,4)$

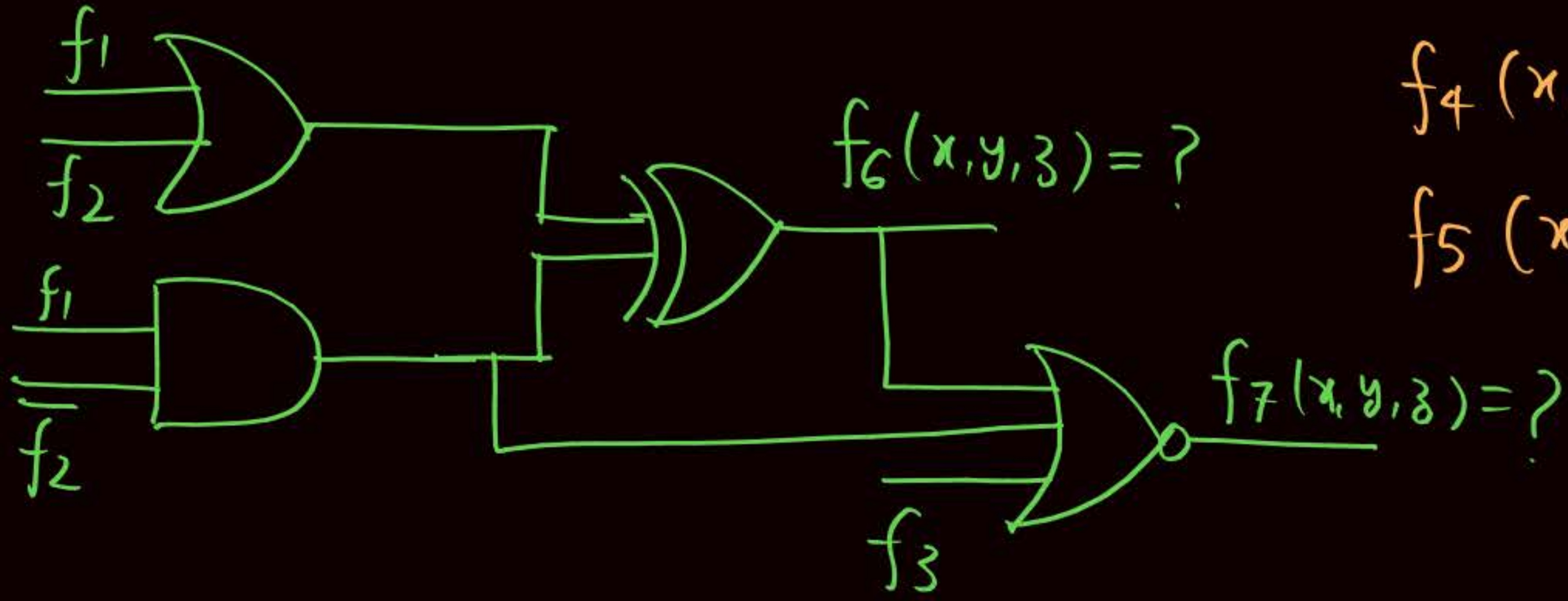
$f_2(x,y,z) = \Sigma(0,2,4,6,7)$

$f_3(x,y,z) = \Sigma(1,2,3,5,6)$



$f_4(x,y,z) = \Sigma\ ?$

$f_5(x,y,z = \Sigma\ ?$



2 Minute Summary

→ H.A & F.A.

Thank you

GW Soldiers !