COMPUTER SCIENCE & IT

DIGITAL LOGIC

Lecture No. 11

Combinational Circuit

By- Chandan Gupta Sir

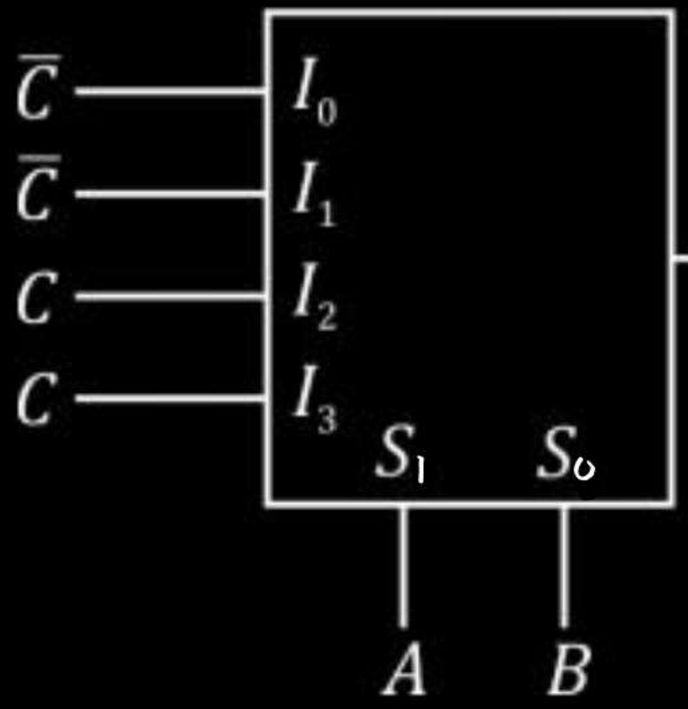
MUX & Question Discussion

DeMUX

Question Discussion Cont.

Question 7

A digital circuit is as given below :



$$y = \overline{A}\,\overline{B}\cdot\overline{C} + \overline{A}B\cdot\overline{C} + A\overline{B}\cdot C + AB\cdot C$$
$$= \overline{A}\,\overline{C}(\overline{B}+B) + AC(\overline{B}+B)$$
$$= A \odot C$$

Output y is

(a) $A \oplus B \oplus C$ $\Rightarrow$ C

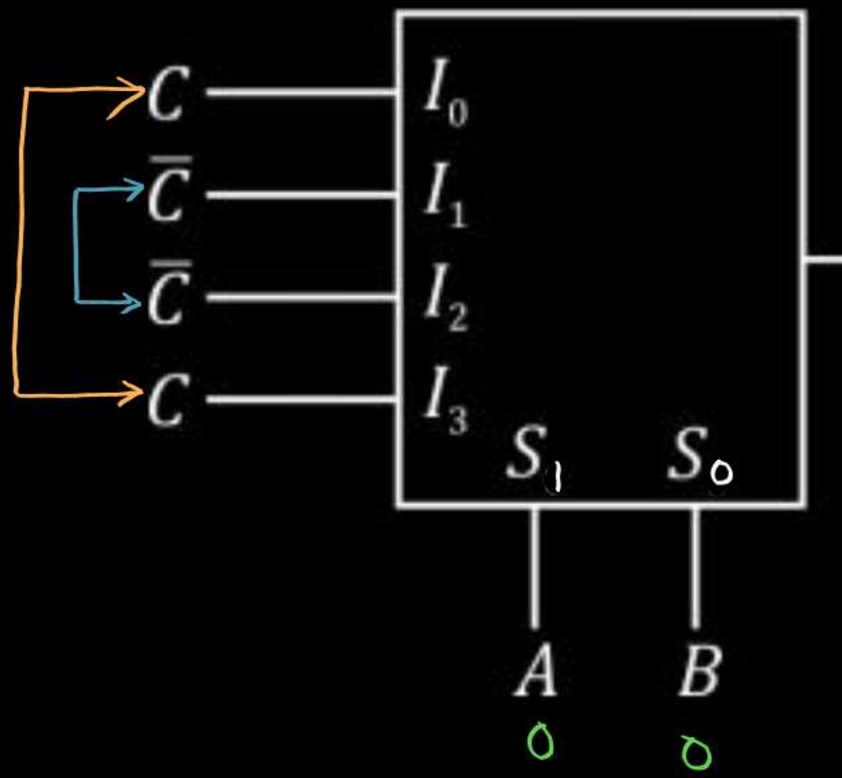
(b) $A \odot C$ $\Rightarrow$ $\overline{C}$, $\overline{C}$

(c) $A \odot B \oplus C$ $\overline{C}$ C

(d) $A \oplus B$ 0

Question 8

A digital circuit is as given below :



$= C \oplus S_1 \oplus S_0$

$y = \bar{A}\bar{B}\cdot C + \bar{A}B\bar{C} + A\bar{B}\cdot\bar{C} + ABC$

$= \Sigma(1,2,4,7) = A \oplus B \oplus C$

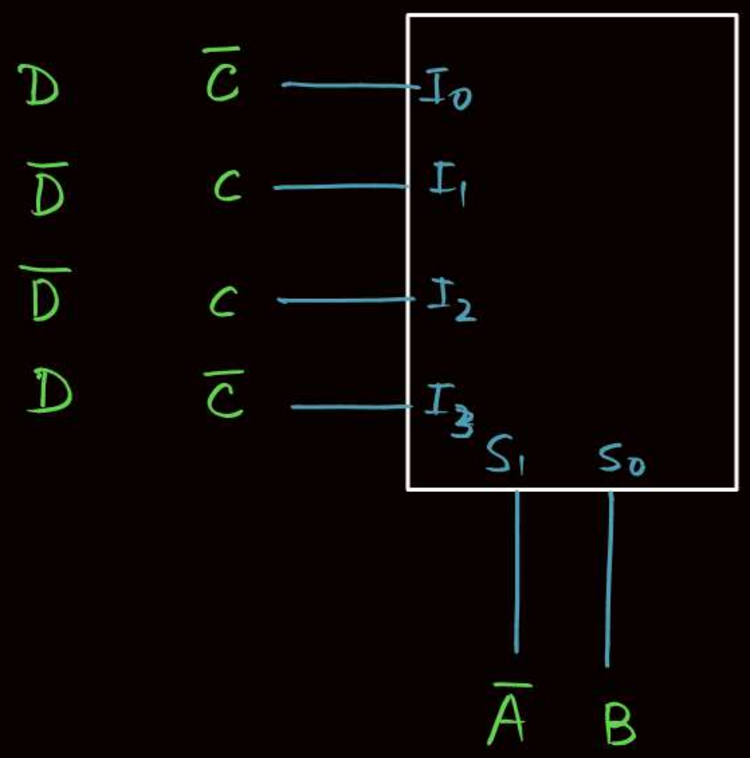
Output y is

(a) $A \oplus B \oplus C$

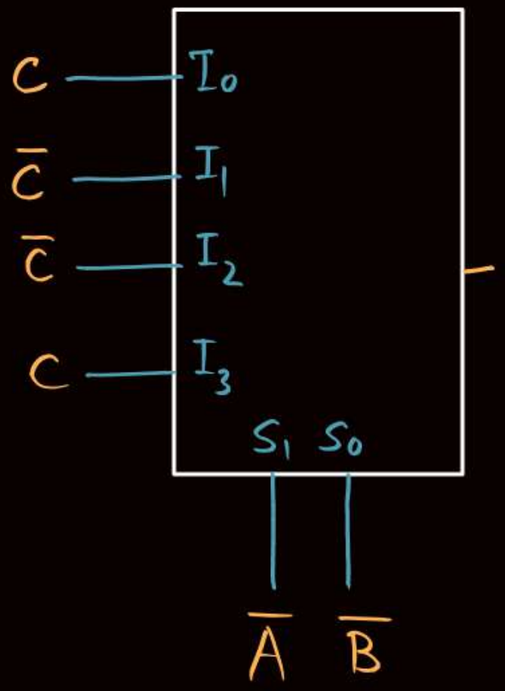
(b) $A \odot B \oplus C$

(c) $\overline{\overline{A \oplus B \odot C}}$

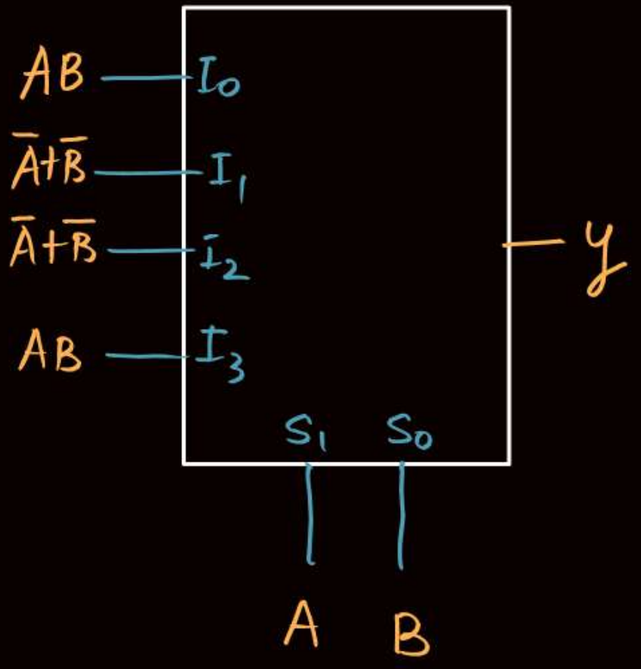
(d) $A \oplus B$



$$= D \oplus S_1 \oplus S_0$$
$$= \bar{C} \oplus \bar{A} \oplus B$$
$$= A \oplus B \oplus C$$



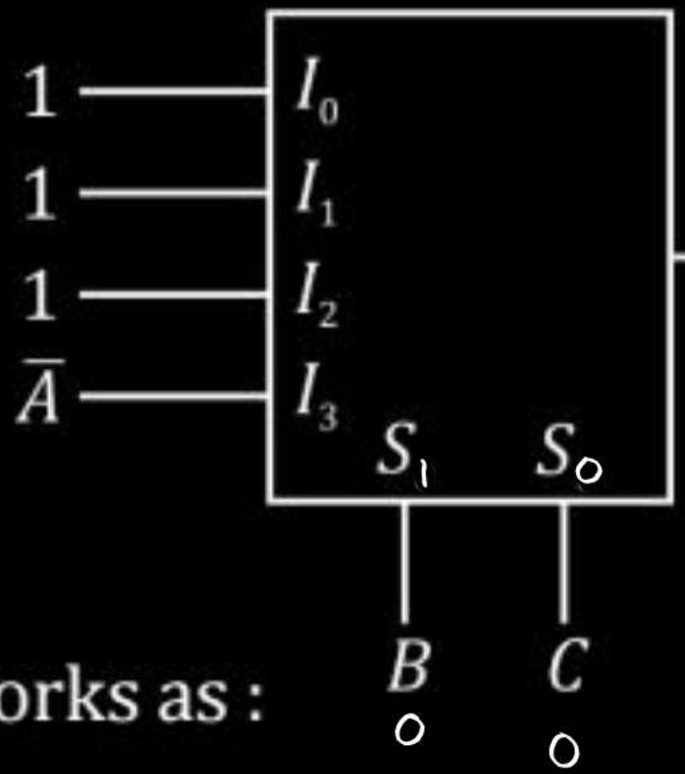
$$= C \oplus S_1 \oplus S_0$$
$$= C \oplus \bar{A} \oplus \bar{B}$$
$$= C \oplus A \oplus B$$
$$= A \oplus B \oplus C$$



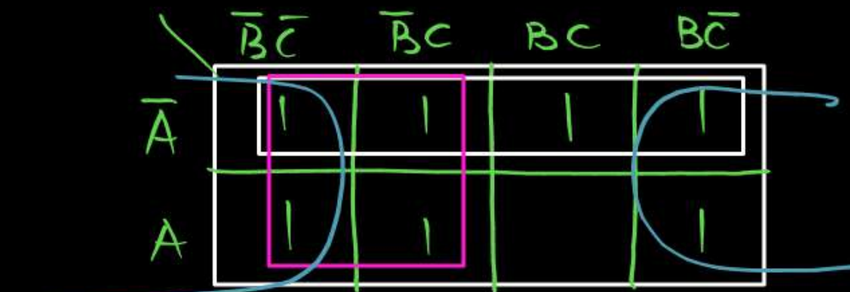
$$= AB \oplus S_1 \oplus S_0$$
$$= A \oplus B \oplus AB$$
$$= (A+B)$$

Question 9

A digital circuit is as given below :



$y = \bar{B}\bar{C}\cdot 1 + \bar{B}C\cdot 1 + B\bar{C}\cdot 1 + B\cdot C\bar{A}$



$= \pi(7)$

$= (\bar{A}+\bar{B}+\bar{C})$

$= \bar{A}+\bar{B}+\bar{C} = \overline{A\cdot B\cdot C}$

Above circuit works as :

(a) 3-input OR gate

(b) 3-input NOR gate

(c) 3-input AND gate

(d) 3-input NAND gate

Question 10

1001 → 9
1011 → 11

0001
0011

A digital circuit is as given below :

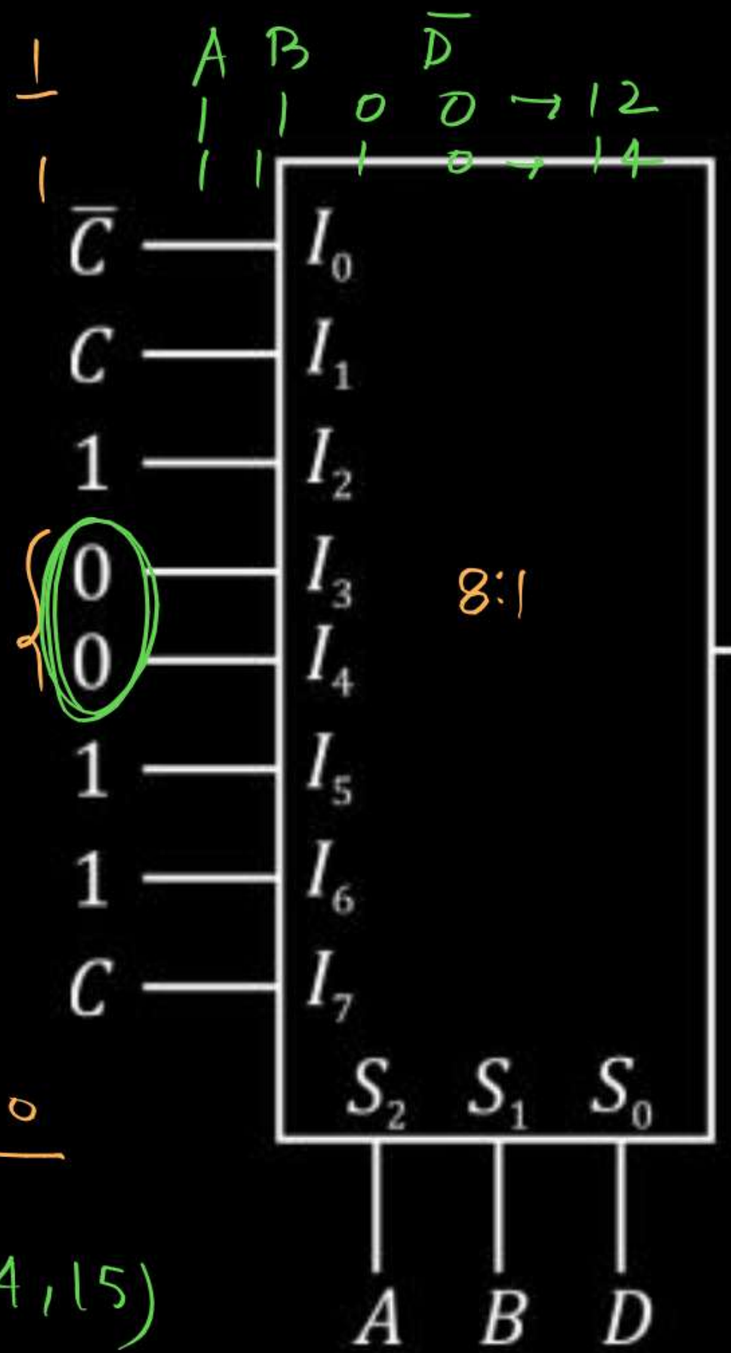
Output y will be : $y(A, B, C, D)$

(a) ~~$y = \Sigma (0,3,4,6,7,9,11,12,14,15)$~~

(b) ~~$y = \Sigma (0,1,3,4,6,8,9,11,12,14,15)$~~

(c) $y = \Sigma (0,3,4,6,9,11,12,14,15)$

(d) ~~$y = \Sigma (0,3,4,6,9,10,11,12,14,15)$~~



$y = A\bar{B}D \cdot 1 + AB\bar{D} \cdot 1 + ABD \cdot C \rightarrow 15$

$\bar{A}\bar{B}\bar{D}\bar{C} \rightarrow 0$

$+\bar{A}\bar{B}CD \rightarrow 3$

$+\bar{A}B\bar{1}\bar{D}$

0100 → 4
0110 → 6

1010

A=1, B=0, D=0

$= \Sigma(0,3,4,6,9,11,12,14,15)$

$\bar{A}BD \cdot 0$

$\bar{A}$ B D

0 1 0 1 → 5 }
0 1 1 1 → 7 } ✗

$A\bar{B}\bar{D} \cdot 0$

1 0 0 0 → 8 }
1 0 1 0 → 10 }

Question 11

A 4 : 1 multiplexer is used for generating output carry of a full adder. A and B are bits to be added while C_{in} is input carry and C_{out} is output carry. Which of the following is choice of signals at I_0, I_1, I_2, I_3.

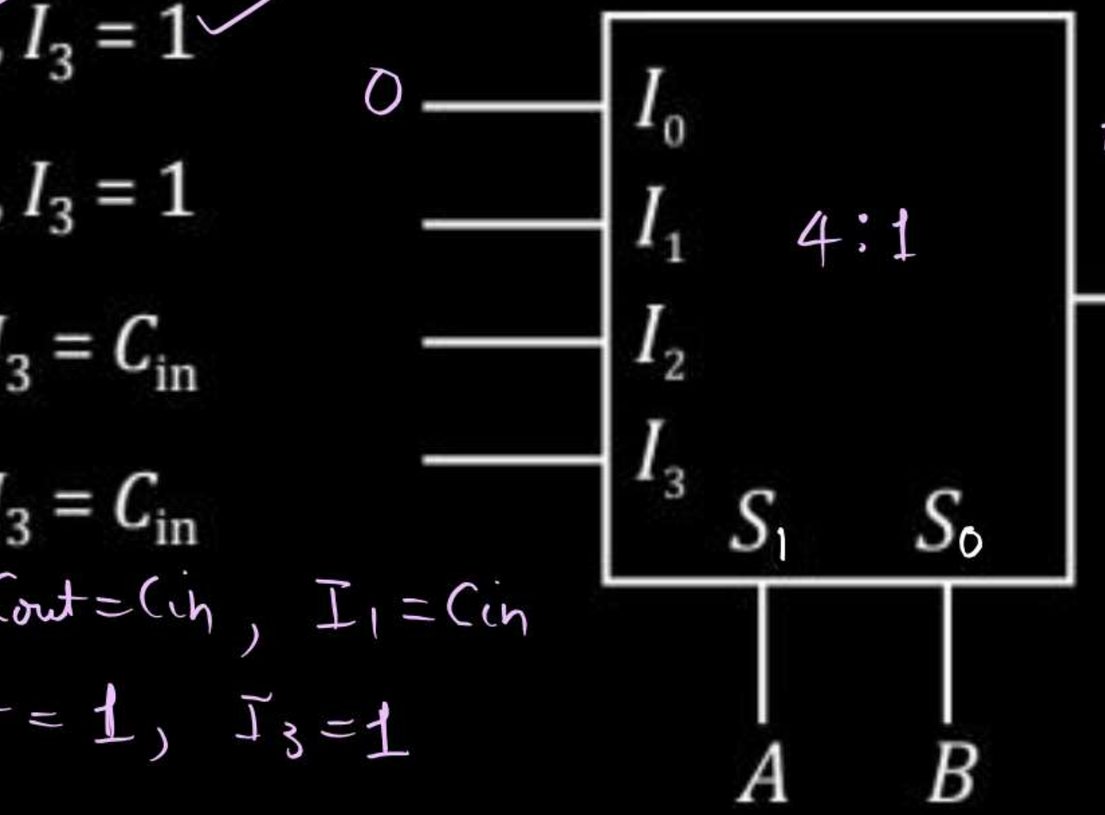
(a) $I_0 = 0, I_1 = C_{in}, I_2 = C_{in}, I_3 = 1$

(b) $I_0 = 1, I_1 = C_{in}, I_2 = C_{in}, I_3 = 1$

(c) $I_0 = C_{in}, I_1 = 0, I_2 = 1, I_3 = C_{in}$

(d) $I_0 = 0, I_1 = C_{in}, I_2 = 1, I_3 = C_{in}$

$C_{out} = AB + BC_{in} + AC_{in}$



$A=B=0 \Rightarrow C_{out} = 0$, $I_0 = 0$

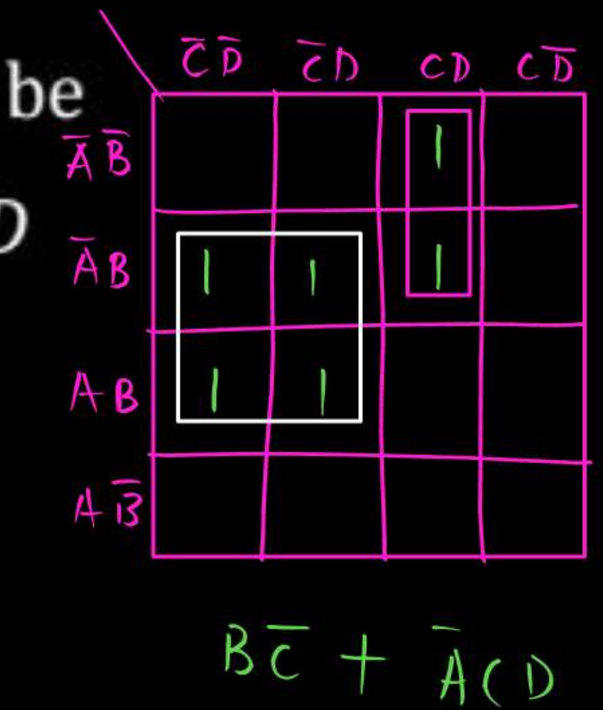
$A=1, B=0, C_{out} = C_{in}$, $I_2 = C_{in}$

$A=0, B=1, \Rightarrow C_{out}=C_{in}, I_1=C_{in}$

$A=1, B=1, C_{out}=1, I_3=1$

Question 12

A digital circuit is as given below :



$y\,(A, B, C, D)$ will be

(a) $A\bar{B}C + A\bar{C}D$

(b) $BC + A\bar{B}D$

(c) $B\bar{C} + \bar{A}CD$

(d) $\bar{B}C + A\bar{B}D$

$B\bar{C} + \bar{A}CD$

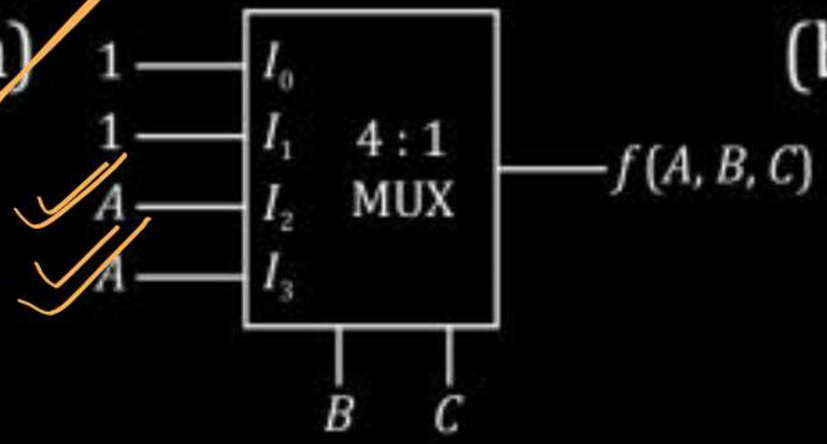
$= \bar{A}\bar{B}CD + \bar{A}B\bar{C}\cdot 1 + \bar{A}BC\cdot D + AB\bar{C}\cdot 1$

Question 13

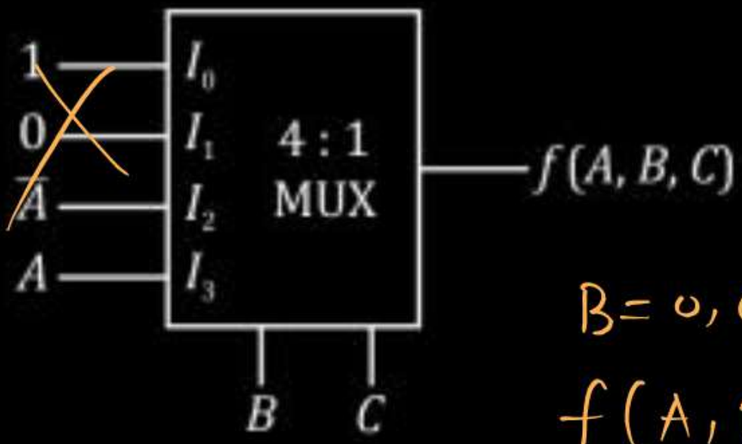
A logical function is given as : $f(A, B, C) = \overline{\bar{A}B + B\bar{C}} + AB$

Its implementation using MUX is given below. Then which implementation is correct

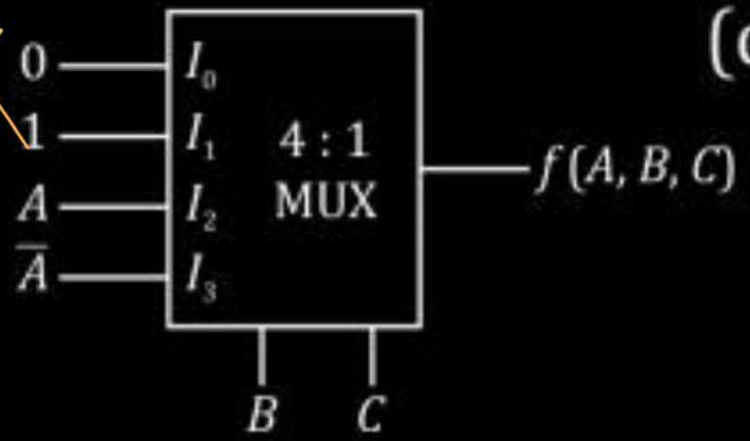
(a)



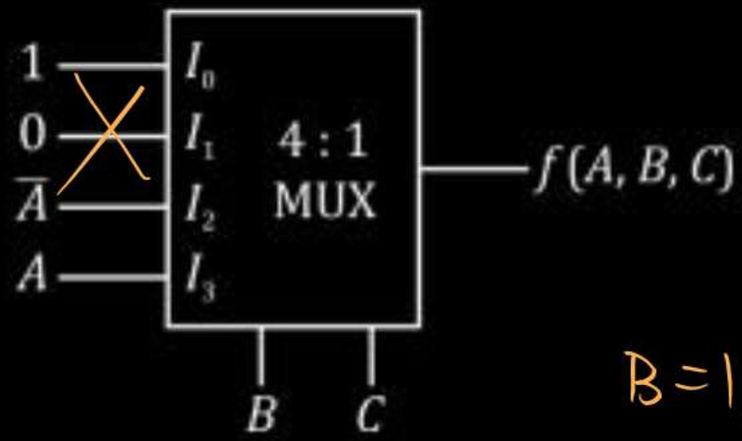
(b)



(c)



(d)



		I_0	I_1	I_2
0	$\bar{A}$	0	1	2
1	A	4	5	6

$B = 0, C = 0$

$f(A, B=0, C=0)$

$= 1, \quad I_0 = 1$

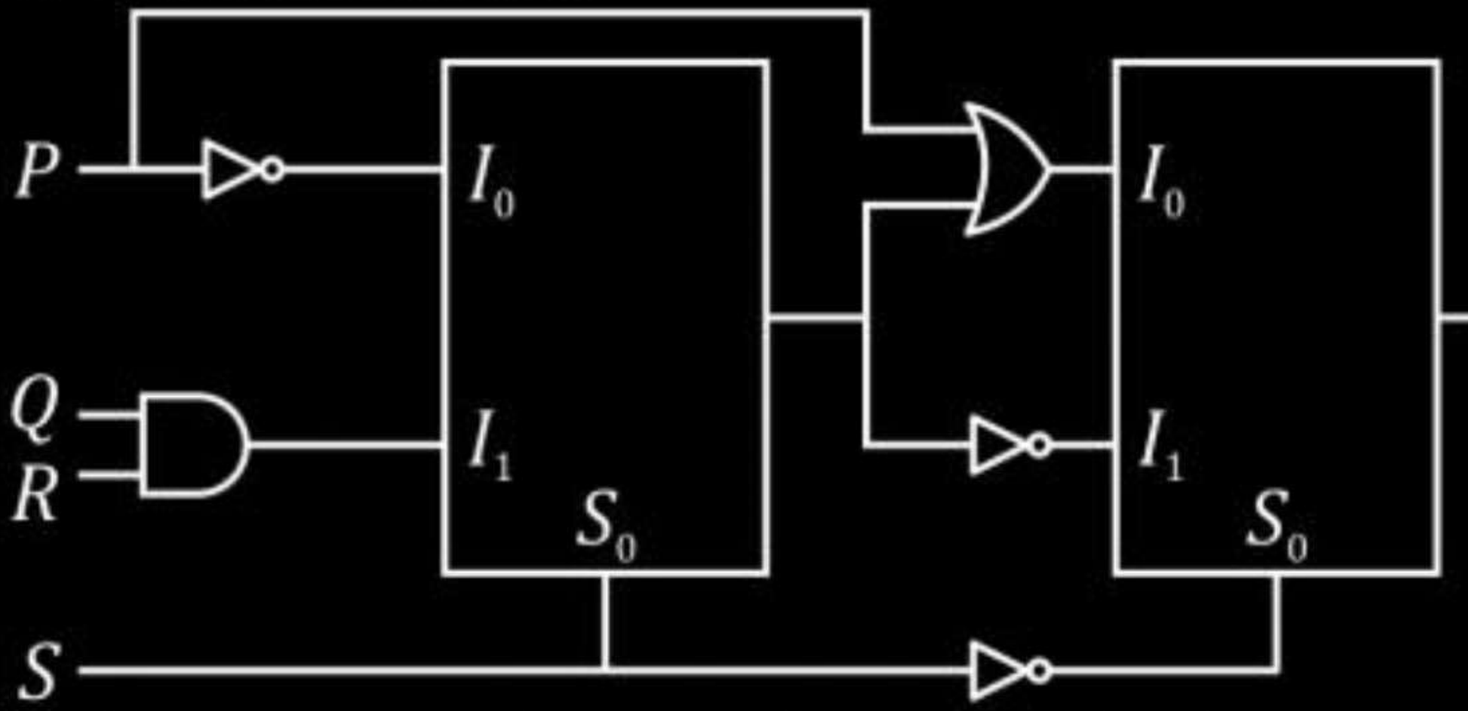
$B = 0, C = 1, \quad f(A, B, C) = I_1 = 1$

$B = 1, C = 0 \quad f(A, B, C) = A \quad I_2 = A$

$B = 1, C = 1 \quad f(A, B, C) = A \quad I_3 = A$

Question 14

A MUX circuit is as given below :



y = 18 nsec – I

y = 17.5 nsec – II

Delay of each NOT gate t_{not} = 4 nsec, delay of AND gate is t_{AND} = 3 nsec, delay of OR gate is t_{OR} = 4.5 nsec and delay of each MUX is 5 nsec. If P, Q, R, S are applied at t = 0, then maximum delay in generating output y is 18 nsec.

H.A. and F.A. using 2 : 1 MUX

- H.A. using 2 : 1 MUX :

$S = x \oplus y \longrightarrow 2\ (2:1)\ MUX$
$C = x \cdot y \longrightarrow 1\ (2:1)\ MUX$
} 3 (2:1) MUX

Note :- 3 (2:1) MUX is required to implement H.A or H.S.

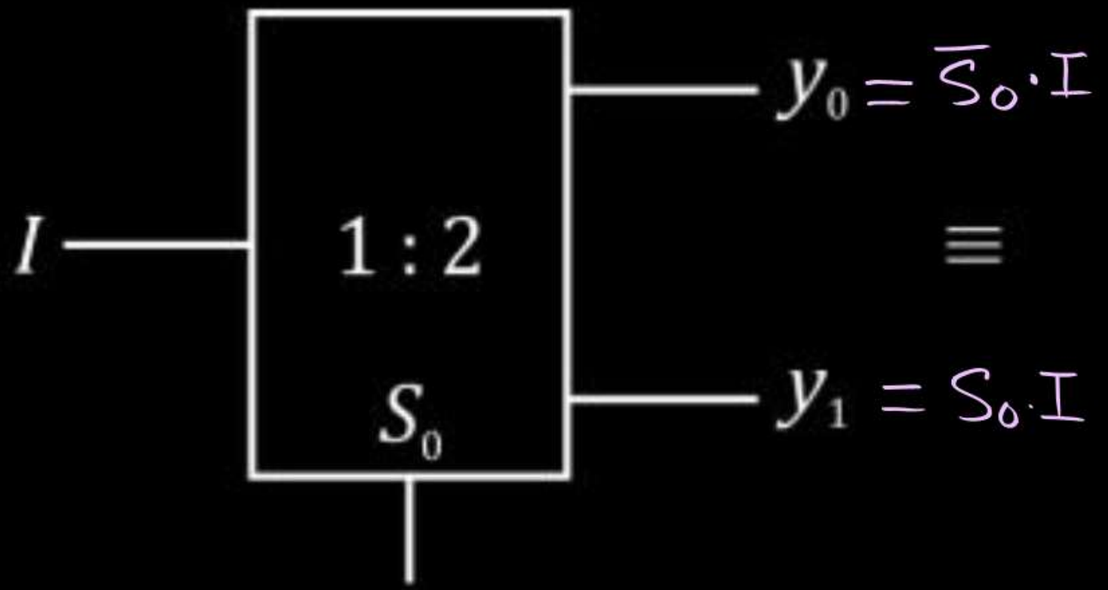
- 7 (2:1) MUX is required to implement F.A or F.S.

DeMUX

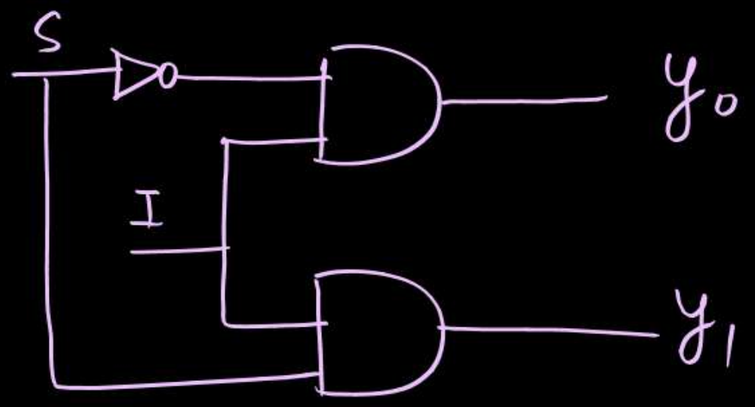
What is DeMUX ?

↳ It is combinational CKt having one i/p & many o/p and on the basis of select line i/p is transferred to one of the o/p line.

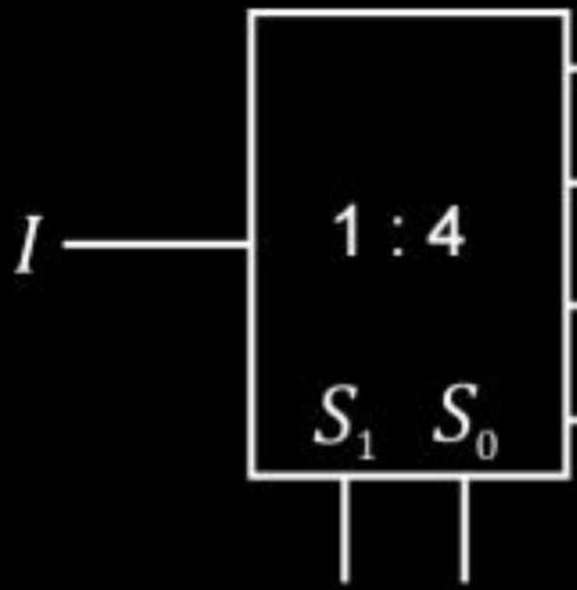
- 1 : 2 DeMUX



Internal Circuit



- 1 : 4 DeMUX



$y_0 = \overline{S_1}\,\overline{S_0} \cdot I$

$y_1 = \overline{S_1} S_0 \cdot I$

$\equiv$

$y_2 = S_1 \overline{S_0} \cdot I$

$y_3 = S_1 S_0 I$

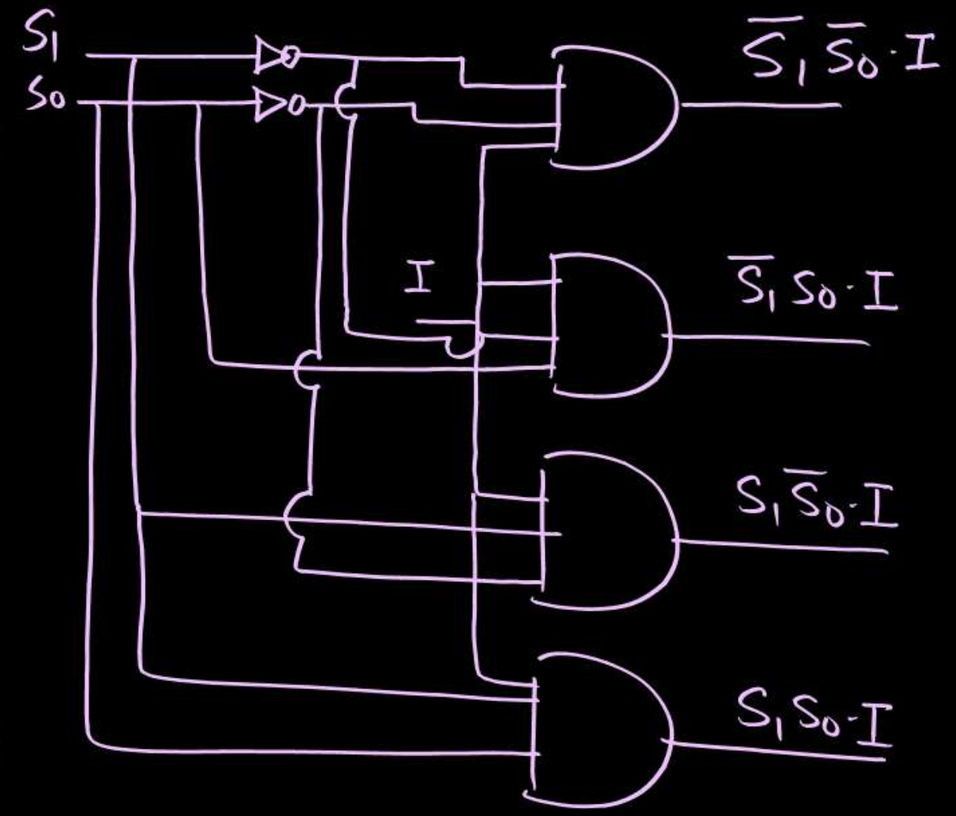
$S_1 = 1,\ S_0 = 0 \Rightarrow y_0 = 0$

$y_1 = 0$

$y_2 = I$

$y_3 = 0$

Internal Circuit



Higher order DeMUX using lower order DeMUX

- $1:4$ ($1:2^2$) $\xrightarrow{\text{Using } 1:2}$ $2+1=3=2^2-1$
- $1:8$ ($1:2^3$) $\xrightarrow{\text{Using } 1:2}$ $4+2+1=7=2^3-1$
- $1:16$ ($1:2^4$) $\xrightarrow{\text{Using } 1:2}$ $8+4+2+1=15=(2^4-1)$
- $1:2^n$ $\xrightarrow{\text{Using } 1:2}$ (2^n-1)

- $1:16 \xrightarrow{\text{Using } 1:4} 4+1$
- $1:32 \xrightarrow{\text{Using } 1:4} \underset{(1:4)}{(8+2)} + 1(1:2) = 11(1:4)$

  One (1:4) will be used as (1:2)
- $1:64 \xrightarrow{\text{Using } 1:8} 8+1$
- $1:256 \xrightarrow{\text{Using } 1:8} \underset{\downarrow (1:8)}{(32+4)} + 1(1:4) = 37(1:8)$

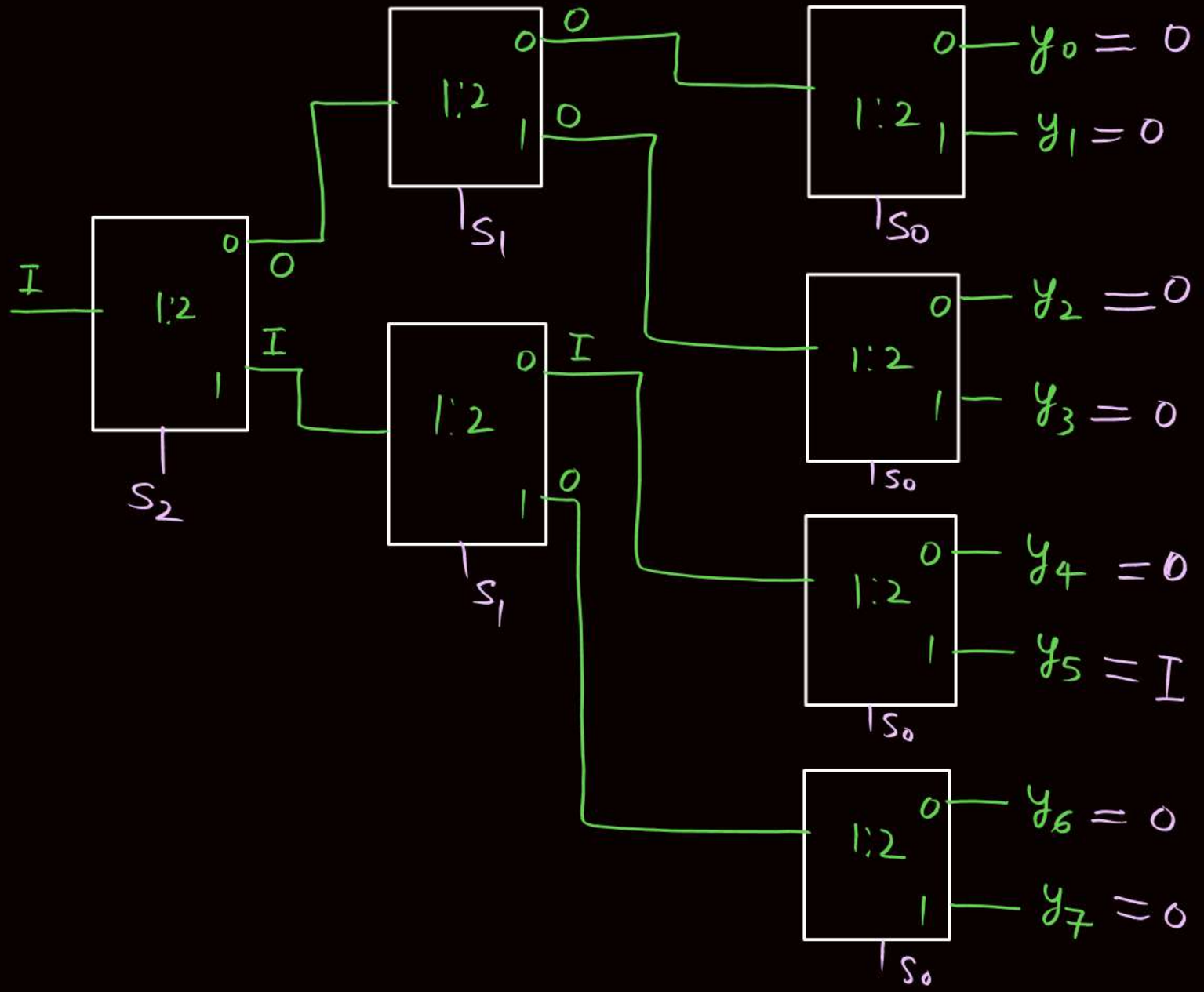
  ↳ One (1:8) will be used as (1:4).

(1:8) $\xrightarrow{1:2}$ 4 + 2 + 1

↳ S_2, S_1, S_1

↳ I, $y_0 - y_7$

$S_2 S_1 S_0 = 101$



Q. Implement (1:8) DeMUX using (1:4) DeMUX.

Q. Implement (1:32) DeMUX using (1:8) DeMUX.

2 Minute Summary

- MUX & Question Discussion
- De MUX.

Thank you

GW

Soldiers !