COMPUTER SCIENCE & IT

DIGITAL LOGIC

Sequential Circuits

Practice Sheet 01 Discussion Notes

By- Chandan Gupta Sir

Question MCQ

★☆☆

In a S-R flip-flop, the present output is Q = 1. then after applying input S = 0, R = 1 and then S = 0, R = 0, output will be:

$Q(n) = 1$

$S=0, R=1 \longrightarrow Q(n+1) = 0$

$S = 0, R = 0 \longrightarrow Q = 0$

A ✓ Q = 0

B Q = 1

C Q = → invalid state

D None of these

Question **MSQ**

In a JK flip-flop output Q = 0. To change it to Q = 1, the inputs J and K will be:

$Q(n)=0 \longrightarrow 1 \quad Q(n+1)$

A J = 1, K = 1

B J = 1, K = X

C J = 0, K = 0

D J = 0, K = 1

$J=1 \qquad K=X$

$J=1,\ K=1 \rightarrow$

$J=1,\ K=0 \rightarrow$ $J=1,\ K=X$

Question MCQ

Which of the following is true?

A S = 1, R = 1, is a valid state input for S-R ff

B J = 1, K = 1 is a invalid state input for J-K ff

C Input (0, 0) is hold state input for both S-R as well as JK ff

D None of these

Question **MCQ**

A flip flop has characteristic equation

$Q(n+1) = \bar{A}\bar{Q} + \bar{B}Q$

Then it will be in toggle mode of operation if

$B = 1, A = 0$

$Q(n+1) = \bar{Q} \rightarrow$ toggle mode of operation

$Q(n+1) = \bar{0}\,\bar{Q} + \bar{1}\,Q = \bar{Q} + 0 = \bar{Q}$

A A = 1, B = 1

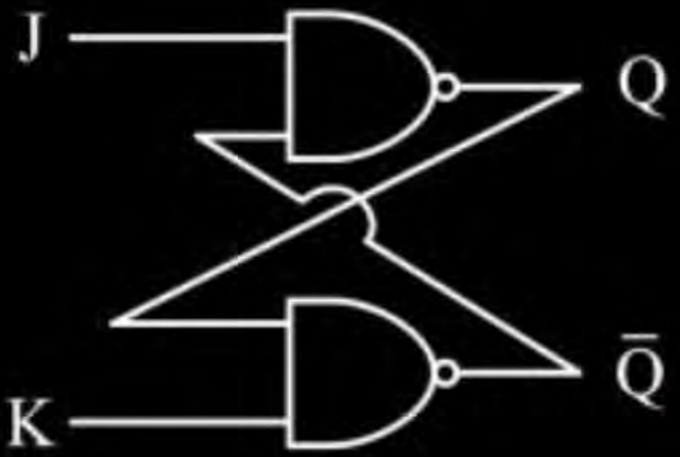
B A = 0, B = 1 ✓

C A = 1, B = 0

D A = 0, B = 0

Question MCQ

A logic circuit is as given below:



Then which of the following is true about above circuit?

A Race around condition at J = 1, k = 1 ✗

B Race around condition at J = 0, k = 0 ✗

C J = 1, K = 1 is invalid state input ✗

D None of these ✓

NAND S = 0, R = 0 → invalid state

NOR → S = 1, R = 1 → invalid state

Question **MCQ**

In J-K FF, to change output from 0 to 1 input is changed from

A. J = 0, K = 0 to J = 0, K = 1

B. J = 0, K = 1 to J = 1, K = 0

C. J = 0, K = 1 to J = 0, K = 0

D. J = 1, K = 0 to J = 0, K = 1

$J=0, K=1 \longrightarrow 0$

$J=1, K=0 \longrightarrow 1$

$J=0, K=0$] 0, 1

$J=1, K=0$] 1

Question MCQ

Which of the following statement is true?

A Master-Slave ff is used to avoid race-around condition.

B Edge triggered J-K FF has problem of race-around condition when J = 1, K = 1

C Race-around condition occurs in S-R ff with S = 1, R = 1

D None of these

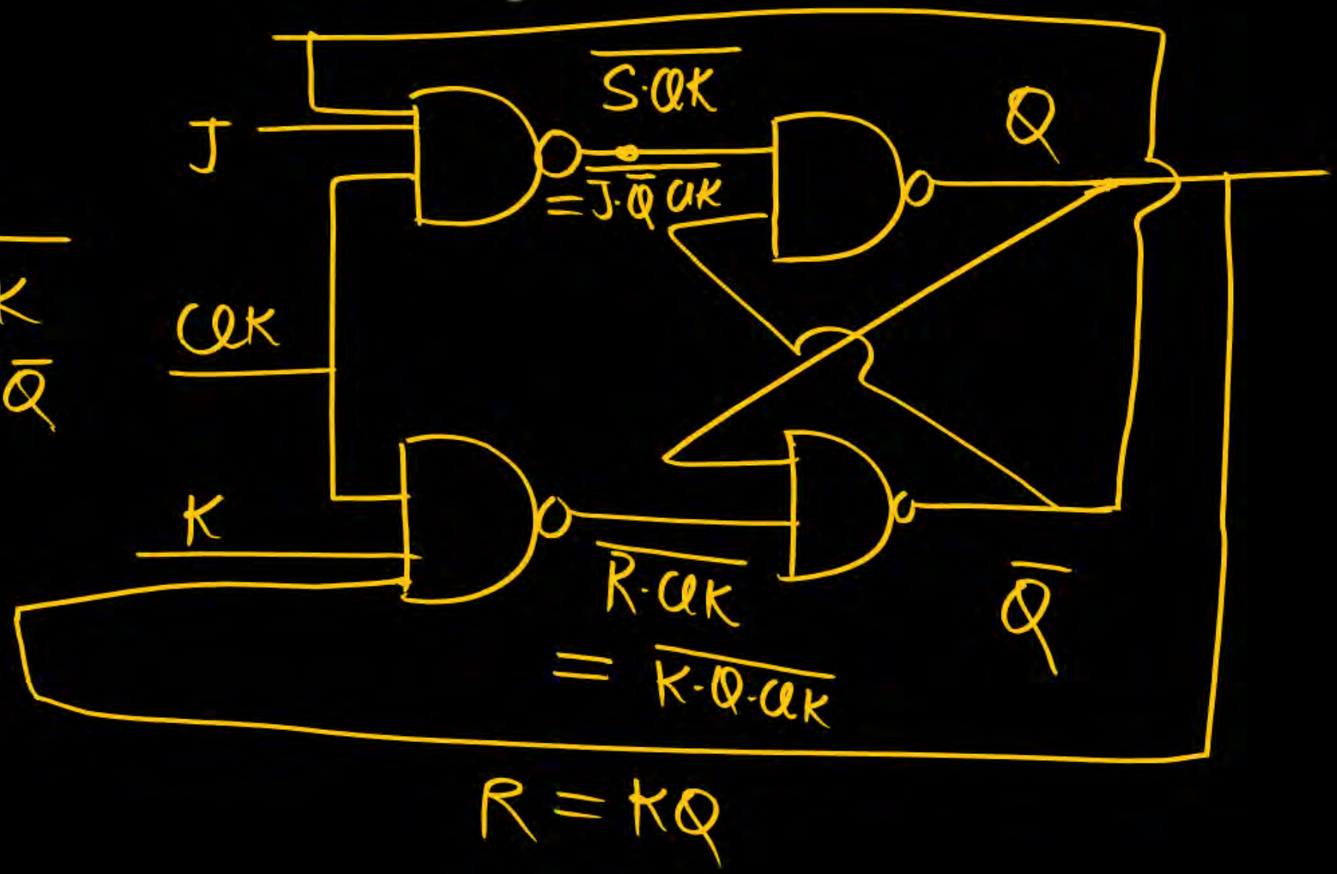
Question **MCQ**

To solve the problem of invalid state at input S = 1 and R = 1 in S-R ff, S and R are replaced by

$\overline{S \cdot CLK}$

$\overline{(J\bar{Q}) \cdot CLK}$

$S = J\bar{Q}$



A $S = J\bar{Q}, R = \bar{K}Q$

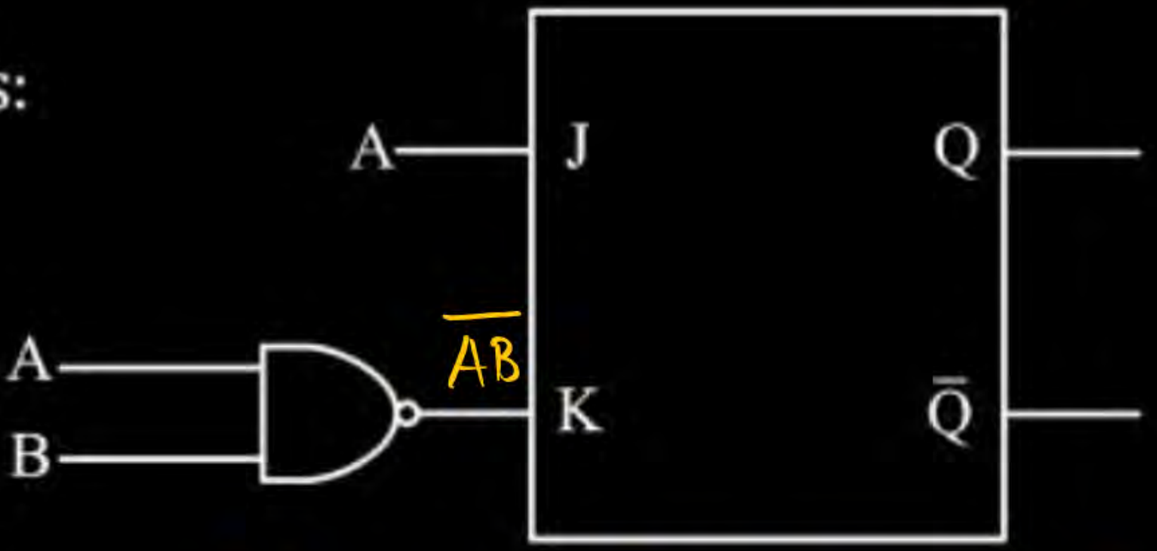
B $S = J\bar{Q}, R = KQ$

C $S = JQ, R = \bar{K}Q$

D $S = JQ, R = K\bar{Q}$

Question **MCQ**

In J-K FF, J and K inputs are given as:



Then which of the following is true?

A $Q(n+1) = A\bar{Q} + AB$

B $Q(n+1) = A\bar{Q} + \bar{B}Q$

C $Q(n+1) = A \oplus B \oplus Q$

D $Q(n+1) = A \oplus B$

$Q(n+1) = J\bar{Q} + \bar{K}Q = A\bar{Q} + \overline{\overline{AB}}Q$

$= A\bar{Q} + ABQ$

$= A[\bar{Q} + (B \cdot Q)]$

$= A[(\bar{Q}+B)\cdot(\bar{Q}+Q)]$

$= A[\bar{Q}+B]$

$Q(n+1) = A\bar{Q} + AB$

Question MCQ

★★☆

Which of the following is true?

A $Q(n+1) = S + \bar{R}Q$ is valid for all S and R values → $S \cdot R = 0$

B $Q(n+1) = J\bar{Q} + \bar{K}Q$ is valid when J.K = 1

C $Q(n+1) = S + \bar{R}Q$ is valid when $S \cdot R = 1$

D $Q(n+1) = S + \bar{R}Q$ is valid when $S \cdot R = 0$

Question MCQ

★☆☆

A counter sequence is given as:
2 – 3 – 1 – 0 – 4 – 7, then MOD no. of the counter is

MOD no. = Total no. of different states

MOD no. = 6

A 7

B 6

C 5

D 4

Question **NAT**

A counter sequence is given as:

3 – 2 – 1 – 4 – 6 – 3 – – – – – –

If its starting state is $(100)_2$ then after application of 1049 clock pulses, counter will be at ___(__1__)$_{10}$___.

3 – 2 – 1 – 4 – 6 $\Rightarrow$ MOD no = 5

Starting state $= (100)_2 = (4)_{10}$

$(4)_{10} \xrightarrow{5\text{ clk}} (4)_{10} \xrightarrow{5\text{ clk}} (4)_{10}$

$(4)_{10} \xrightarrow[209\times5]{1045} (4)_{10} \xrightarrow{1046} 6 \xrightarrow{1047} 3 \xrightarrow{1048} 2 \xrightarrow{1049} 1$

Question **NAT**

A sequential circuit is as given below:

Value of fout will be 2.75 MHz.

Counter sequence :

1 – 2 – 9 – 11 $\Rightarrow$ MOD no = 4

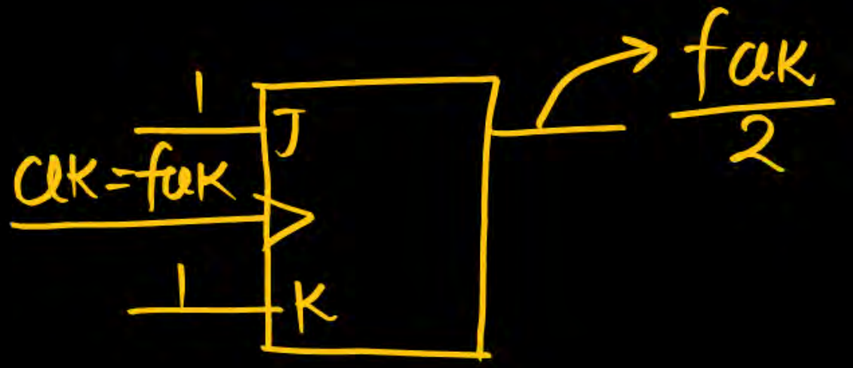
$f_{out} = \frac{11 MHz}{4}$

$= 2.75 MHz$

Question MCQ

★★☆

Which of the following is not true?



A In asynchronous counter different FFs are driven by different clock — True

B In asynchronous counter at output of each FF input frequency is divided by 2 — True

C The sequence 0 – 1 – 3 -2 require 2 FFs to design it with asynchronous counter → not true

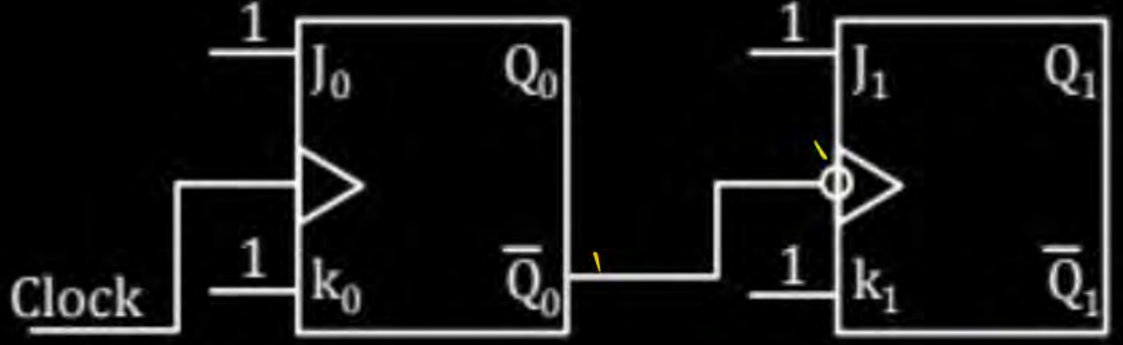
D Fixed up sequence and fixed down sequence is possible to design with asynchronous counter → True

Question MCQ

★★☆

2 FFs → Total state = $2^2 = 4$

A sequential circuit is as given below:
The above circuit is



$\overline{Q}_0 \rightarrow (1 - 0)$

$Q_0 \rightarrow (0 \rightarrow 1)$

A MOD-4 up counter

B MOD-4 down counter

C MOD-4 neither up nor down counter

D MOD-2 counter

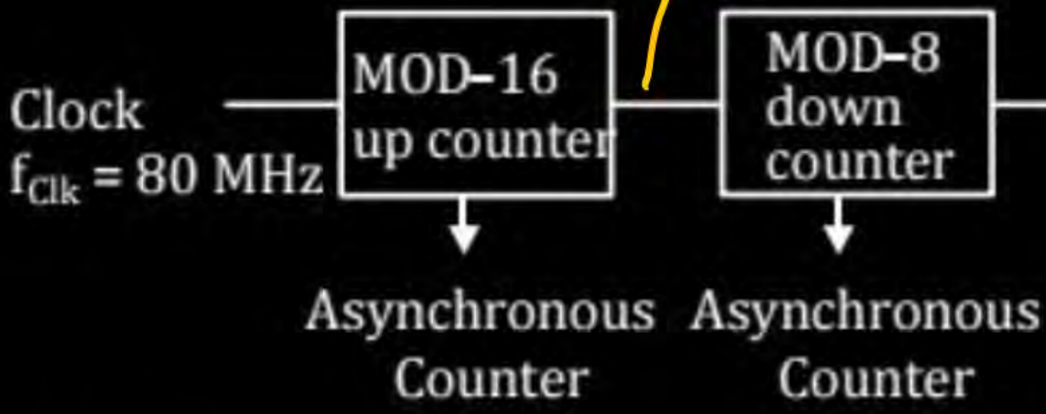
$Q_0 \rightarrow$ toggles at every clk

$Q_1 \rightarrow$ toggle when $\overline{Q}_0$ $(1-0) \longrightarrow Q_0 \rightarrow (0-1)$

	Q_1	Q_0
	0	0
clk-1	1	1
clk-2	1	0
clk-3	0	1
clk-4 →	0	0

Question MCQ

A sequential circuit as given below:
Value of f_{out} will be



$f_1 = \frac{f_{clk}}{16} = 5\ MHz$

$= \frac{f_1}{8}$

$= \frac{5}{8}$

$= 0.625\ MHz$

A Can not be calculated as one block is up-counter and other is down counter

B 5 MHz

C 0.625 MHz

D 3.33 MHz

Question MCQ

MOD-12 counter can be designed

$M = N_1 \cdot N_2$

A Cascading two MOD-6 counter ✗ [36]

B Cascading MOD-4 counter and MOD-8 counter ✗ [32]

C ✓ Cascading MOD-4 & MOD-3 counter 12

D Cascading MOD-3 & MOD-9 counter [27] ✗

Question NAT

★★☆

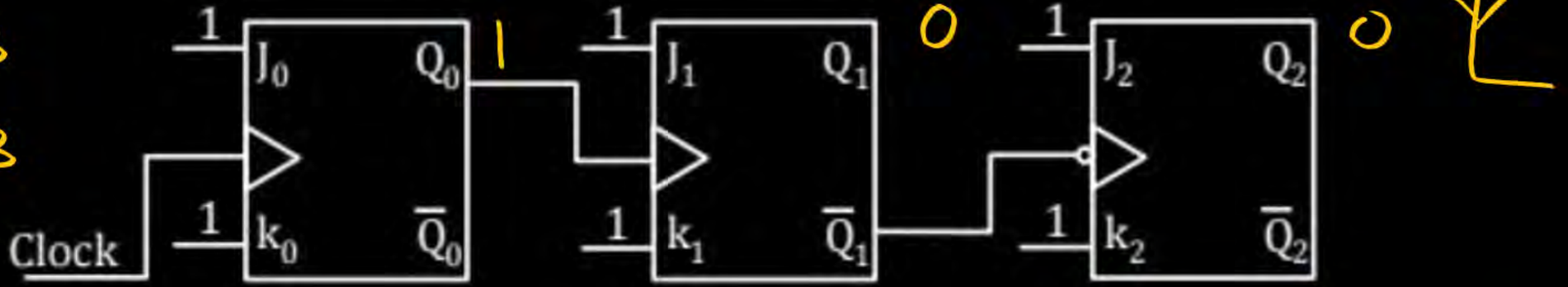
$2^3 = 8 \rightarrow$ MOD-8 down counter

$0 - 7$

A sequential circuit is as given below:

Initially counter is at $Q_0Q_1Q_2 = (100)_2$ then after 2 clock pulses, o/p will be

$\_\_\_(7)_{10}\_\_\_$.



$Q_0 \rightarrow$ LSB

$Q_2 \rightarrow$ MSB

	MSB Q_2	Q_1	LSB Q_0
	0	0	1
1st	0	0	0
2nd	1	1	1
3rd	1	1	0

$\rightarrow Q_2Q_1Q_0 = (011) = 3$

1 0 0

0 1 1

0 1 0 ✗

$\overline{Q}_1 \rightarrow (1 - 0)$

$\downarrow$

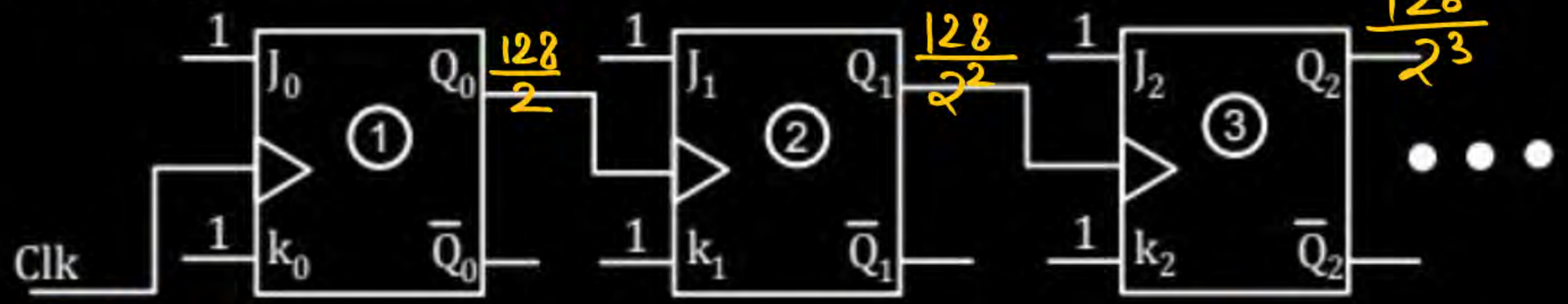
$Q_1 \rightarrow (0 - 1)$

Question MCQ

★★☆

2^{20} = MOD no
↳ down counter

A sequential circuit is as given below:
Total 20 FFs are connected as shown above:
If input clock frequency is 128 MHz then, at output of 16th FF frequency of the waveform will be:



= 128 MHz

$f_{16} = \frac{128}{2^{16}}$ MHz $= \frac{2^7}{2^{16}}$ MHz $= \frac{1}{2^9}$ MHz

$= \frac{1000}{512}$ KHz $= \frac{1000 \text{ KHz}}{2^9}$

A 8 MHz

B 12.8 MHz

C 1.95 KHz

D 4 MHz

Question NAT

★★☆

Sequential circuit A is designed with 5 FFs and sequential circuit –B is designed with 6-FFs, then maximum MOD no. possible combinedly using sequential circuit-A & sequential circuit-B is 2048.

Circuit-A → 5 FF ⟶ Max^m MOD no. $M_1 = 2^5 = 32$

Circuit-B — 6 FF → Max^m MOD no. $M_2 = 2^6 = 64$

Max^m MOD no combindly $M = M_1 \cdot M_2$ [Cascading]

$= 2^5 \times 2^6$

$= 2^{11} = 2048$

$= 2 \cdot 2^{10}$

Question NAT

★★☆

To design a MOD-224 counter, minimum no. of FFs required is 8.

$n \geq \log$ MOD no.

$n \geq \log_2 224 \Rightarrow n \geq 7.80$

$\lceil n \rceil \geq 8$

8 FFs $\longrightarrow 2^8$ states

$= 256$ states

Max^m n

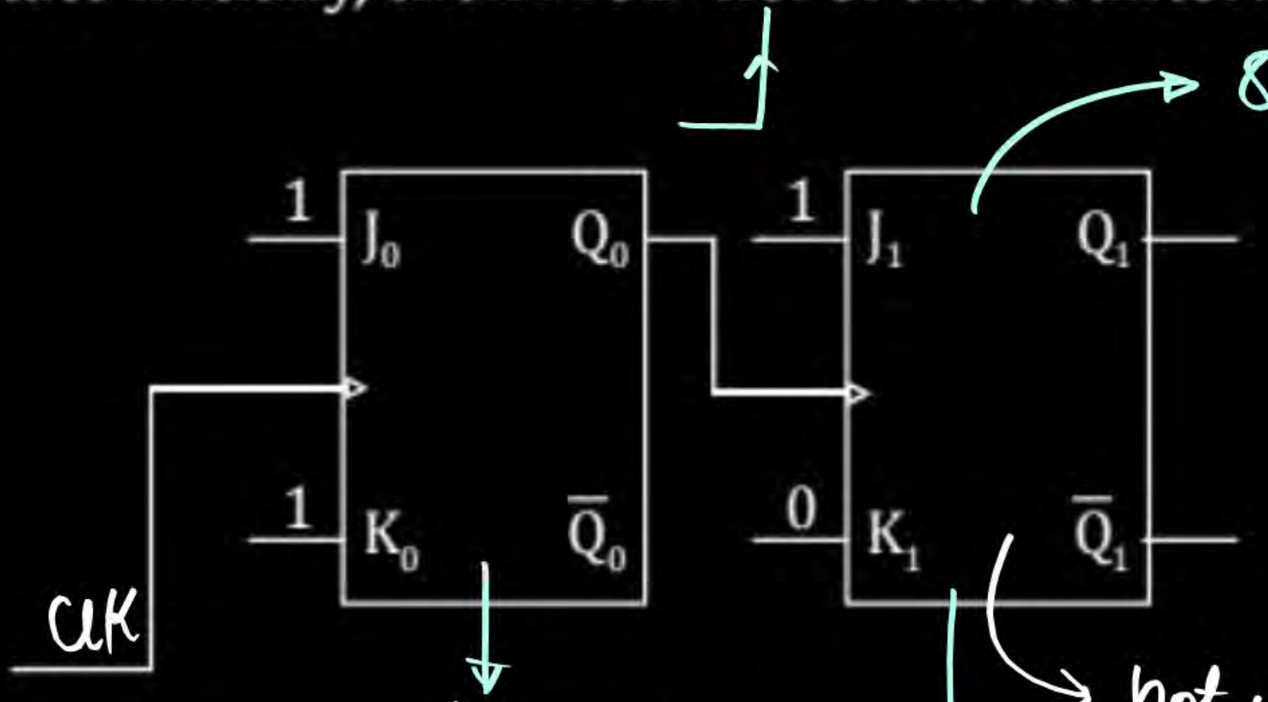
n FFs $\longrightarrow 2^n \longrightarrow$ 8 state

7 FFs $\longrightarrow 2^7$ states $= (128)$

Question MCQ

A sequential circuit is as given below:

Both the ffs are at reset state initially, then MOD-no. of the counter:



$Q_1(n+1) = J_1\overline{Q}_1 + \overline{K}_1 Q_1$

$= 1\cdot\overline{Q}_1 + \overline{0}\,Q_1$

$= \overline{Q}_1 + Q_1$

$= 1$

A MOD-4 counter

B MOD-3 counter

C MOD-2 counter

D None of these

	Q_1	Q_0
	0	0
Clk-1	1	1
Clk-2	1	0
Clk-3	1	1
Clk-4	1	0
Clk-5	1	1
Clk-6	1	0
Clk-7	1	1

0-2-3-0-2-3
-0-2-3

2-3-2-3-2-3

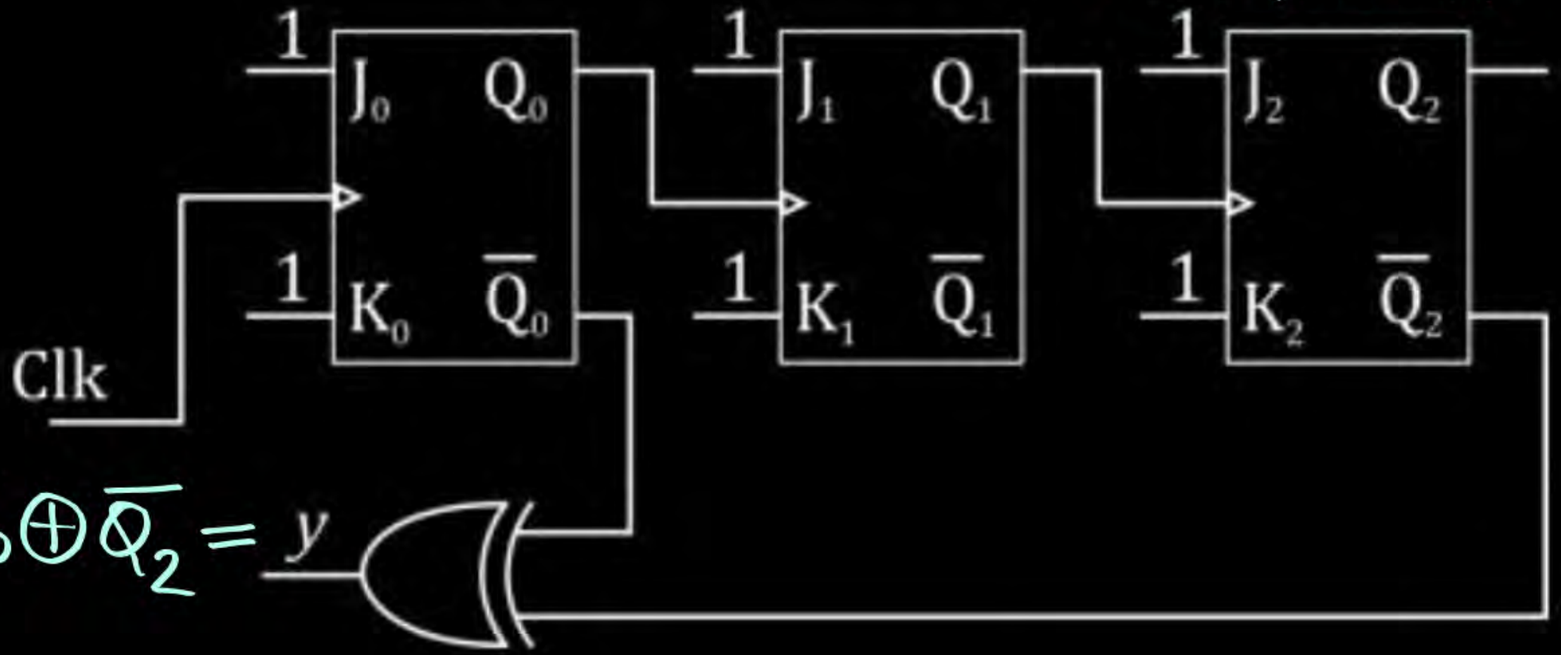
Question NAT

★★☆

A sequential circuit is as given below:

down counter
↳ MOD-2^3

$Q_2 Q_1 Q_0$



$Q_0 \oplus Q_2 = \overline{Q}_0 \oplus \overline{Q}_2 = y$

We have applied 32 clock pulses then number of times output y toggles is 24

	Q_2	Q_1	Q_0	y
	0	0	0	0
clk-1	1	1	1	0
clk-2	1	1	0	1
clk-3	1	0	1	0
clk-4	1	0	0	1
clk-5	0	1	1	1
clk-6	0	1	0	0
clk-7	0	0	1	1
clk-8	0	0	0	0

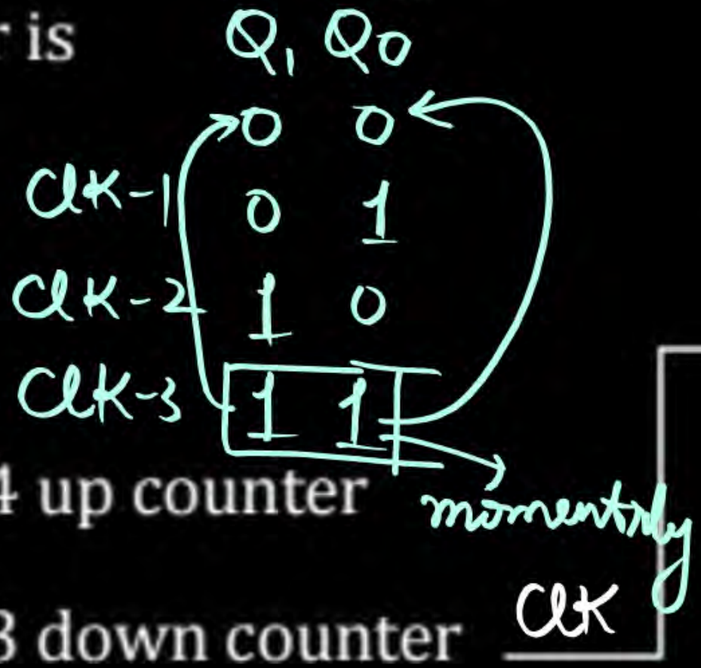
$\longrightarrow 6+6+6+6=24$

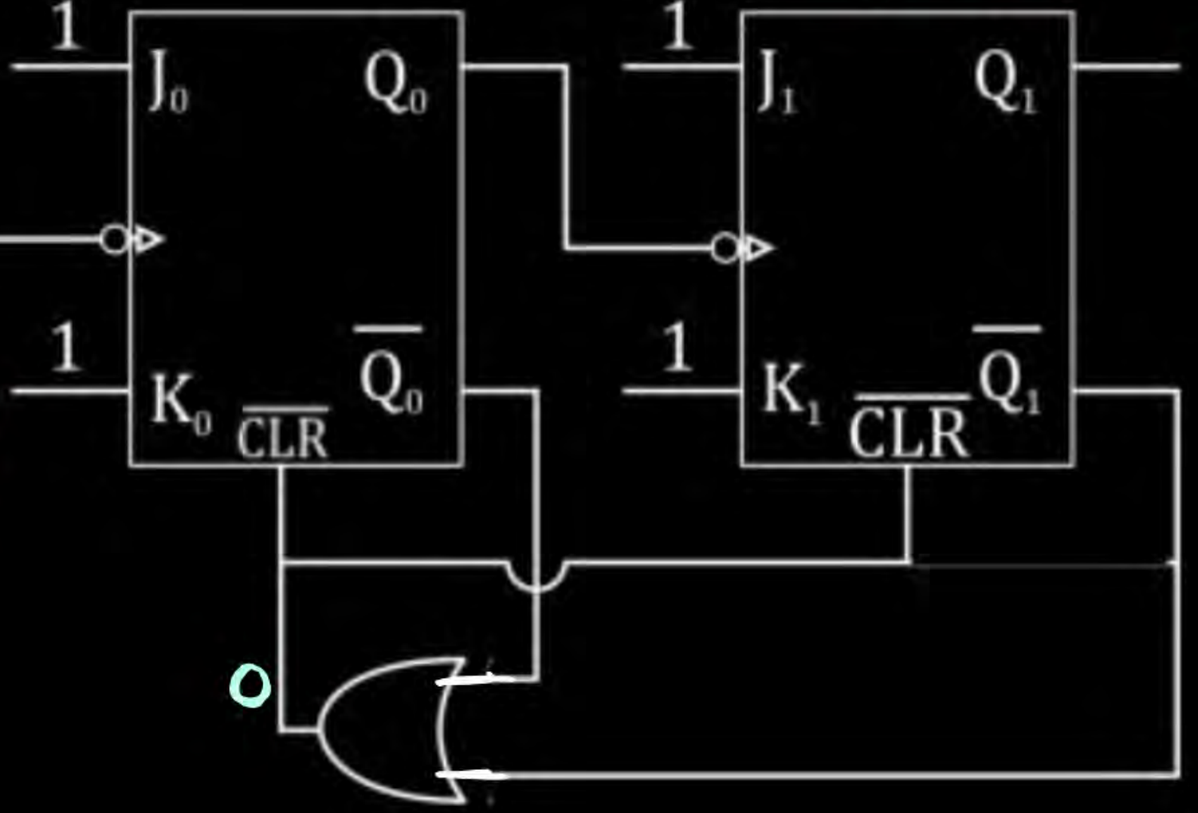
Question MCQ

★★☆

A sequential circuit is as given below:

The counter is





up-counter

$\overline{Q}_0 = 0 \rightarrow Q_0 = 1$

$\overline{Q}_1 = 0$ → CL pin activated $Q_1 = 1$

A Mod-4 up counter

B Mod-3 down counter

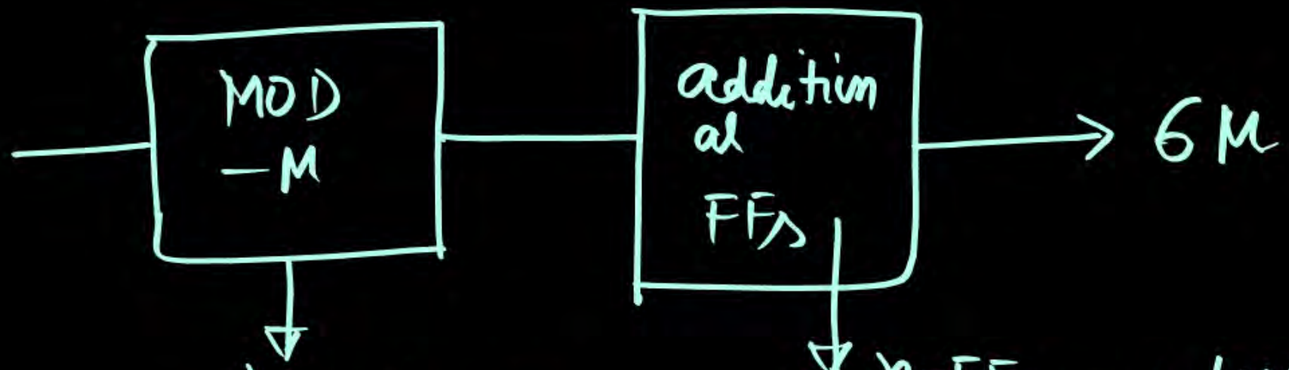
C Mod-3 up counter

D Mod-4 down counter

Question NAT

Asynchronous counter designed using 4-FFs has Mod number M. By adding FFs in cascade, we changed the MOD number to 6M, then the minimum number of additional FFs used is 3.

Asynchronous Counter → 4FF → Mod no = M



$n \geq 3$

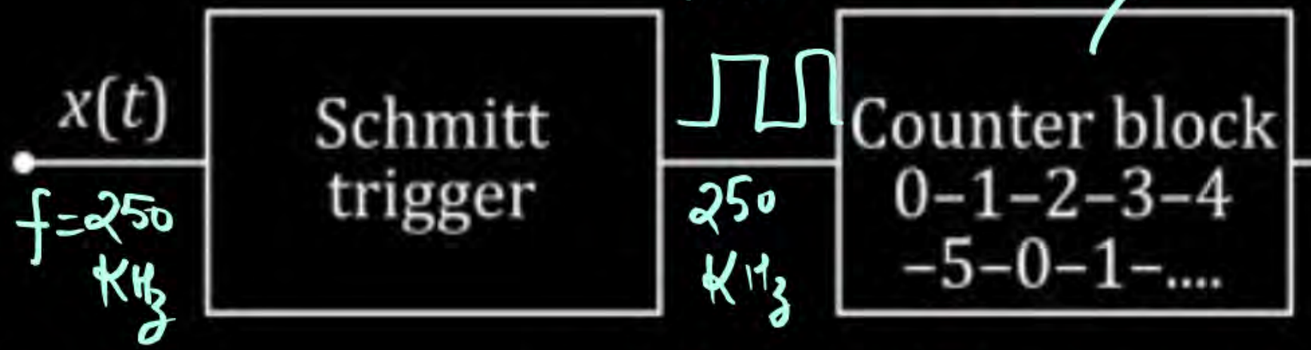
using this we have to design MOD-6 counter and for this $n \geq 3$

Question NAT

★★★

0-1-2-3-4-5-0-1-2-3-4-5

A sequential circuit is designed as shown:

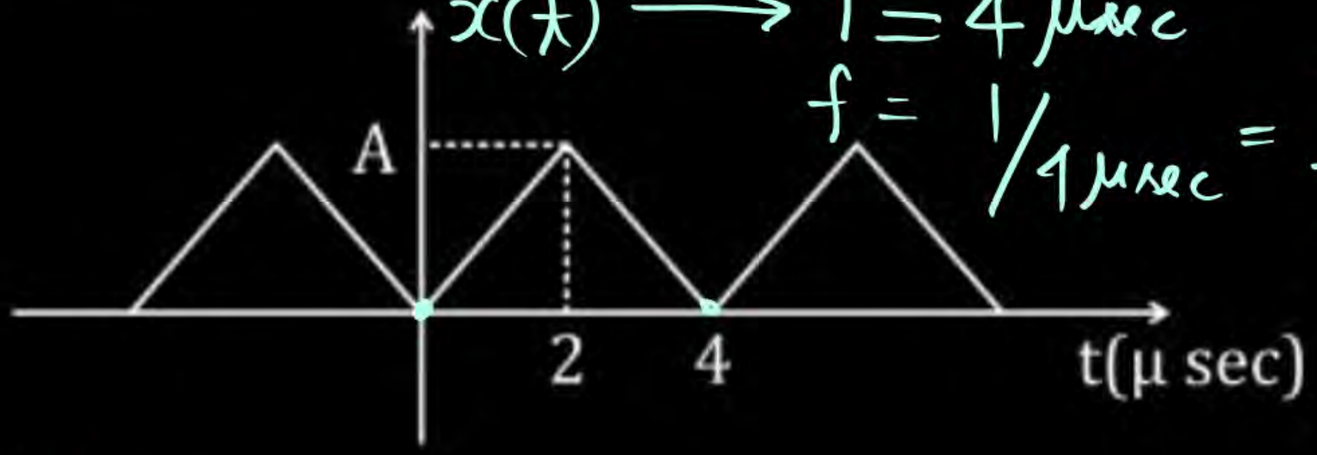


$f_{ak} = 250\ KHz$

MOD-6

$$F_{out} = \frac{f_{ak}}{6} = \frac{250}{6}\ KHz = 41.66\ KHz$$

x(t) is given as



$x(t) \longrightarrow T = 4\ \mu sec$

$$f = 1/4\ \mu sec = \frac{10^6}{4}\ Hz = \frac{10^3}{4}\ KHz = 250\ KHz$$

The value of F_{out} 41.67 kHz

Question MCQ

upcounter

A sequential circuit is as given below:

If above sequential circuit has to work as MOD-3 counter then logic circuit will be:

Q_1 Q_0

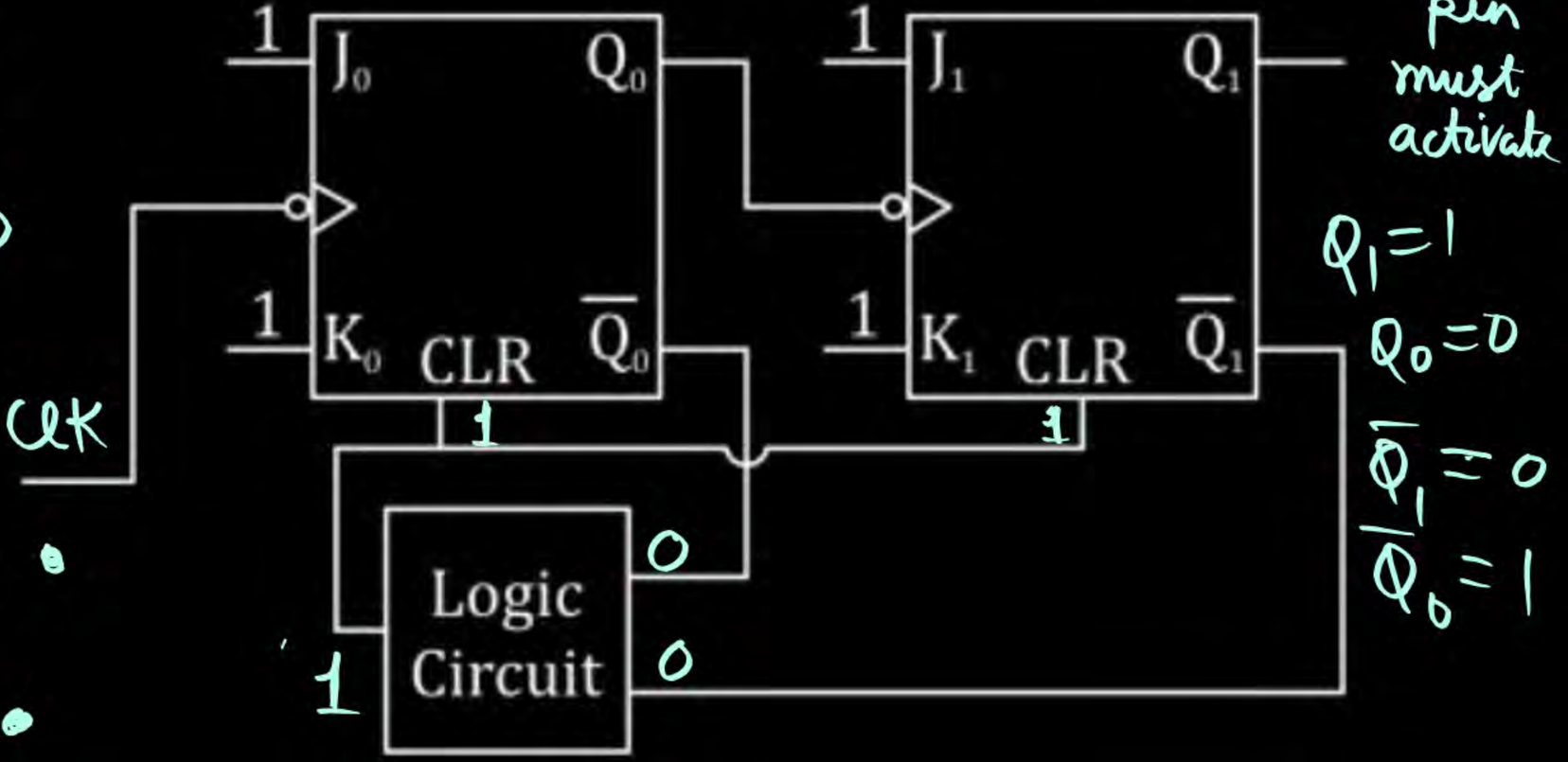
0 0

CLK-1 0 1

CLK-2 1 0

CLK-3 (1 1)

When $Q_1 = 1$ & $Q_0 = 1 \rightarrow$ CLR pin must activate



$Q_1 = 1$

$Q_0 = 0$

$\overline{Q}_1 = 0$

$\overline{Q}_0 = 1$

A ✗ Two input OR gate

B ✗ Two input AND gate

C ✗ Two input NAND gate

D ✓ Two input NOR gate

Question **MCQ**

Which of the following is true:

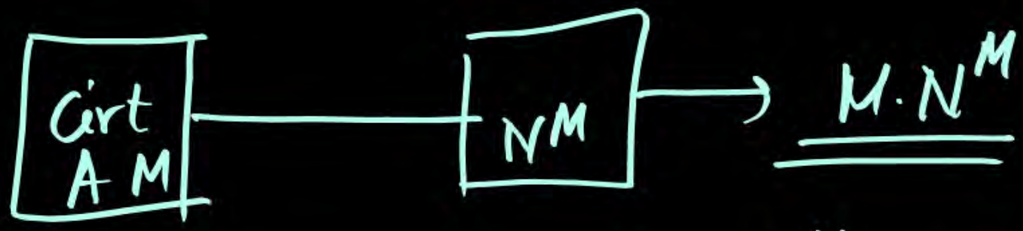
A Asynchronous counters are faster compare to synchronous counters.

B For same MOD-number, synchronous counters require fewer FFs compared to asynchronous counter

C Sequence 0-1-2-3-0 can be designed only in asynchronous counter.

D Sequence 0-1-3-2-0 can be designed only in synchronous counter.

Question MCQ



$M \cdot N^M$

★☆☆

We have two sequential circuits:

Circuit-A → MOD number M.

Circuit-B → MOD number N.

To design a counter of MOD no. M^N, we can

M^N — counter

$N \cdot N \cdot N \cdots$ M times $= N^M$

$M^2 \times M \times M$

$M \cdot M \cdot M \cdot M \cdots$ N times $= M^N$

A Cascade Circuit-A and Circuit-B ✗

B Cascade N Blocks of circuit-A ✓

C Cascade M blocks of circuit-B ✗

D Cascade circuit A with M blocks of circuit-B. ✗

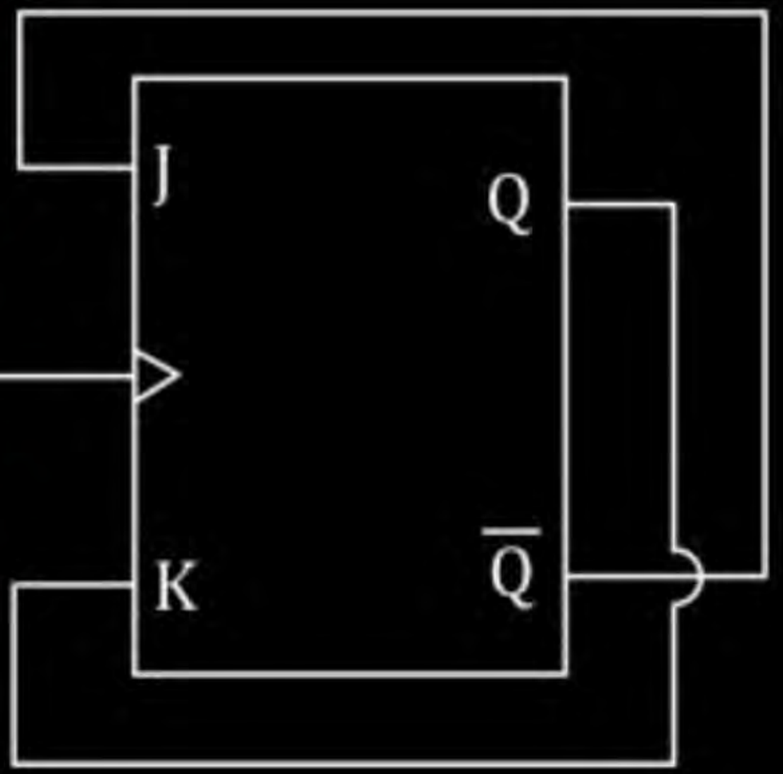
Question MCQ

★★☆

Lets consider the circuit given below:

Counter is at Q = 0 initially, then after applying clock pulses the sequence generated at $\bar{Q}$ will be

		Q	$\bar{Q}$
	1	1	0
	2	0	1
	3	1	0
	4	0	1
	5	1	0
	6	0	1



$Q(n+1) = J\bar{Q} + \bar{K}Q$

$= \bar{Q}\cdot\bar{Q} + \bar{Q}\cdot Q$

$= \bar{Q} + 0$

$Q(n+1) = \bar{Q}$

A. 1010101010.....

B. 1100110011005...

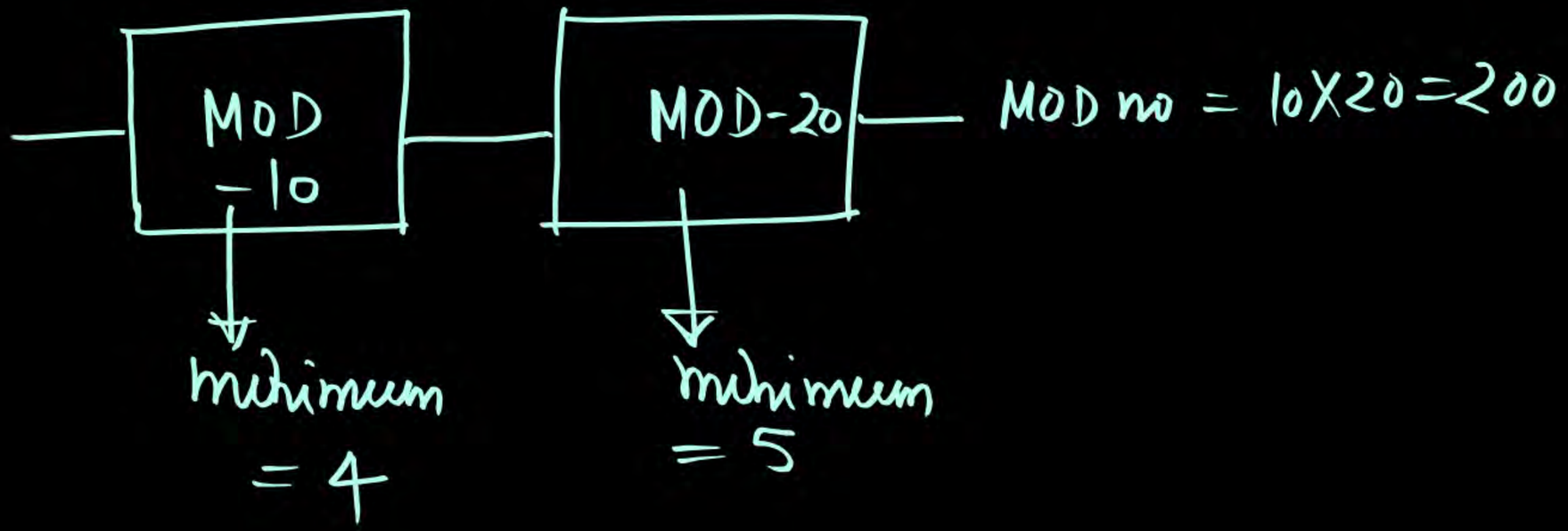
C. 0110001010011...

D. 01011011101....

Question NAT

★★☆

MOD-10 & MOD-20 counters are cascaded to design MOD-200 counter, then minimum number of ffs required is 9.



Question MSQ (A, B)

An asynchronous counter is designed using 10 FFs having MOD No. 1000. Delay of each FF used is 8-n sec, then for which clock frequencies, counter will work properly.

Worst case delay = $10 \times 8 = 80$ nsec

for proper operation

$T_{clk} \geq 80$ nsec

$\frac{1}{T_{clk}} \leq \frac{1}{80\text{nsec}}$

$f_{clk} \leq \frac{10^9}{80}$ Hz

$f_{clk} \leq \frac{10^3}{80}$ MHz

$f_{clk} \leq 12.5$ MHz

- A ✓ 12.5 MHz.
- B ✓ 1.25 MHz.
- C ✗ 125 MHz.
- D ✗ 25 MHz.

Question MCQ

We have M0D-8 asynchronous counter, counting in up-sequence. Delay of each FF is t_d. Initially it is at $(011)_2$ and 1-clock is applied then decoding errors that will appear →

MOD-8 (0-7)

011

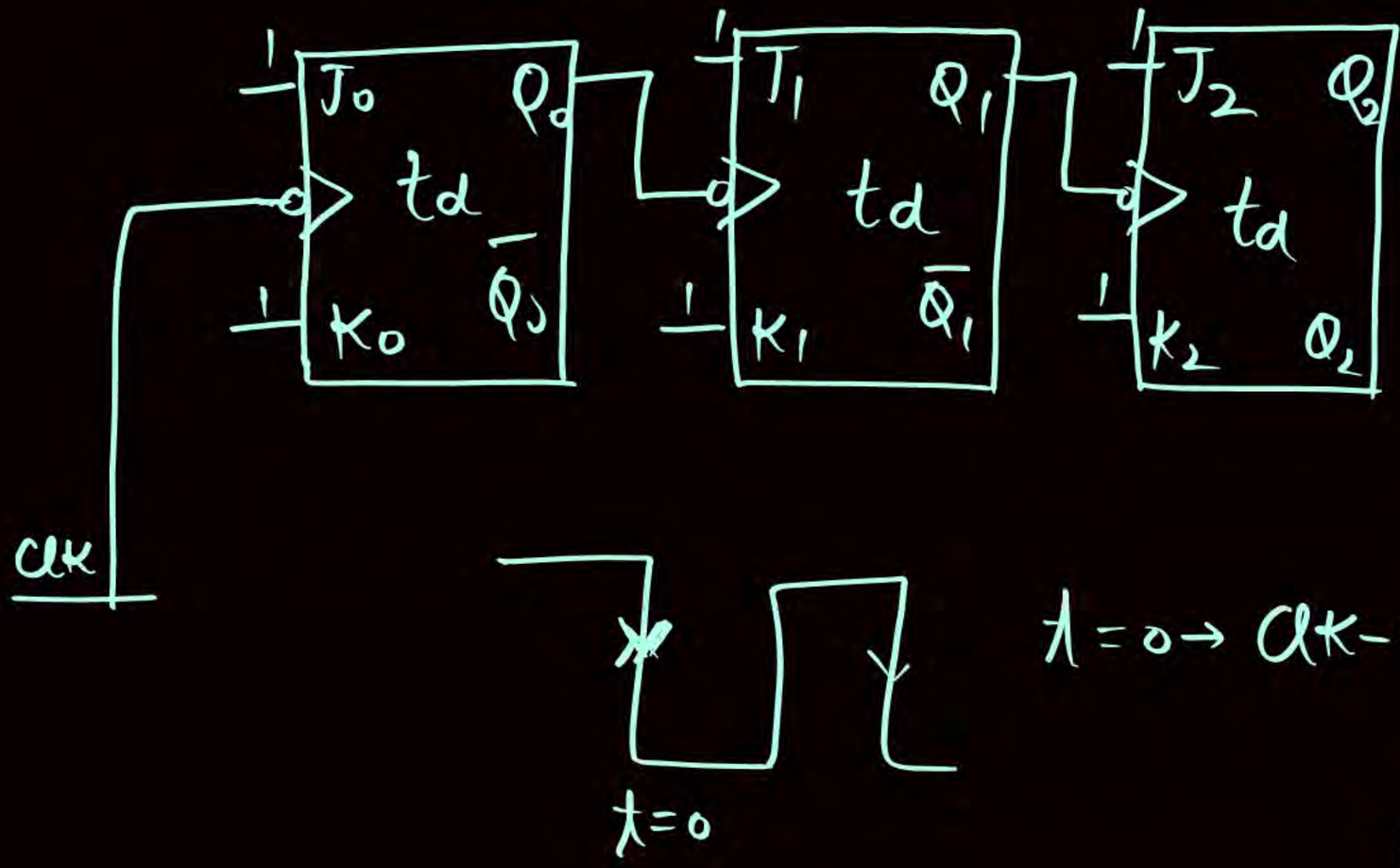
100

A $(010)_2$ & $(000)_2$

B $(000)_2$ & $(101)_2$

C $(101)_2$ & $(010)_2$

D $(010)_2$ & $(110)_2$



t = 0 → clk-1

t=2td t=td t=0

Q2 Q1 Q0

0 1 1 → td → t=td

0 1 0 → td → t=2td

0 0 0 → t=3td

1 0 0

Question **NAT**

We have a MOD-128 down counter starting with state $(111)_{10}$. After application of 370 clock pulses, counter will be at $\_\_(\underline{\quad 125 \quad})_{10}\_\_$

Starting state $(111)_{10} \xrightarrow{128 \text{ clk}} (111)_{10} \xrightarrow{128 \text{ clk}} (111)_{10} \xrightarrow{111 \text{ clk}} (0)_{10}$

$370 - 256 = (114)$

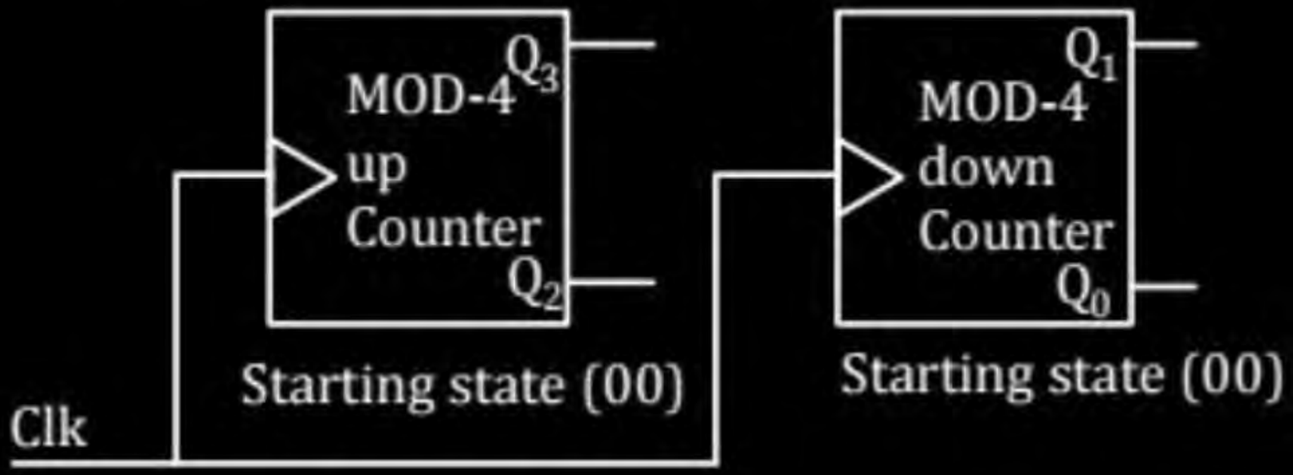
MOD-128 down counter → $0 - 127$

$(125)_{10} \xleftarrow{3} 126 \xleftarrow{2} 127 \xleftarrow{1} (0)_{10}$

$127 - 126 - 125 - - - - - 0 - 127 - 126 -$

Question MCQ

A sequential circuit is as given below:
After applying clock pulses, which count sequence will not appear at output $Q_3Q_2Q_1Q_0$ is



A $(0)_{10}$

B $(7)_{10}$

C $(10)_{10}$

D $(11)_{10}$

	Q_3	Q_2	Q_1	Q_0	
	0	0	0	0	$\longrightarrow (0)_{10}$
CLK-1	0	1	1	1	$\longrightarrow (7)_{10}$
CLK-2	1	0	1	0	$\longrightarrow (10)_{10}$
CLK-3	1	1	0	1	$\longrightarrow (13)_{10}$
CLK-4	0	0	0	0	

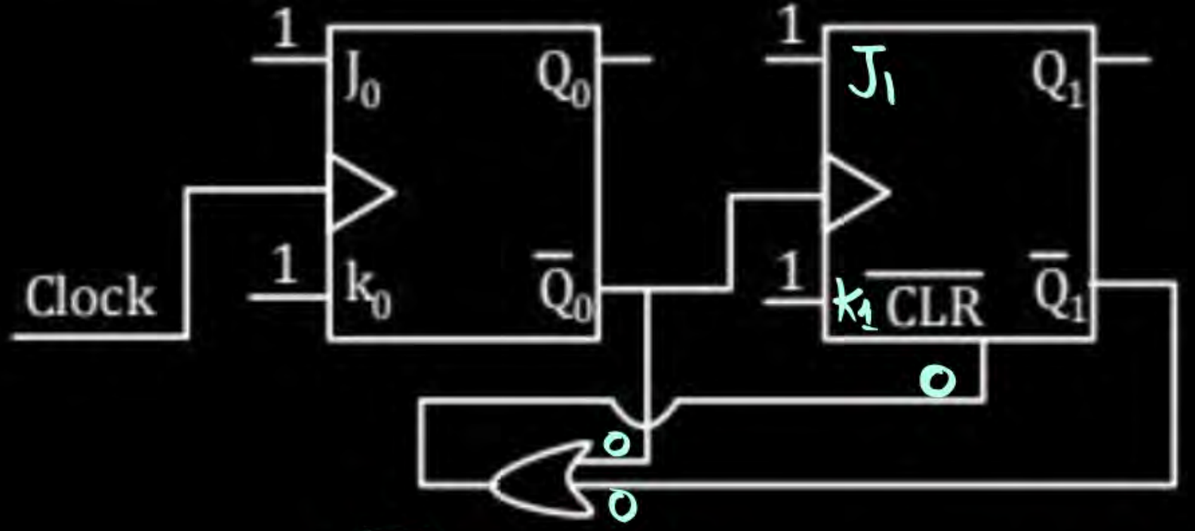
0-3-2-1-0—

Question MCQ

★★☆

Asynchronous up counter

We have sequential circuit as given below: -
The above circuit is



A MOD-3 counter

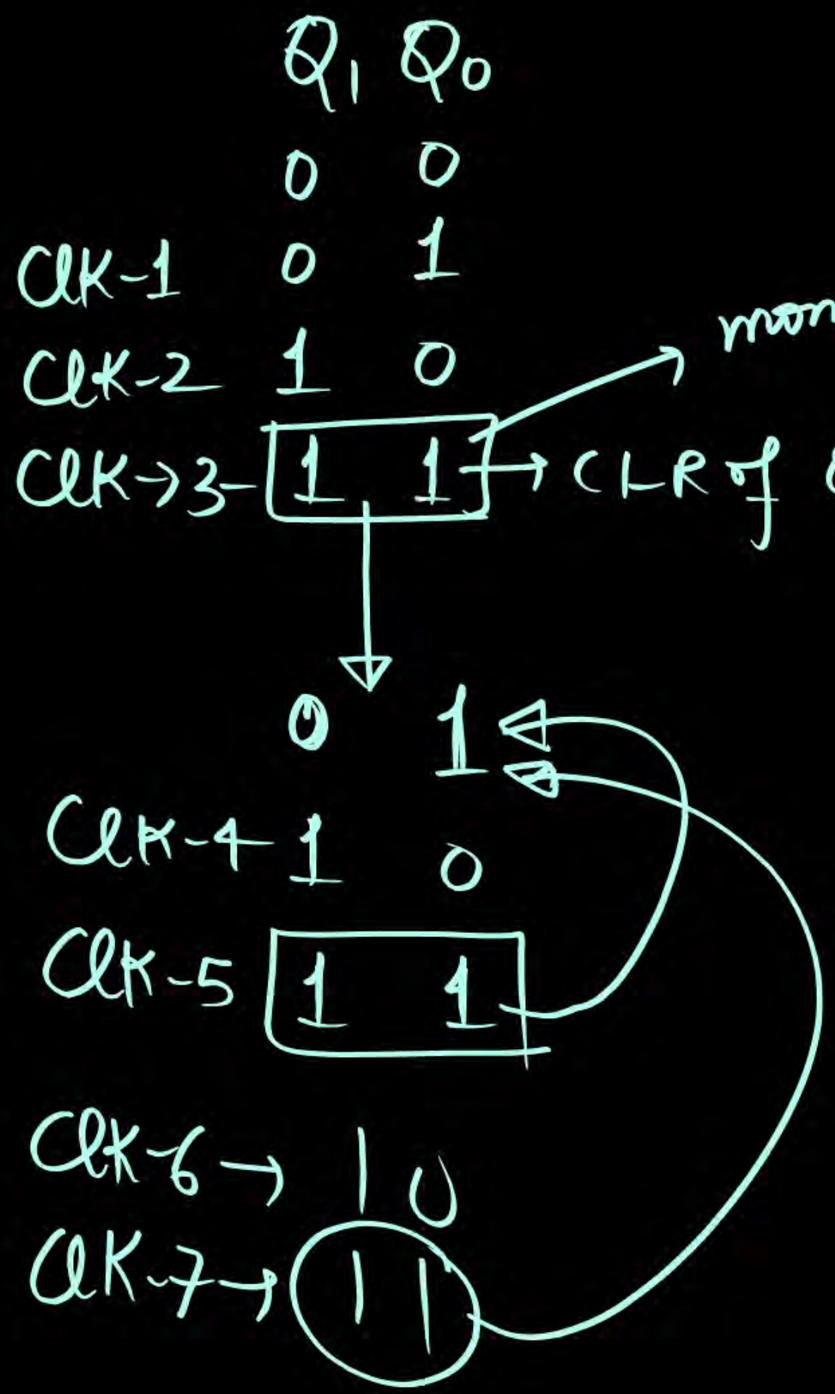
B MOD-2 counter

C MOD-4 counter

D None of these

$\overline{Q}_0 = 0$, $\overline{Q}_1 = 0$ → CLR of Q_1 will activated.

$Q_0 = 1$, $Q_1 = 1$ → CLR pin of Q_1 will activated.



MOD-2 Counter → 1-2-1-2-1-2

Question NAT

MOD-32 up counter has starting state $(00110)_2$ and MOD-16 down counter has starting state $(0110)_2$. After application of 75 clock pulses up counter is in state M and down counter is in state N then value of M + N is __$(28)_{10}$__.

0-31 ← MOD-32 → up counter → starting state $(00110)_2 = (6)_{10}$

MOD-16 → down counter → starting state → $(0110)_2 = (6)_{10}$

↳ 0-15 ⟹ 15-14-13-12 ··· 0→15

up $(6)_{10} \xrightarrow{32\text{ clk}} (6)_{10} \xrightarrow{32\text{ clk}} (6)_{10} \xrightarrow{11\text{ clk}} (17)_{10} = M$

down $(6)_{10} \xrightarrow{16\text{ clk}} (6)_{10} \xrightarrow{16\text{ clk}} (6)_{10} \xrightarrow{16} (6)_{10} \xrightarrow{16\text{ clk}} (6)_{10} \xrightarrow{6\text{ clk}} (0)_{10} \xrightarrow{1\text{ clk}} (15)_{10}$

$N = (11)_{10} \xleftarrow{4\text{ clk}}$

Question MCQ

★☆☆

Which of the following is true about decoding error in asynchronous counter?

A It is removed by using additional signalling

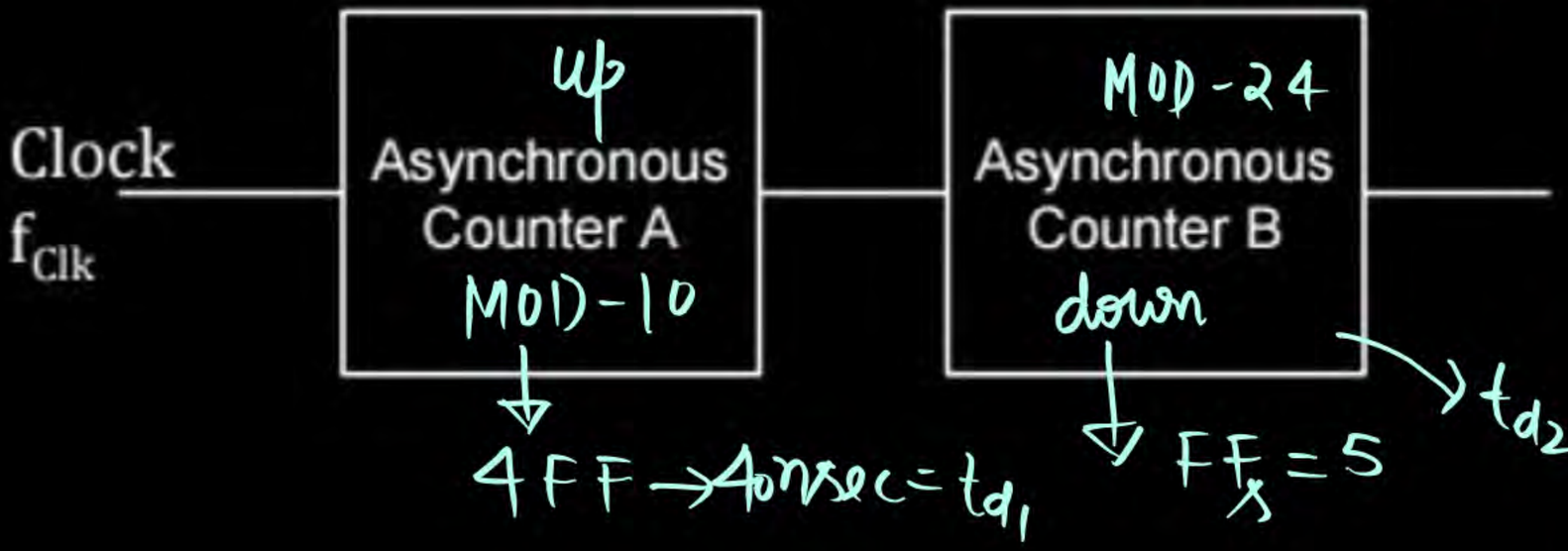
B It can be avoided using strobe signal

C Decoding error is present in asynchronous as well as in synchronous counter

D None of these

Question **NAT**

A sequential circuit is as given below:



$T_d = t_{d_1} + t_{d_2} = 90nsec$

$T_{clk} \geq T_d \quad f_{clk} \leq \frac{1}{T_d}$

$f_{clk} \leq \frac{1}{90nsec}$

$f_{clk} \leq \frac{10^9}{90}$ Hz

4 FF → $40nsec = t_{d_1}$

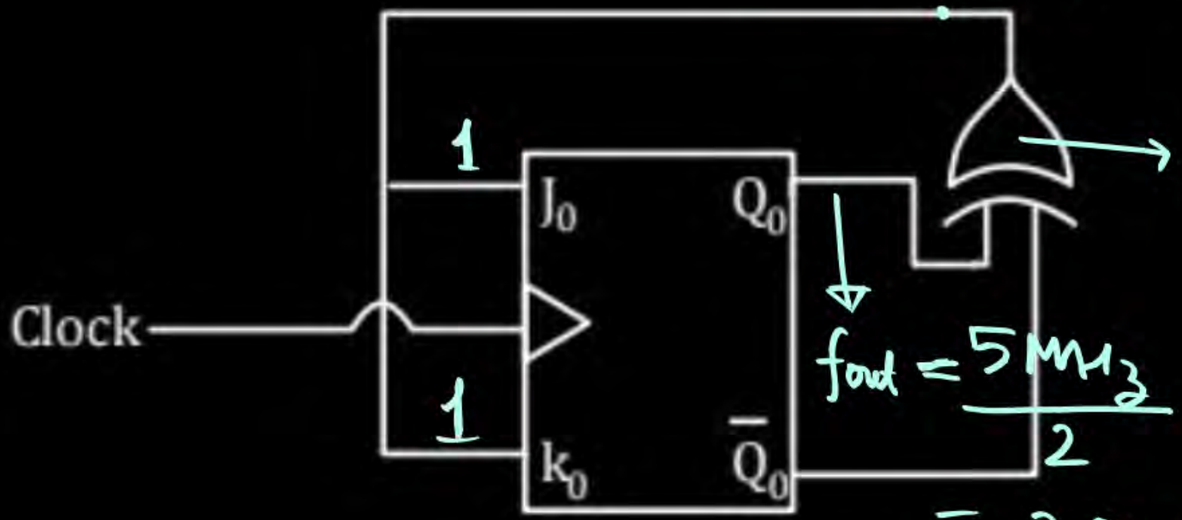
$FF_s = 5$

$f_{clk} \leq \frac{100}{9}$ MHz

Counter A is MOD-10 up counter and counter B is MOD-24 down counter. FF used in designing has equal delay of t_d = 10nsec. Then maximum clock frequency value of f_{Clk} that can be used to have proper operation of the circuit is 11.11 MHz.

Question **NAT**

A sequential circuit is as given below:
If input clock frequency is 5 MHz, the frequency of output waveform at output Q_0 is 2.5 MHz.



$1 = Q_0 \oplus \overline{Q}_0$

$Q_0(n+1) = J_0\overline{Q}_0 + \overline{K}_0 Q_0$

$Q_0(n+1) = 1\cdot\overline{Q}_0 + \overline{1}\, Q_0 = \overline{Q}_0$

Q_0

0

$f_{out} = \frac{5\text{ MHz}}{2}$

$= 2.5$ MHz

CLK-1 1

CLK-2 0

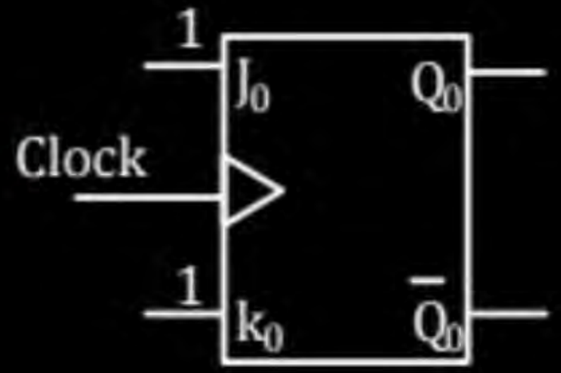
CLK-3 1

→ MOD-2 counter

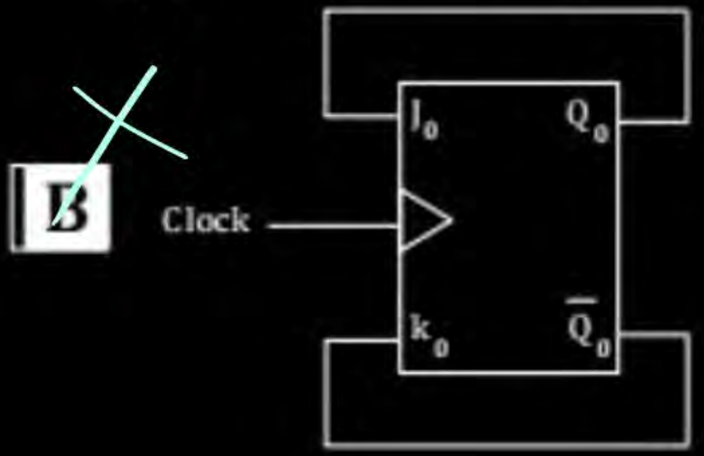
Question **MSQ** (A, C, D)

Which of the following circuit represents toggle mode of operation.

A

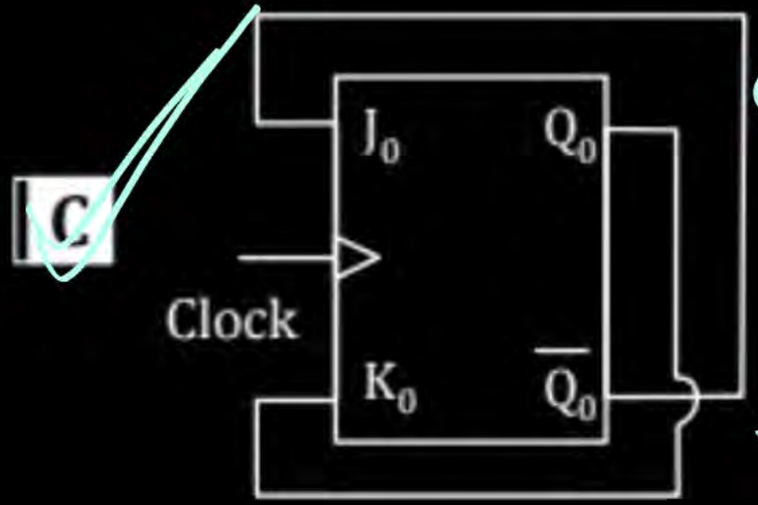


B



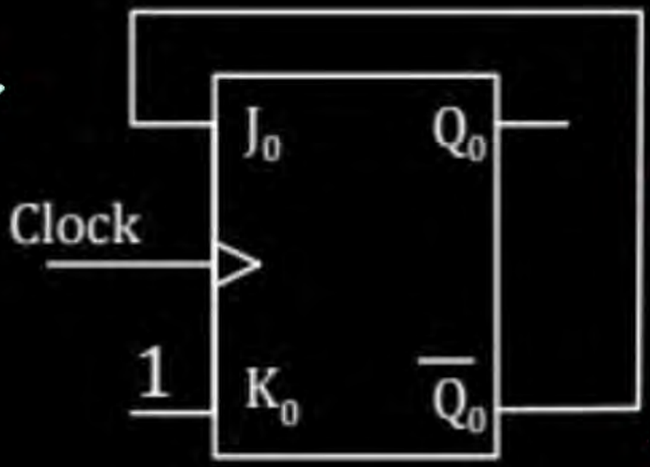
$$Q_0(n+1) = J_0\cdot\overline{Q_0} + \overline{K_0}Q_0$$
$$= Q_0\cdot\overline{Q_0} + Q_0\cdot Q_0$$
$$= 0 + Q_0 = Q_0$$

C



$$Q_0(n+1) = \overline{Q_0}\cdot\overline{Q_0} + \overline{Q_0}\cdot Q_0$$
$$= \overline{Q_0}$$

D



$$Q_0(n+1) = \overline{Q_0}\cdot\overline{Q_0} + \overline{T}\cdot Q_0$$
$$= \overline{Q_0}$$

Question MSQ (A, C, D)

T-FF
↳ $Q(n+1) = T \oplus Q(n)$

for this $A \odot B = T$

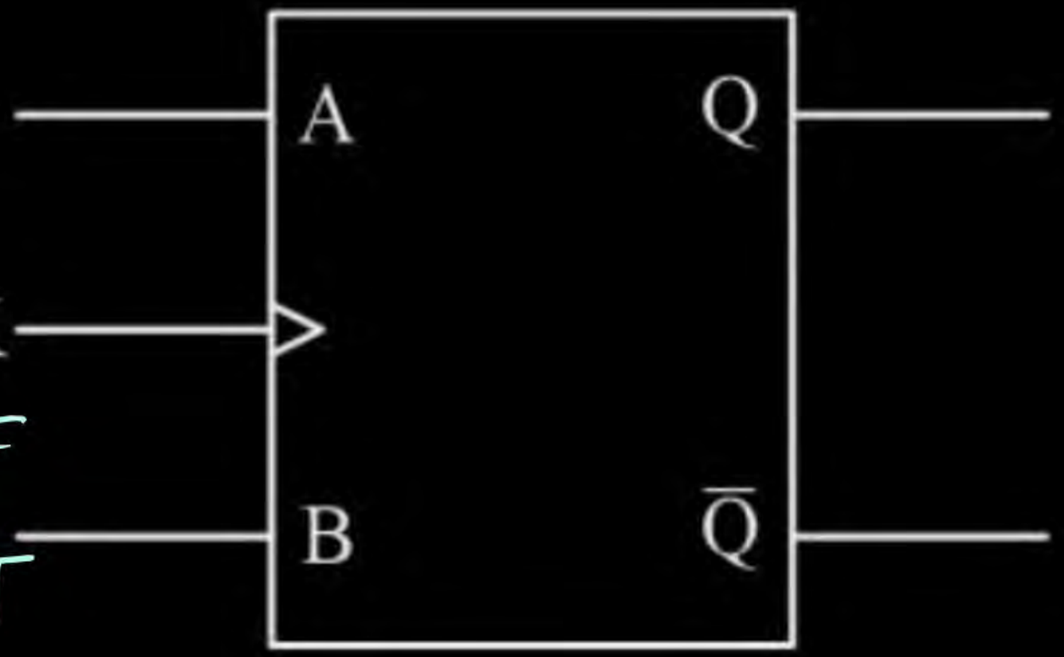
A FF is given as:

Characteristic equation of above FF is

$Q(n+1) = A \odot B \oplus Q(n)$

To convert this FF into T-FF,

A & B will be:



A. $A = T, B = 1$ $A \odot B = T \odot 1 = T$

B. $A = \overline{T}, B = 1$ $\overline{T} \odot 1 = T \oplus 1 = \overline{T}$

C. $A = \overline{T}, B = 0$ $\overline{T} \odot 0 = T \oplus 0 = T$

D. $A = 0, B = \overline{T}$ $0 \odot \overline{T} = T$

Question MCQ

To convert J-K FF into D-FF, J-K input will be

A $J = \bar{D}, K = D$

B $J = K = D$

C $J = D, K = \bar{D}$

D $J = K = \bar{D}$

JK to D $\rightarrow$ $J = D$, $K = \bar{D}$

JK to T $\longrightarrow$ $J = T$, $K = T$

$Q(n+1) = J\bar{Q} + \bar{K}Q = D\bar{Q} + DQ = D[\bar{Q} + Q]$

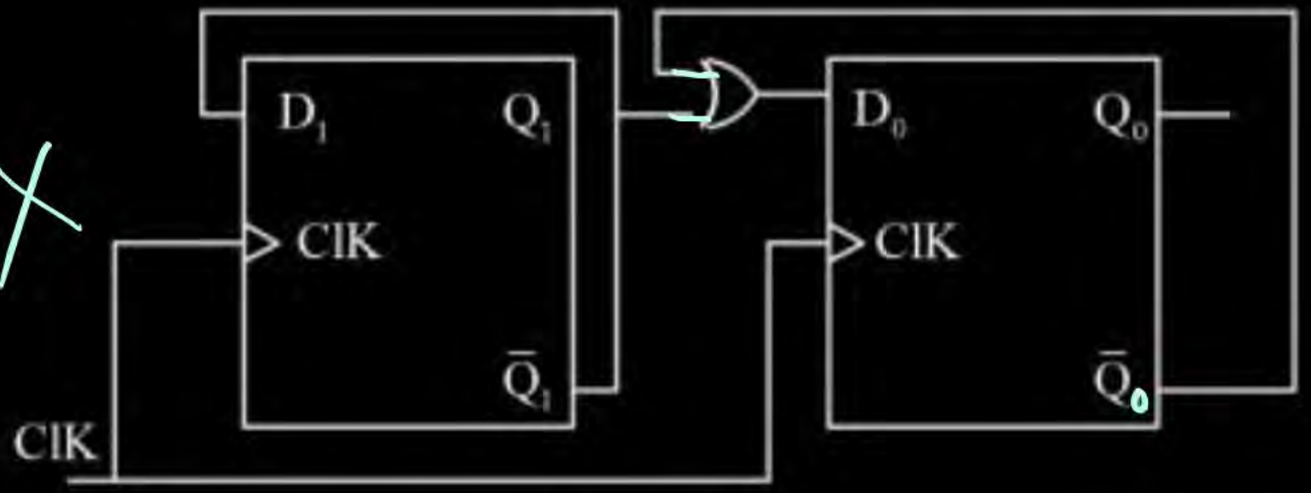
$= D \cdot 1 = D$

Question MCQ

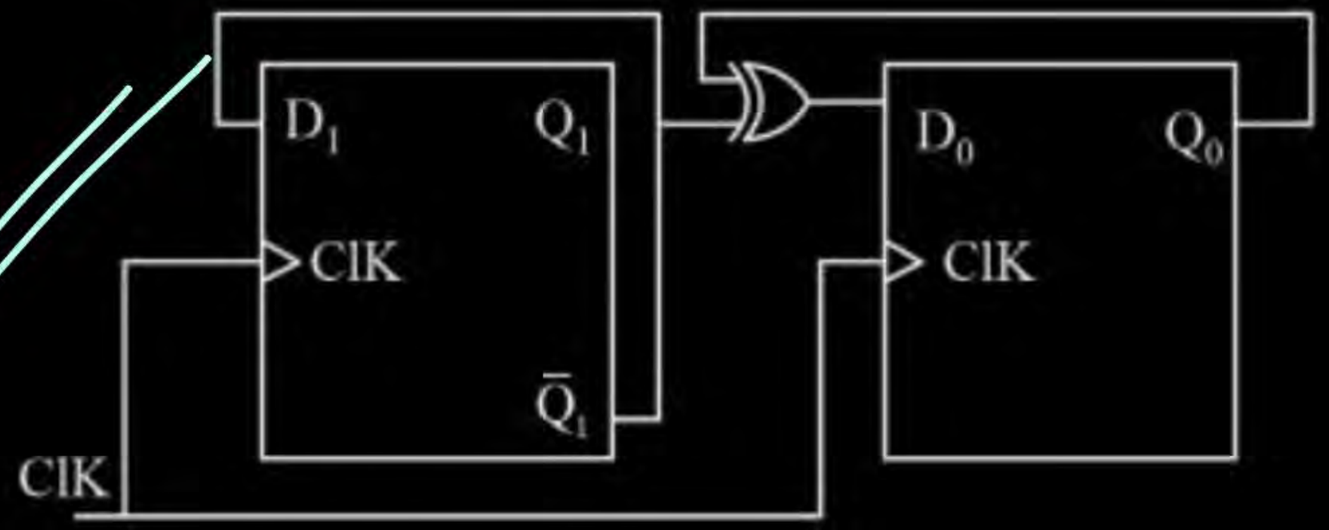
★★★

To design a counter with counting sequence 0 – 3 – 1 – 2 – 0 the circuit will be

A ✗

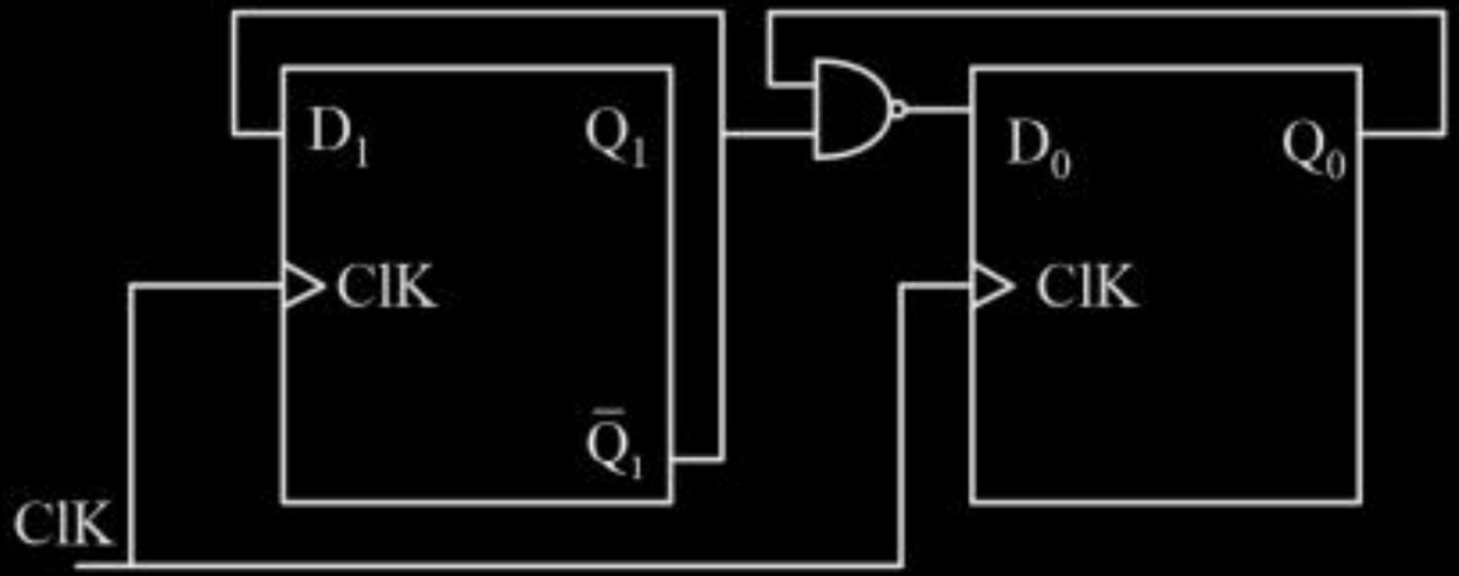


B



Q_1	Q_0	$Q_0(n+1)$
0	0	$= D_0$
1	1	$= \bar{Q}_0 + \bar{Q}_1$
0	1	$= \overline{Q_0 \cdot Q_1}$
1	0	$Q_0(n+1)$
0	0	$= Q_0 \oplus \bar{Q}_1$
		$= Q_0 \odot Q_1$

C

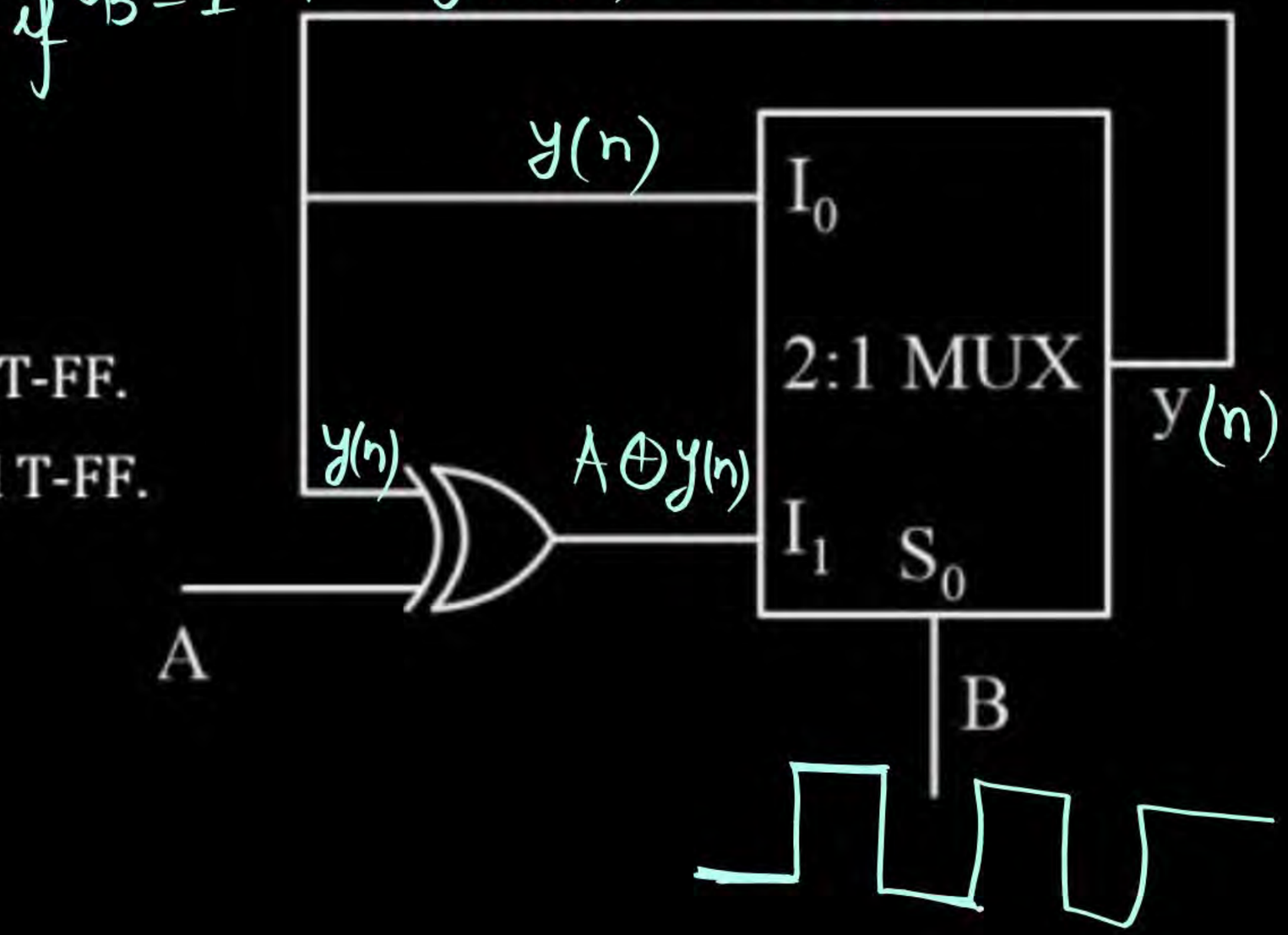


D None of these

Question MCQ

A circuit is as given below:

The circuit can work as



A. Positive level triggered T-FF.

B. Negative level triggered T-FF.

C. Level triggered D-FF.

D. Edge triggered T-FF

Question MCQ

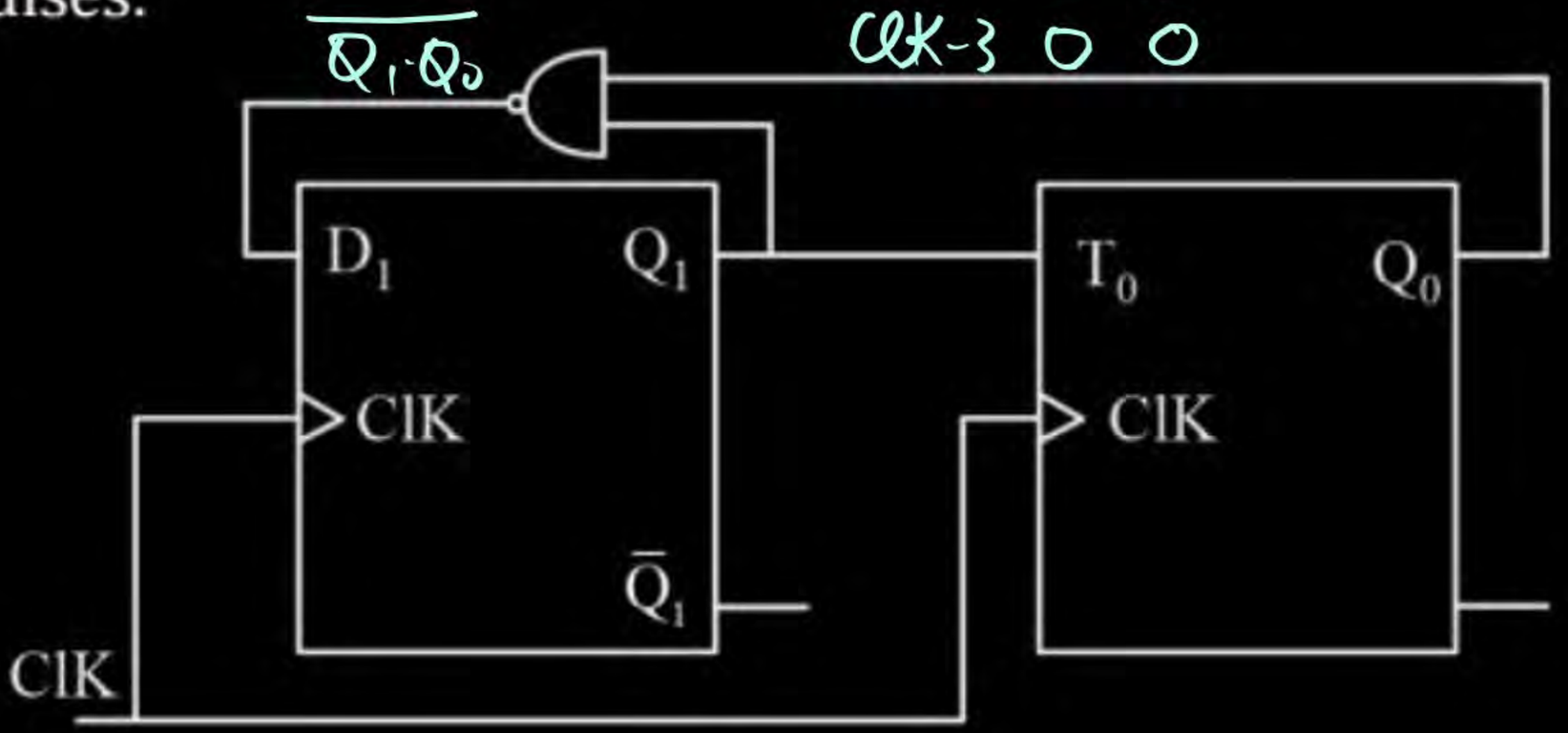
$Q_0(n+1) = T_0 \oplus Q_0 = Q_1 \oplus Q_0$

$Q_1(n+1) = D_1 = \overline{Q_1 \cdot Q_0}$

	Q_0	Q_1
	0	0
CLK-1	0	1
CLK-2	1	1
CLK-3	0	0

A circuit is as given below:

Initially FFs are at rest $Q_0Q_1 = (00)_2$, then sequence that will be generated after application of clock pulses:



A. 00 – 10 – 11 – 00

B. 00 – 01 – 10 – 11 – 00

C. 00 – 01 – 11 – 00

D. 00 – 01 – 11 – 10 – 00

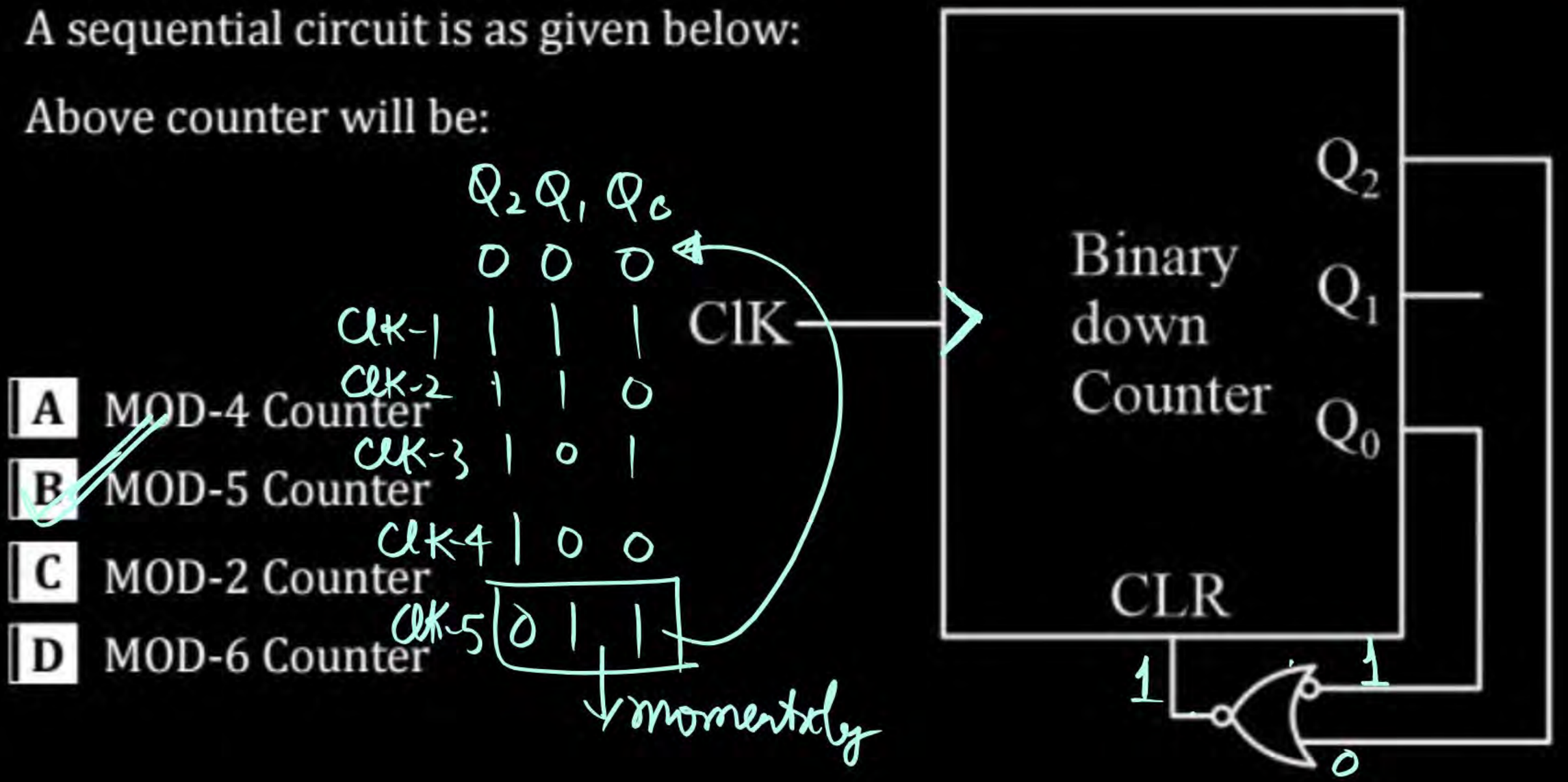
Question MCQ

★★☆

$Q_2 = 0$ & $Q_0 = 1 \rightarrow$ CLR pin activated

A sequential circuit is as given below:

Above counter will be:



A MOD-4 Counter

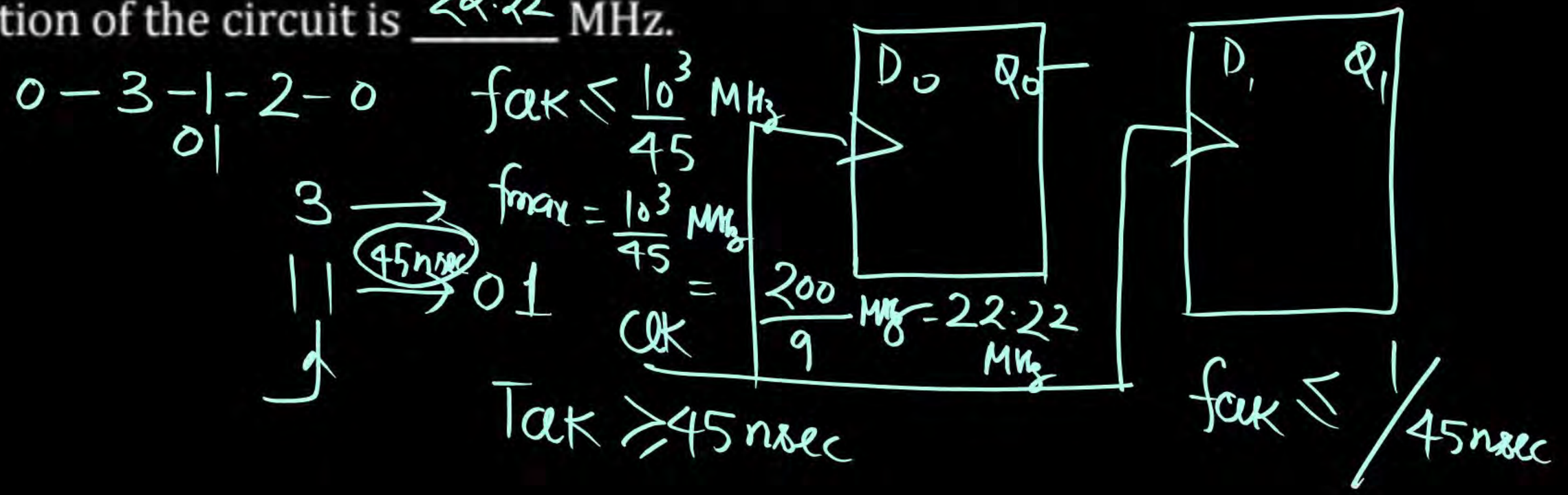
B MOD-5 Counter

C MOD-2 Counter

D MOD-6 Counter

Question **NAT**

A synchronous counter is designed using D-FFs that generate sequence 0 – 3 – 1 – 2 – 0. FFs used have delay of t_d = 45 nsec and logic gates used has zero delay, then maximum clock frequency that can be used to have proper operation of the circuit is 22.22 MHz.



Question MCQ

$Q_1(n+1) = J_1\overline{Q_1} + \overline{K_1}Q_1$

$= \overline{Q_0}\cdot\overline{Q_1} + Q_0Q_1 = Q_1 \odot Q_0$

$Q_0(n+1) = J_0\overline{Q_0} + \overline{K_0}Q_0 = \overline{Q_1}\,\overline{Q_0} + 0 = \overline{Q_1 + Q_0}$

A sequential circuit is as given below:

Initially counter is at $Q_1Q_0 = (11)_2$ then after applying clock next state will be

$Q_1\ Q_0$

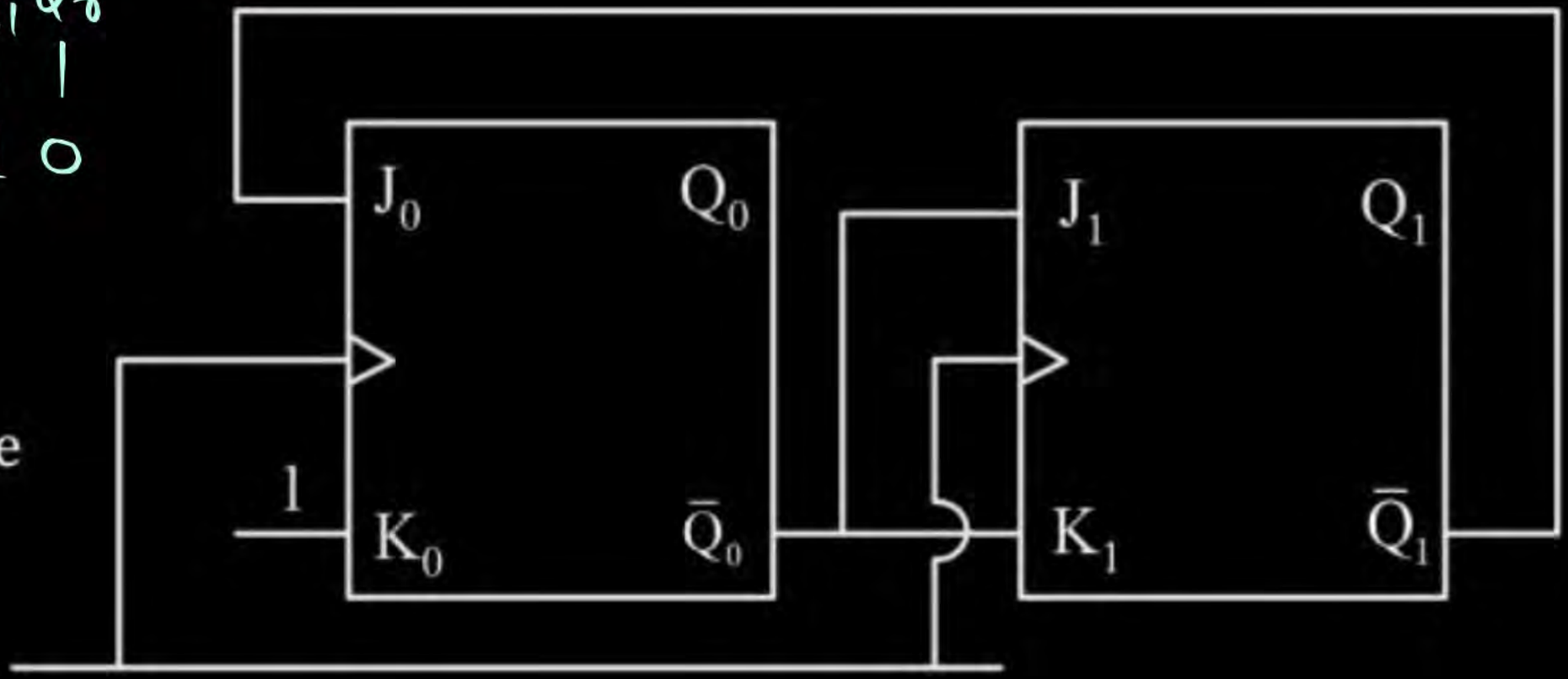
$Clk\text{-}1$ 1 0

A $(01)_2$

B $(10)_2$

C $(00)_2$

D None of these



Question MCQ

We have a T-FF, to convert it into D-FF, input T must be

$T \Rightarrow \quad Q(n+1) = T \oplus Q(n)$

DFF $\rightarrow Q(n+1) = D$

A $D \odot Q$ ✗

B $D \oplus Q$ ✓

C D ✗

D $\overline{D}$ ✗

$T = D \oplus Q(n) \Rightarrow Q(n+1) = \underline{D \oplus Q(n)} \oplus Q(n)$

$Q(n+1) = D \oplus 0 = D$

Question **MCQ**

We want to design a counter with counting sequence 0 – 1 – 2 – 3 – 0, using
Circuit-A → Asynchronous counter $\longrightarrow FF_s = 2 \rightarrow T_d = 50\,nsec$
Circuit-B → Synchronous counter $\rightarrow FF_s = 2$
$(T_{clk})_A \geq (50\,nsec)$
FFs used in circuit-A and circuit-B are of same logic family and logic gates used has 0 delay while FFs have delay of 25 nsec. Then which of the following is true?

$(T_d)_B = 25\,nsec$
$(T_{clk})_B \geq 25\,nsec$
$(f_{clk})_A \leq 1/50\,nsec$
$(f_{clk})_{A\,max} = 1/50\,nsec$

A ✗ Maximum clock frequency is same in both the circuits.

B ✓ Maximum clock frequency is double in circuit-B compare to circuit-A.

C ✗ Maximum clock frequency is half in circuit-B compare to circuit-A

D None of these

$(f_{clk})_B \leq 1/25\,nsec$
$(f_{clk})_{B\,max} = 1/25\,nsec = 2 \cdot 1/50\,nsec$

Question **NAT**

★★☆

A counter has to be designed to generate a sequence $0 - 2 - 2^2 - 2^3 - 2^4 - 2^5 - 2^6$, to design the counter appropriate number of FFs needed is 7.

$0 - 2 - 4 - 8 - 16 - 32 - (64)$ MOD no $= 7$

$2^6 = 64$

6 → FF → MOD no = 64

$0 - (63)$

2^6	2^5	2^4	2^3	2^2	2^1	2^0
1	0	0	0	0	0	0

$= (64)_{10}$

$2^7 = \underline{128}$

Thank you

GW

Soldiers !