CS & IT ENGINEERING

Operating System

Memory Management

Lecture - 3

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Recap of Previous Lecture

Topic Non-Contiguous MMT

Topic Paging

Topic Address Translation

Topics to be Covered

Topic Address Translation

Topic Performance of Paging

Topic : Paging

logical address

Process

000	a	00
001	b	
010	c	01
011	d	
100	e	10
101	f	
110	g	11
111	h	

Page Table

00	110
01	010
10	100
11	001

Physical Memory

0000		000
0001		
0010	g	001
0011	h	
0100	c	010
0101	d	
0110		011
0111		
1000	e	100
1001	f	
1010		101
1011		
1100	a	110
1101	b	
1110		111
1111		

CPU requires content 'f', hence it generates it's logical address ⇒ 101

⇓

Divide logical address

CPU wants to access byte 1 of page $(10)_2$.

→ search page table for page no. $(10)_2$

⇓

frame no. ⇒ $(100)_2$

⇓

CPU's required content is available at byte 1 of frame $(100)_2$

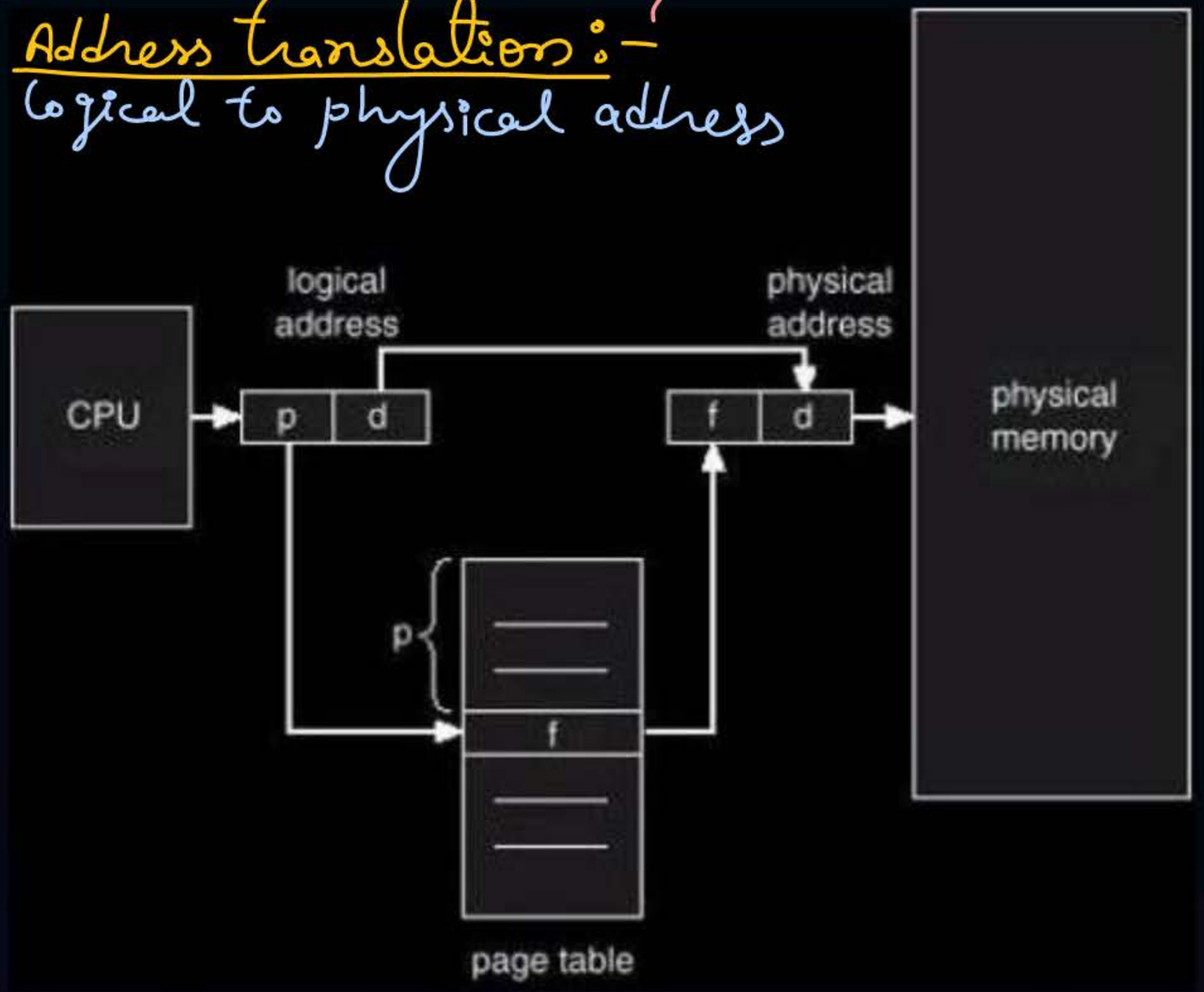
⇓

Physical address = | f | d | ⇒ | 100 | 1 |

Topic : Paging

Address translation :-
logical to physical address

→ done by a h/w called as MMU (Mem. Mgmt Unit)



Topic : Paging

- Process is divided in equal size of pages
- Physical memory is divided in same equal size of frames
- Processor will have a view of process and its pages
- Pages are scattered in frames
- Page table is used to map a process page to a physical frame
- Number of entries in page table = Number of pages in process
- OS maintains a page table for each process

$$\text{no. of pages in process} = \frac{\text{process size}}{\text{page size}}$$

$$\text{no. of frames in main memory} = \frac{\text{physical mem size}}{\text{page size}}$$

Logical address space (L.A.S.) $\Rightarrow$ process size

→ Collection of all logical addresses.

Physical address space (P.A.S.) $\Rightarrow$ Physical mem. size

→ collection of all physical addresses

$L.A.S. = 2^{LA}$ bytes

$LA = \log_2(LAS)$ bits

$P.A.S. = 2^{PA}$ bytes

$P.A. = \log_2(PAS)$ bits

Page table size

= no. of entries in P.T. * 1 P.T. entry size

= no. of pages in process * 1 P.T. entry size

1 P.T. entry size = frame no. bits + extra bits

Ques) L.A. = 20 bits

P.A. = 28 bits

Page size = 256 bytes $= 2^8$ B

Process size (L.A.S.) $= 2^{20}$ bytes

no. of pages in process $= \frac{2^{20}\ B}{256\ B}$

$= \frac{2^{20}}{2^8} = 2^{12}$

⇓

Page no. = 12 bits

1. No. of pages in process $= 2^{12}$
2. No. of bits for page no. = 12 bits
3. No. frames in memory $= 2^{20}$
4. No. of bits for frame no. = 20 bits
5. No. of bits for offset = 8 bits
6. Page table size = 80 k bits or 10 k bytes

physical mem size $= 2^{28}$ bytes

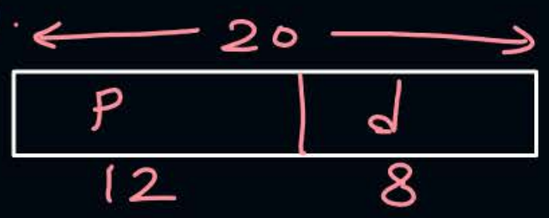
no. of frames $= \frac{2^{28}\ B}{256\ B} = \frac{2^{28}}{2^8} = 2^{20}$

⇓

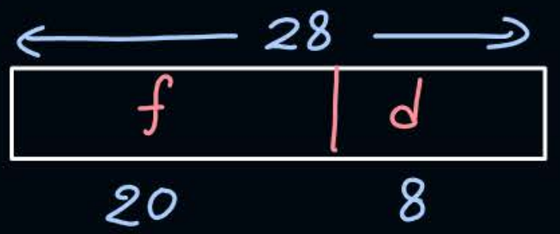
frame no. = 20 bits

Method 2 :-

L.A.



P.A.



P.T. size = 2^{12} * 20 bits

= 80 k bits

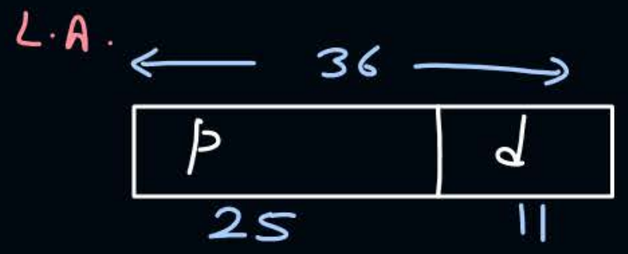
= 10 k bytes

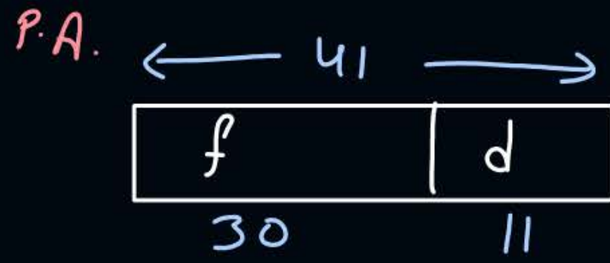
Ques 2)

L.A. = 36 bits

P.A. = 41 bits

Page size = 2k bytes = 2^{11}B





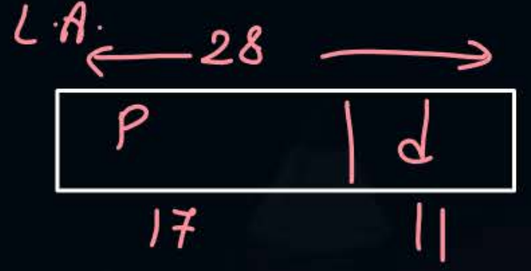
1. No. of pages = 2^{25}
2. Page no. bits = 25 bits
3. No. of frames = 2^{30}
4. frame no. bits = 30 bits
5. bits for offset = 11 bits
6. Page table size = 2^{25} * 30 bits

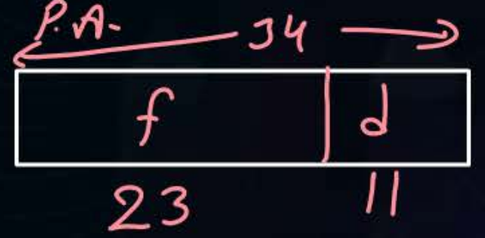
Topic : Question

$K = 2^{10}$
$M = 2^{20}$
$G = 2^{30}$

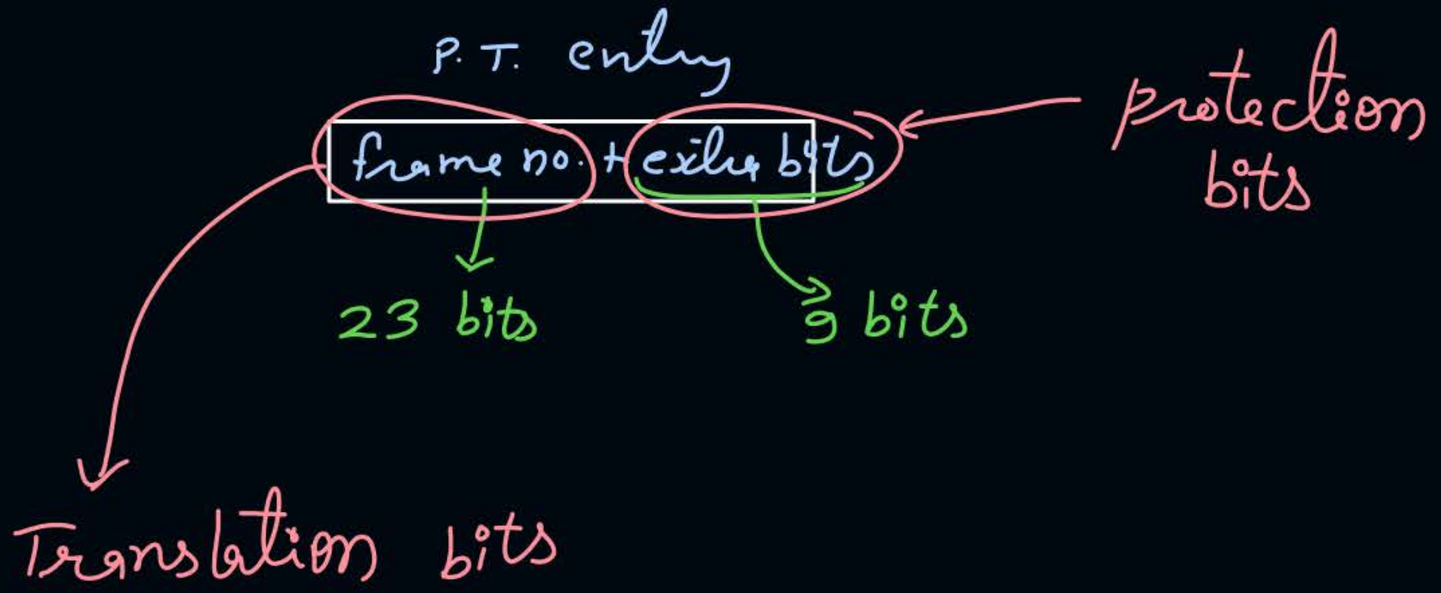
#Q. Consider a paged memory system where the logical address of 28 bits and physical address of 34 bits. If each page table entry is of 4 bytes and page size is 2KB (2^{11} B) then:

1. Number of pages in process? $= 2^{17}$
2. Number of frames in main memory? $= 2^{23}$
3. Number of bits for page number? 17 bits
4. Number of bits for frames? $= 23$ bits
5. Number of entries in page table? 2^{17}
6. Page table size? $2^{17} * 4$ bytes $= 2^{17} * 2^2$ B $= 2^{19}$ B $= 512$ KB





1 P.T. entry = 4 bytes = 32 bits



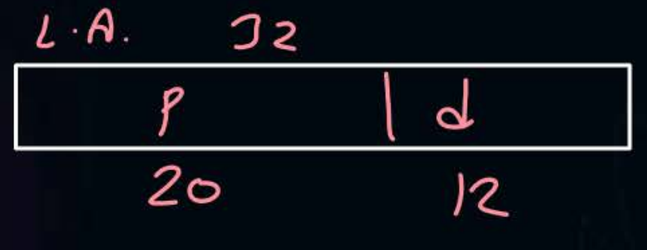
Topic : Question

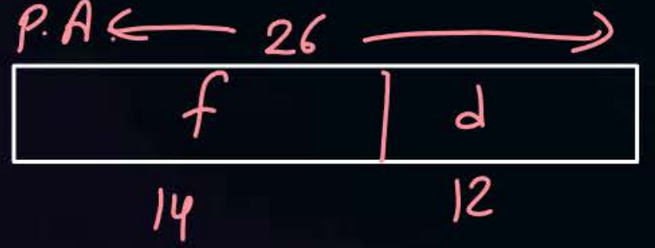
[GATE-2001]

$2^6 \cdot 2^{20} B = 2^{26} B \Rightarrow P.A = 26$ bits

#Q. Consider a machine with 64 MB physical memory and a 32-bit virtual (logical) address space. If the page size is 4 KB, what is the approximate size of the page table?

$2^2 \cdot 2^{10} = 2^{12} \Rightarrow d = 12$ bits





P.T. size =

$= 2^{20} * (14 + \text{extra bits})$

$= 14$ M bits

$\simeq 2$ M bytes

A. 16 MB

B. 8 MB

C. ✓ 2 MB

D. 24 MB

[MCQ]

H. W.

#Q. Consider a paged memory system where the process size is 16MB and main memory size is 4GB. The page size is 2KB.

A Number of pages in process?

B Number of frames in main memory?

C Number of bits for page number?

D Number of bits for frames?

E Number of entries in page table?

F Page table size?

[MCQ]

H.W.

#Q. Consider a paged memory system where the process size is 128MB and main memory size is 2GB. The page size is 1KB.

A Number of pages in process?

B Number of frames in main memory?

C Number of bits for page number?

D Number of bits for frames?

E Number of entries in page table?

F Page table size?

[MCQ]

H. W.

#Q. Consider a paged memory system where the logical address is 25 bits and physical address is 33 bits. The page size is 4KB.

A. Number of pages in process?

B. Number of frames in main memory?

C. Number of bits for page number?

D. Number of bits for frames?

E. Number of entries in page table?

F. Page table size?

[MCQ]

H.W.

[GATE-2015]

#Q. A computer system implements 8 kilobyte pages and a 32–bit physical address space. Each page table entry contains a valid bit, a dirty bit, three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the logical address supported by the system is _____ bits?

2 mins Summary

Topic Address Translation

Topic Performance of Paging

Happy Learning

THANK - YOU