Design of Phase Locked Loop using 7nm FinFet Technology

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***Abstract*—This paper presents the design and implementation of a high-performance Phase-Locked Loop (PLL) using the ASAP 7nm Process Design Kit (PDK). The PLL, designed with an 8x frequency multiplier, targets a reference input frequency of 128.55 MHz and generates an output frequency of 1.028 GHz. Key components include a Phase-Frequency Detector (PFD), a charge pump, a second-order passive loop filter, an Current Starved Voltage-Controlled Oscillator (CSVCO), and a frequency divider. The design utilizes predictive scaling techniques for 7nm FinFET I/O pads and demonstrates efficient locking behavior with minimal phase noise and jitter, meeting the stringent demands of modern high-speed communication systems.**

Keywords—Phase locked Loop, Charge Pump PLL,

I. INTRODUCTION

In this paper, we present the design and implementation of a Phase-Locked Loop (PLL) with a Current Starved Voltage-Controlled Oscillator (CSVCO) using 7nm FinFET technology. Scaling down to 7nm brings significant improvements in performance, power, and area, but also introduces challenges related to short-channel effects, leakage currents, and variability. The PLL targets applications in clock generation and signal synchronization for high-speed data systems, with a focus on low power consumption and high-frequency operation. Compared to the previous designs in 180nm technology, this work focuses on leveraging FinFET's high current drive and reduced leakage to optimize the design for the GHz range.

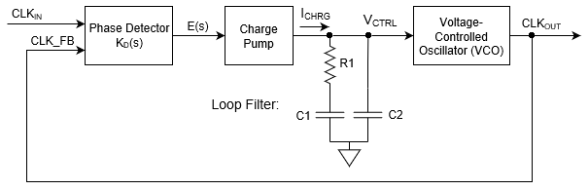

Figure 1. Design Of PLL using CSVCO and Charge Pump

II. DESIGN METHODOLOGY

The Current Starved Voltage-Controlled Oscillator (CSVCO) in 7nm FinFET technology efficiently tunes between 1.024 GHz and 2.56 GHz, using bias current control and an LC tank circuit for low power consumption. The Phase-Frequency Detector (PFD) and charge pump leverage FinFET logic and matched current mirrors for rapid phase detection and precise current regulation. A second-order RC loop filter stabilizes the control voltage, while a frequency divider scales the VCO output by a factor of 8. Operating at 0.75V, the PLL targets a frequency range of 1.024 GHz to 2.56 GHz with a 160 MHz reference. Simulations with open-source tools validate minimal jitter and low phase noise, showcasing the CSVCO's advancements in frequency tuning and efficiency for high-speed, low-power applications.

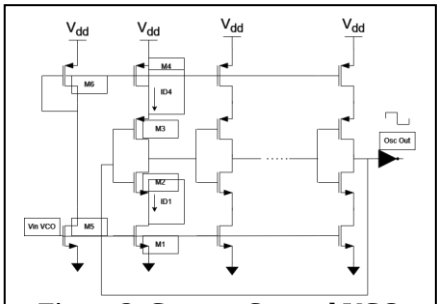

Figure 2. Current Starved VCO

III. ISSUES AND IMPROVEMENTS

Key challenges, such as mitigating short-channel effects and minimizing leakage currents, were addressed by optimizing transistor sizes, biasing conditions, and using multi-fin devices for better control. FinFETs' superior gate control helped reduce process variability, ensuring robust performance across corners. The shift from 180nm CMOS to 7nm FinFET technology brought substantial improvements, with the CSVCO achieving higher frequencies (1.024 GHz to 2.56 GHz) and reduced power consumption due to a lower supply voltage (0.75V). The design also occupies less area, making it ideal for compact, high-performance circuits.

IV. CONCLUSION AND FUTURE SCOPE

Future work could explore adaptive biasing techniques to minimize power consumption in low-frequency modes and expand the design for multi-band operation, enhancing its applicability in communication systems. Additionally, investigating fully digital PLLs (DPLLs) may provide greater flexibility and programmability, optimizing performance for a wider range of next-generation electronic applications.

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