**Assignment -2**

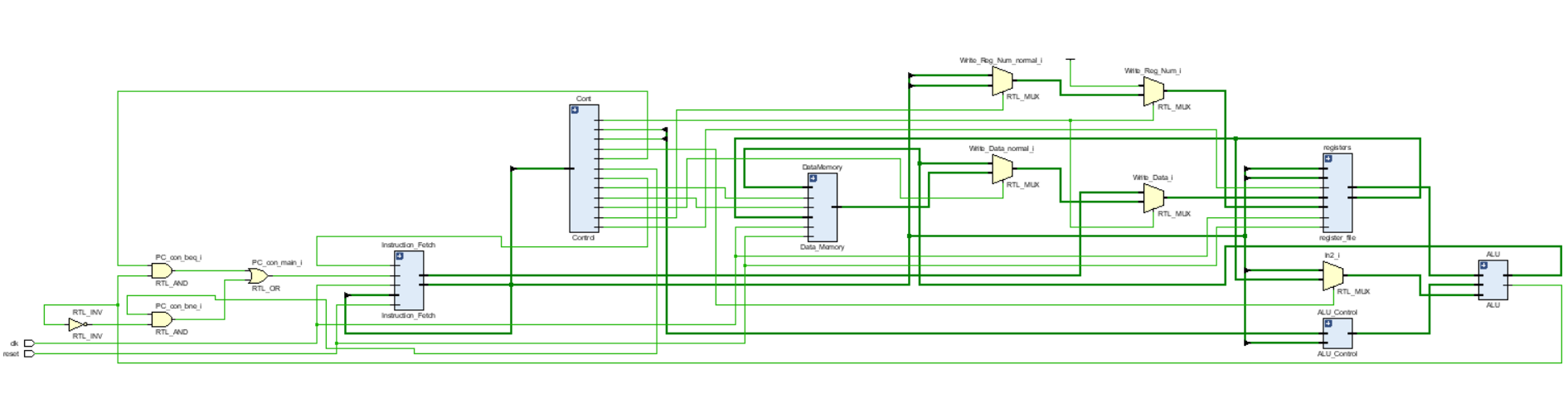
**Computer Architecture Lab**

**Group no. 14**

**Name : Kaushik Kalakonda**

**ID Student : 2020A3PS0468H**

**The RTL Schematic of the processor showing the required data path and control path:**



***Truth Table of Main Control Unit:***

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction**  **Type** | **RegDst** | **ALUSource** | **MemtoReg** | **RegWrite** | **MemRead** | **MemWrite** | **Branch** | **Branch1** | **ALUOp1** | **ALUOp0** | **Jump** | **AL** |
| **R** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |
| **LW** | **0** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **SW** | **x** | **1** | **x** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| **BEQ** | **x** | **0** | **x** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **0** |
| **BNE** | **x** | **0** | **x** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** |
| **J** | **x** | **x** | **x** | **0** | **0** | **0** | **x** | **x** | **x** | **x** | **1** | **0** |
| **JAL** | **x** | **x** | **x** | **1** | **0** | **0** | **x** | **x** | **x** | **x** | **1** | **1** |

***Truth Table for the ALU Control Unit:***

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **ALUOp** | | **Function Code** | | | | | | **ALU Control Input** | | | | **Desired ALU Action** |
| **0** | **0** | **x** | **x** | **x** | **x** | **x** | **x** | **0** | **0** | **1** | **0** | **add** |
| **x** | **1** | **x** | **x** | **x** | **x** | **x** | **x** | **0** | **1** | **1** | **0** | **sub** |
| **1** | **x** | **x** | **x** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **add** |
| **1** | **x** | **x** | **x** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **sub** |
| **1** | **x** | **x** | **x** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **and** |
| **1** | **x** | **x** | **x** | **0** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **or** |
| **1** | **x** | **x** | **x** | **1** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **slt** |
| **1** | **x** | **x** | **x** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **xor** |
| **1** | **X** | **x** | **x** | **0** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **nor** |

***Program loaded in the instruction memory:***

Instruction Memory contains the following program:

**Start: add $t0,$t1,$t2**

**sw $t2, 0($t3)**

**lw $t5, 0($t3)**

**and $t0,$t1,$t2**

**or $t0,$t1,$t2**

**j label //label=6**

**label: bne $t30, $t31**

**beq $t30, $t31**

**slt $t0,$t1,$t2**

**xor $t0,$t1,$t2**

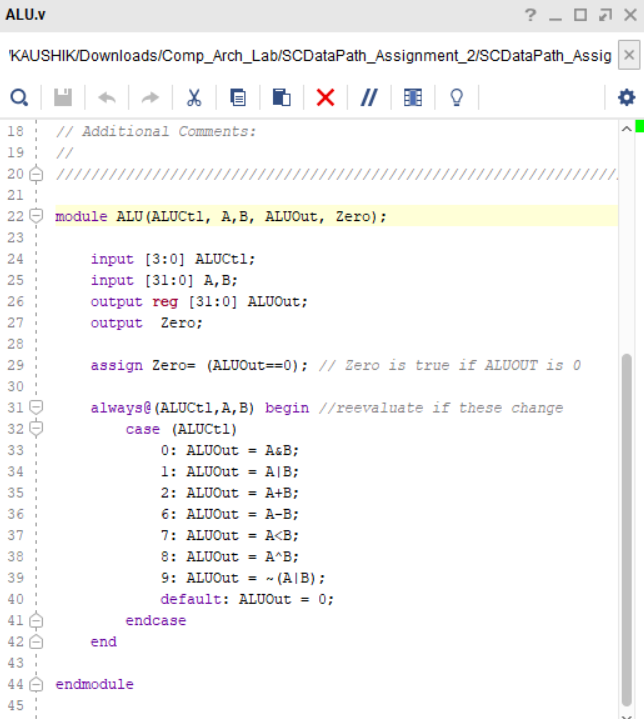
**nor $t0,$t1,$t2**

**sub $t0,$t1,$t2**

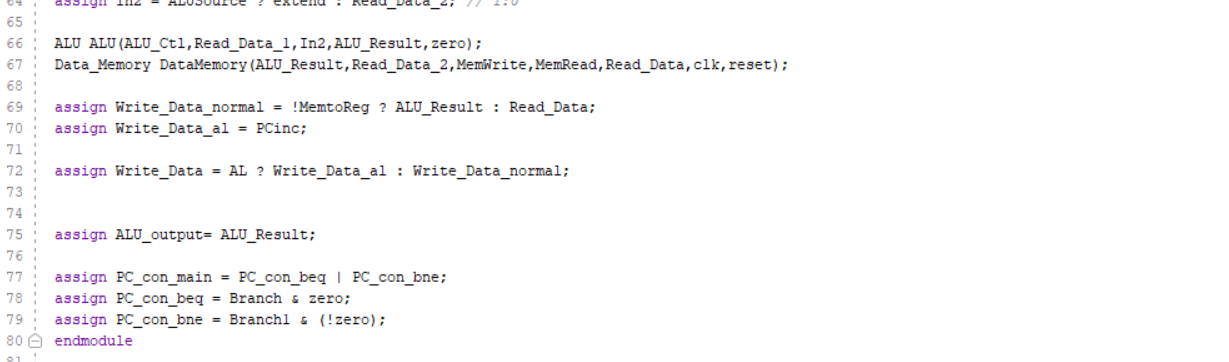
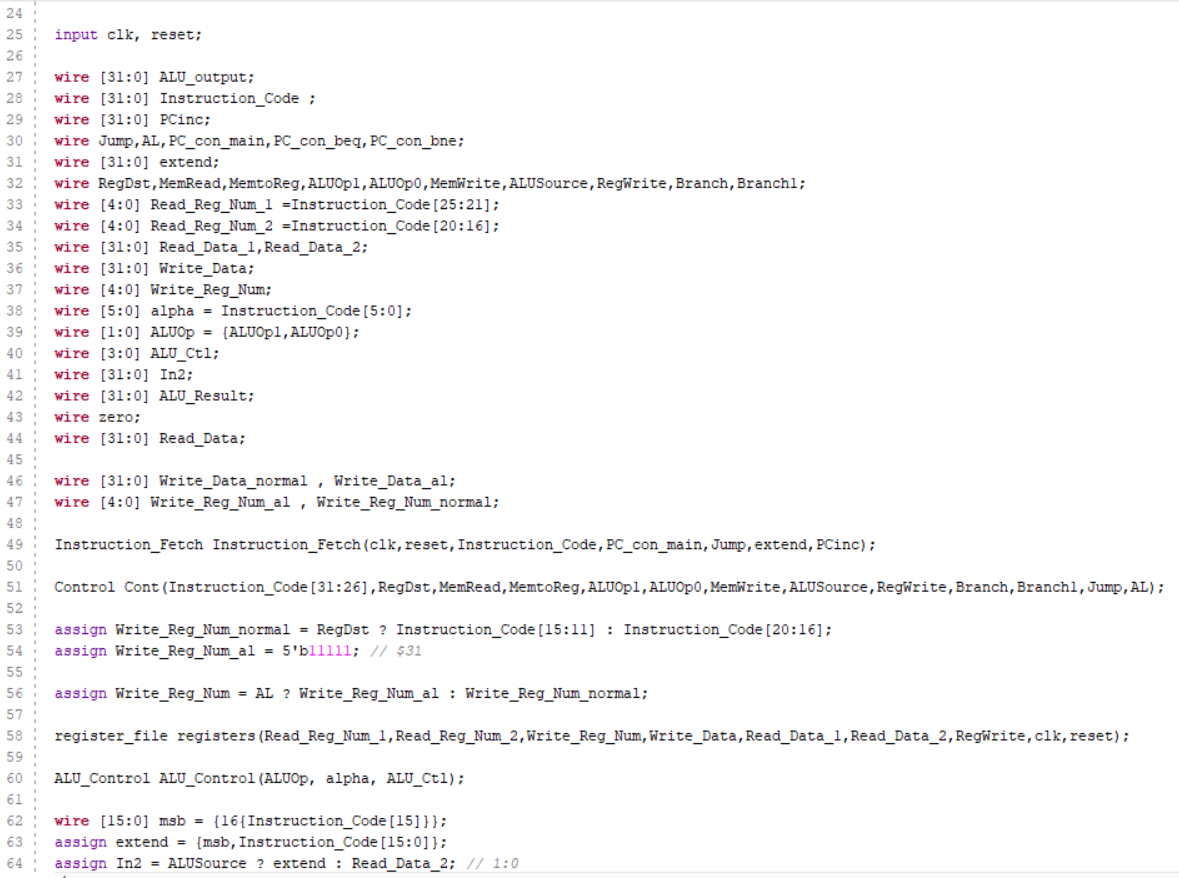
**jal Start**

***Verilog Code for all the modules:***

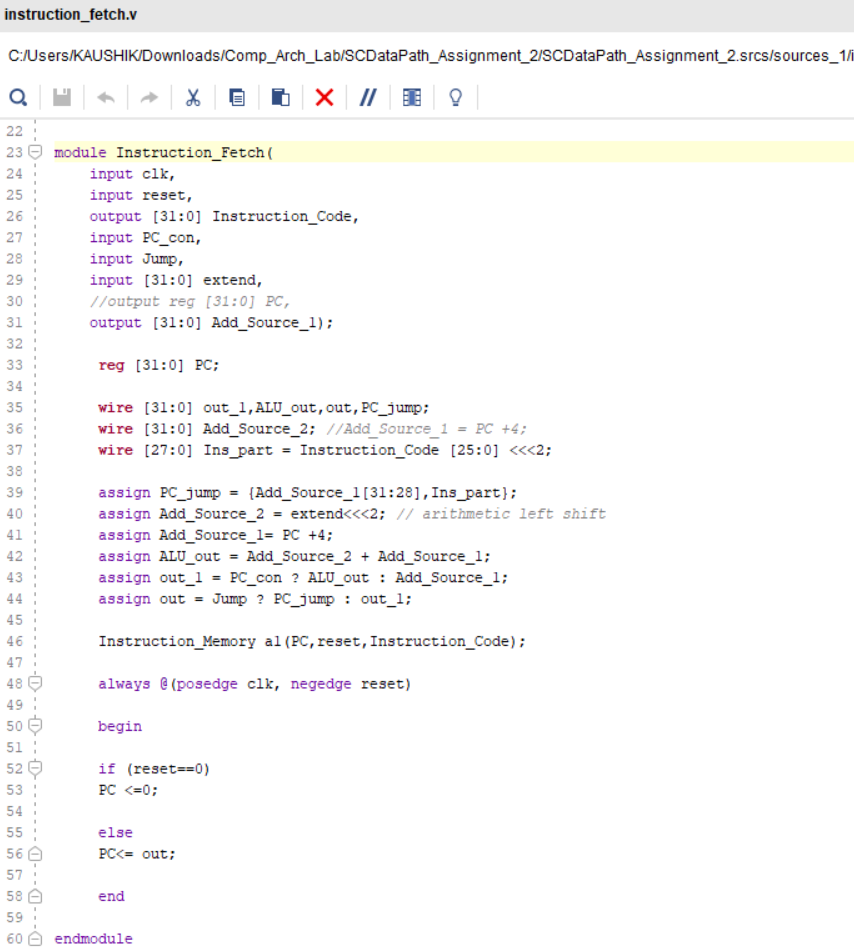
**ALU.v**

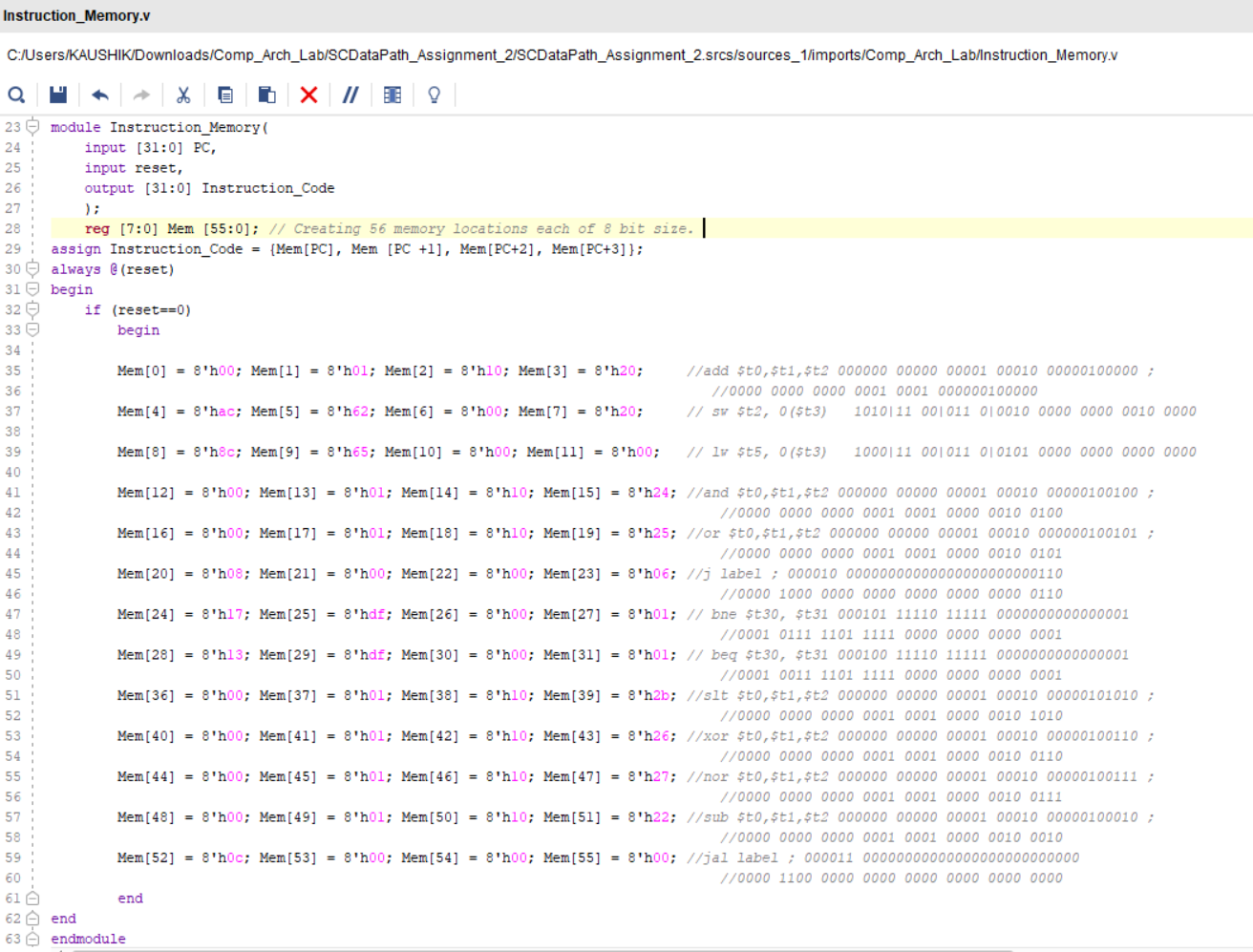
****

**SCDataPath.v**

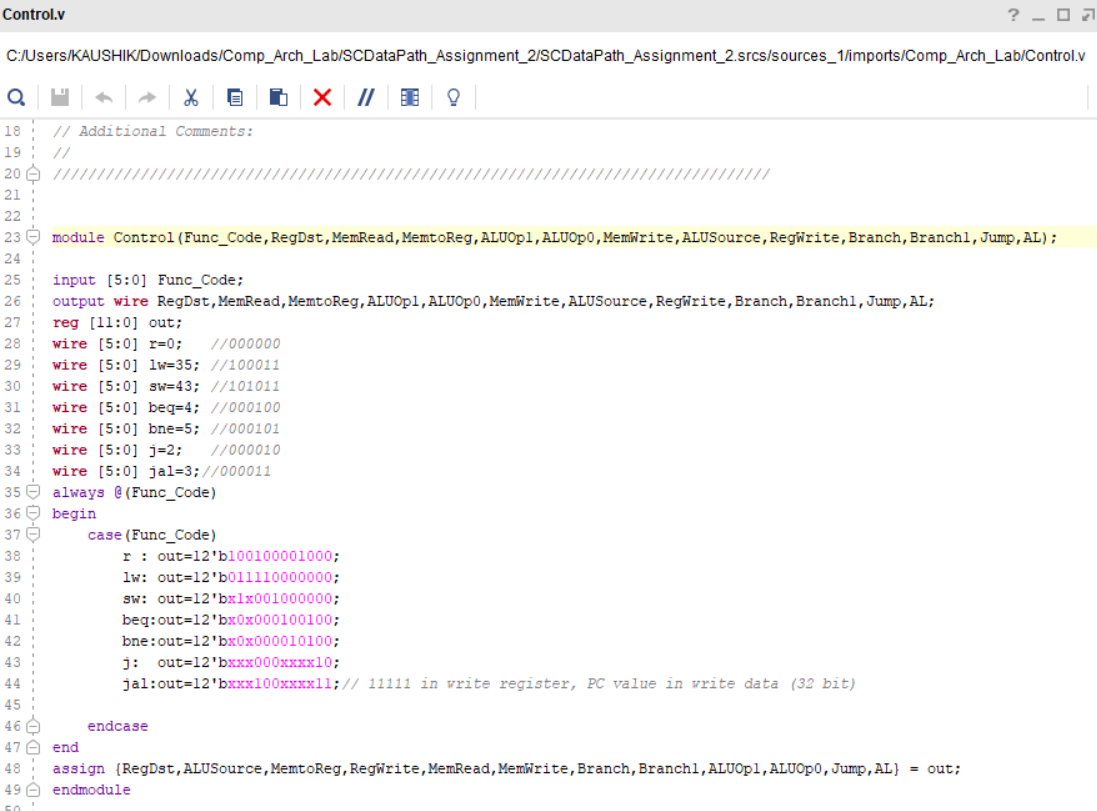
****

**Instruction\_fetch.v**

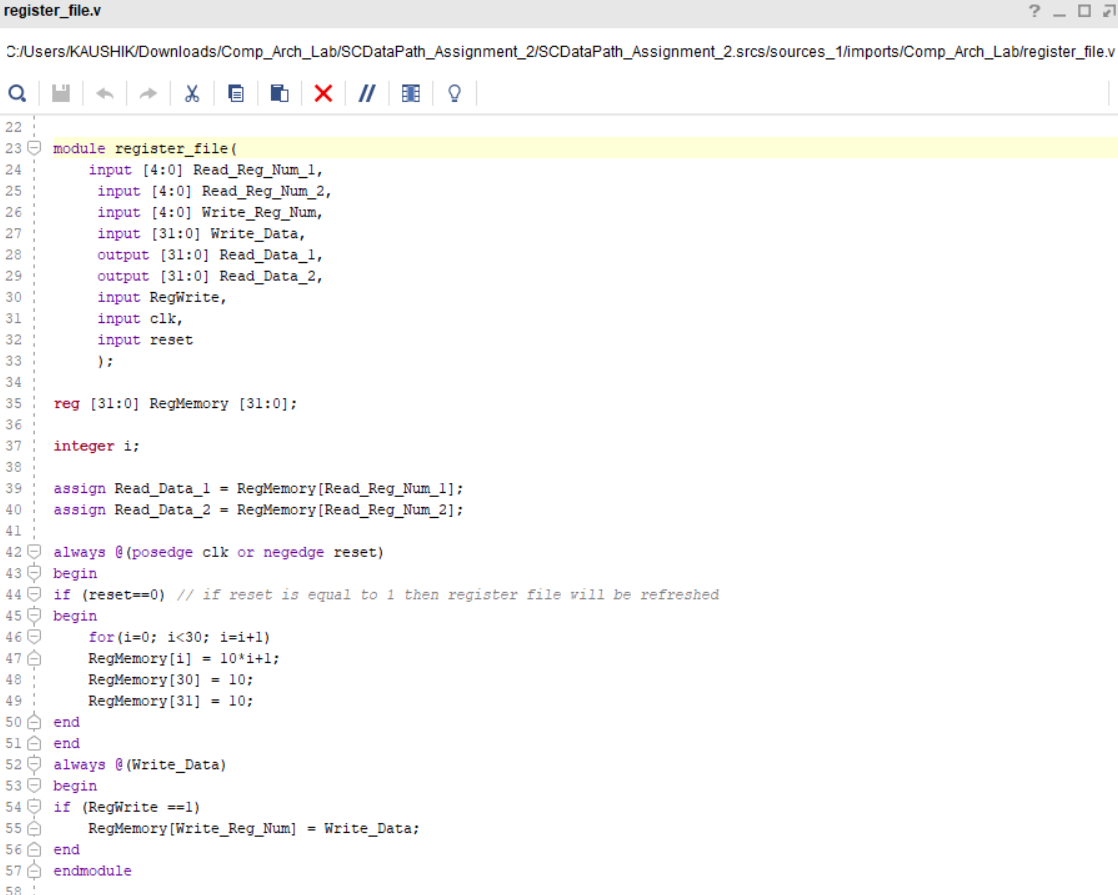
****

**Instruction\_Memory.v**

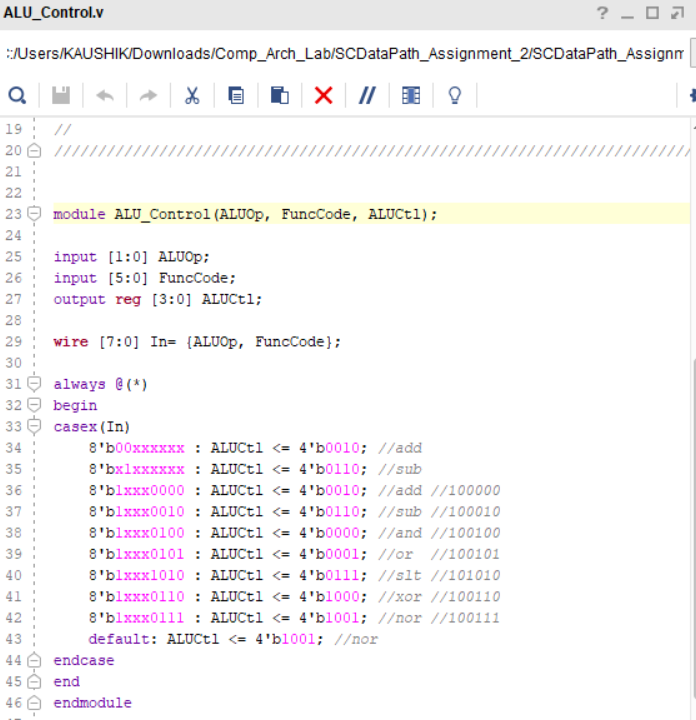
**Control.v**

****

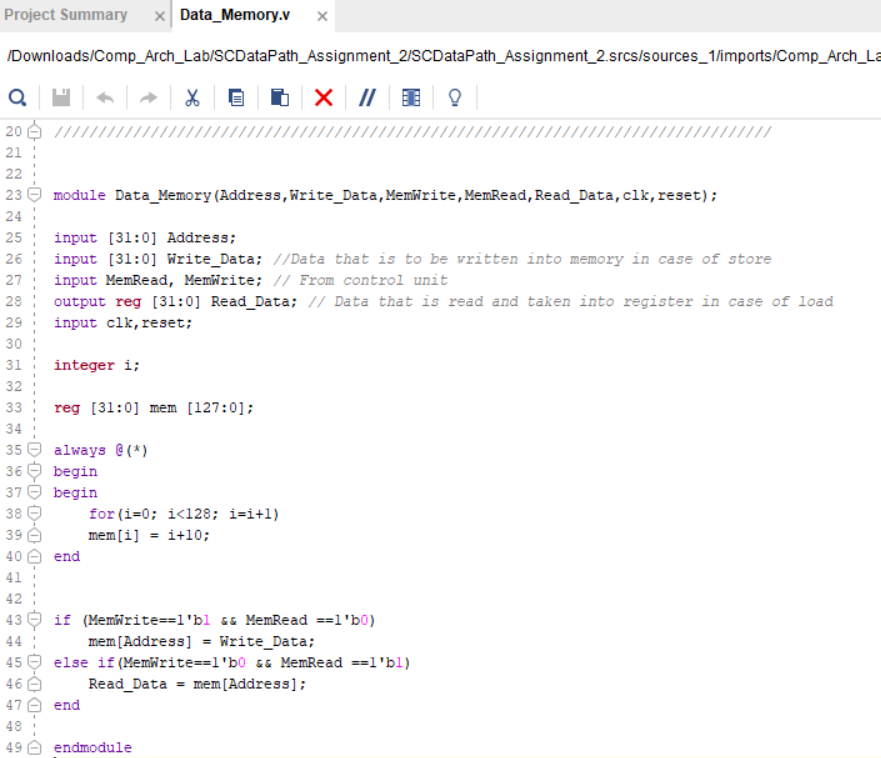
**Register\_file.v**

****

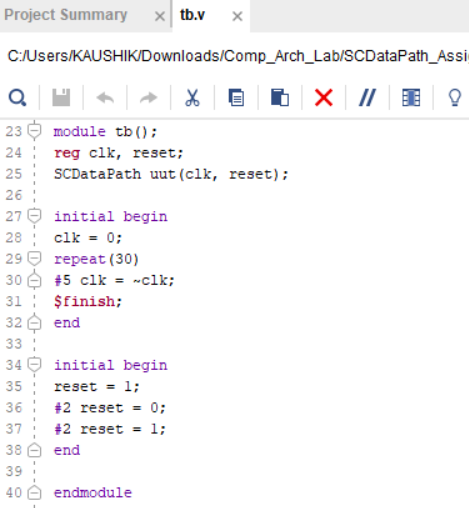
**ALU\_Control.v**

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**Data\_Memory.v**

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**Testbench:**

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***Output Waveform:***

