CS5120
HLS and Zynq Board

Dr. Unnikrishnan C

Introduction : Vitis HLS

- **High-level synthesis (HLS)**

A hardware design process that translates an algorithmic description into a register transfer level (RTL) hardware description language. RTL specifies the exact behavior of the circuit on a cycle-by-cycle basis.

- **RTL**

Register-transfer level (RTL) is a hardware design abstraction which models a synchronous digital circuit using logical operations that occur between hardware registers.

- **C/RTL cosimulation**

The process of verifying an RTL design generated by HLS using testvectors captured from the C testbench.

- **IP core**

An RTL-level component with well-defined interfaces enabling it to be incorporated into a larger design.

Introduction : Vitis HLS

- **Logic Synthesis**
  - The process of converting an RTL design into a netlist of device-level primitives.
- **Netlist**

  An intermediate design artifact consisting of device-level primitive elements and the connections between them.

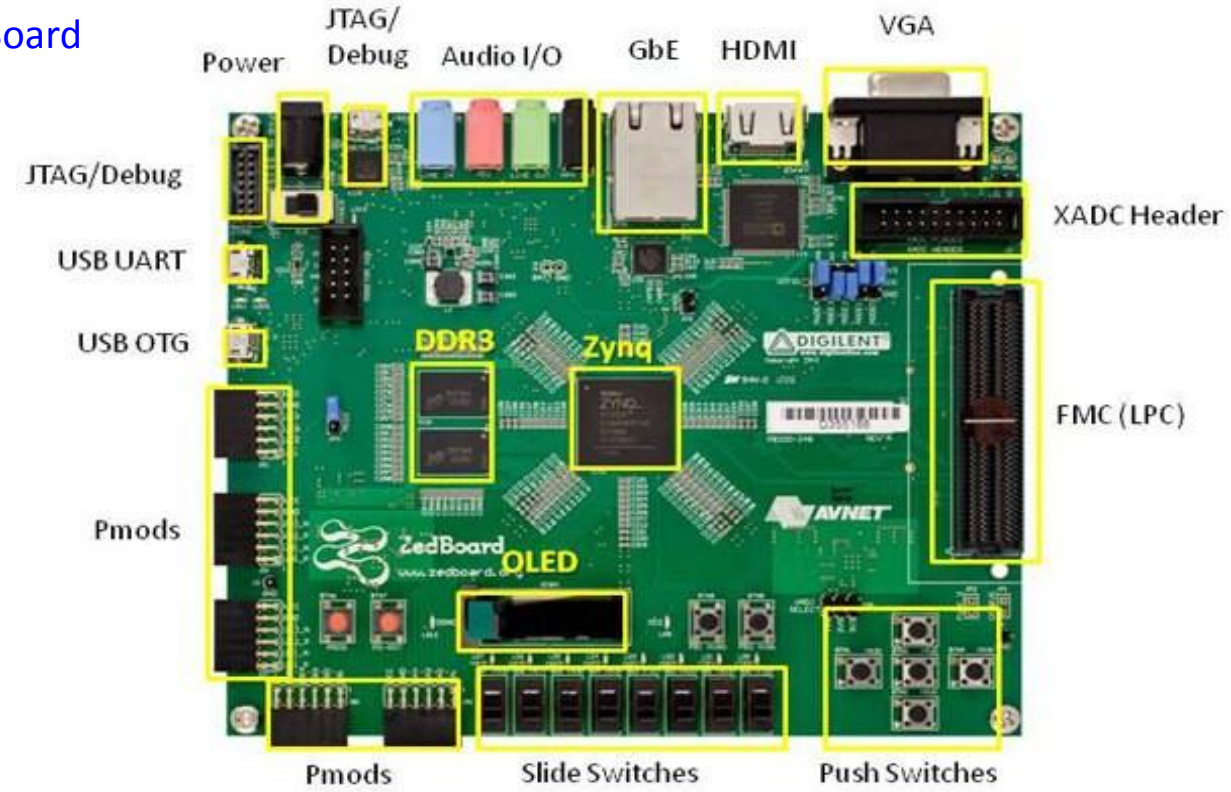
- **Place and route**

  The process of converting a netlist of device-level primitives into the configuration of a particular device.

- **Switchbox**

  Switchbox connects routing channels to provide a flexible routing structure for data routed between the programmable logic and I/O block.

Xilinx Zed Board



* SD card cage and QSPI Flash reside on backside of board

Resources in Zed Board (Zynq 7000 Series)

- Look UP Table (LUT)
  - Resource inside an FPGA
  - Implements Combinational Logic
  - Can be thought of as a small table that stores truth table.
  - In Xilinx 7 series LUTs are typically 6 input LUTs.
  - Can be used implement Shift registers and RAM.
- Flip Flops
  - Stores one bit data.
  - Can be used to implement Registers, Counters, Finite State Machines etc.
- BRAM
  - Hardening programmable logic
  - A memory block inside FPGA that acts like a RAM.
  - Optimized for Size and Speed.
  - Used to implement FIFO, Buffers, Instruction/Data Memory

Resources in Zed Board (Zynq 7000 Series)

- DSP Slice
  - Dedicated Arithmetic Unit
  - Hardening the FPGA
  - Xilinx 7000 Series DSP slices are called DSP48E
  - Operation: D= AxB +C
  - Can do multiplication, Addition, and multiply and accumulate.
  - Used in FIR, FFTs, Matrix Multiplication, Digital signal processing (DSP) etc.
  - Typical Size: A (25 bits), B(18 bits), C and D (48 bit)
- Processing System (PS)
  - Non Programmable processor part of the Zynq 7000 series
  - Has a Dual core ARM Cortex-A9 processor, Memory, AXI interfaces, peripherals etc.
- InterConnects
  - AXI interconnect between PS and Programmable Logic (PL)
  - AXI-4, AXI4-lite, AXI4-Stream.
- Direct Memory Access (DMA)
  - Transfer data between DDR memory and Programmable Logic, initiated by PS.
  - CPU does other work during this time.