

Block Design - inputoutput*

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Run Linter
- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Diagram

Run Automation

Automatically make connections in your design by checking the boxes of the blocks to connect. Select a block on the left to display its configuration options on the right.

Block Properties

processing_system7_0

Name: processing_system
Parent name: inputoutput

Description

This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action cannot be undone. Zynq™ block automation applies current board preset and generates external connections for FIXED_IO, Trigger and DDR interfaces.

NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box if you wish to retain previous configuration.

Instance: /processing_system7_0

Options

Make Interface External: FIXED IO: DDR
Apply Board Preset:
Cross Trigger In: Disable
Cross Trigger Out: Disable

Tcl Console

```

INFO: [IP_Flow 19-2313] Info
create_project -f . -o .
set_property board_part zc702
create_bd_design "inputoutput"
Write : C:\Users\User\Sil
create_bd_design: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1401.383 ; gain = 106.121
update_compile_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
...

```

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File Edit Flow Tools Reports Window Layout View Help Q: Quick Access

Diagram

processing_system7_0

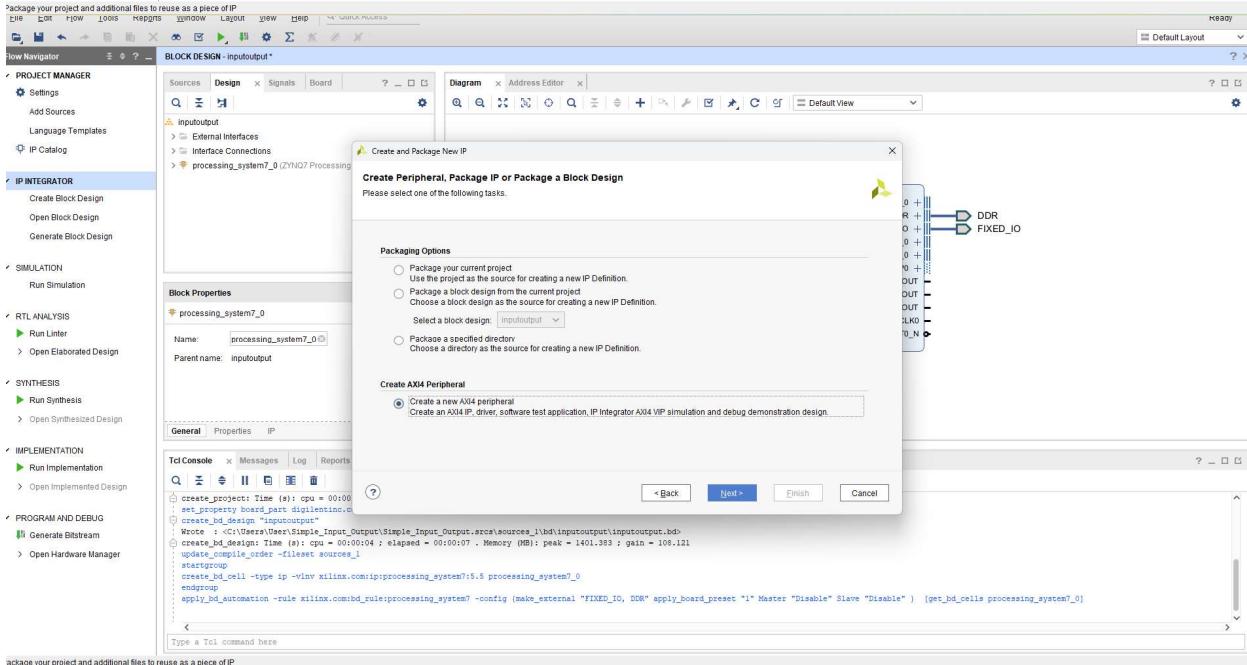
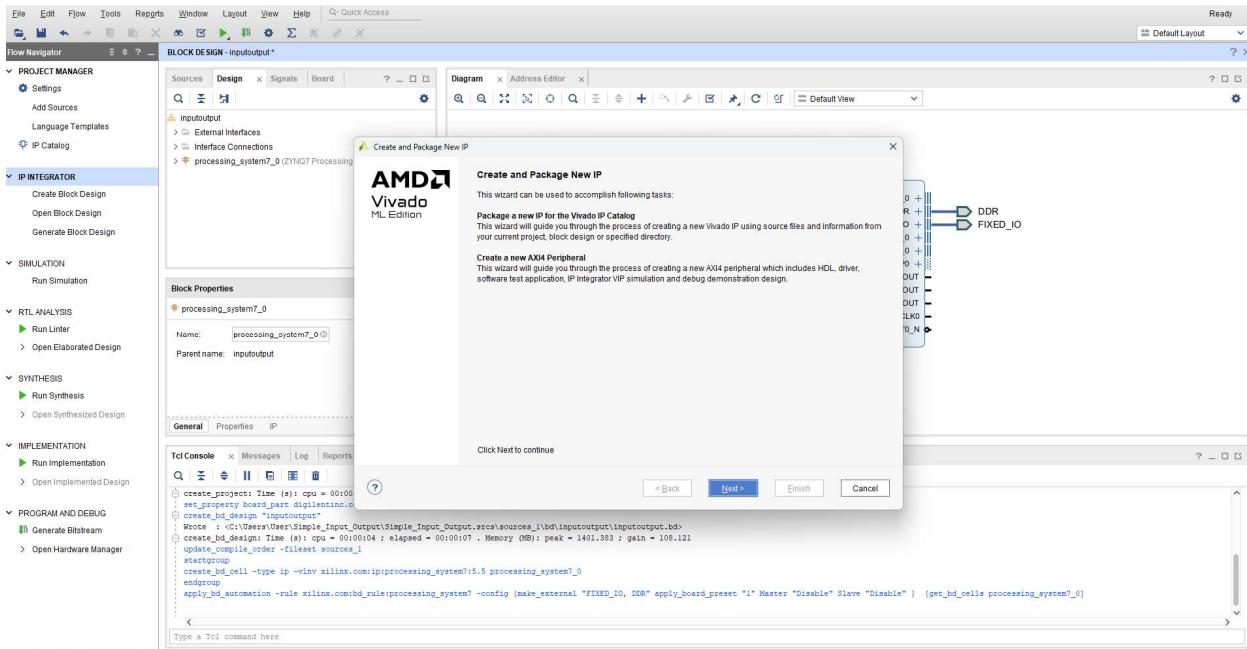
ZYNQ7 Processing System

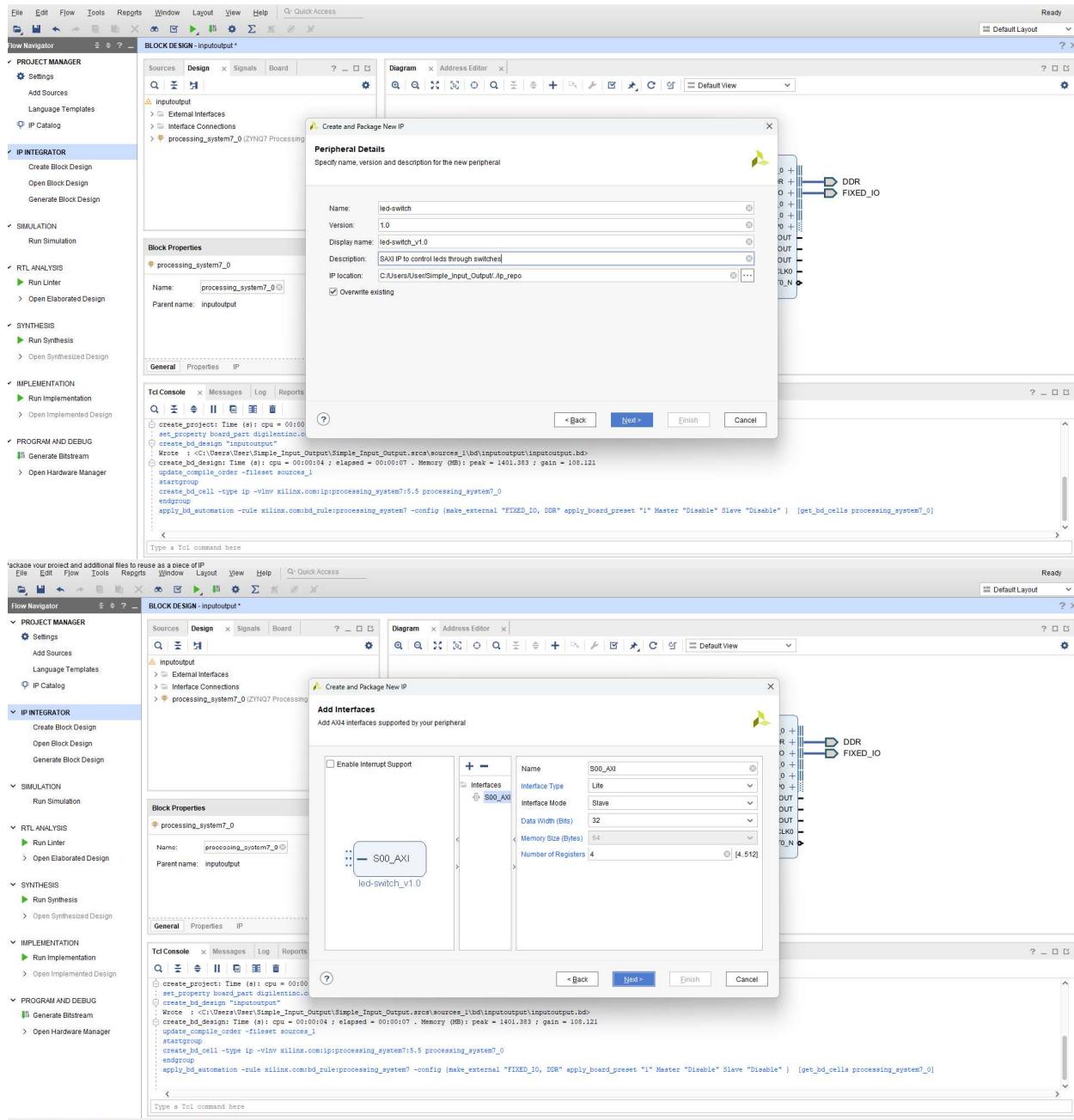
Tcl Console

```

INFO: [IP_Flow 19-2313] Info
create_project -f . -o .
set_property board_part zc702
create_bd_design "inputoutput"
Write : C:\Users\User\Sil
create_bd_design: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1401.383 ; gain = 106.121
update_compile_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" } [get_bd_cells processing_system7_0]
...

```





Top Window (Vivado 2017.4):

Block Design - inputoutput

PROJECT MANAGER:

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR** (Selected)

 - Create Block Design
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 - Generate Block Design

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- PROGRAM AND DEBUG

 - Generate Bitstream
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Diagram: Shows the `processing_system7_0` block with various pins and connections.

Create Peripheral: A dialog box showing the peripheral generation summary and options to add it to the repository or verify it using AXI4 VIP or JTAG interface.

Tcl Console:

```

create_project -force -dir "C:/Users/User/Simple_Input_Output" -part xc7z020clg484-1
create_bd_design "inputoutput"
write_bdf -force -file "C:/Users/User/Simple_Input_Output/sources_1/bd/inputoutput/inputoutput.bd"
create_bd_design -Time (s) :cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB) : peak = 1401.303 ; gain = 108.121
generate_ip_order -fileset sources_1
startgroup
create_bd_cell -type ip -vlnr xilinx.com:processing_system7:5.3 processing_system7_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" } [get_bd_cells processing_system7_0]
...

```

Bottom Window (Vivado 2017.4):

Block Design - inputoutput

PROJECT MANAGER:

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR** (Selected)

 - Create Block Design
 - Open Block Design
 - Generate Block Design

- SIMULATION

 - Run Simulation

- RTL ANALYSIS

 - Run Linter
 - Open Elaborated Design

- SYNTHESIS

 - Run Synthesis
 - Open Synthesized Design

- IMPLEMENTATION

 - Run Implementation
 - Open Implemented Design

- PROGRAM AND DEBUG

 - Generate Bitstream
 - Open Hardware Manager

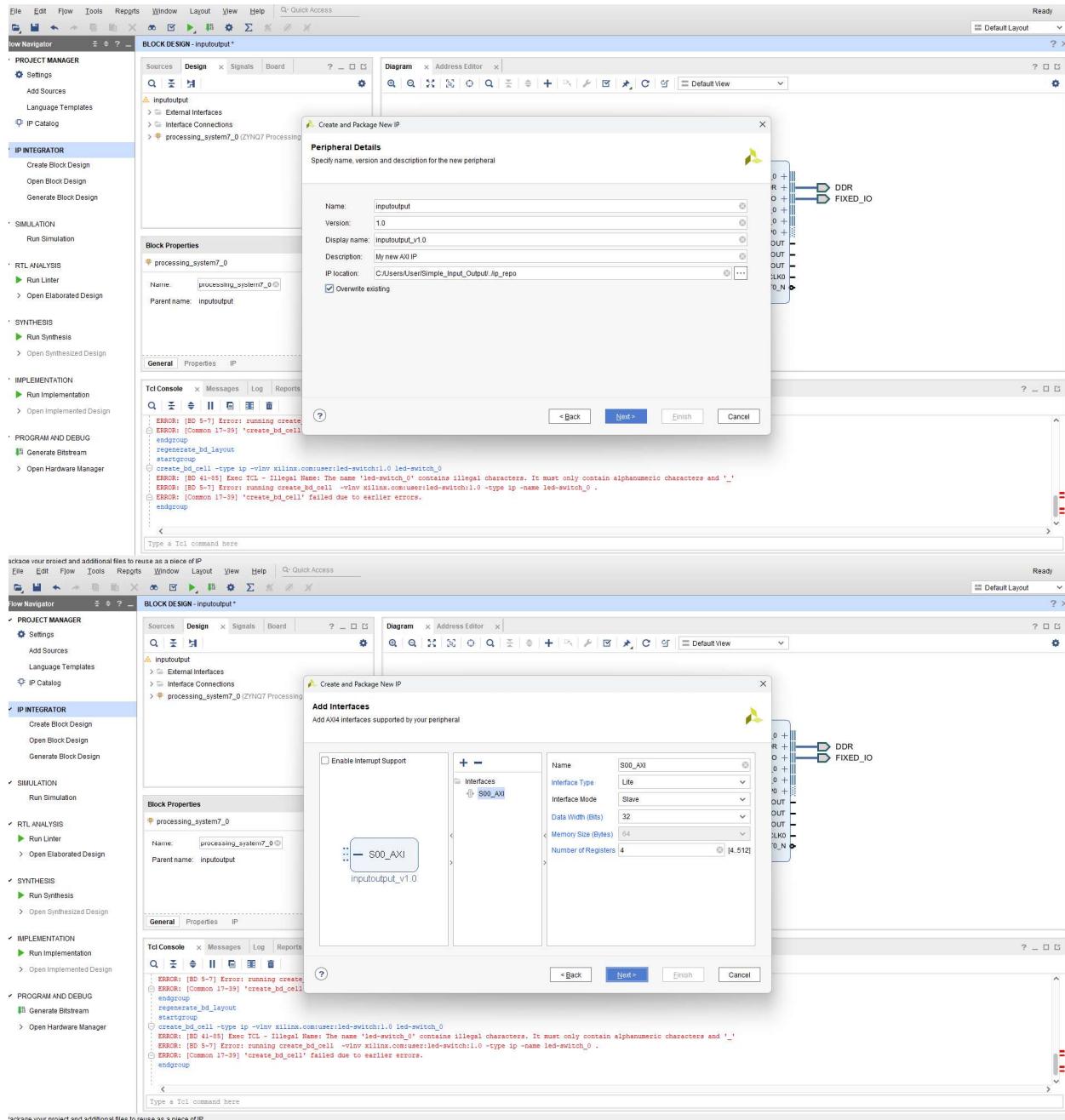
Diagram: Shows the `processing_system7_0` block with various pins and connections, including `led-switch_v1_0`.

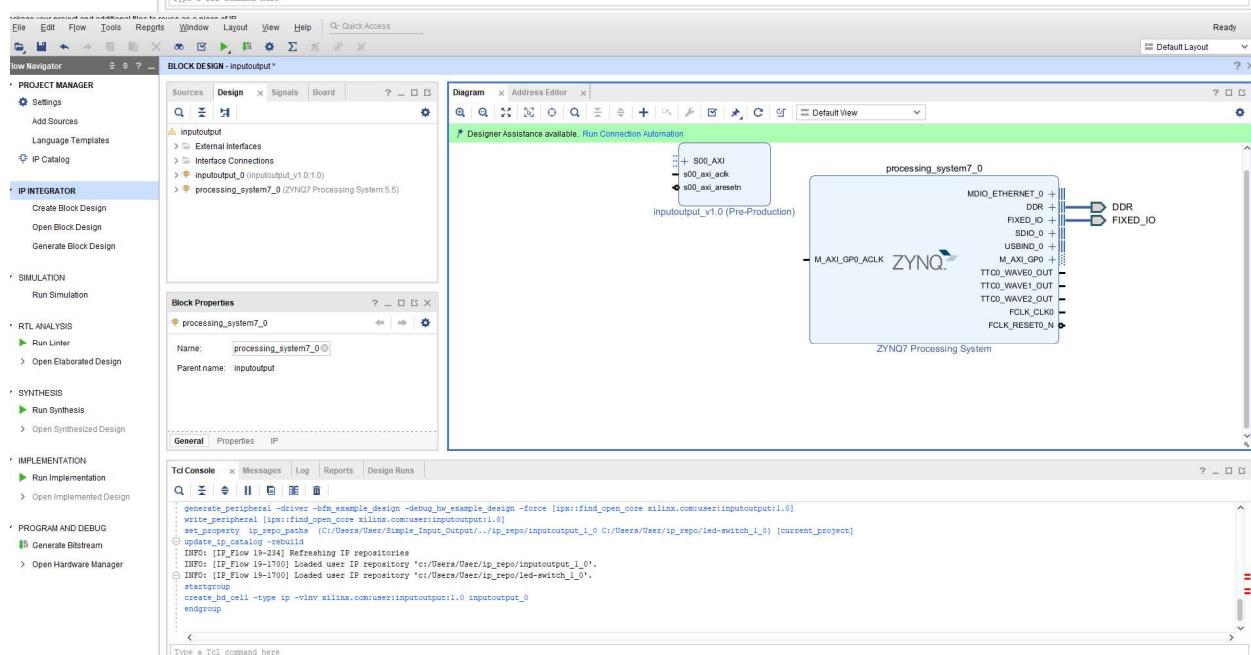
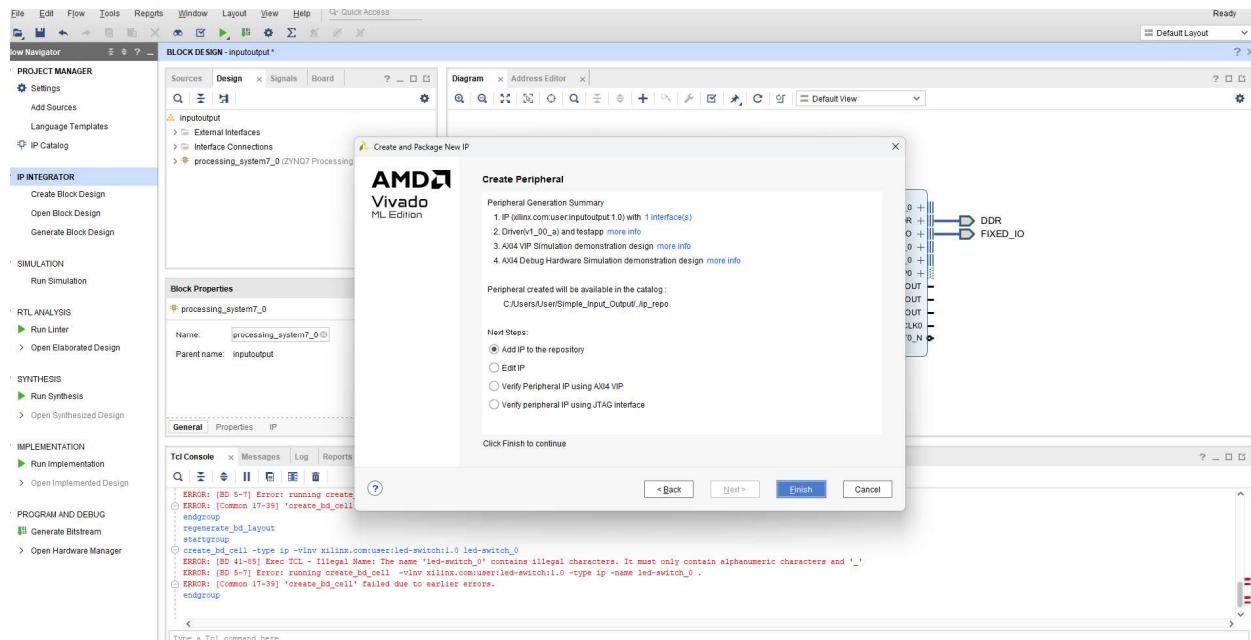
Tcl Console:

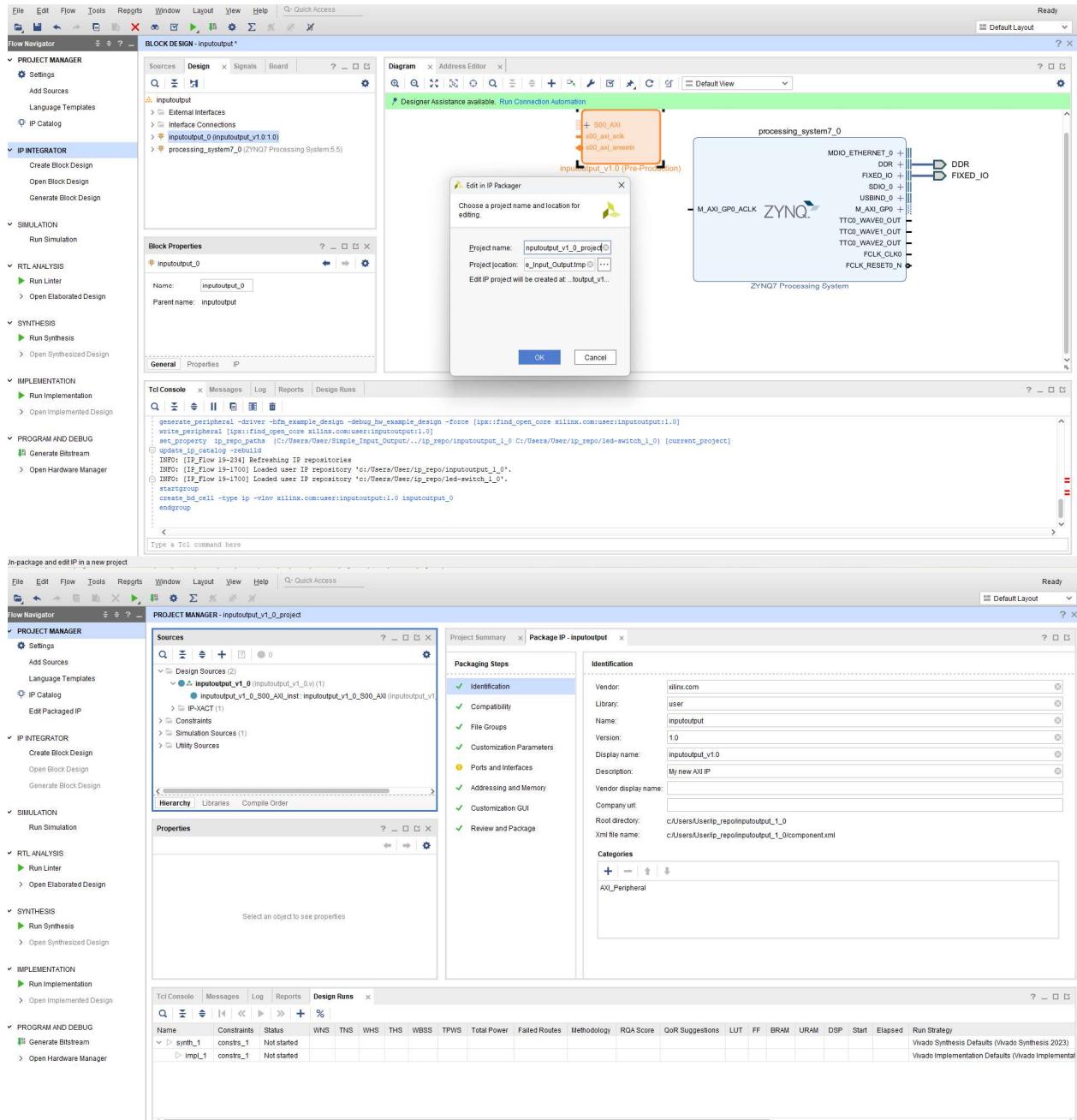
```

endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master "Disable" Slave "Disable" } [get_bd_cells processing_system7_0]
create_peripheral -fileset sources_1 -name led-switch_v1_0 -ip_repo_path "C:/Users/User/Simple_Input_Output/..//ip_repo/led-switch_v1_0"
create_peripheral -fileset sources_1 -name led-switch_v1_0 -interface_mode slave -addr_type 16 -ip_repo_path "C:/Users/User/Simple_Input_Output/..//ip_repo/led-switch_v1_0"
generate_peripheral -driver -bfm_example_design -debug_hw_example_design -force [ipx::find_open_core xilinx.com:user:led-switch_v1_0]
write_peripheral [ipx::find_open_core xilinx.com:user:led-switch_v1_0] (processing_system7_0)
set_property ip_repo_paths C:/Users/User/Simple_Input_Output/..//ip_repo/led-switch_v1_0 [current_project]
update_ip_catalog -rebuild
INFO: [IP_Flow 14-234] Refreshing IP repositories
INFO: [IP_Flow 14-1700] Loaded user IP repository 'C:/Users/User/IP_REPO/led-switch_v1_0'
...

```







PROJECT MANAGER - inputoutput_v1_0_project

Sources

```

1: 10000000000000000000000000000000
2: 10000000000000000000000000000000
3: 10000000000000000000000000000000
4: 10000000000000000000000000000000
5: 10000000000000000000000000000000
6: 10000000000000000000000000000000
7: 10000000000000000000000000000000
8: 10000000000000000000000000000000
9: 10000000000000000000000000000000
10: 10000000000000000000000000000000
11: 10000000000000000000000000000000
12: 10000000000000000000000000000000
13: 10000000000000000000000000000000
14: 10000000000000000000000000000000
15: 10000000000000000000000000000000
16: 10000000000000000000000000000000
17: 10000000000000000000000000000000
18: 10000000000000000000000000000000
19: 10000000000000000000000000000000
20: 10000000000000000000000000000000
21: 10000000000000000000000000000000
22: 10000000000000000000000000000000
23: 10000000000000000000000000000000
24: 10000000000000000000000000000000
25: 10000000000000000000000000000000
26: 10000000000000000000000000000000
27: 10000000000000000000000000000000
28: 10000000000000000000000000000000
29: 10000000000000000000000000000000
30: 10000000000000000000000000000000

```

Source File Properties

General Properties

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constrs_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

PROJECT MANAGER - inputoutput_v1_0_project

Sources

```

372 : // Address decoding for reading registers
373 : case ( axi_araddr[ADDR_LSB-1:ADDR_BITS:ADDR_LSB] )
374 :     2'h0 : reg_data_out <= 4'b0000;
375 :     2'h1 : reg_data_out <= 4'b0001;
376 :     2'h2 : reg_data_out <= 4'b0010;
377 :     2'h3 : reg_data_out <= 4'b0011;
378 :     default : reg_data_out <= 4'b0000;
379 : endcase
380 :
381 :
382 : // Output register or memory read data
383 : always @posedge S_AXI_ACLK
384 : begin
385 :     if ( S_AXI_ARVALID == 1'b0 )
386 :         begin
387 :             axi_rdata <= 0;
388 :         end
389 :     else
390 :         begin
391 :             // When there is a valid read address (S_AXI_ARVALID) with
392 :             // acceptance of read address by the slave (axi_arready),
393 :             // output the read data
394 :             if ( s1v_reg_rden )
395 :                 begin
396 :                     axi_rdata <= reg_data_out; // register read data
397 :                 end
398 :             end
399 :         end
400 : end
401 : // Add user logic here

```

Source File Properties

General Properties

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constrs_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator

PROJECT MANAGER - inputoutput_v1_0_project

Sources

- Design Sources (2)
 - inputoutput_v1_0 (inputoutput_v1_0.v)
 - IP-XACT (1)
- Constraints
- Simulation Sources (1)
- Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

- Enabled
- Location: c:\Users\Userip_repolinputoutput_v1_0\hdl
- Type: Verilog
- Library:
- Size: 14.2 KB
- Modified: Today at 18:09:10 PM

General Properties

Tcl Console Messages Log Reports Design Runs

```

Project Summary | Package IP - inputoutput_v1_0_S00_AXI.v | inputoutput_v1_0_S00_AXI.x | inputoutput_v1_0.v | 
c:\Users\Userip_repolinputoutput_v1_0\hdl\inputoutput_v1_0_S00_AXI.v

379 endcase
380
381 // Output register or memory read data
382 always @(posedge S_AXI_ACLK)
383 begin
384   if (S_AXI_ARESETN == 1'b0)
385     begin
386       axi_data <= 0;
387     end
388   else
389     begin
390       // When there is a valid read address (S_AXI_AVALID) with
391       // acceptance of read address by the slave (axi_arready),
392       // output the read data
393       if (S_AXI_ARVALID)
394         begin
395           axi_data <= reg_data_out; // register read data
396         end
397     end
398   end
399
400   // Add user logic here
401 assign led_o = S_AXI_ARVALID[7:0];
402
403   // User logic ends
404
405 endmodule
406
407

```

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constraints_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constraints_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

File Edit Flow Tools Reports Window Layout View Help Quick Access

Flow Navigator

PROJECT MANAGER - inputoutput_v1_0_project

Sources

- Design Sources (2)
 - inputoutput_v1_0 (inputoutput_v1_0.v)
 - IP-XACT (1)
- Constraints
- Simulation Sources (1)
- Utility Sources

Hierarchy Libraries Compile Order

Source File Properties

- Enabled
- Location: c:\Users\Userip_repolinputoutput_v1_0\hdl
- Type: Verilog
- Library:
- Size: 2.2 KB
- Modified: Today at 18:04:23 PM

General Properties

Tcl Console Messages Log Reports Design Runs

```

Project Summary | Package IP - inputoutput_v1_0_S00_AXI.v | inputoutput_v1_0_S00_AXI.x | inputoutput_v1_0.v | 
c:\Users\Userip_repolinputoutput_v1_0\hdl\inputoutput_v1_0.v

1 timescale 1 ns / 1 ps
2
3 module inputoutput_v1_0
4
5   // Users to add parameters here
6
7   // User parameters ends
8   // Do not modify the parameters beyond this line
9
10
11
12   // Parameters of Axil Slave Bus Interface S00_AXI
13   parameter integer C_S00_AXI_DATA_WIDTH = 32;
14   parameter integer C_S00_AXI_ADDR_WIDTH = 4;
15
16   (
17     // Users to add ports here
18     input wire [7:0] s00_axi_awaddr,
19     output wire [7:0] led_o,
20     // User ports ends
21     // Do not modify the ports beyond this line
22
23
24   // Ports of Axil Slave Bus Interface S00_AXI
25   input wire [0:0] s00_axi_aclk,
26   input wire [0:0] s00_axi_aresetn,
27   input wire [C_S00_AXI_ADDR_WIDTH-1 : 0] s00_axi_awaddr,
28   input wire [2 : 0] s00_axi_awprot,
29   input wire [0:0] s00_axi_awvalid,
30   output wire s00_axi_awready,

```

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constraints_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constraints_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

Project Manager - inputoutput_v1_0_project

Sources

- Design Sources (2)
 - inputoutput_v1_0 (inputoutput_v1_0.v) (1)
 - IP-XACT (1)
- Constraints
- Simulation Sources (1)
- Utility Sources

Source File Properties

inputoutput_v1_0.v

- Enabled
- Location: c:\Users\Userip_repolinputput_1_0\hdl\inputoutput_v1_0.hdl
- Type: Verilog
- Library:
- Size: 2.2 KB
- Modified: Today at 18:04:23 PM

Tcl Console

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constrs_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

Project Summary

Package IP - inputoutput

inputoutput_v1_0_S00_AXI.v

```

c:/Users/Userip_repolinputput_1_0\hdl\inputoutput_v1_0.v

52 :     .S_AXI_ACLK(m00_axi_aclk),
53 :     .S_AXI_ARESETN(m00_axi_arestn),
54 :     .S_AXI_AWADDR(m00_axi_awaddr),
55 :     .S_AXI_AWPROT(m00_axi_awprot),
56 :     .S_AXI_AWVALID(m00_axi_awvalid),
57 :     .S_AXI_AWREADY(m00_axi_awready),
58 :     .S_AXI_WDATA(m00_axi_wdata),
59 :     .S_AXI_WSTRB(m00_axi_wstrb),
60 :     .S_AXI_WVALID(m00_axi_wvalid),
61 :     .S_AXI_WREADY(m00_axi_wready),
62 :     .S_AXI_BRESP(m00_axi_bresp),
63 :     .S_AXI_BVALID(m00_axi_bvalid),
64 :     .S_AXI_BREADY(m00_axi_bready),
65 :     .S_AXI_ARADDR(m00_axi_araddr),
66 :     .S_AXI_ARPROT(m00_axi_arprot),
67 :     .S_AXI_ARVALID(m00_axi_arvalid),
68 :     .S_AXI_ARREADY(m00_axi_arready),
69 :     .S_AXI_RDATA(m00_axi_rdata),
70 :     .S_AXI_RRESP(m00_axi_rresp),
71 :     .S_AXI_RVALID(m00_axi_rvalid),
72 :     .S_AXI_RREADY(m00_axi_rready),
73 :     .switches_in(switches_in),
74 :     .leds_out(leds_out)
75 :
76 :
77 : // Add user logic here
78 :
79 : // User logic ends
80 :
81 endmodule

```

PROJECT MANAGER - inputoutput_v1_0_project

Sources

- Design Sources (2)
 - inputoutput_v1_0 (inputoutput_v1_0.v) (1)
 - IP-XACT (1)
- Constraints
- Simulation Sources (1)
- Utility Sources

Source File Properties

inputoutput_v1_0.v

- Enabled
- Location: c:\Users\Userip_repolinputput_1_0\hdl\inputoutput_v1_0.hdl
- Type: Verilog
- Library:
- Size: 2.4 KB
- Modified: Today at 18:12:26 PM

Tcl Console

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constrs_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

Packaging Steps

Identification

- Vendor: xilinx.com
- Library: user
- Name: inputoutput
- Version: 1.0
- Display name: inputoutput_v1_0
- Description: My new AXI IP
- Vendor display name:
- Company url:
- Root directory: c:\Users\Userip_repolinputput_1_0
- Xml file name: c:\Users\Userip_repolinputput_1_0\component.xml

Categories

- AXI_Peripheral

PROJECT MANAGER - inputoutput_v1_0_project

Sources

- Design Sources (2)
 - inputoutput_v1_0 (inputoutput_v1_0.v) (1)
 - IP-XACT (1)
- Constraints
- Simulation Sources (1)
- Utility Sources

Source File Properties

inputoutput_v1_0.v

- Enabled
- Location: c:\Users\userip_repo\inputoutput_v1_0\hdl
- Type: Verilog
- Library:
- Size: 2.4 KB
- Modified: Today at 18:12:26 PM

Packaging Steps

- Identification
- Compatibility
- File Groups**
- Customization Parameters
- Ports and Interfaces
- Addressing and Memory
- Customization GUI
- Review and Package

File Groups

Name	Library Name	Type	Is Include	File Group Name	Model Name
Standard					
Advanced					
Verilog Synthesis (2)				inputoutput_v1_0	inputoutput_v1_0
Verilog Simulation (2)					
Software Driver (6)					
UI Layout (1)					
Block Diagram (1)					

Tcl Console

Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constrs_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

Dell SupportAssist

Optimize your PC
Run our suite of optimization tools now to ensure your PC is up to date and running at its best.

PROJECT MANAGER - inputoutput_v1_0_project

Sources

- Design Sources (2)
 - inputoutput_v1_0 (inputoutput_v1_0.v) (1)
 - IP-XACT (1)
- Constraints
- Simulation Sources (1)
- Utility Sources

Source File Properties

inputoutput_v1_0.v

- Enabled
- Location: c:\Users\userip_repo\inputoutput_v1_0\hdl
- Type: Verilog
- Library:
- Size: 2.4 KB
- Modified: Today at 18:12:26 PM

Packaging Steps

- Identification
- Compatibility
- File Groups**
- Customization Parameters
- Ports and Interfaces**
- Addressing and Memory
- Customization GUI
- Review and Package

Review and Package

IP has been modified. 1 warning, 2 info messages

Summary

Display name: inputoutput_v1_0
Description: My new AXI IP
Root directory: c:\Users\userip_repo\inputoutput_v1_0

After Packaging

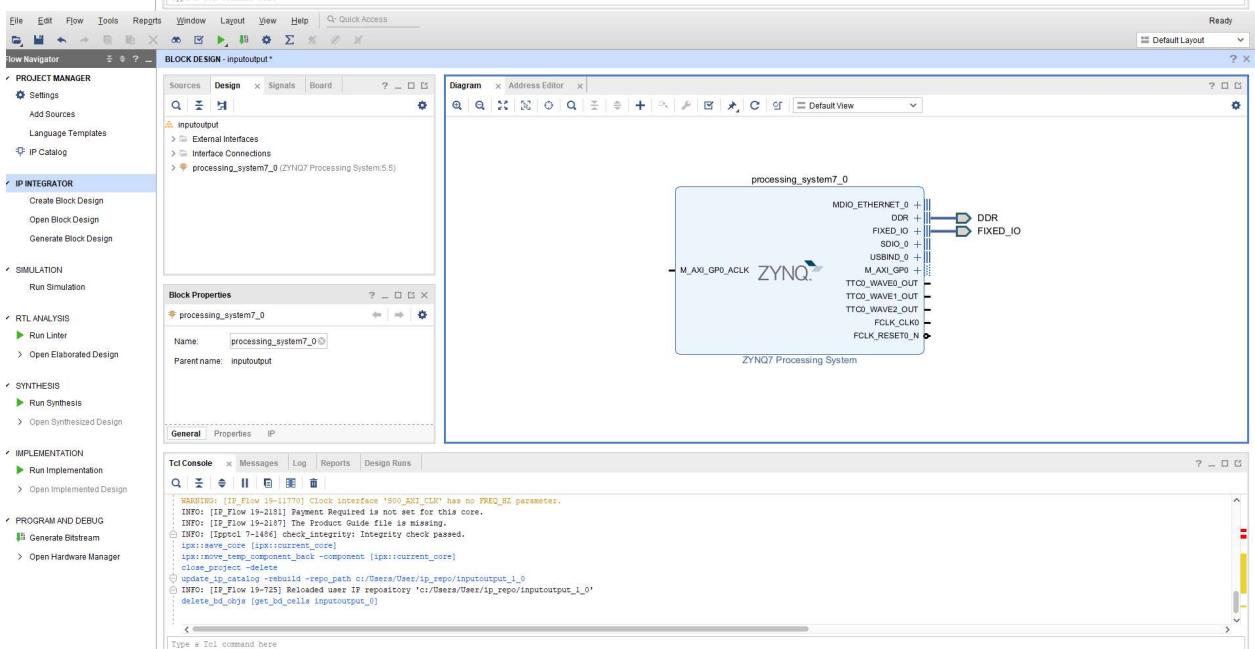
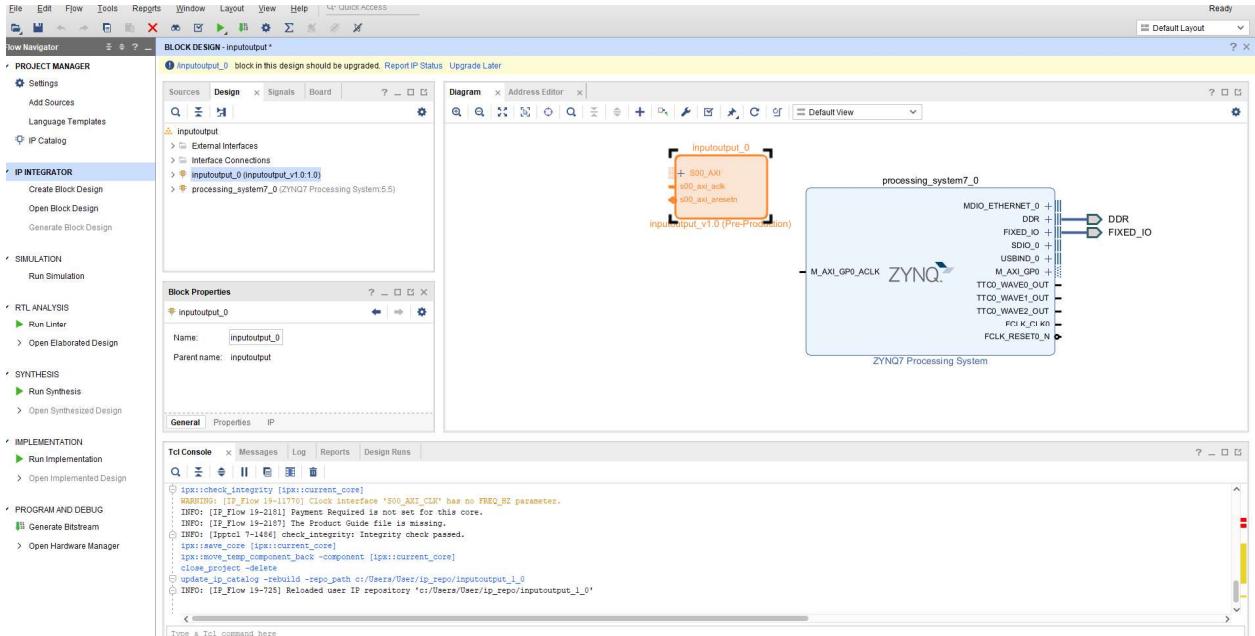
An archive will not be generated. Use the settings link below to change your preference
Project will be removed after completion
Edit packaging settings

Re-Package IP

Tcl Console

Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoR Suggestions	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started																			Vivado Synthesis Defaults (Vivado Synthesis 2023)
impl_1	constrs_1	Not started																			Vivado Implementation Defaults (Vivado Implementation 2023)

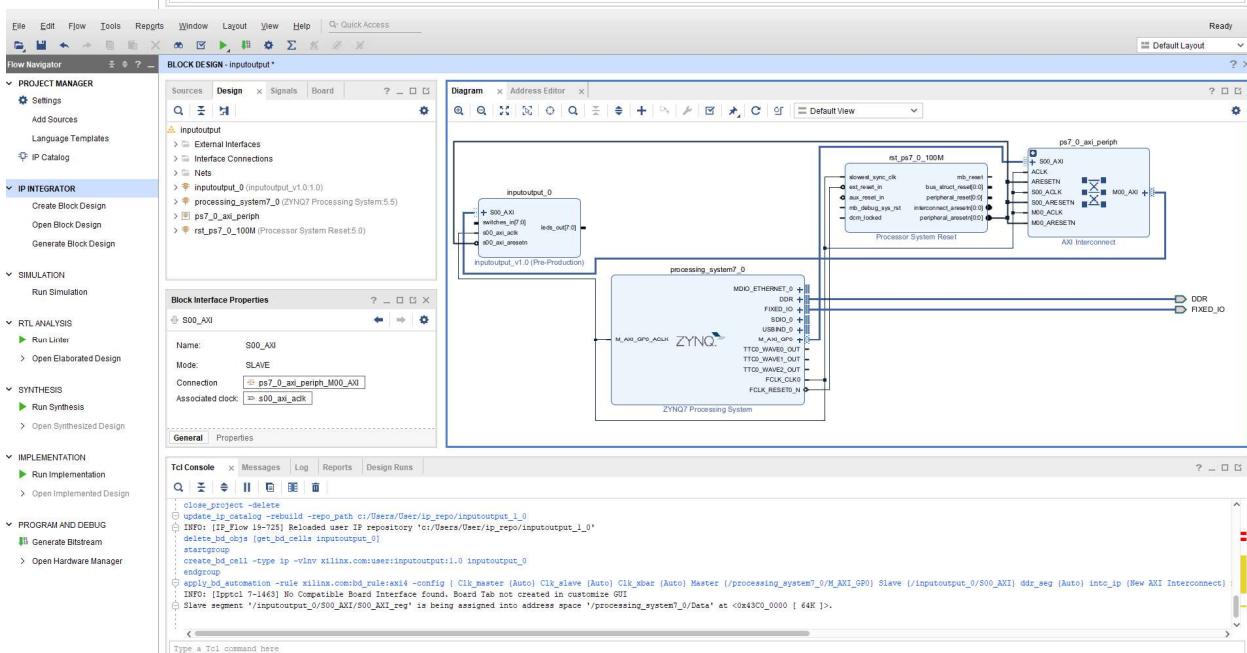
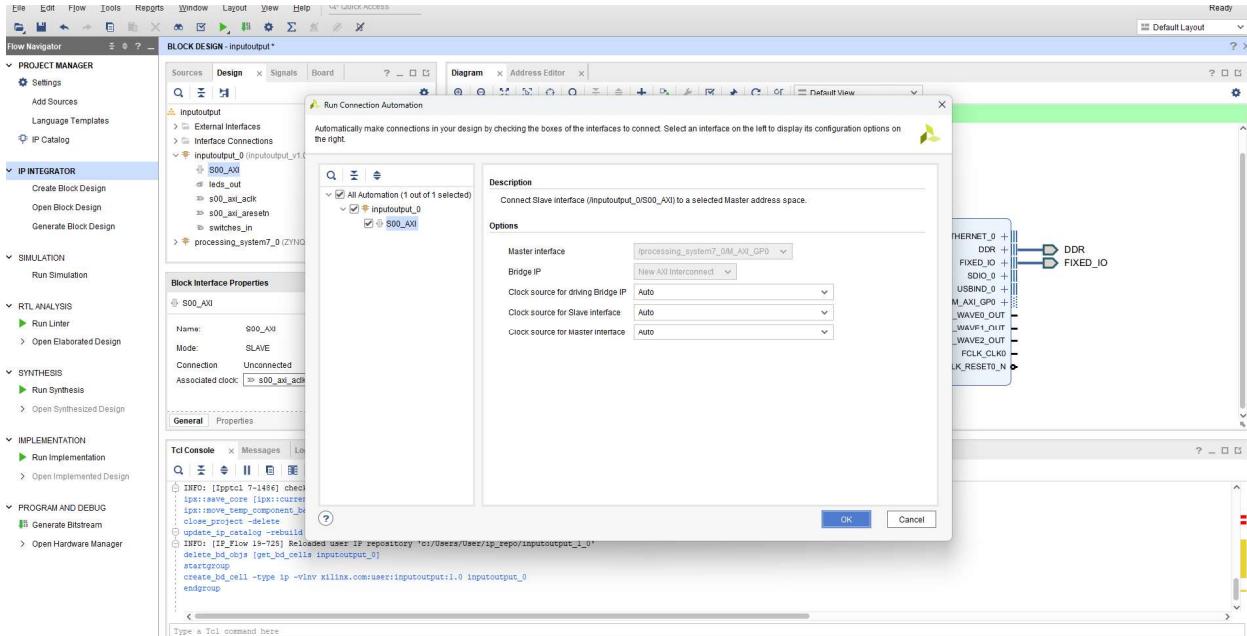


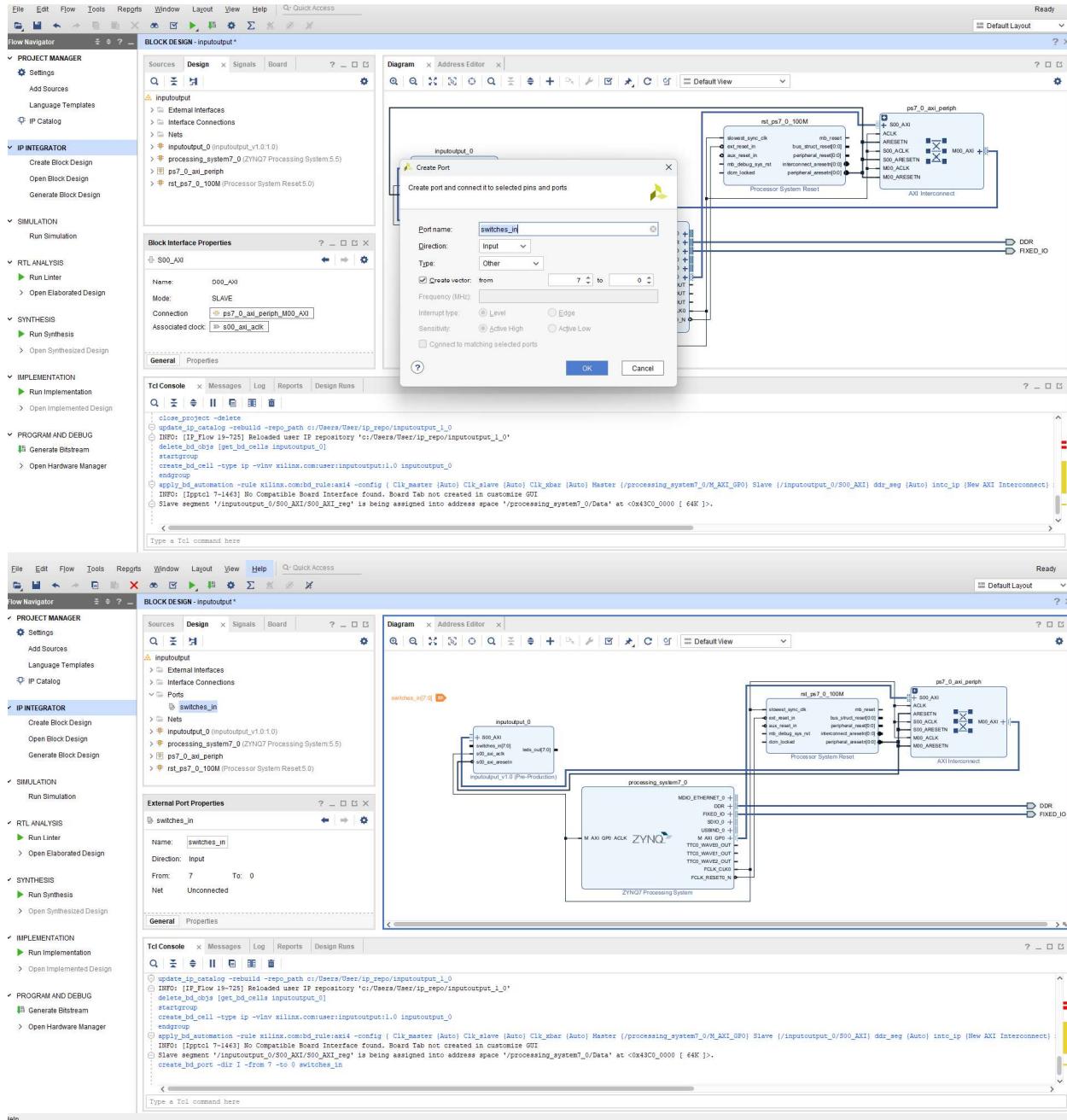
Top Window (Screenshot 1):

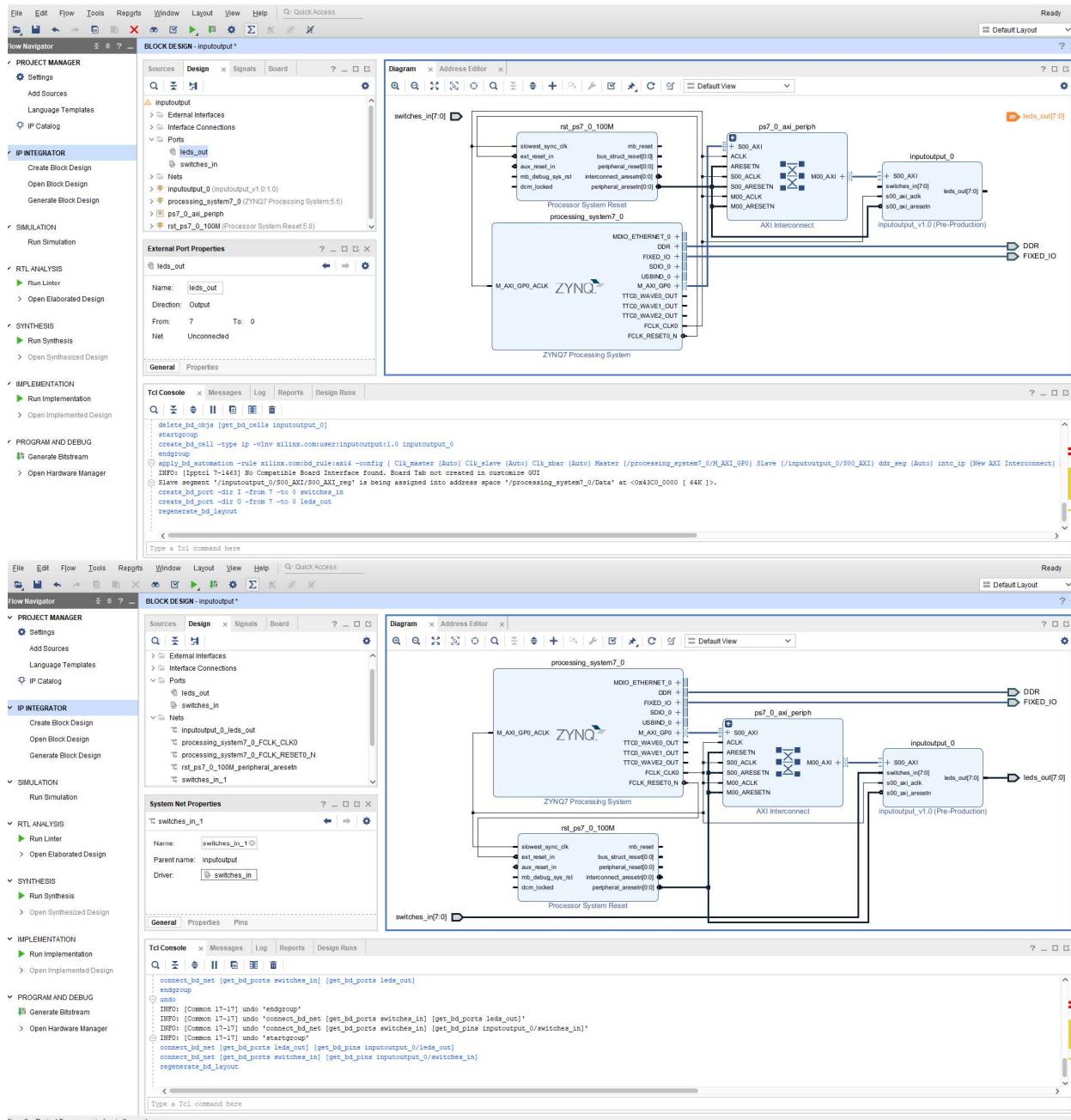
The top window shows the "BLOCK DESIGN - Input/Output" interface. A central diagram area displays a "processing_system7_0" block labeled "ZYNQ Processing System". The block has several pins listed on its right side: MDIO_ETHERNET_0, DDR, FIXED_IO, SDIO_0, USBND_0, M_AXI_GPO_ACLK, TTCl_WAVE0_OUT, TTCl_WAVE1_OUT, TTCl_WAVE2_OUT, FCLK_CLK0, and FCLK_RESET0_N. On the left, a tree view under "inputoutput" shows "processing_system7_0 (ZYNQ7 Processing System:5.5)" and "inputoutput_v1.0". Below this is the "Block Properties" panel for "processing_system7_0". The "Tcl Console" tab at the bottom shows a series of informational and debug messages from IP Flow.

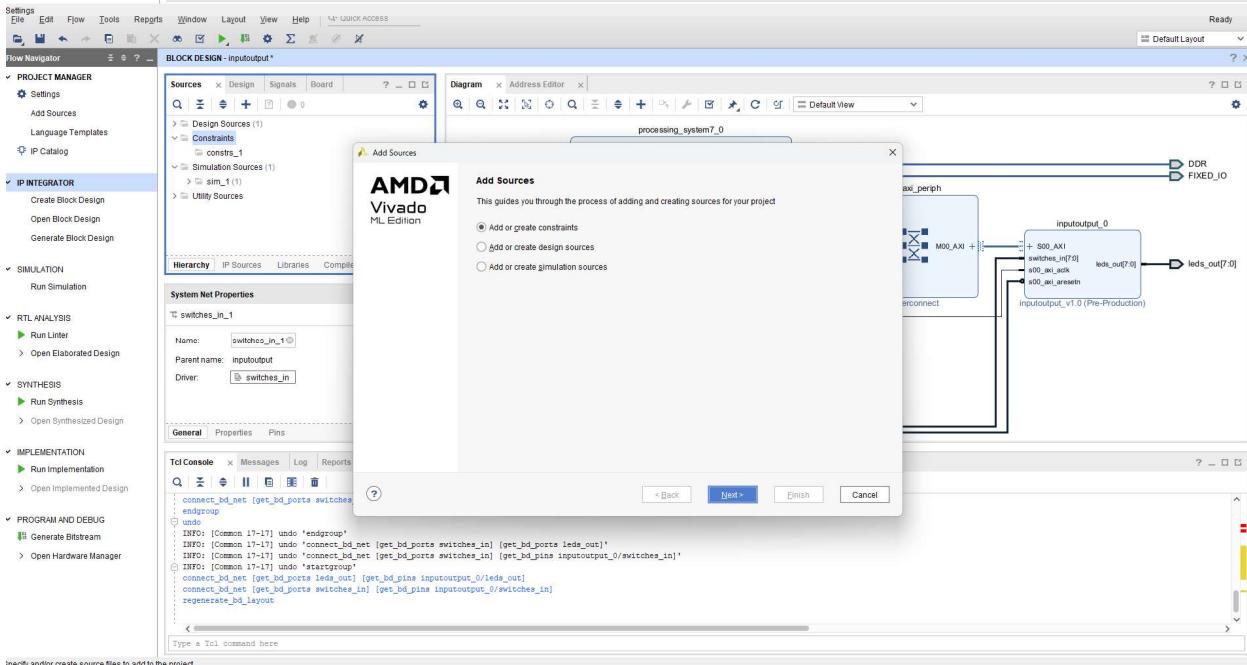
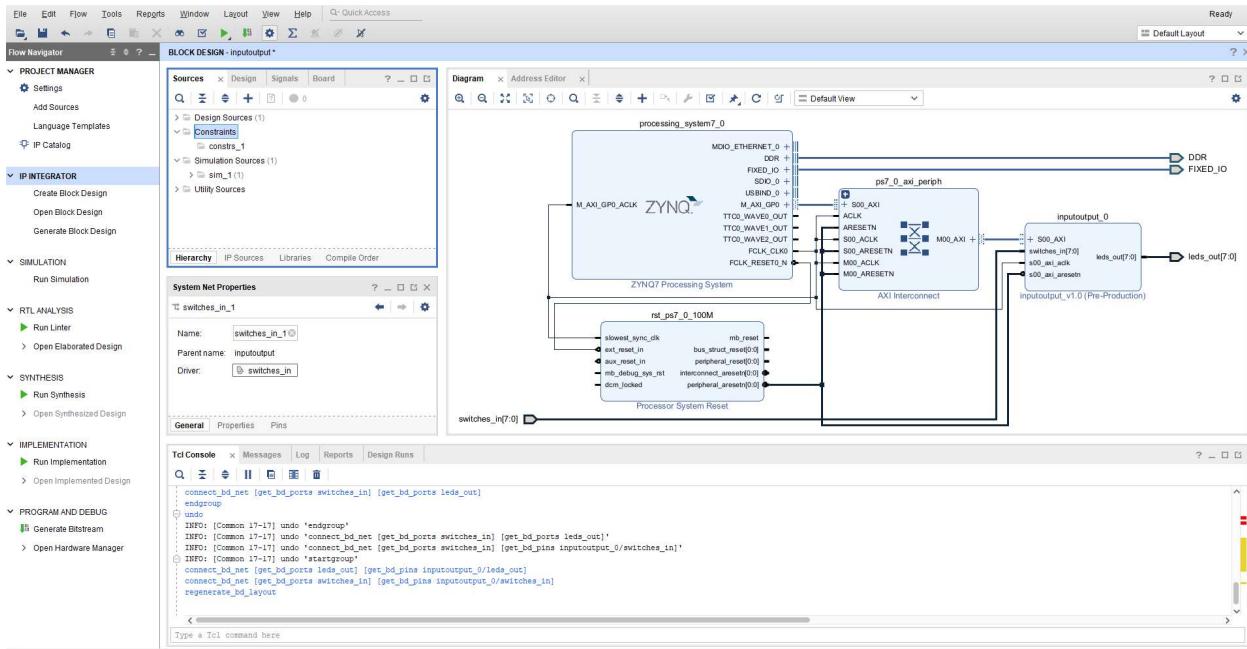
Bottom Window (Screenshot 2):

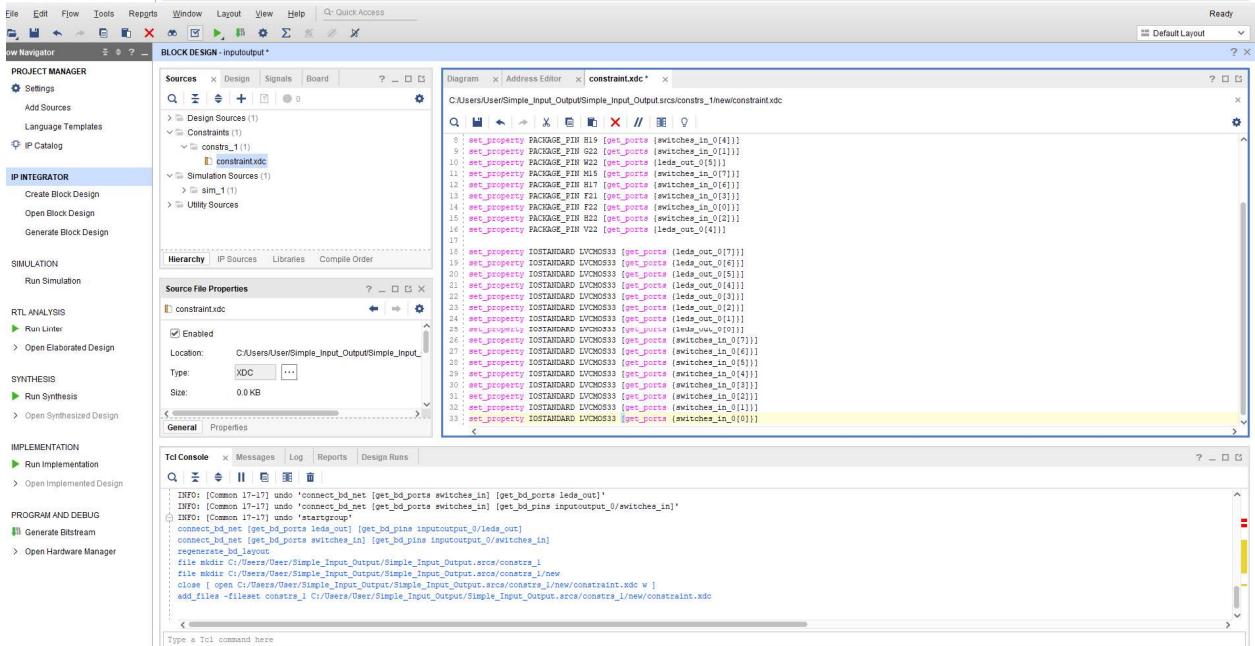
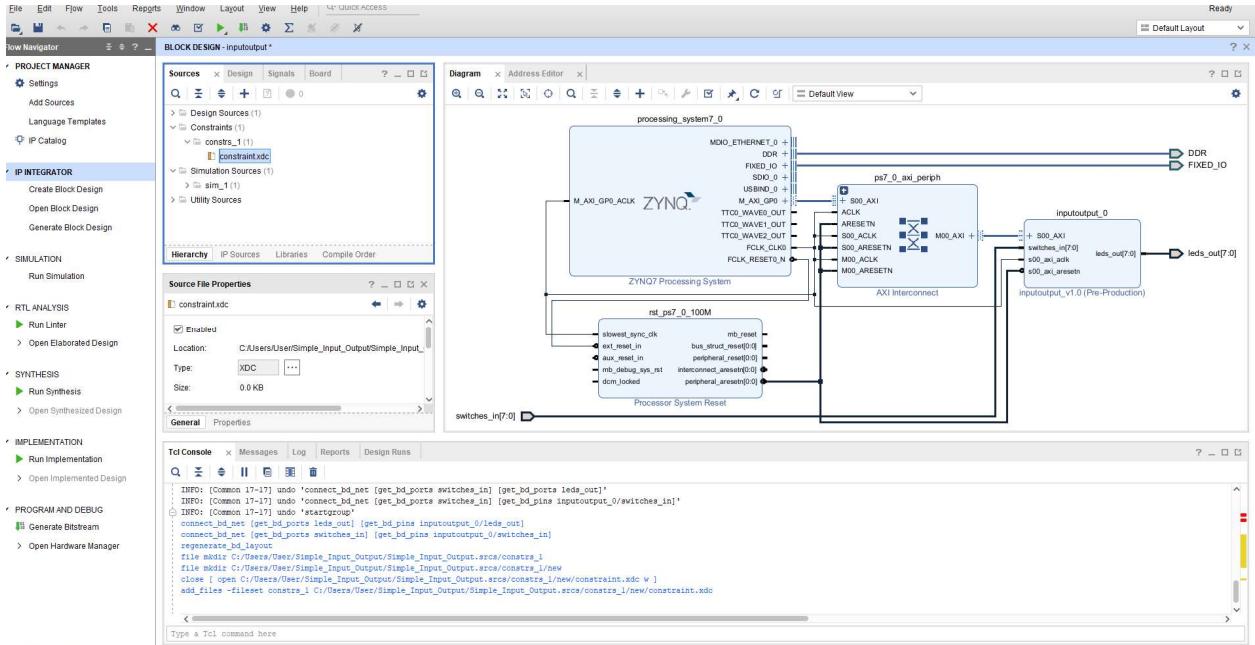
The bottom window also shows the "BLOCK DESIGN - Input/Output" interface. It features a similar "processing_system7_0" block and "inputoutput_v1.0" connection. In this screenshot, a specific connection between the "processing_system7_0" block and the "inputoutput_v1.0" component is highlighted with a yellow box. The "Tcl Console" tab at the bottom shows a subset of the same informational and debug messages.











Block Design - Inputoutput

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Run Linter
- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Tcl Console

```

INFO: [Common 17-17] undo 'connect_bd_net [get_bd_ports switches_in] [get_bd_ports leds_out]'
INFO: [Common 17-17] undo 'connect_bd_net [get_bd_ports switches_in] [get_bd_pins inputoutput_0/switches_in]'
INFO: [Common 17-17] undo 'startrgroup'
connect_bd_net [get_bd_ports leds_out]
connect_bd_net [get_bd_pins inputoutput_0/switches_in]
connect_bd_net [get_bd_ports switches_in] [get_bd_pins inputoutput_0/switches_in]
regenerate_bd_layout
file mkdir C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1
file mkdir C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1/new
close [ open C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1/new/constraint.adc w ]
adc_files -tlistest constrs_1 C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1/new/constraint.adc

```

Flow Navigator

BLOCK DESIGN - inputoutput

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Tcl Console

```

regenerate_bd_layout
file mkdir C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1
file mkdir C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1/new
close [ open C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1/new/constraint.adc w ]
adc_files -tlistest constrs_1 C:/Users/User/Simple_Input_Output/Simple_Input_Output.scs/constrs_1/new/constraint.adc
validate_bd_design
CRITICAL WARNING: [PSU-1] Parameter : PCU_UFARAMAM_DDR_DQS_TO_CLK_DELAY_0 has negative value <-0.073 . FS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-2] Parameter : PCU_UFARAMAM_DDR_DQS_TO_CLK_DELAY_1 has negative value <-0.034 . FS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-3] Parameter : PCU_UFARAMAM_DDR_DQS_TO_CLK_DELAY_2 has negative value <-0.03 . FS DDR interfaces might fail when entering negative DQS skew values.
CRITICAL WARNING: [PSU-4] Parameter : PCU_UFARAMAM_DDR_DQS_TO_CLK_DELAY_3 has negative value <-0.082 . FS DDR interfaces might fail when entering negative DQS skew values.

```

Diagram

