Test Plan:

1. **(Hit and Miss Test):**
   1.1 Read Miss
   - Read an address from the trace file. It will be a compulsory miss.

   1.2 Read Hit
   - Read from the same address again. Now it has to be a hit.

   1.3 Write Miss
   - Give a different address to write to a cache line. It should be a miss.

   1.4 Write Hit
   - Write to the same address. Now it should be a hit.

2. **Testing PLRU:**
   2.1 Access pattern validation
   - Read from 16 addresses such that all those point to the same index. All of them will be compulsory misses.
   - Read from same 16 addresses, but now all of them will be hit.
   - Check the PLRU bits, and all the bits should be 1's because the cache line was sequentially filled.

   2.2 Checking Replacement policy

   2.2.1 Checking before any access
   - Now perform a read with an address such that it goes to the same index but with a different tag. Now it will be a miss.
   - Now way 0 has to be evicted because it was least recently used with respect to PLRU.

   2.2.2 Checking replacement policy after access.
   - Now read from way 7 address.
   - Now give a new address with the same index but a different tag.
   - According to PLRU, way 8 should be evicted.

   2.2.3 Checking after multiple access to the same cache line.
   - Now read way 13 address.
   - Write to way 13. Read again from Way 13. Perform a write again to way 13.
   - Despite multiple accesses, the PLRU bits should not change after each access.
   - Give an address again with the same index but a different tag. Way 2 should be evicted.

   2.3 Check for cache clearing
   - After performing a set of accesses and replacements, PLRU bits a set to a particular state.
   - Now perform a clear cache by giving operation code 8.
   - All PLRU bits should be 0's

3. **Testing Mode 8 and 9:**
   - Give a set of addresses with different operation codes.

   3.1 Mode 9
   - Give the command with operation code 9. See if the contents of caches are printed.

   3.2 Mode 8
   - To clear the cache, we give command with operation code 8.
   - Now give command with operation code 9 again. Nothing should be printed because we cleared the cache.

4. **We have to also write a test case for the correct implementation of the MESI protocol for all the caches.**
5. **We have to write a test case for the Snoop results and if the MESI protocol is observed after snooping.**