Introduction to ARM Cortex-M4F and its peripherals

TM4C123GH Tiva C Board

Dr. Munesh Singh

Indian Institute of Information Technology Design and Manufacturing
Kancheepuram, Chennai, Tamil Nadu

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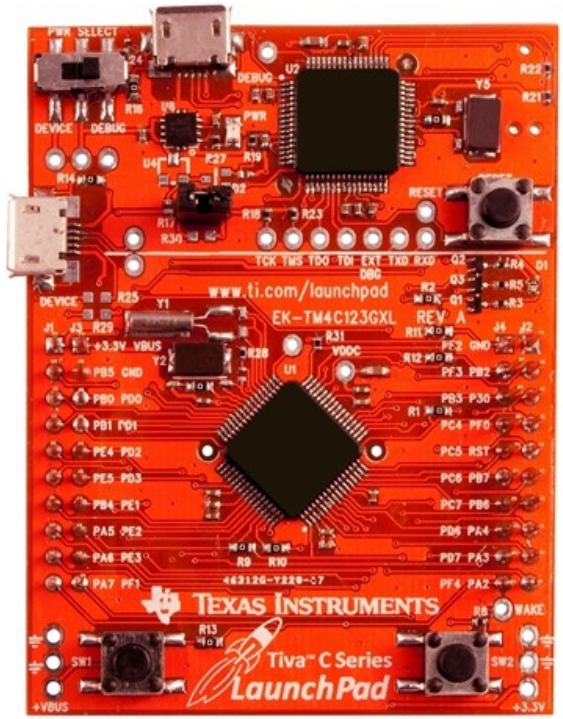
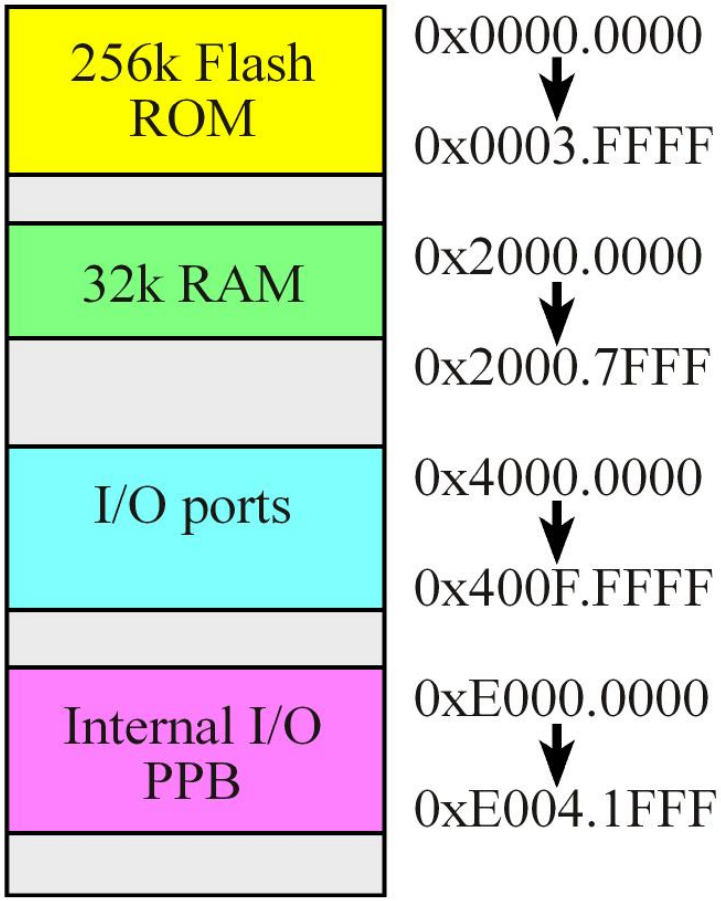
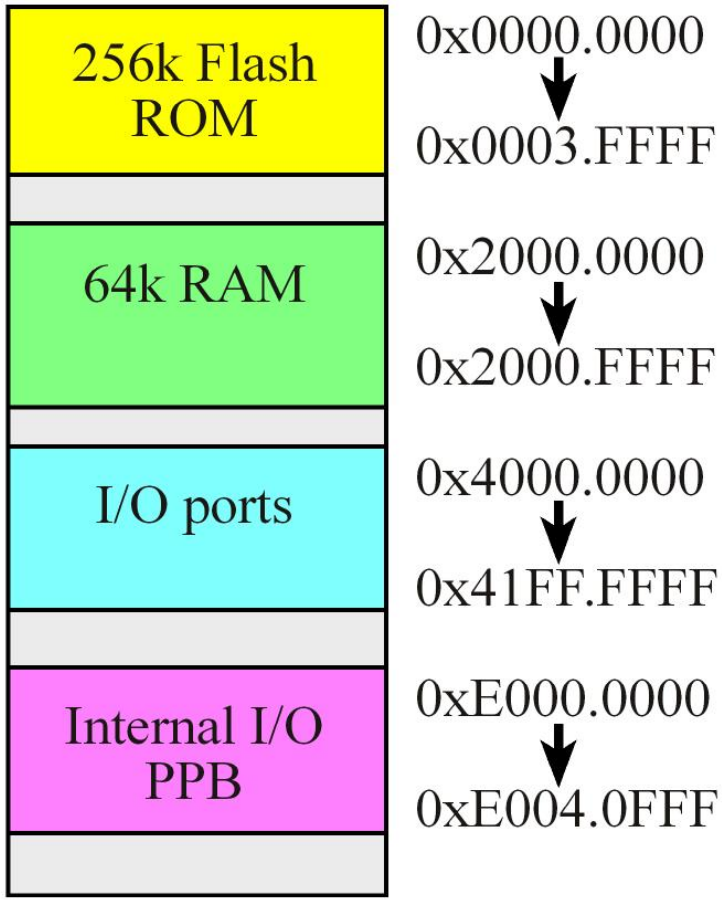
About the TM4C123GH TivaC Board

- Developed by Texas Instruments
- CPU: ATM Cortex@M4
- 256 KB single-cycle Programmable Flash memory
- 32 KB single-cycle SRAM
- 2KB of EEPROM
- 80-MHz operation; 100 DMIPS performance
- Supports a wide choice of integrated Development Environments (IDEs) including IAR, ARM Kiel, GCC based IDEs.



TM4C123GH Memory Map





TM4C123GH Clock Sources

- **Precision Internal Oscillator (PIOSC)** 16 MHz
- **Main Oscillator (MOSC) using**
  - An external single-ended clock source
  - An external crystal
- **Internal 30 kHz Oscillator**
  - intended for use during Deep-Sleep power-saving modes
- **Hibernation Module Clock Source**
  - 32,768Hz crystal
  - Intended to provide the system with a real-time clock source

Board Specifications

Communication Interfaces

- Eight Universal Asynchronous Receivers/Transmitter UART (UART)
- Four Synchronous Serial Interface (SSI)
- Four I2C modules with four transmission speeds including high-speed mode
- Two Controller Area Network (CAN) 2.0 A/B controllers
- Universal Serial Bus (USB) USB 2.0 OTG/Host/Device

Board Specifications

System Integration

- Micro Direct Memory Access (DMA) ARM PrimeCell 32-channel configurable DMA controller
- General-Purpose Timer (GPTM) Six 16/32-bit GPTM blocks and Six 32/64-bit Wide GPTM blocks
- Two Watchdog Timer (WDT)
- 43 General-Purpose Input/Output (GPIO) Six physical GPIO blocks (port A, port B, port C, port D , port E , port F)

Advanced Motion Control

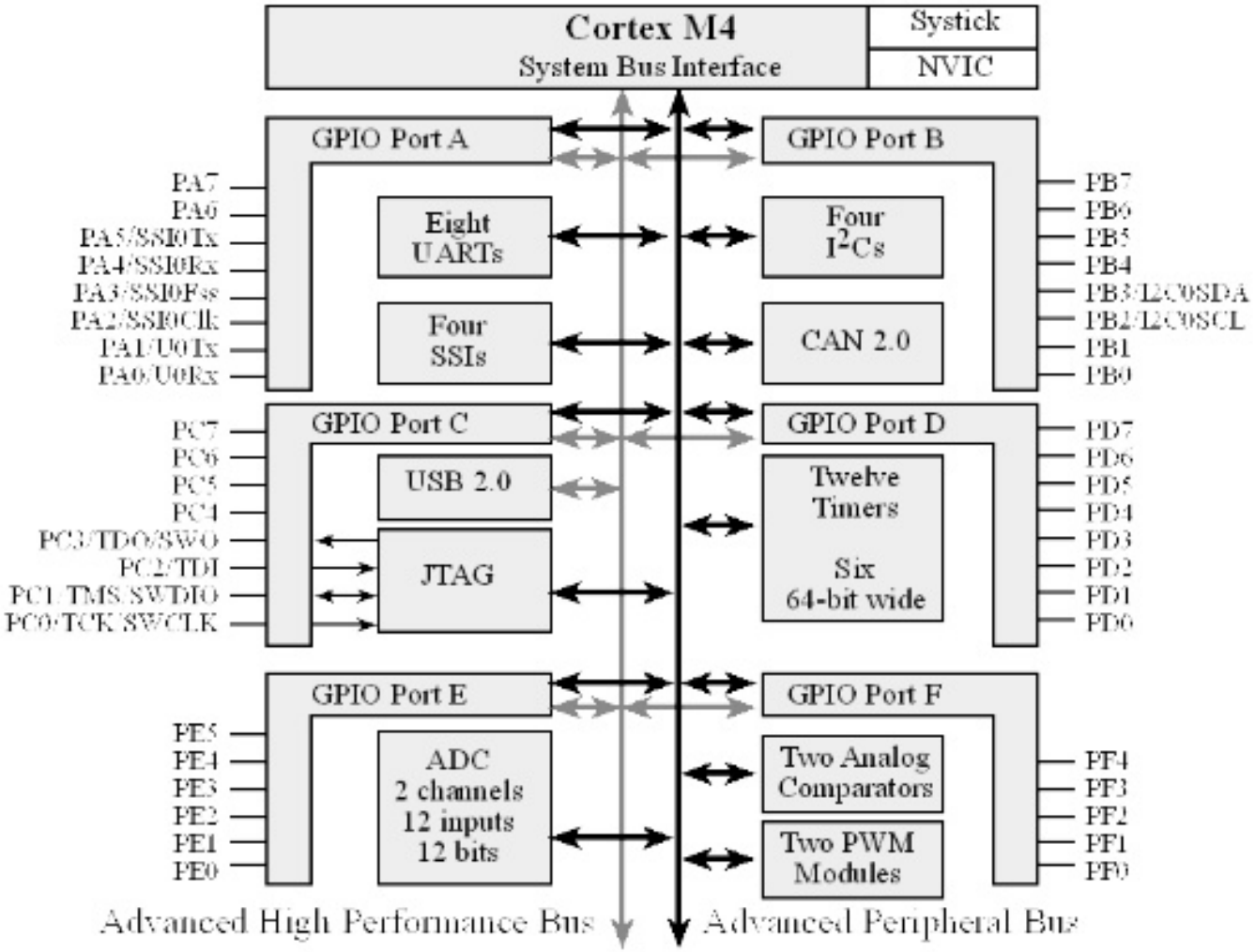
- Four Pulse Width Modulator (PWM) Two PWM modules, each with four PWM generator blocks and a control block, for a total of 16 PWM outputs.
- Two Quadrature Encoder Interface (QEI)

Board Specifications

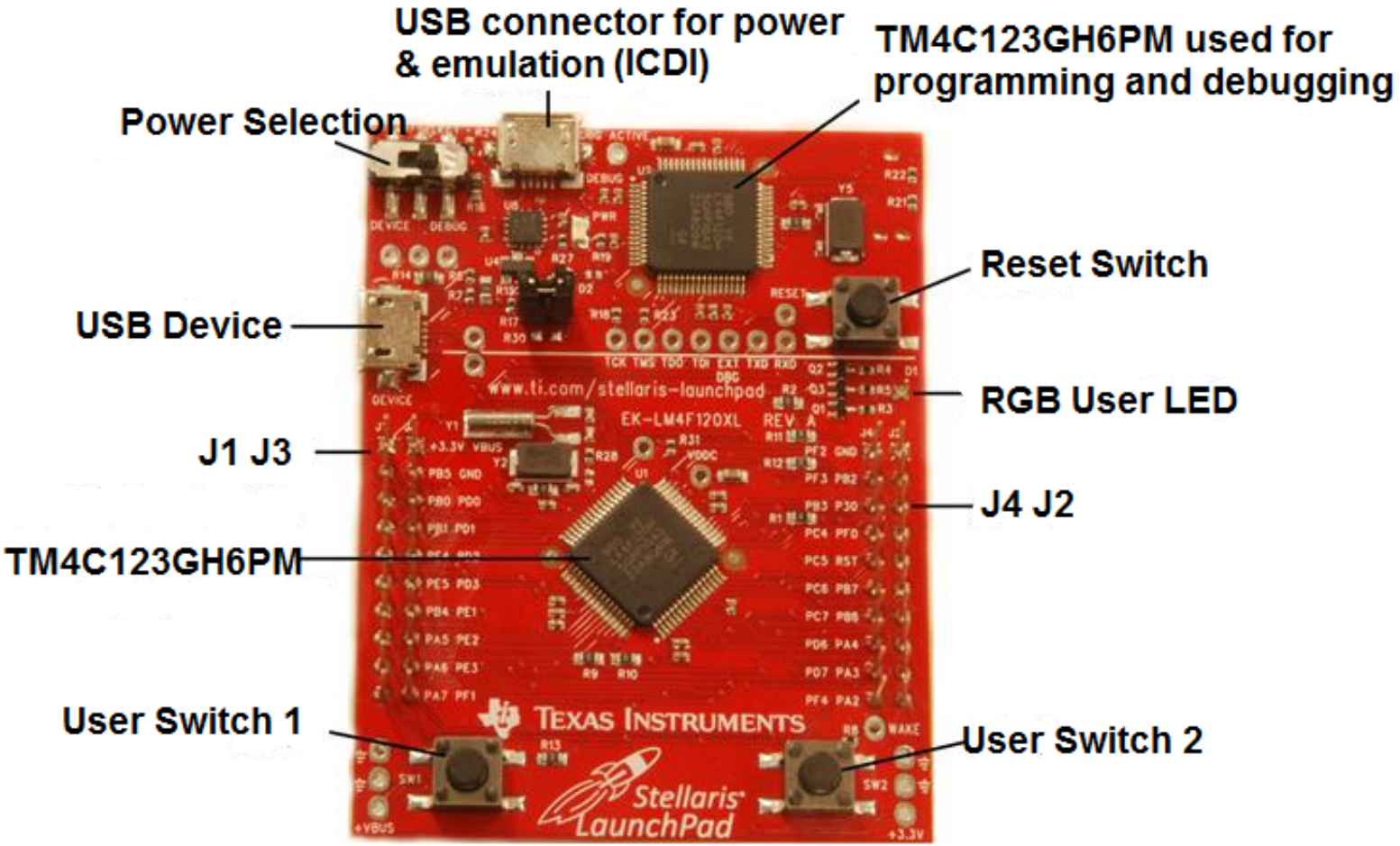
Analog Support

- Analog-to-Digital Converter (ADC) Two 12-bit ADC modules, each with a maximum sample rate of one million samples/second
- Analog Comparator Controller Two independent integrated analog comparators
- Digital Comparator 16 digital comparators with four transmission speeds including high-speed mode
- JTAG and Serial Wire Debug (SWD) One JTAG module with integrated ARM SWD

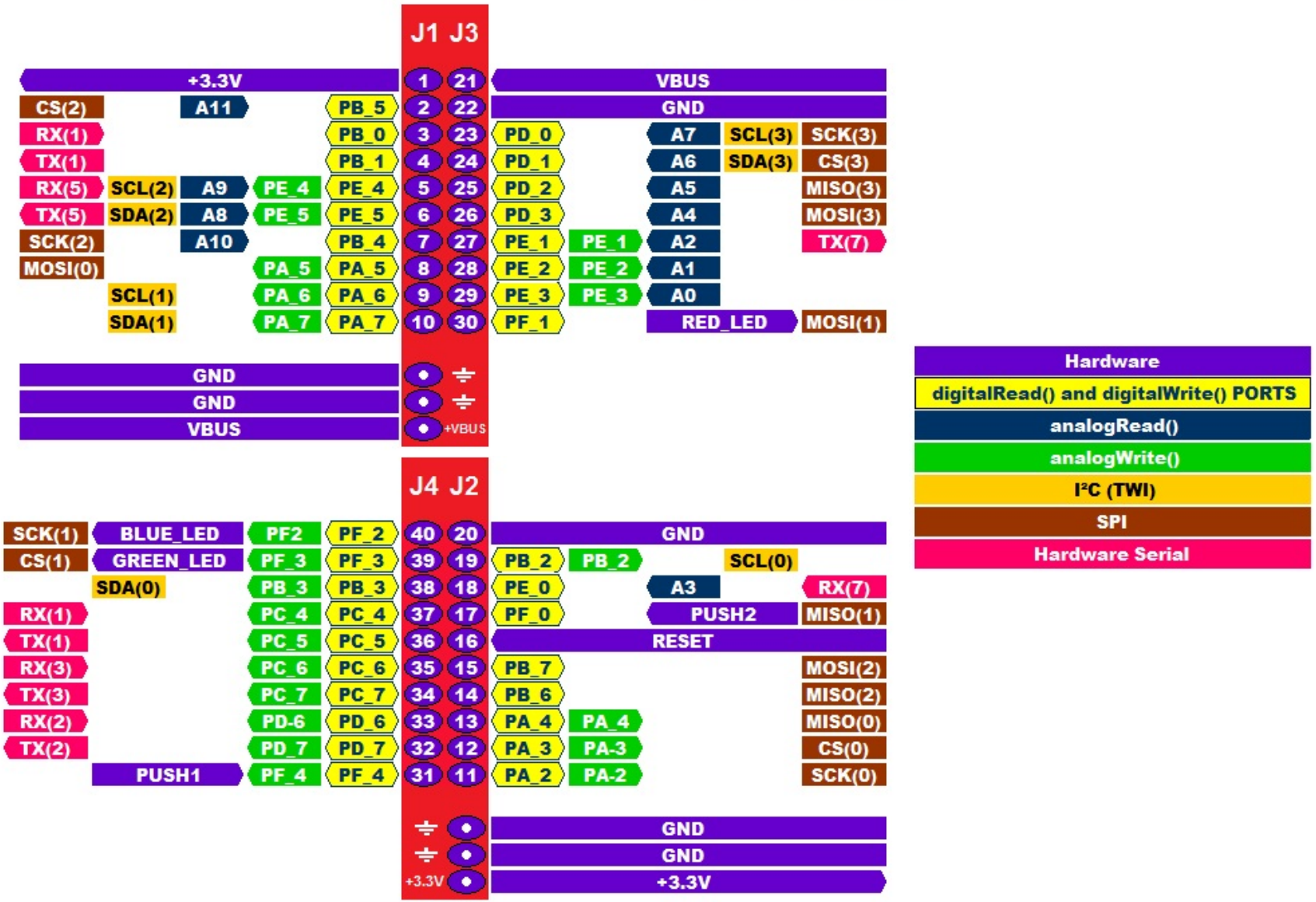
- **General-Purpose Input/Outputs**



ARM Cortex-M4 Tiva C

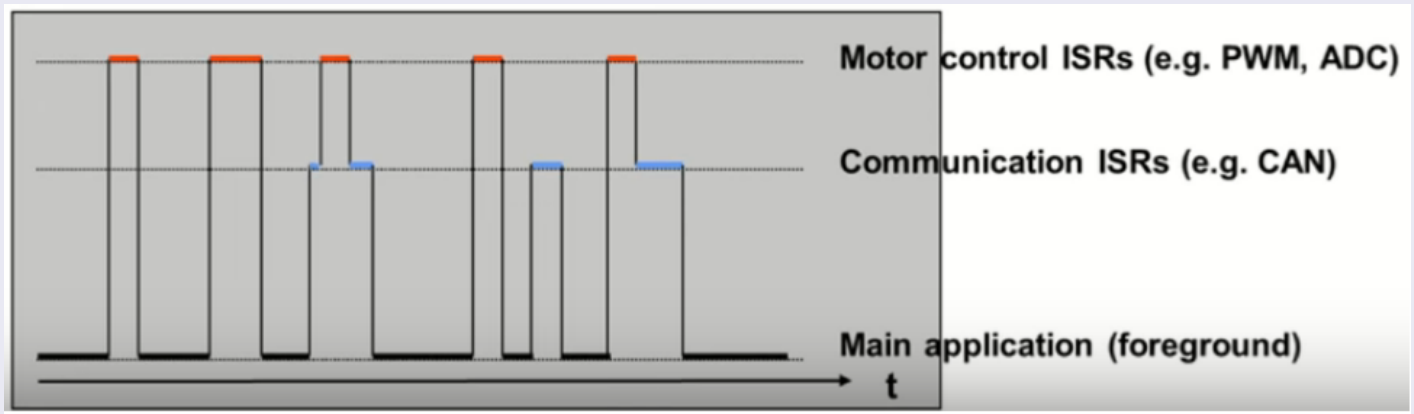


TM4C123GH Pin Layout



Nested Vectored Interrupt Controller (NVIC)

- Handles exceptions and interrupts
- 7 exceptions and 71 interrupts
- 8 programmable priority levels, priority grouping
- Automatic state saving and restoring
- Automatic reading of the vector table entry
- Preemptive/Nested Interrupts
- Deterministic: Always 12 cycles or 6 tail-chaining

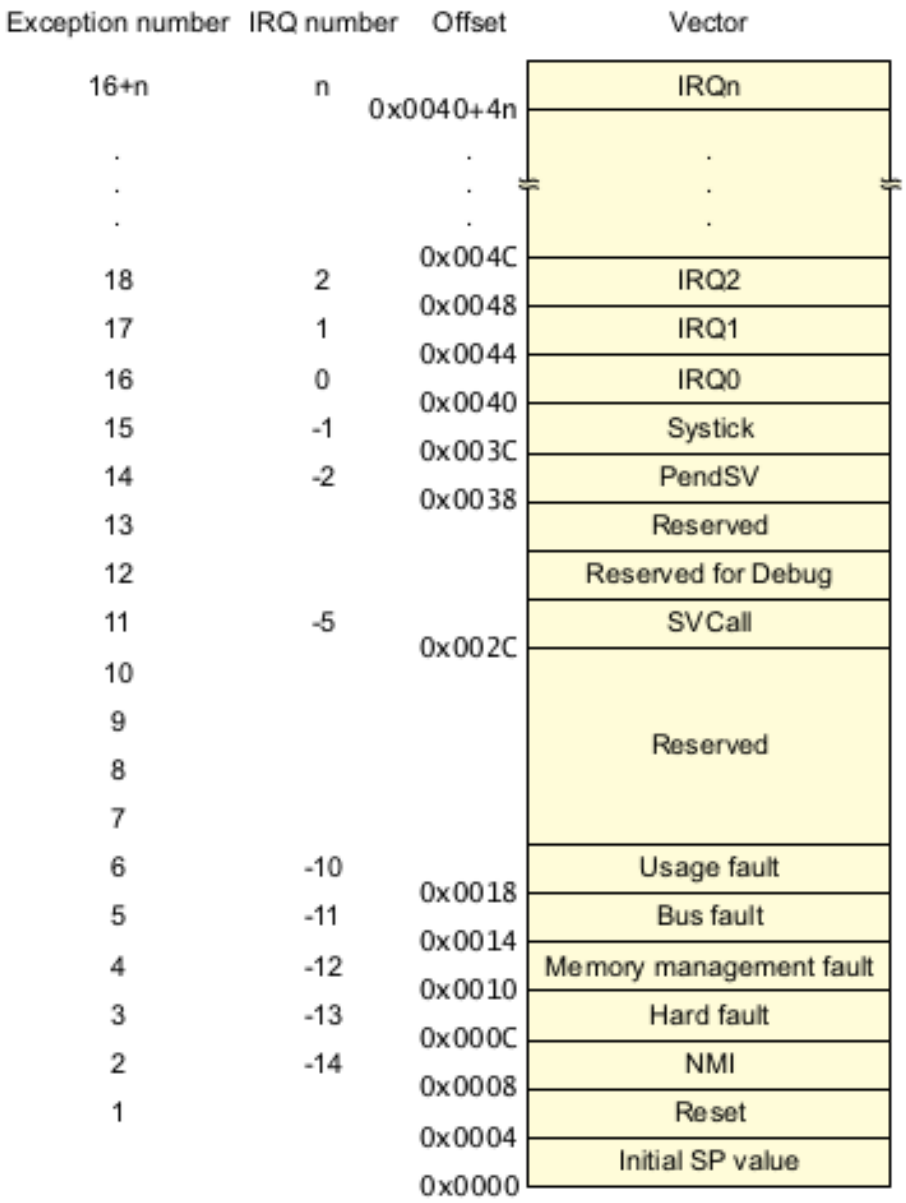


Cortex-M4 Interrupt Handling

- Interrupt handling is automatic. No instruction overhead.
- **Entry**
  - Automatically pushes registers R0-R3, R12, LR, PSR, and PC onto the stack
  - In parallel, ISR is pre-fetched on the instruction bus, ISR ready to start executing as soon as stack PUSH complete
- **Exit**
  - Processor state is automatically restored from the stack
  - In parallel, interrupted instruction is pre-fetched ready for execution upon completion of the stack POP

Cortex-M4 Vector Table

- After reset, vector table is located at address 0
- Each entry contains the address of the function to be executed.
- Open startup_css.c to see the vector table coding

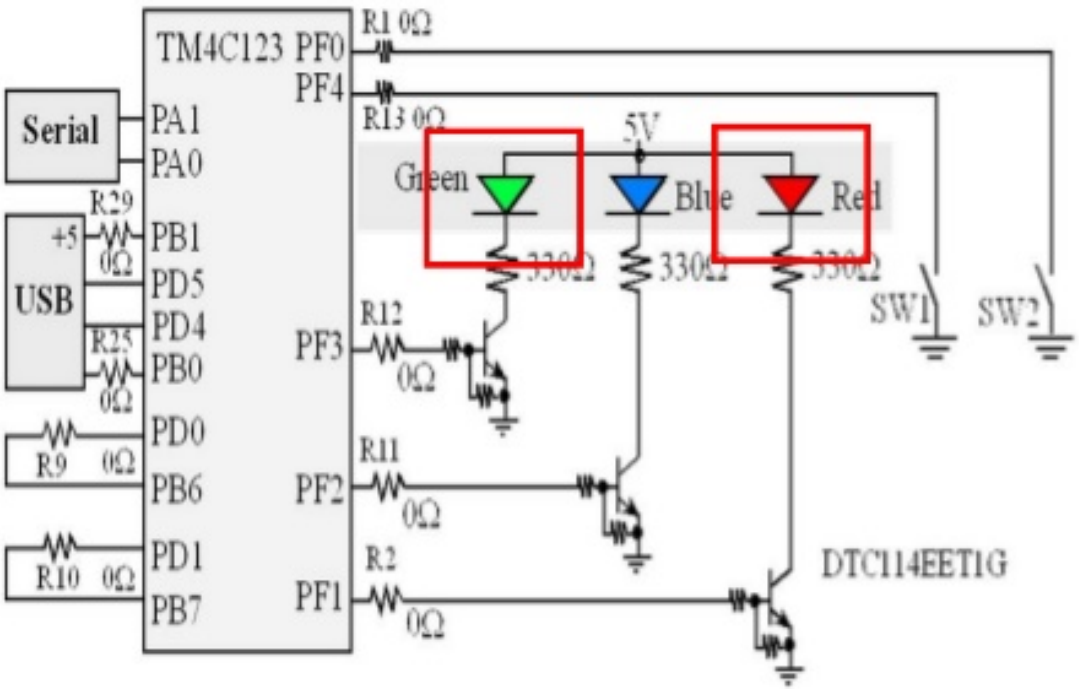


First Step to Glow On Board LEDs on TM4C123GH

- **TM4C123GH6PM Overview:**

First Program :

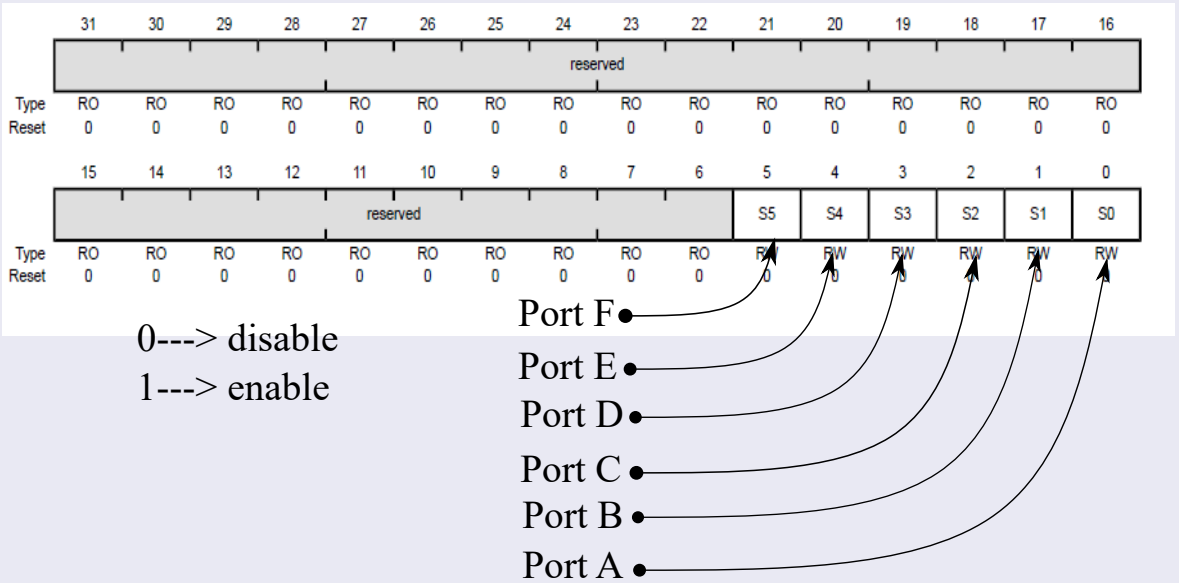
Blink Led red & Green



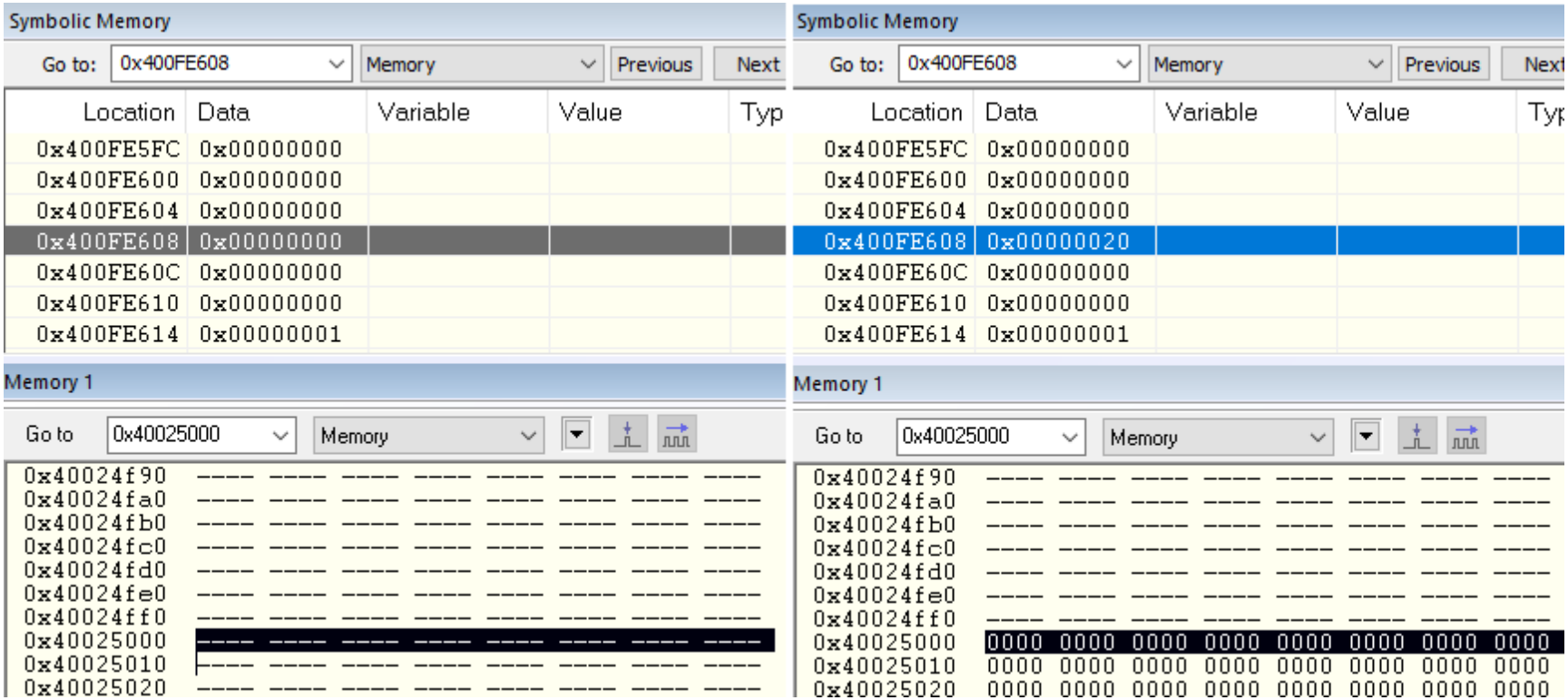
Steps to Enable Digital GPIO Port

First RCGCGPIO Register to Set

- General-Purpose Input/Output Sleep Mode Clock Gating Control
  - **Base:** 0x400FE000
  - **Offset:**0x608
  - **Actual Address:**0x400FE608
- ARM architecture has by default disable clock to I/O port for power saving purpose.



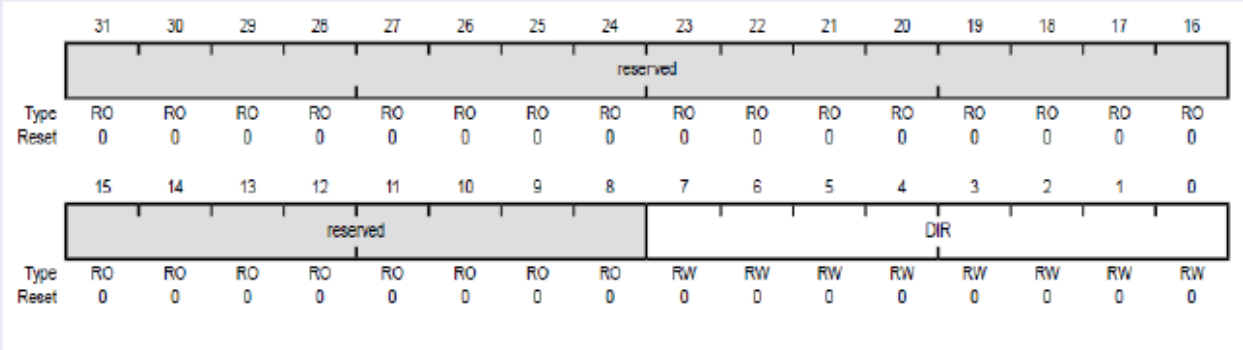
Visualize the registers on IDE



Direction Register

Second GPIODIR Register to set

- This register decide the direction of the signal either input or output
  - **Base:** 0x40025000
  - **Offset:**0x400
  - **Actual Address:**0x40025400



0---> Cooresponding pin input
1---> Cooresponding pin output

0:7 Bits

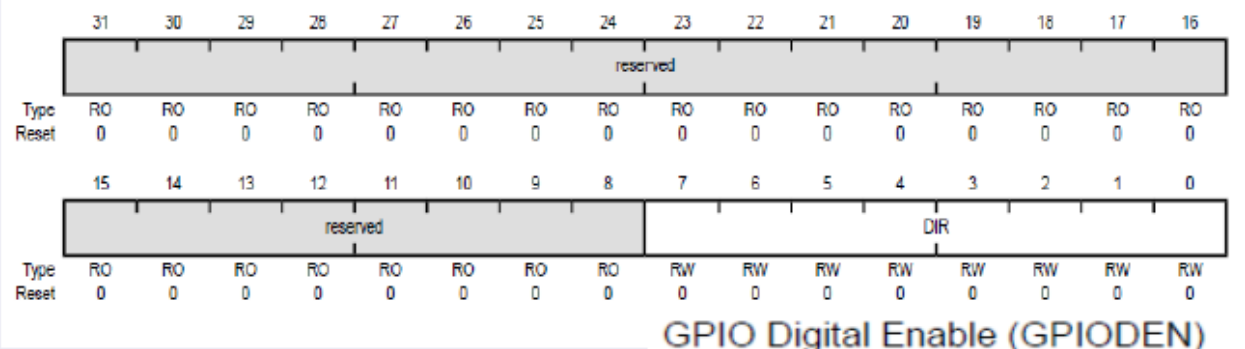
GPIO Direction (GPIODIR)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
Offset 0x400
Type RW, reset 0x0000.0000

Digital Function Register

Third GPIODEN Register to set

- This register decide the functionality either Digital or Analog
  - **Base:** 0x40025000
  - **Offset:**0x51C
  - **Actual Address:**0x4002551C



GPIO Digital Enable (GPIODEN)

0---> Disable Digital function

1---> Enable Digital function

0:7 Bits

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
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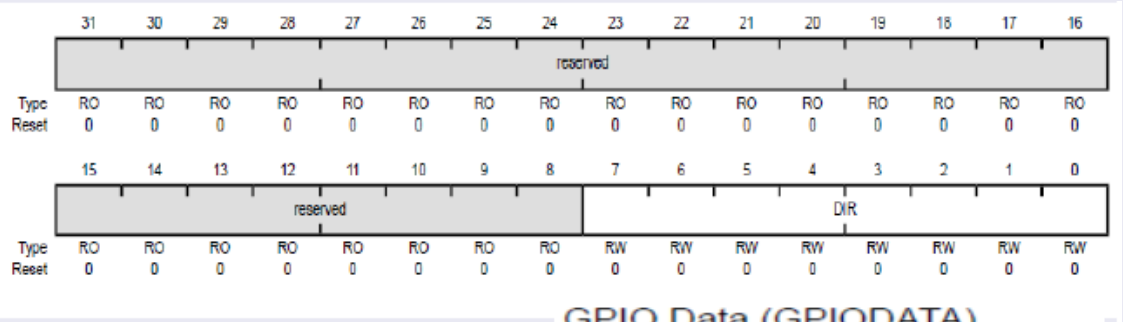
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
Offset 0x51C
Type RW, reset -

Data Register

Fourth GPIODATA Register to set

- This register enable the signal on corresponding I/O pins
  - **Base:** 0x40025000
  - **Offset:**0x000
  - **Actual Address:**0x40025000
- GPIODATA register specify individual pin address at the particular port.



0:7 Bits

2 1 8 4 2 1 8 4 2 1
9 8 7 6 5 4 3 2 1 0 **Addr**

7 6 5 4 3 2 1 0 **Pin**

All seven port if want to use

3FC

0x400253FC

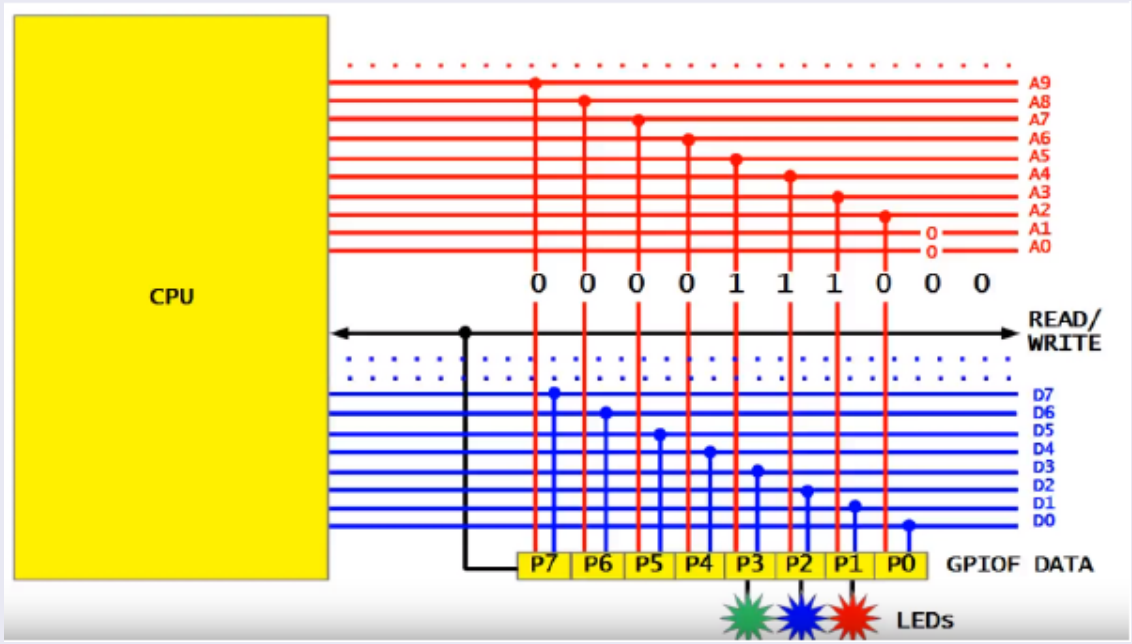
GPIO Data (GPIODATA)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
Offset 0x000
Type RW, reset 0x0000.0000

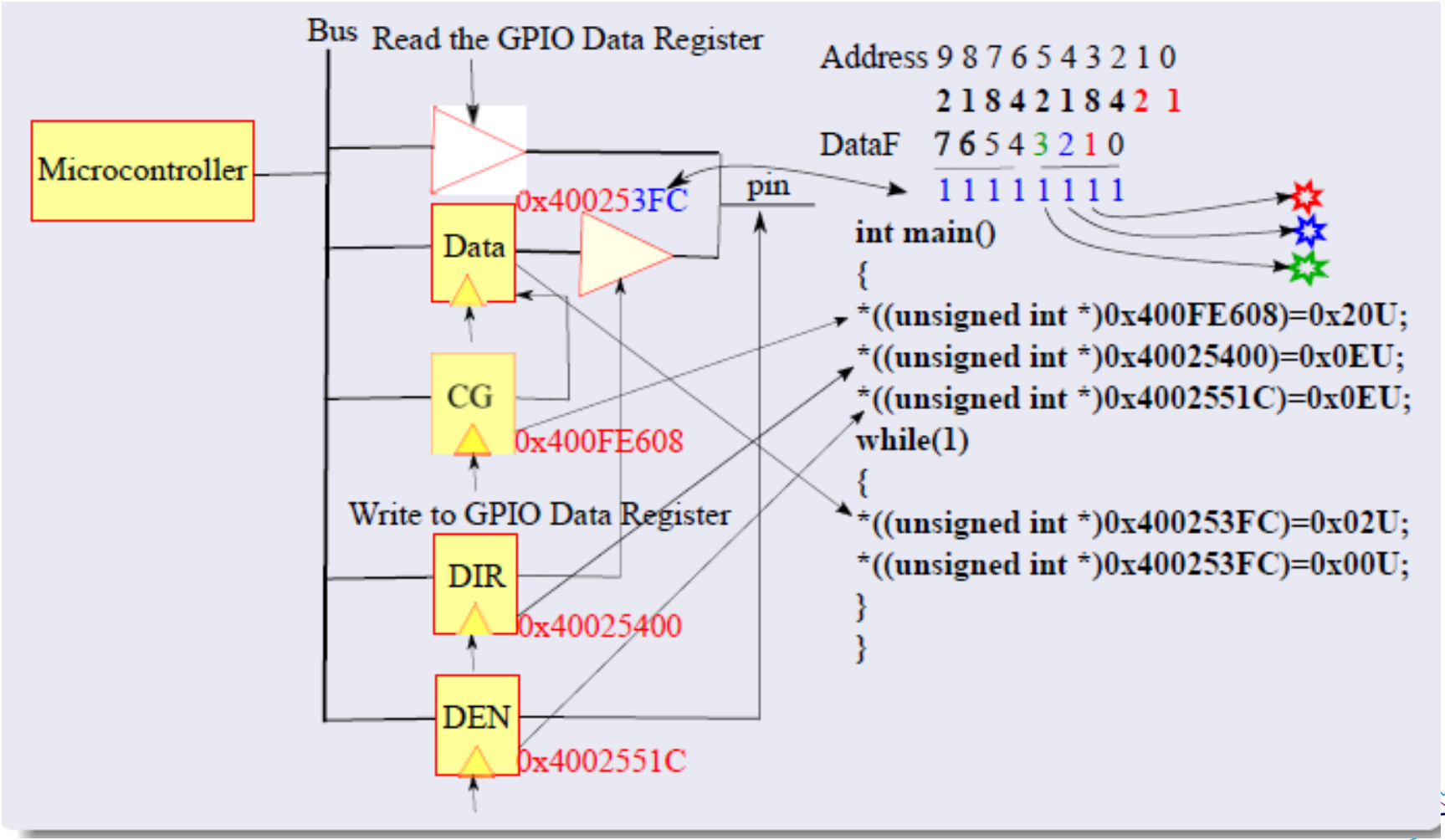
Setting Indiviual Pin address on GPIODATA Register

Address for Indiviaul Pin of Port F

- This register enable the signal on corresponding I/O pins
  - **Base:** 0x40025000
  - **Offset:**0x000
  - **Actual Address for all Pin at Port F:**0x400253FC
  - **Actual Address for RED LED pin at Port F :**0x40025080



Simple Program to Glow RED LED



Thank You