Analog Lab Manual

Revision 4.0
IC615
ASSURA410
MMSIM121
IES122

Developed By
University Support Team
Cadence Design Systems, Bangalore

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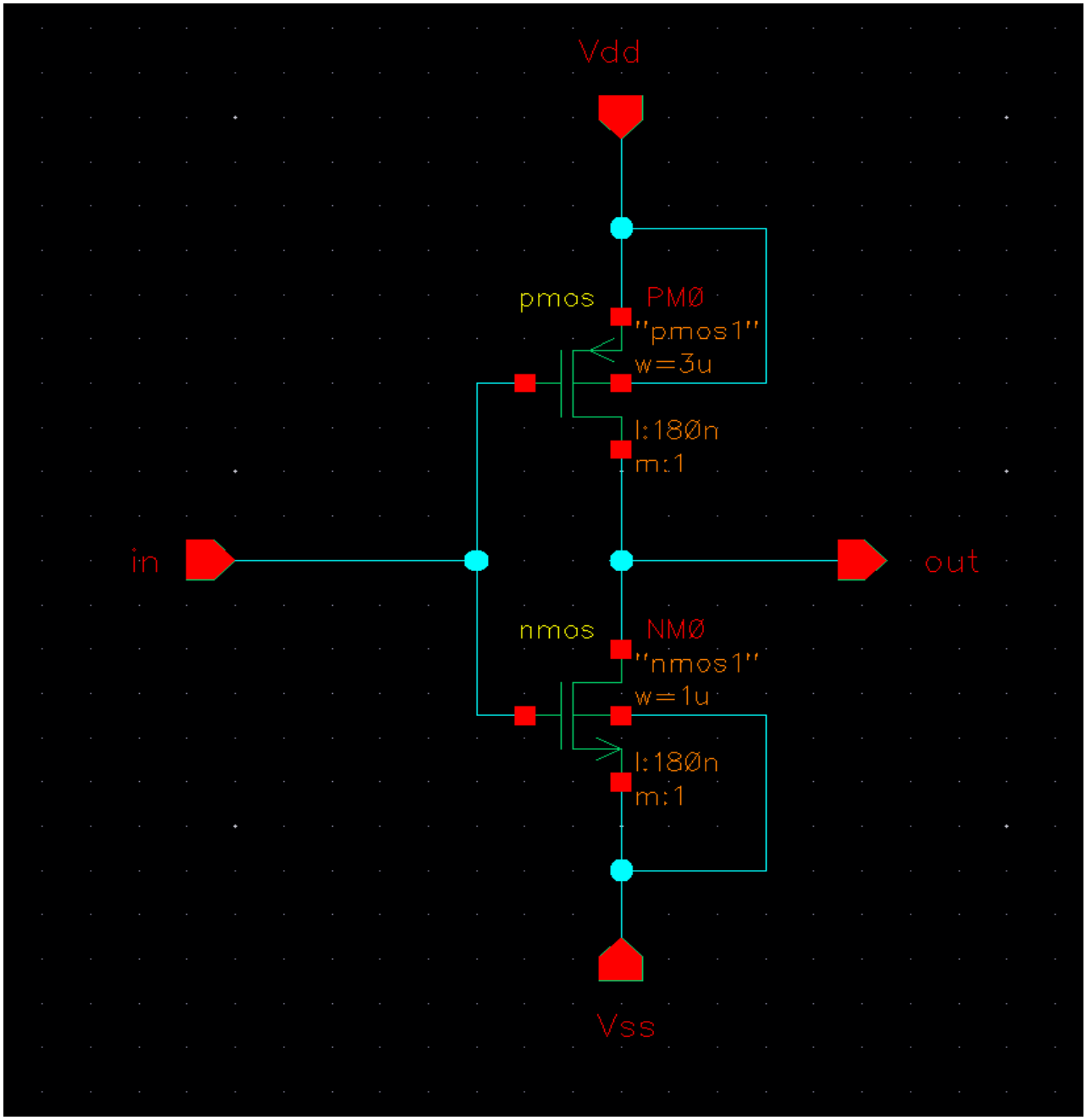
Lab 1: Inverter in CIC Flow

Schematic Capture



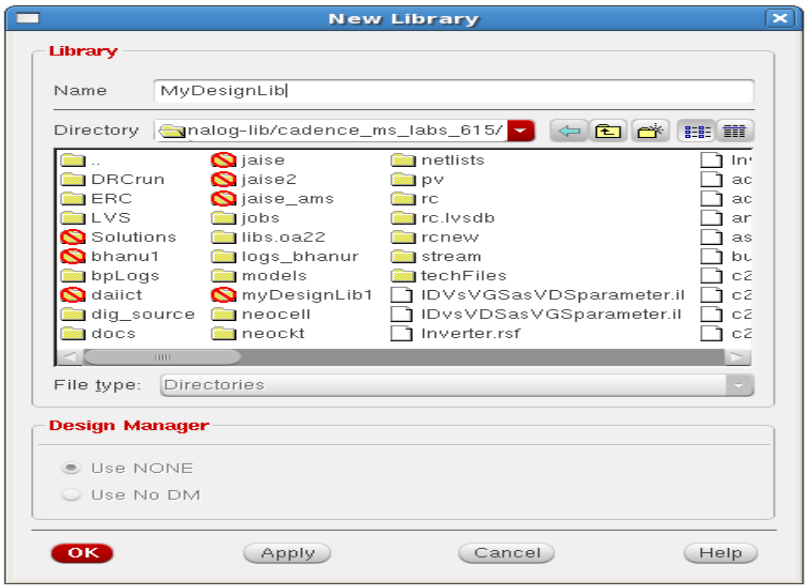
Schematic Entry

Objective: To create a library and build a schematic of an Inverter

Below steps explain the creation of new library "**MyDesignLib**" and we will use the same throughout this course for building various cells that we going to create in the next labs.

Creating a New library

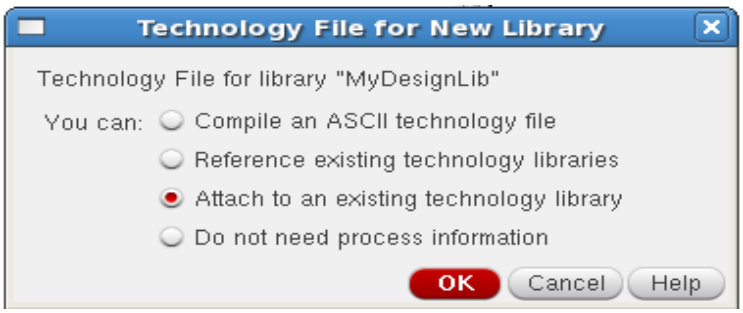
1. Execute **Tools – Library Manager** in the CIW (Command Interpreter Window) to open Library Manager.
2. In the Library Manager, execute **File – New – Library**. The new library form appears.
3. In the "New Library" form, type "**MyDesignLib**" in the Name section.



4. In the field of Directory section, verify that the path to the library is set to **~/Database/cadence_analog_labs_615** and click **OK**.

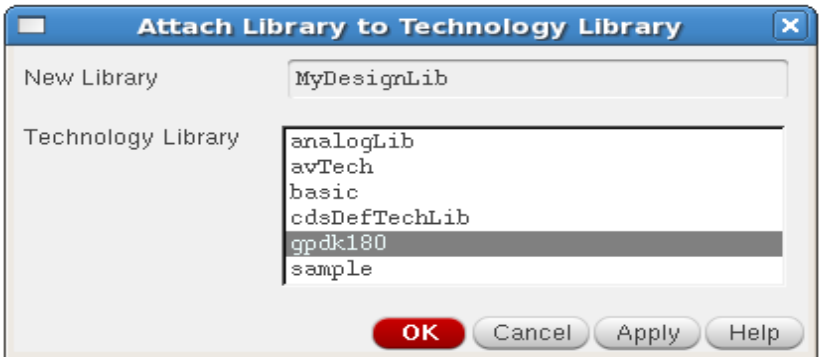
Note: New library an also be created directly from the CIW by executing **File - New – Library**

5. A "**Technology File for New library**" form appears, select option "**Attach to an existing technology library"** and click **OK**.

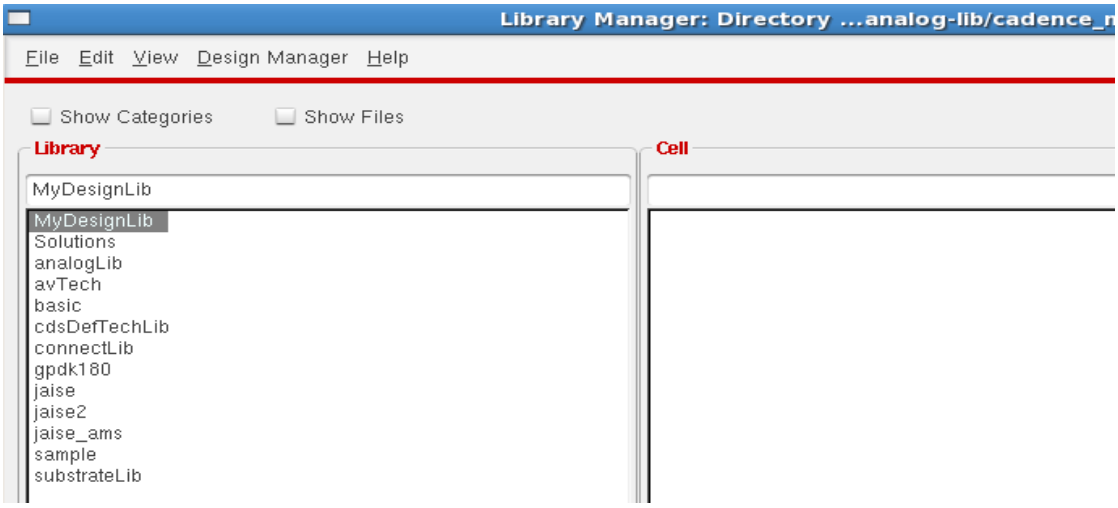


Note: A technology file is not required if you are not interested to do the layouts for the design.

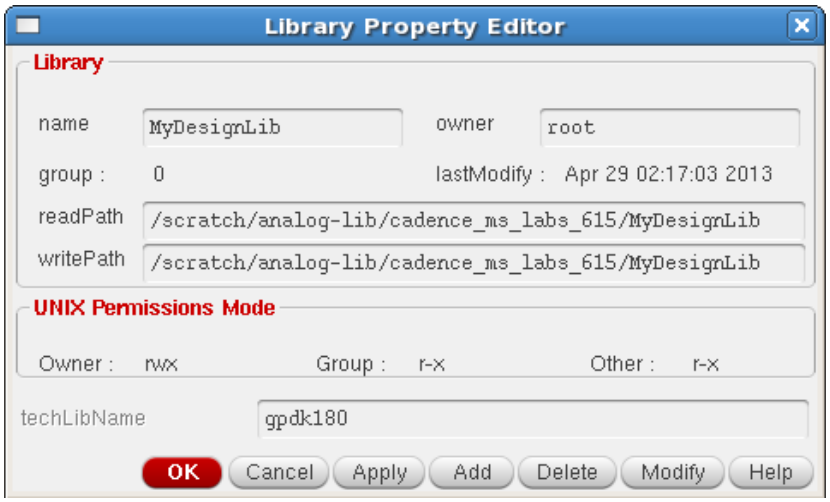
6. A **"Attach library to Technology Library"** form appears, select option **"gpdk180"** from the cyclic field and click **OK**



7. After creating a new library we can verify it from the "**Library Manager"**



8. If we right click on the "**MyDesignLib**" and select properties, we can find that "**gpdk180"** library is attached as techLib to "**MyDesignLib**".

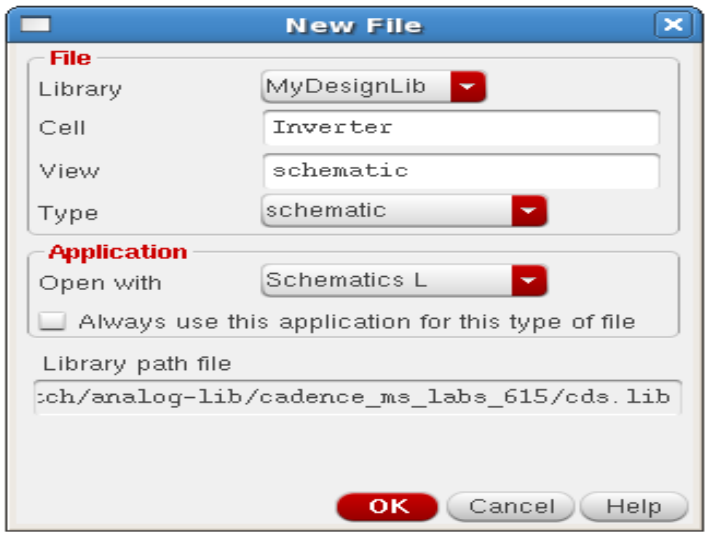


Creating a Schematic Cellview

In this section we will learn how to open new schematic window in the new "**MyDesignLib**" library and build the inverter schematic as shown in the figure at the start of this lab.

1. In the CIW or Library manager, execute **File – New – Cellview**.

2. Set up the **"New File"** window as follows:



Note: Do not edit the Library path file and the one above might be different from the path shown in your window.

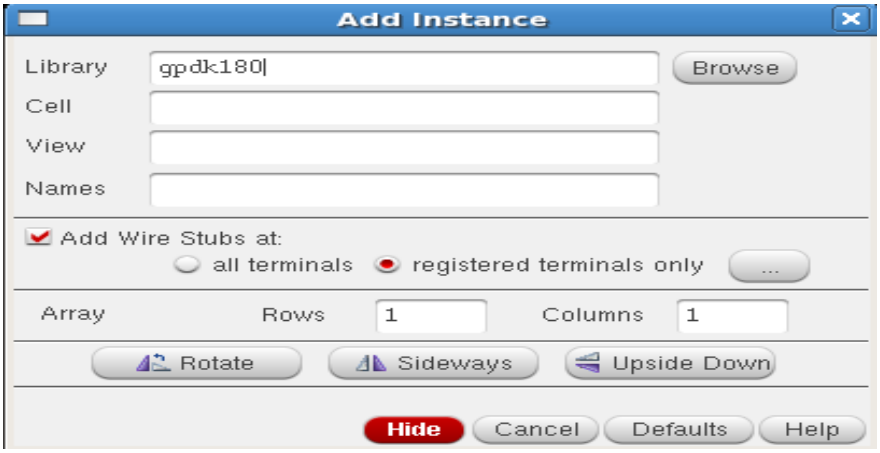
3. Click **OK** when done the above settings. A blank schematic window for the **Inverter** design appears.

Note: Make sure the Library name is same as what we created earlier, **"MyDesignLib".**

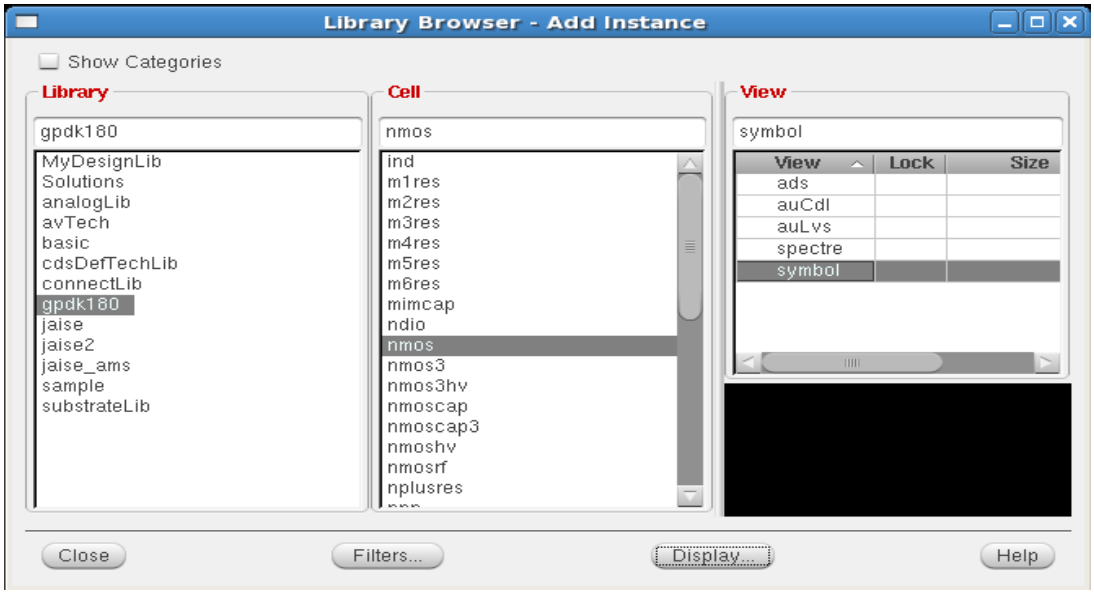
Adding Components to schematic

1. In the Inverter schematic window, click the **Instance** fixed menu icon  to display the Add Instance form.

Tip: You can also execute **Create — Instance** or press **i**.

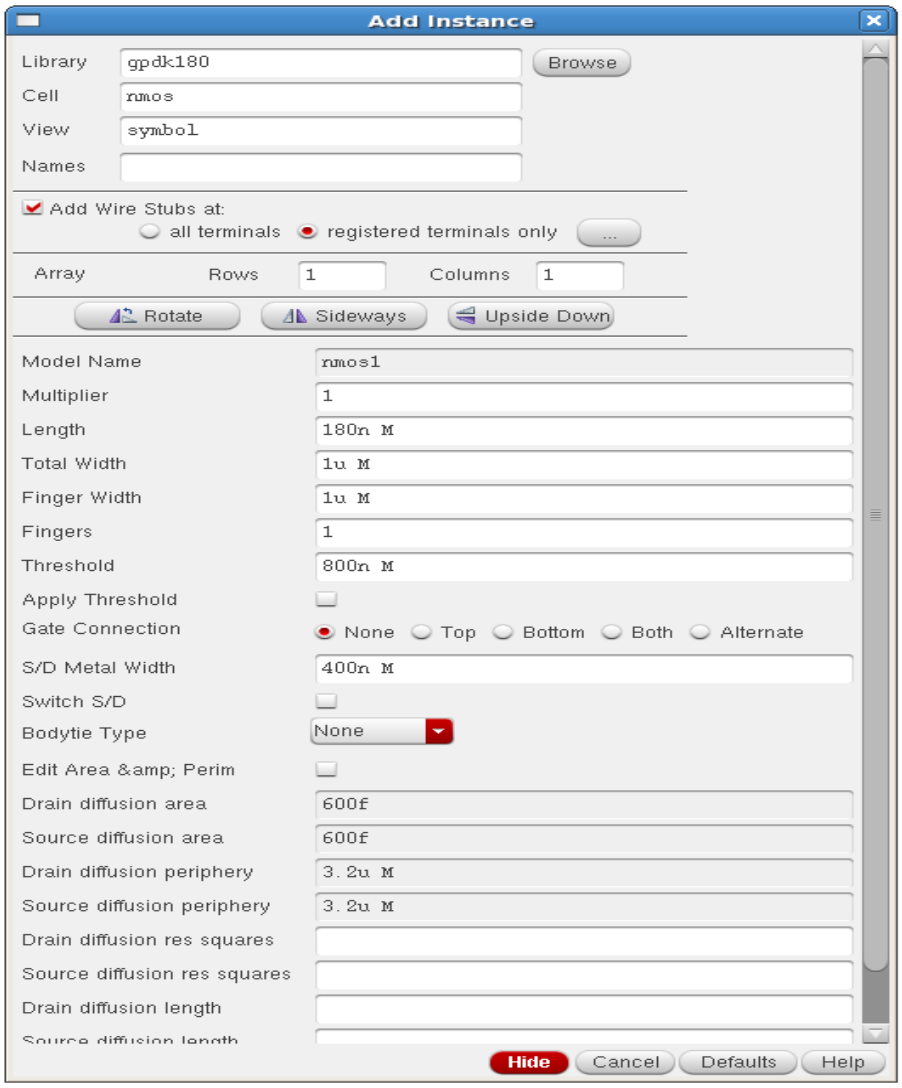


2. Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view.



You will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.

Instantiating the nmos symbol is shown below as an example



3. After you complete the Add Instance form, move your cursor to the Schematic window and **left click** to place a component.

4. After entering components, click **Cancel** in the Add Instance form or press ***Esc.***
This is a table of components for building the Inverter schematic.

Library name	**Cell Name**	**Properties**
gpdk180	pmos	Total Width= **wp**, Length=180n
gpdk180	nmos	Total Width = 1u, Length=180n

If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters.

Use the **Edit— Move** command if you place components in the wrong location.

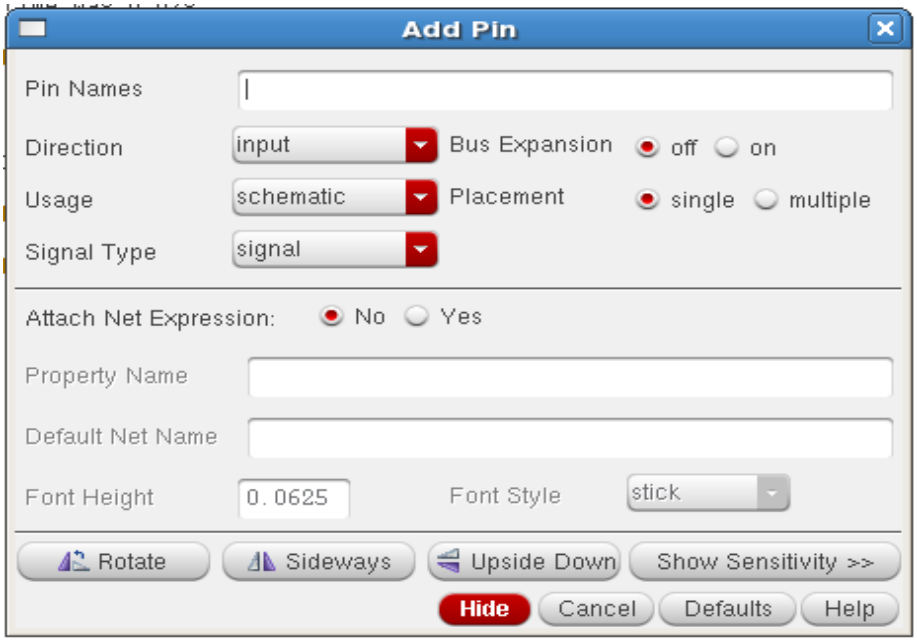
You can rotate components at the time you place them, or use the **Edit— Rotate** command after they are placed.

Adding pins to Schematic

1. Click the **Pin** fixed menu icon in the schematic window. 

Tip: You can also execute **Create — Pin** or press **p**.

The Add pin form appears.



2. Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Names	Direction
in, Vdd, Vss	input
out	output

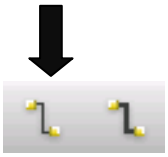
Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.

3. Select **Cancel** from the Add – pin form after placing the pins.

In the schematic window, execute **Window— Fit** or press f to fit all the components to the schematic editor window.

Adding Wires to a Schematic

Add wires to connect components and pins in the design.



1. Click the **Wire (narrow)** icon in the schematic window.

Tip: You can also press the **w** key, or execute **Create — Wire (narrow).**

2. In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.

3. Follow the prompts at the bottom of the design window and **left click** on the destination point for your wire. A wire is routed between the source and destination points.

4. Complete the wiring as shown in figure and when done wiring press **ESC** key in the schematic window to cancel wiring.

Note: A single node cannot have more than 3 branches.

Saving the Design

1. Click the **Check and Save** icon in the schematic editor window.

2. Observe the CIW output area for any errors.

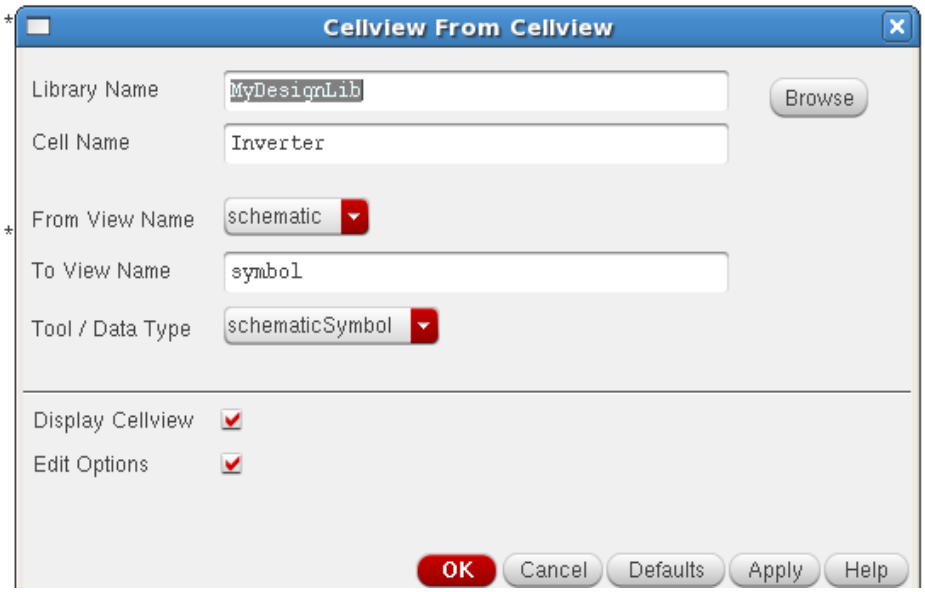
Symbol Creation

Objective: To create a symbol for the Inverter

In this section, you will create a symbol for your inverter design so you can place it in a test circuit for simulation. A symbol view is extremely important step in the design process. The symbol view must exist for the schematic to be used in a hierarchy. In addition, the symbol has attached properties (cdsParam) that facilitate the simulation and the design of the circuit.

1. In the Inverter schematic window, execute **Create — Cellview— From Cellview**.

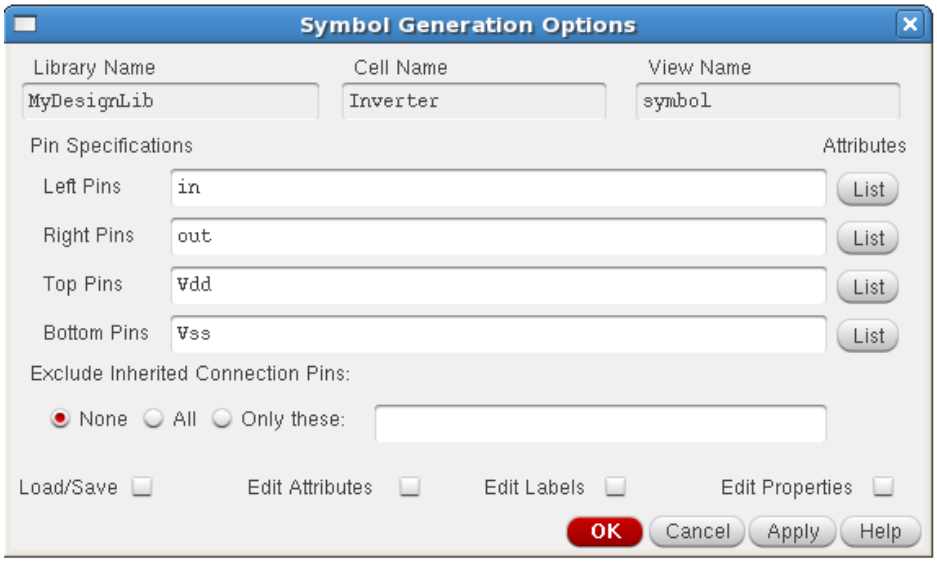
The "**Cellview From Cellview"** window appears. With the Edit Options function active, you can control the appearance of the symbol to generate.



2. Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **schematicSymbol**.

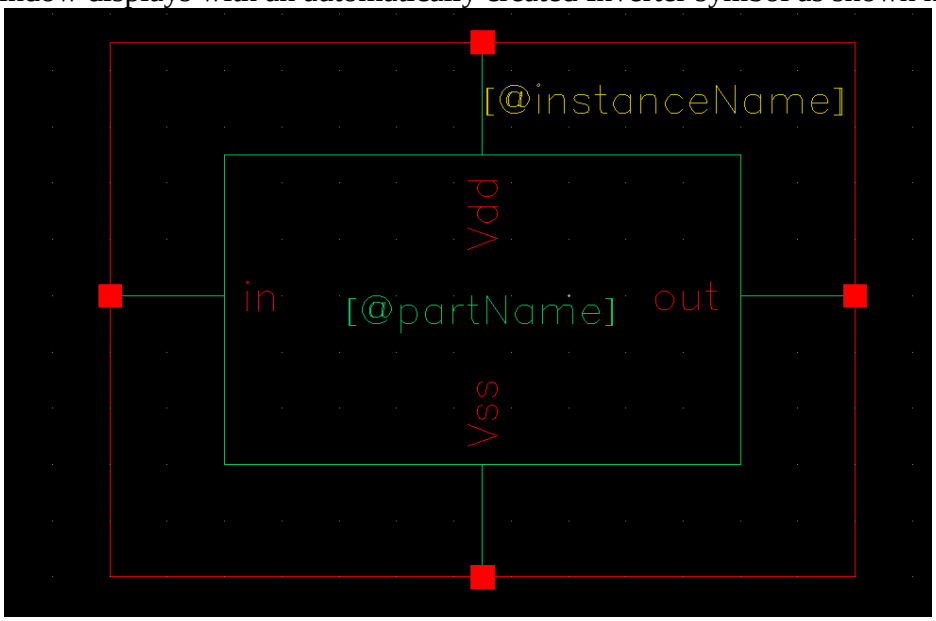
3. Click **OK** in the **"Cellview From Cellview"** form.

4. The **"Symbol Generation options"** window appears. Arrange the pins the way the symbol should have them.



5. Click **OK** in the **"Symbol Generation Options"** form.

6. A new window displays with an automatically created Inverter symbol as shown here.



Editing a Symbol

In this section we will modify the inverter symbol to look like an Inverter gate symbol.

1. Move the cursor over the automatically generated symbol, until the green rectangle is highlighted, **left click** to select it.

2. Click **Delete** icon in the symbol window, similarly select and delete the outer red rectangle.

3. Execute **Create – Shape – polygon**, and draw a shape similar to triangle.

4. After creating the triangle press ***Esc*** key.

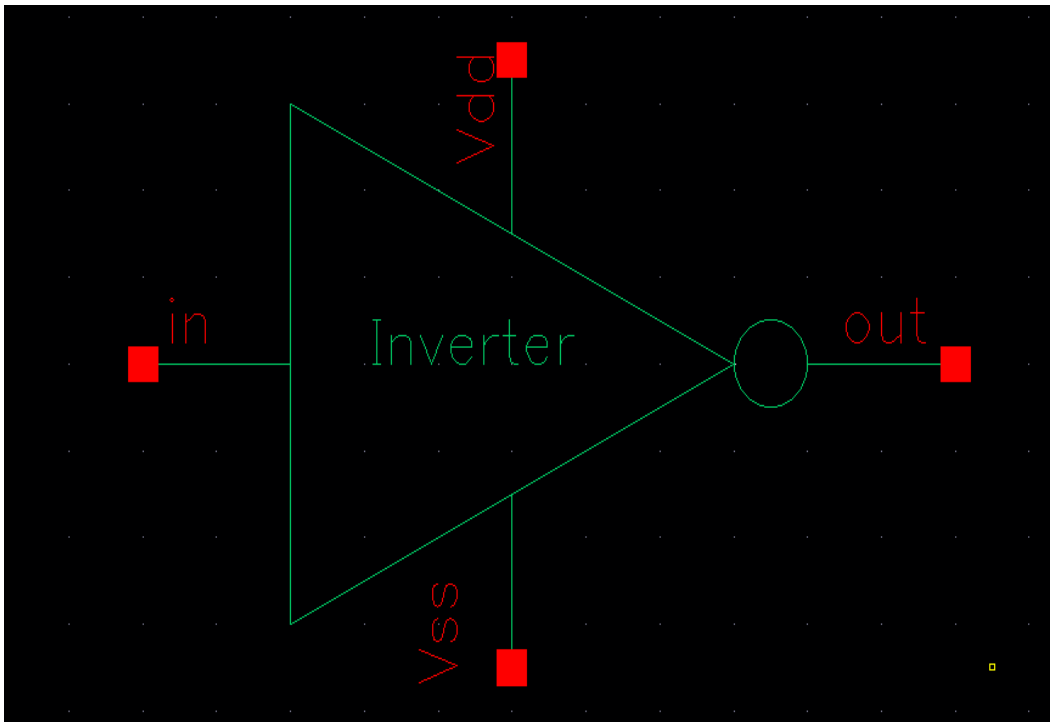
5. Execute **Create – Shape – Circle** to make a circle at the end of triangle.

6. You can move the pin names according to the location.

7. Execute **Create – Selection Box**. In the Add Selection Box form, click **Automatic**. A new red selection box is automatically added.

8. After creating symbol, click on the **save** icon in the symbol editor window to save the symbol.

9. In the symbol editor, execute **File – Close** to close the symbol view window.



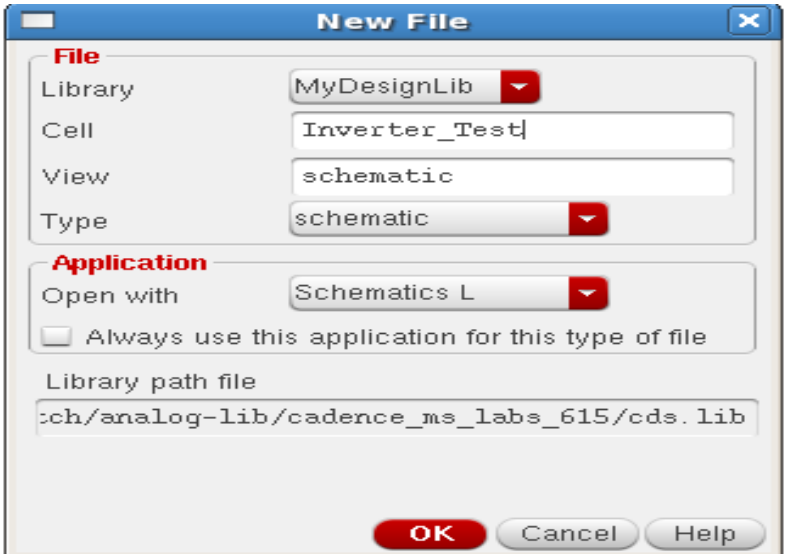
Building the Test Design

Objective: To build an Inverter Test circuit using Inverter symbol

You will create the Inverter_Test cellview that will contain an instance of the Inverter cellview.

1. In the CIW or Library Manager, execute **File – New – Cellview**.

2. Set up the **New File** form as follows



3. Click **OK** when done. A blank **Schematic Editor** window for the **Inverter_Test** design appears.

Building the Inverter_Test Circuit

1. Using the component list and Properties/Comments in this table, build the **Inverter_Test** schematic.

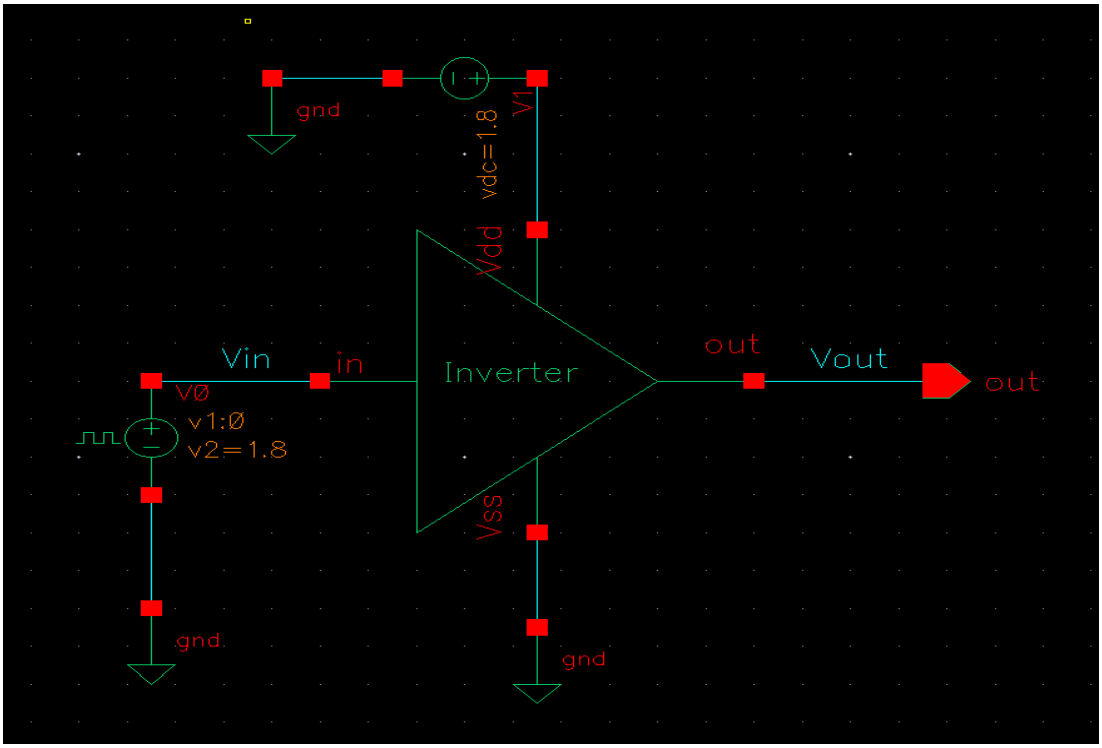
Library name	Cellview name	Properties
MyDesignLib	Inverter	Symbol
analogLib	Vpulse (as input signal)	voltage1=0, voltage2=1.8,period =20n, pulse width= 10n.
analogLib	vdc	DC voltage =1.8
analogLib	gnd	

2. Add the above components using **Create — Instance** or by pressing **i**. 

3. Click the **Wire (narrow)** icon and wire your schematic. 

4. Click **Create — Wire Name** or press **L** to name the input **(Vin)** and output **(Vout)** wires as in the below schematic. 

5. Click on the **Check and Save** icon to save the design. 



6. Leave your **Inverter_Test** schematic window open for the next section.

Analog Simulation with Spectre

Objective: To set up and run simulations on the Inverter_Test design

In this section, we will run the simulation for Inverter and plot the transient; DC characteristics and we will do Parametric Analysis after the initial simulation.

Starting the Simulation Environment

1. In the **Inverter_Test** schematic window, execute **Launch – ADE L**
The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

Choosing a Simulator

Set the environment to use the **Spectre® tool**, a high speed, highly accurate analog simulator. Use this simulator with the **Inverter_Test** design, which is made-up of analog components.

1. In the simulation window (ADE), execute **Setup— Simulator/Directory/Host**.

2. In the Choosing Simulator form, set the Simulator field to **Spectre** (Not spectreS) and click **OK**.

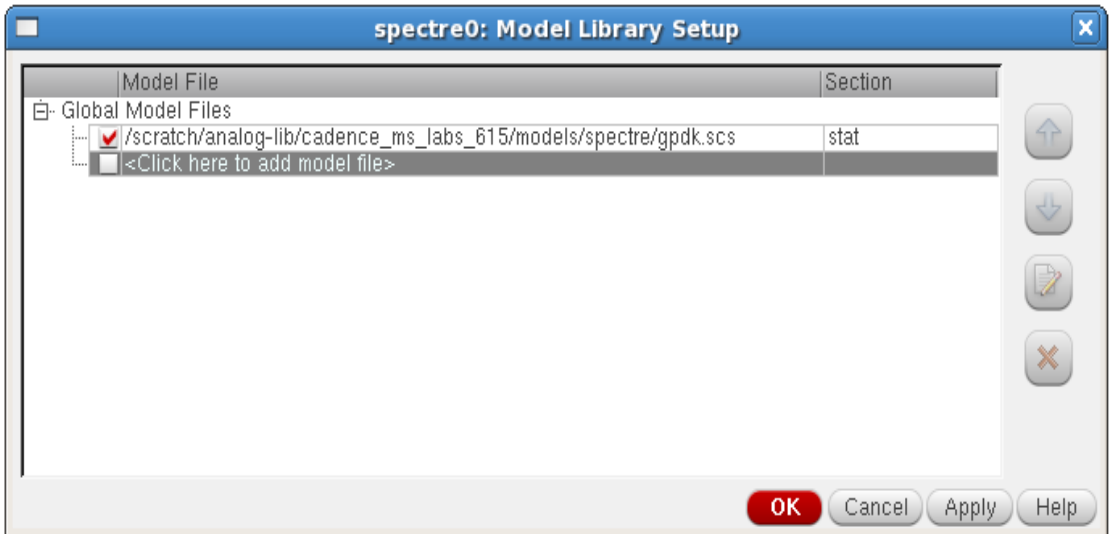
Setting the Model Libraries

The Model Library file contains the model files that describe the nmos and pmos devices during simulation.

1. In the simulation window (ADE L), execute **Setup - Model Libraries.**

The Model Library Setup form appears. Click the **browse** button  to add **gpdk.scs** if not added by default as shown in the **Model Library Setup** form.
Remember to select the section type as **stat** in front of the gpdk.scs file.

The Model Library Setup window should looks like the figure below.



To view the model file, highlight the expression in the **Model Files** field and Click **Edit File**.

2. To complete the Model Library Setup, move the cursor and click **OK.**

Choosing Analysis

This section demonstrates how to view and select the different types of analysis to complete the circuit when running the simulation.

1. In the Simulation window (ADE), execute **Analysis - Choose Analysis** or click the 

Choose - Analysis icon.

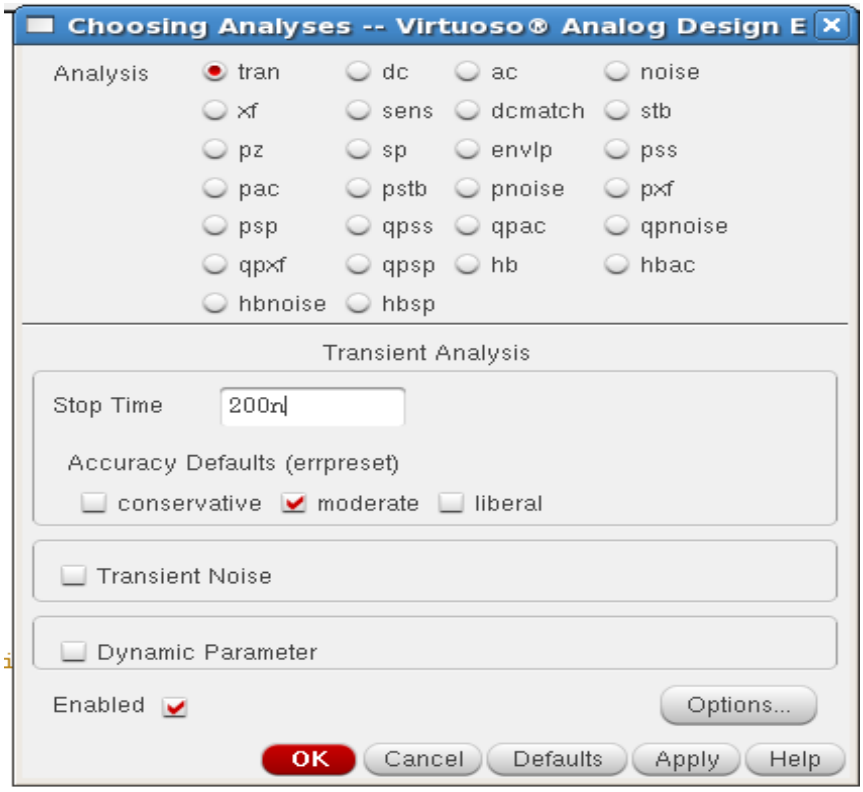
The Choosing Analysis form appears. This is a dynamic form, the bottom of the form changes based on the selection above.

2. To setup for transient analysis

   a. In the Analysis section select **tran**.

   b. Set the stop time as **200n**.

   c. Click at the **moderate** and **Enabled** buttons at the bottom, and then click **Apply**.



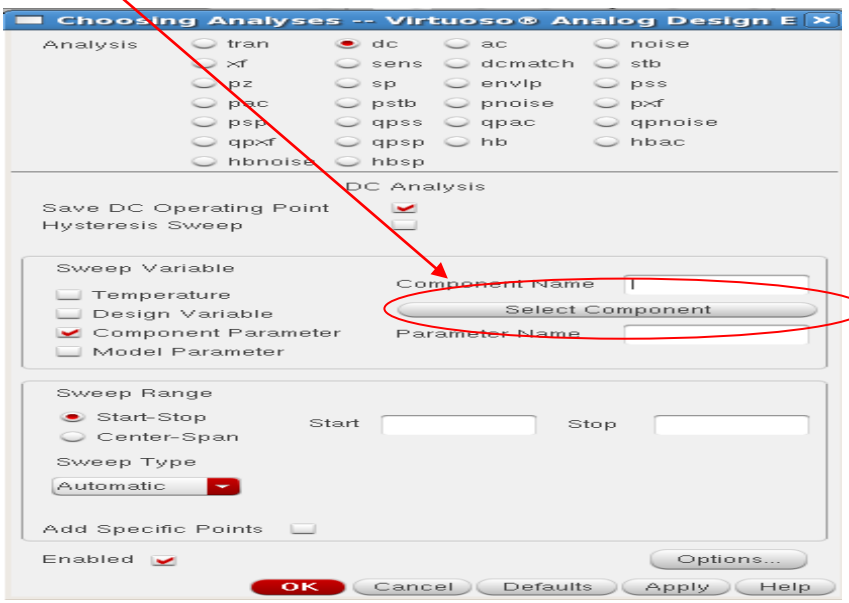
3. To set up for DC Analysis:

   a. In the Analysis section, select **dc**.

   b. In the DC Analysis section, turn on **Save DC Operating Point.**

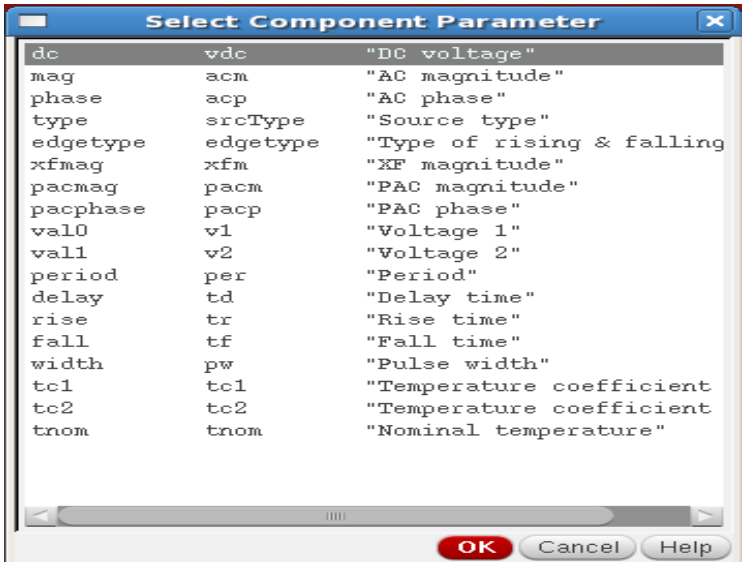
   c. Turn on the **Component Parameter**.

   d. Click the **Select Component**, Which takes you to the schematic window.



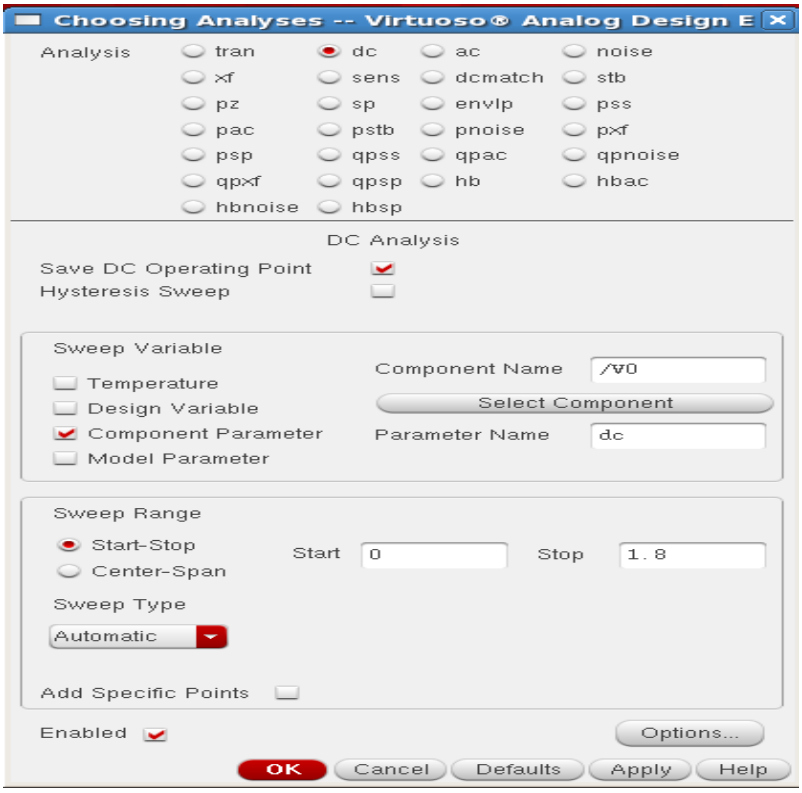
e. Select input signal **vpulse source** in the test schematic window.

f. Select **DC Voltage** in the "**Select Component Parameter"** window and click **OK**.



f. In the analysis form, enter **start** and **stop** voltages as **0** to **1.8** respectively.

g. Check the enable button and then click **Apply.**



4. Click **OK** in the Choosing Analysis Form.

Setting Design Variables

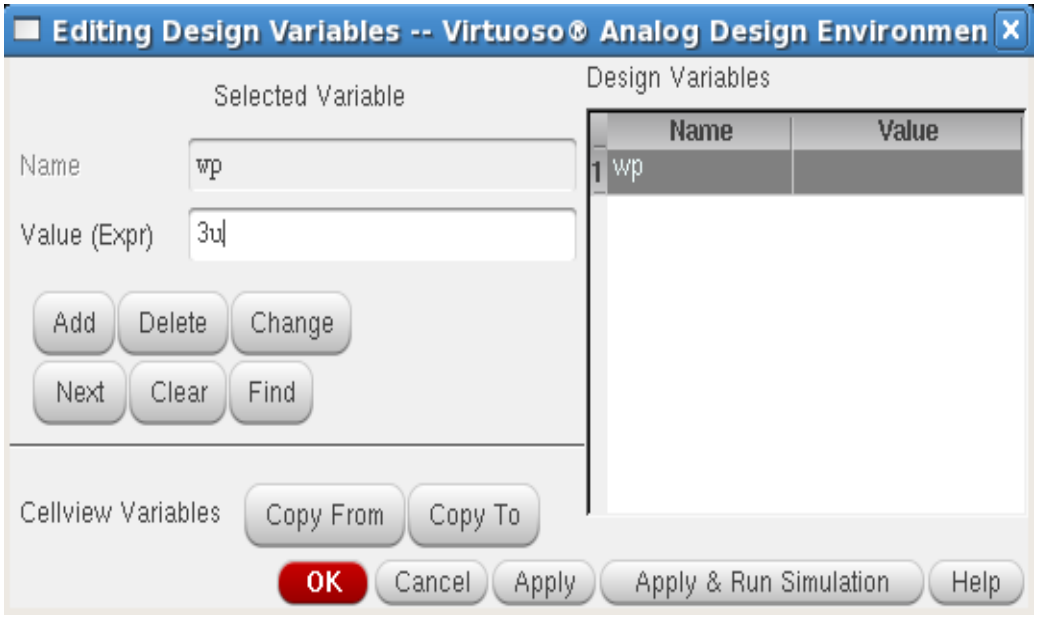
Set the values of any design variables in the circuit before simulating. Otherwise, the simulation will not run.

1. In the Simulation window, execute **Variables – Edit variables** or click the  **Edit Variables** icon present in the ADE L window. The **"Editing Design Variables"** window appears.

2. Click **Copy From** at the bottom of the window. The design is scanned and all variables found in the design are listed. In a few moments, the **wp** variable appears in the Table of Design variables section.

3. Set the value of the **wp** variable: - With the **wp** variable highlighted in the Table of Design Variables, click on the variable name **wp** and enter the following:

Value (Expr)	3u



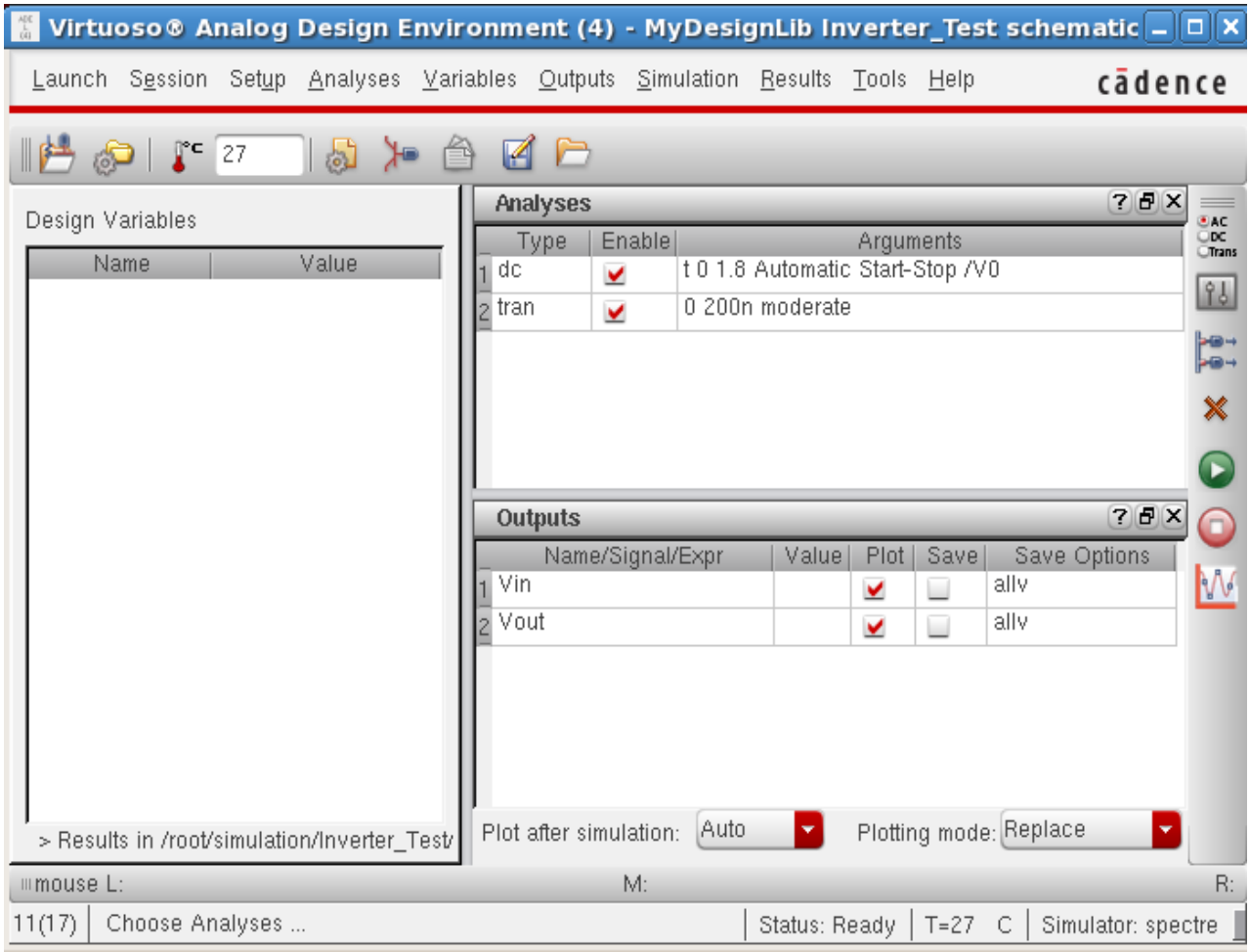
4. Click **Change** and notice the update in the Table of Design Variables, Click **OK** to exit.

Selecting Signals for Plotting

1. Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.

2. Follow the prompt at the bottom of the schematic window, Click on output net **Vout**, input net **Vin** of the Inverter_Test. Press ***Esc*** with the cursor in the schematic after selecting it.

After setting the transient and DC analysis and also the signals for wave plotting, the ADE L window will look like the figure below.

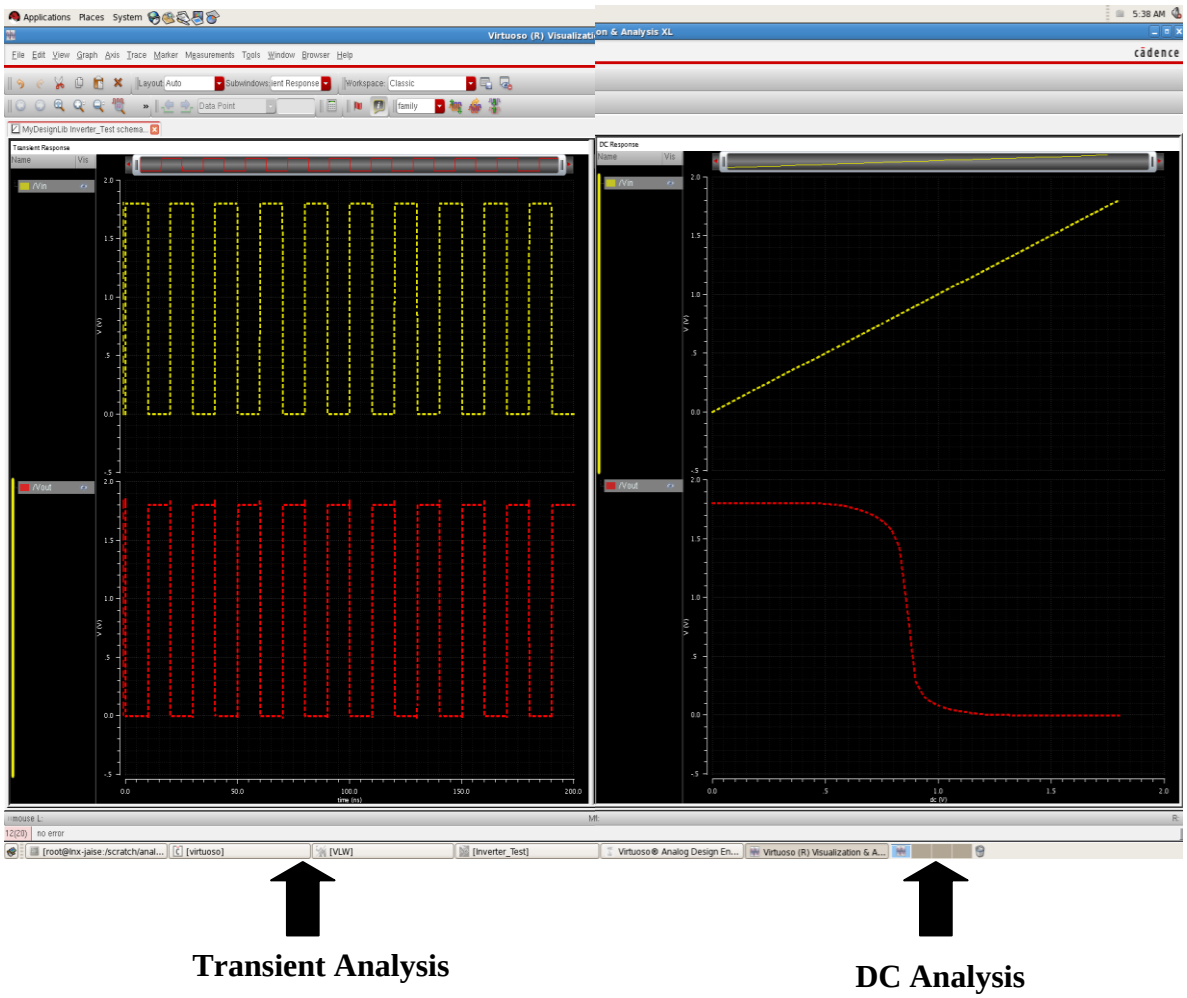


Running the Simulation

1. Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation or the  **Netlist and Run** icon present in the ADE L window, this will create the netlist as well as run the simulation.

2. When simulation finishes, the Transient, DC plots automatically will be popped up along with log file.

3. Click on the **Split Current Strip** icon  to separate the wave plots.



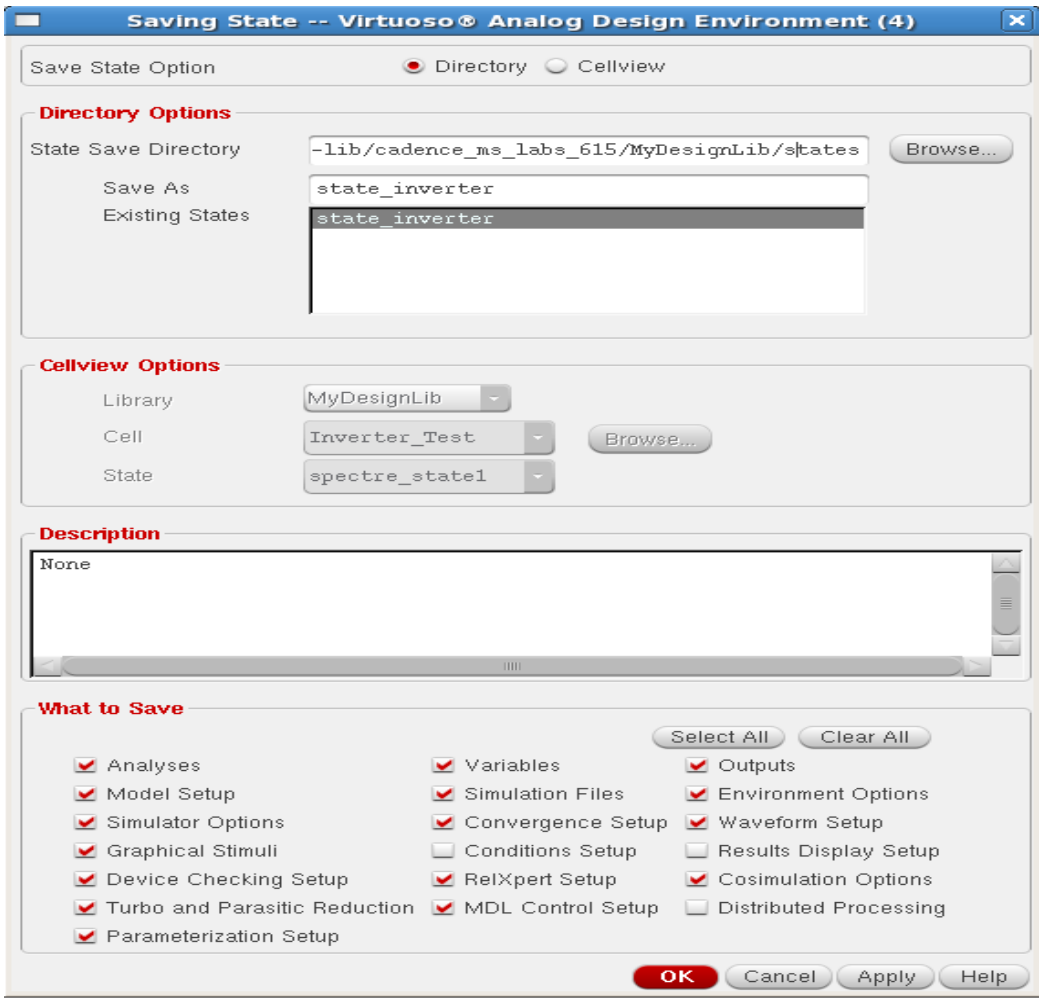
Transient Analysis **DC Analysis**

Saving the Simulator State

We can save the simulator state, which stores information such as model library file, outputs, analysis, variable etc. This information restores the simulation environment without having to type in all of setting again.

1. In the Simulation window, execute **Session – Save State**. The Saving State form appears.

2. Set the **Save State Directory** field to the directory in which the state should be saved. Change the **Save as** field to **state_inverter** (any valid identifier) and make sure all options are selected under **What to save** field.

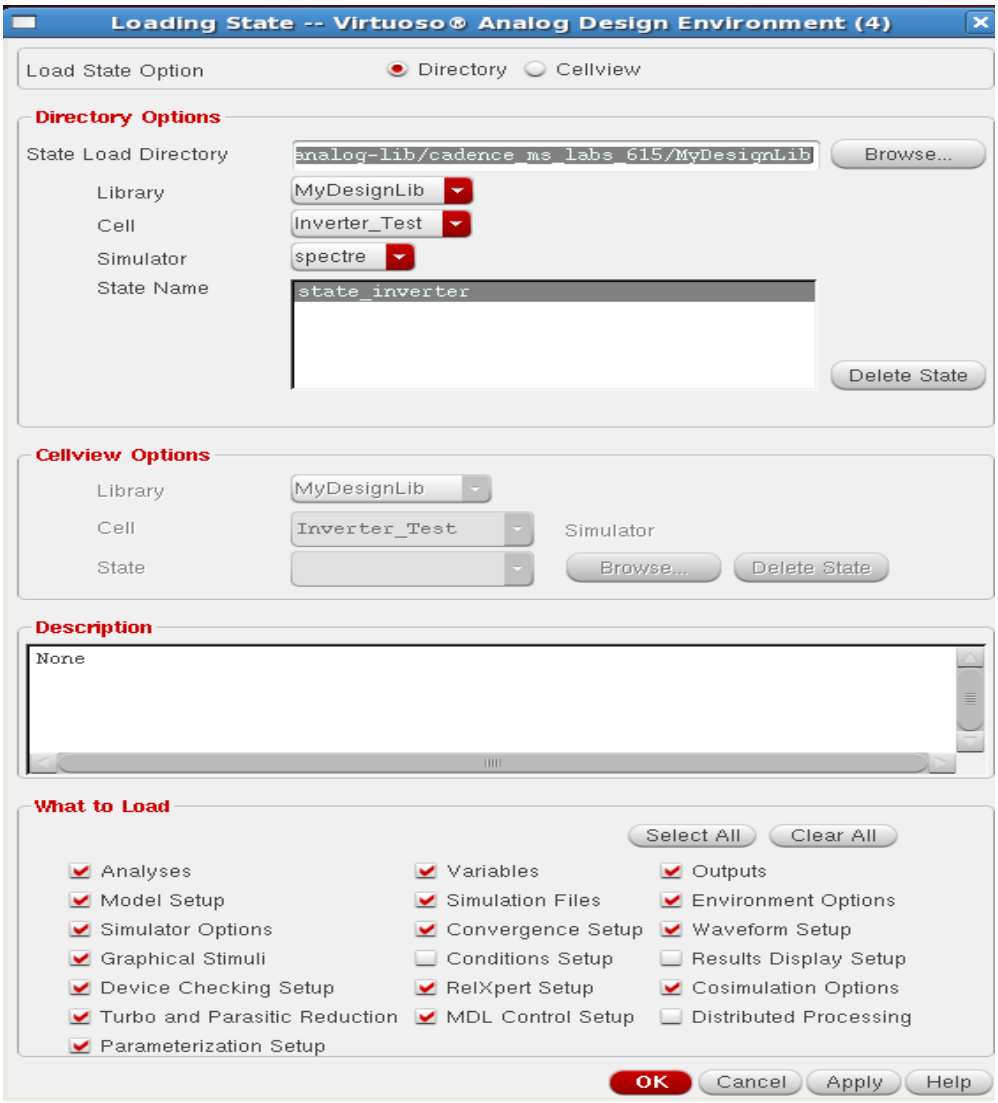


3. Click **OK** in the saving state form. The Simulator state is saved.

Loading the Simulator State

1. From the ADE window execute **Session – Load State.**

2. In the Loading State window, set the State name to **state_inverter** as shown



3. Click **OK** in the Loading State window.

Parametric Analysis

Parametric Analysis yields information similar to that provided by the Spectre sweep feature, except the data is for a full range of sweeps for each parametric step. The Spectre sweep feature provides sweep data at only one specified condition.

You will run a parametric DC analysis on the **wp** variable, of the pmos device of the Inverter design by sweeping the value of **wp**.

Starting the Parametric Analysis Tool

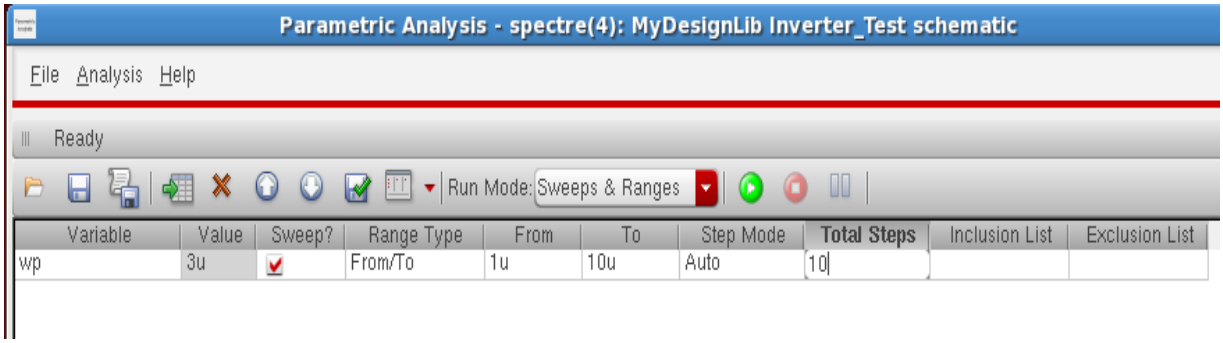
1. In the Simulation window, execute **Tools—Parametric Analysis**. **The Parametric Analysis** form appears.
2. In the **Parametric Analysis** window, double click on the **Add Variable field**. Then an option for selecting the variable appears. This option leads to a selection window with a list of all variables in the design that you can sweep. This list includes the variables that appear in the Design Variables section of the Simulation window.

3. In the selection window, click on **wp**, the Variable Name field for Sweep in the Parametric Analysis form is set to **wp**.

4. Change the **Range Type, Step Mode** and **Total Steps** fields in the Parametric Analysis form as shown below:

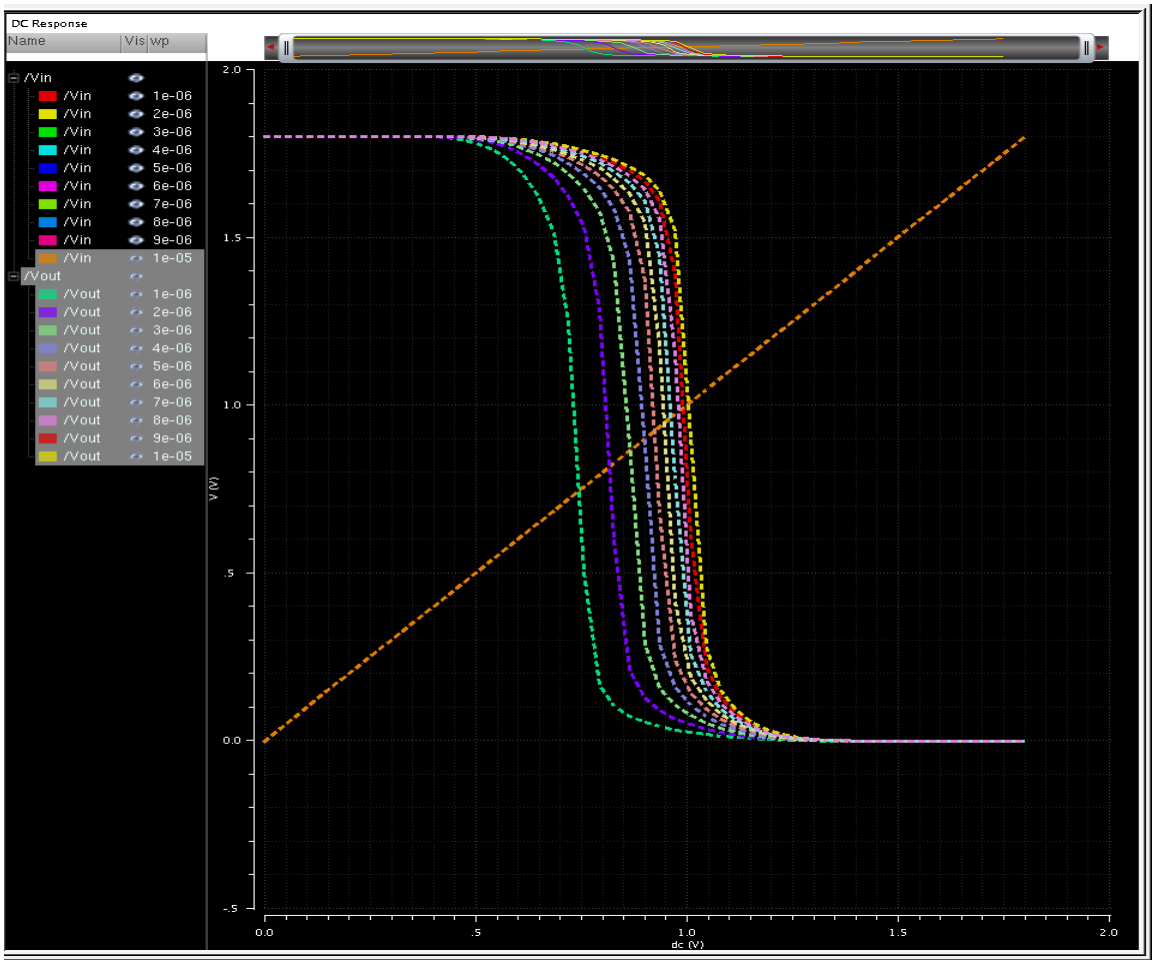
Range Type	**From/To**	From →	**1u**	To →	**10u**
Step Control	**Auto**				
Total Steps	**10**				

These numbers vary the value of the **wp** of the pmos between 1um and 10um at ten evenly spaced intervals.



5. Execute **Analysis—Start Selected** or click the  **Run Selected Sweeps** icon in the **Parametric Analysis** window.

The **Parametric Analysis** window displays the number of runs remaining in the analysis and the current value of the swept variable(s). Look in the upper left corner of the window. Once the runs are completed the **wave scan** window comes up with the plots for different runs.

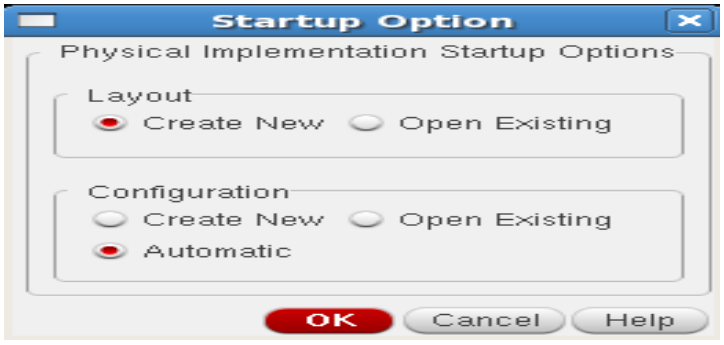


Note: Change the **wp** value of pmos device back to 3u and save the schematic before proceeding to the next section of the lab. To do this, use **Edit Property** option.

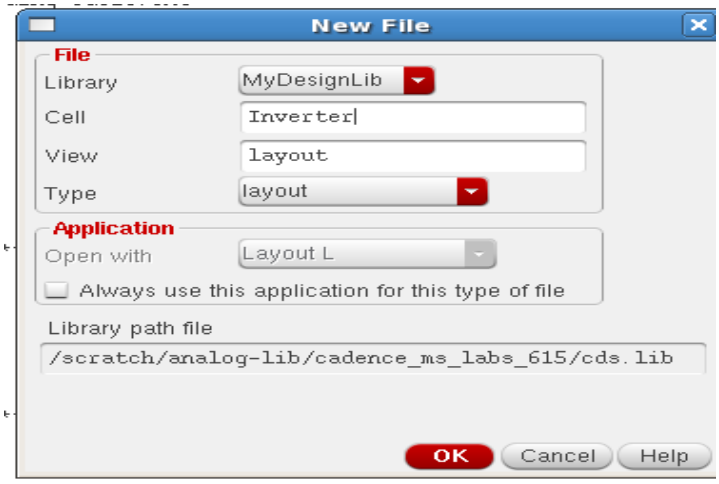
Creating Layout View of Inverter

1. From the **Inverter** schematic window menu execute **Launch – Layout XL**. A "**Startup Option"** form appears.

2. Select **Create New** option and click **OK.**

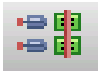


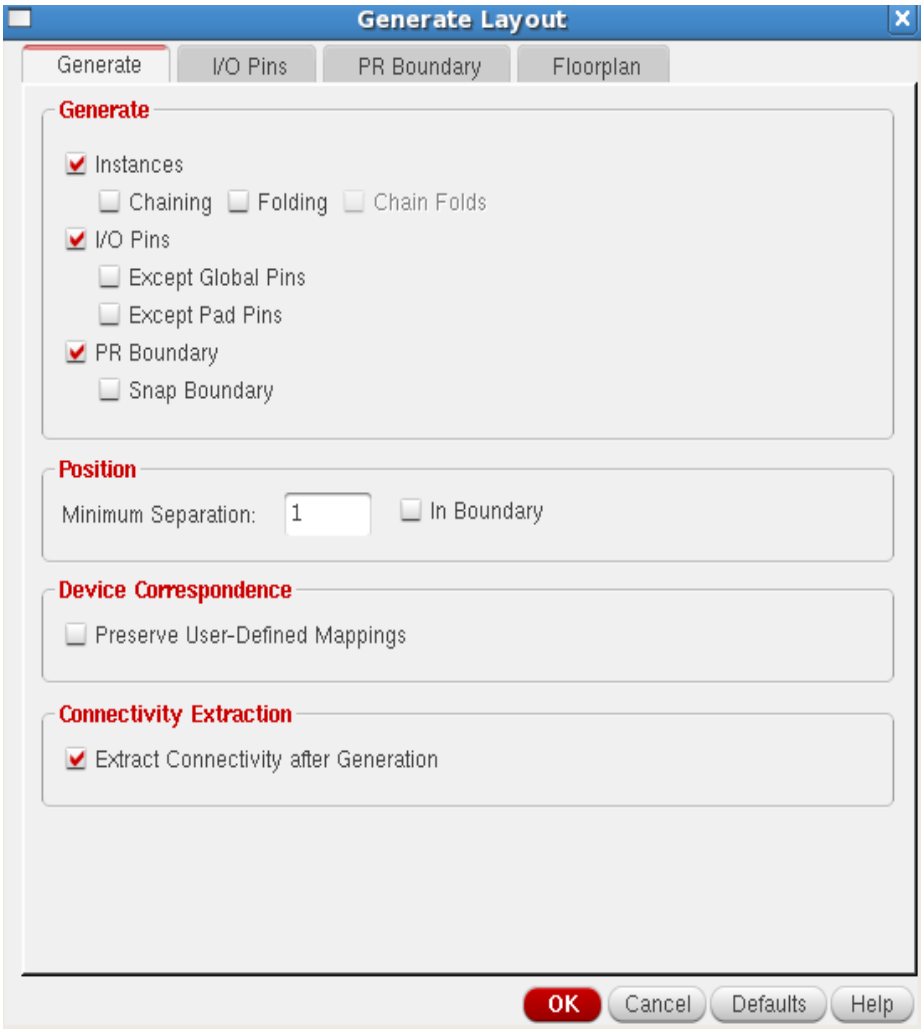
3. A **"New File"** form appears, Check the Library (**MyDesignLib**), Cellname **(Inverter)** and Viewname **(layout).**



4. Click **OK** from the **"New File"** Window. **LSW** (Layer Select Window) and a blank layout window appear along with schematic window.

Adding Components to Layout

1. Execute **Connectivity – Generate – All from Source** or click the icon  in the **"Layout Editor window"**, **Generate Layout** form appears. Click **OK** which imports the schematic components in to the Layout window automatically.



2. Re arrange the components with in PR-Boundary as shown in the next page.

3. We can stretch the PR-Boundary to our requirement by executing **Edit-stretch** or click the stretch icon  and them the PR-Boundary. Press ***Esc*** after stretching. We can also use this feature to stretch Wire and routing elements.

Tip: Press **S** to stretch.

4. To move the components, execute **Edit-Move** or click the **Move** icon  and then click on the component which is to be moved. . Press ***Esc*** after moving.

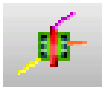
Tip: Press **M** to move.

5. To rotate a component, Select the component and execute **Edit –Properties**. Now select the degree of rotation from the property edit form.

6. To know the distance between different components, or to measure the area consumed by the design, execute **Tools - Create Ruler.** Press ***Esc*** after measurements.

Tip: Press **K** for ruler.

Making interconnection

1. Execute **Connectivity –Nets – Show/Hide selected Incomplete Nets** or click  the icon in the Layout Menu.

2. Try to move a device to get the connectivity information, which shows the guide lines (or flight lines) for the inter connections of the components.

3. From the layout window execute **Create – Shape – Path** or **Create wire or click**  or **Create – Shape – Rectangle (**for vdd and gnd bar**)** and select the appropriate Layers from the **LSW** window and Vias for making the inter connections.

Creating Contacts/Vias

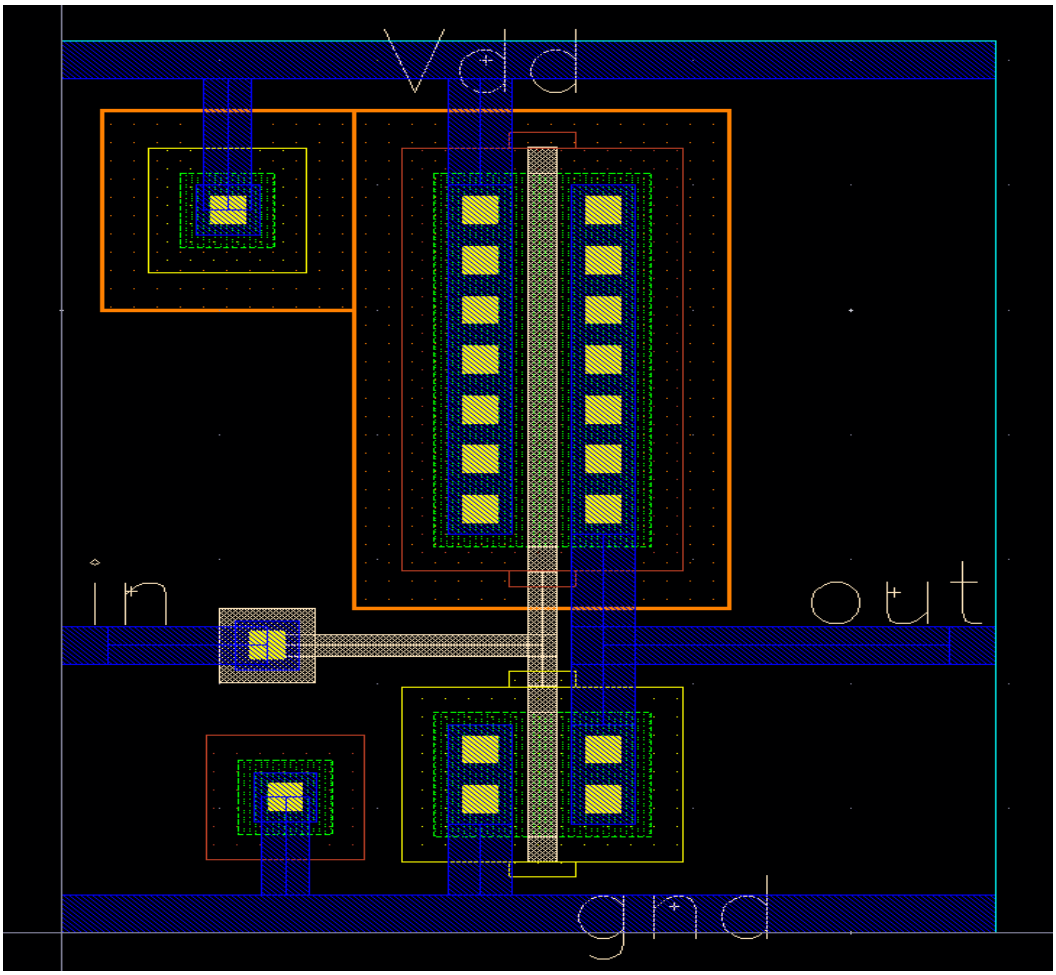
We will use the contacts or vias to make connections between two different layers.

1. Execute **Create — Via** or click  icon to place different Contacts, as given in below table.

Connection	Contact Type
For Metal1- Poly Connection	Metal1-Poly
For Metal1- Psubstrate Connection	Metal1-Psub
For Metal1- Nwell Connection	Metal1-Nwell

Saving the design

1. Save your design by selecting **File — Save** or click  to save the layout and layout should appear as below



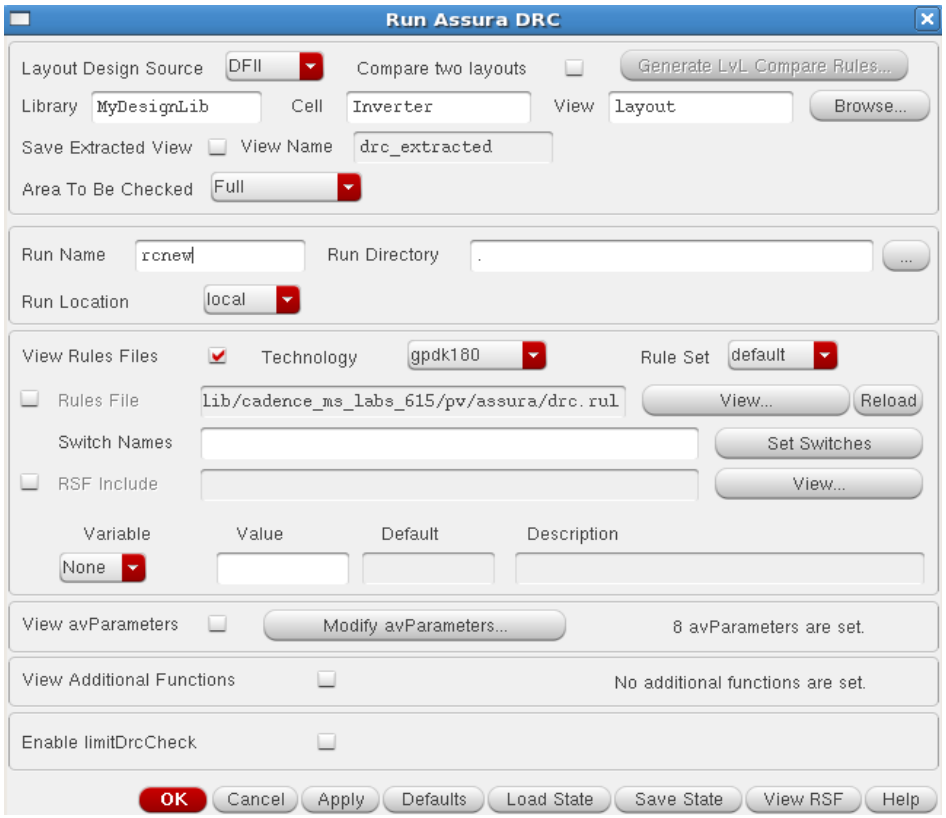
Physical Verification

Assura DRC

Here we check whether our design obeys the design rules.

Running a DRC

1. Select **Assura - Run DRC** from layout window. The DRC form appears. The Library and Cellname are taken from the current design window, but rule file may be missing. Select the Technology as **gpdk180.** This automatically loads the rule file.



3. Click **OK** to start DRC.

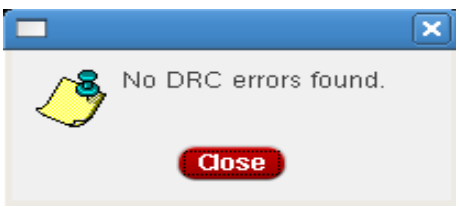
4. A Progress form will appears. You can click on the watch log file to see the log file.

5. When DRC finishes, a dialog box appears asking you if you want to view your DRC results, and then click **Yes** to view the results of this run.

6. If there any DRC error exists in the design, **View Layer Window** (VLW) and **Error Layer Window** (ELW) appears. Also the errors highlight in the design itself.

7. You can refer to rule file also for more information, correct all the DRC errors and **Re – run** the DRC.

8. If there are no errors in the layout then a dialog box appears with **No DRC errors found** written in it, click on **close** to terminate the DRC run.



Assura LVS

In this section we will perform the LVS check that will compare the schematic netlist and the layout netlist.

Running LVS

1. Select **Assura – Run LVS** from the layout window. The **"Run Assura LVS"** form appears. It will automatically load both the schematic and layout view of the cell.

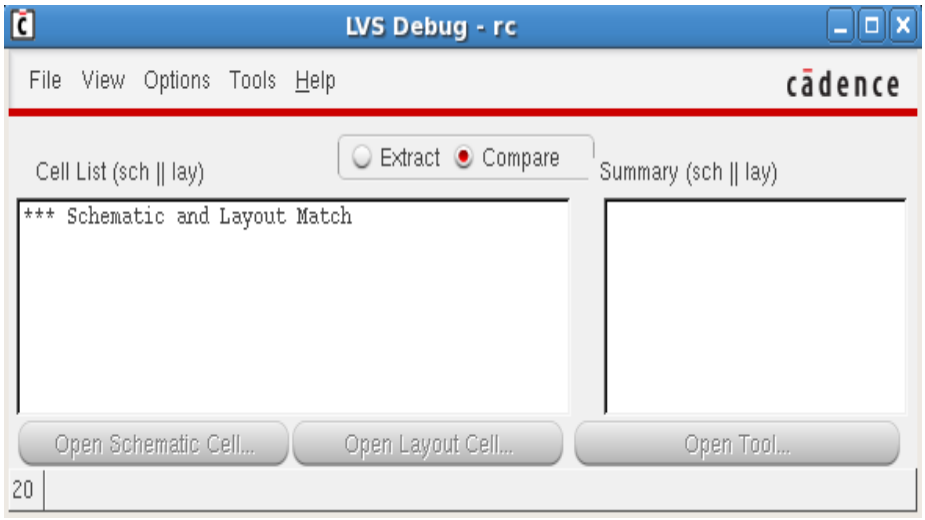
2. Click **OK** to run LVS.

3. Once the LVS is completed, a window informs that the LVS completed successfully and asks if you want to see the results of this run. Click **Yes** in the window.

4. If the schematic and layout do not matches, **LVS Debug** window appears, and you are directed into **LVS Debug Environment.**

5. In the **LVS Debug** window you can find the details of mismatches and you need to correct all those mismatches and **Re – run** the LVS till you will be able to match the schematic with layout.

6. If the schematic and layout matches completely, you will get a window displaying **Schematic and Layout Match.** Close the window to terminate the LVS run.

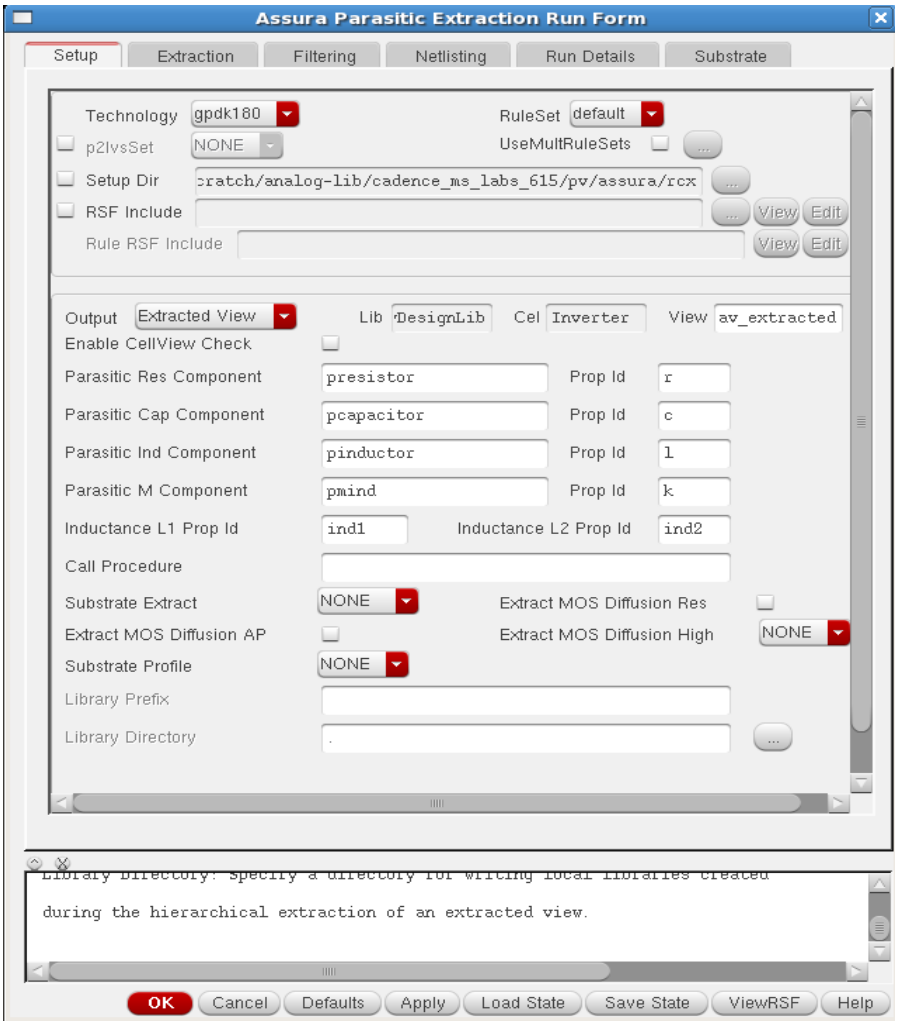


Assura RCX

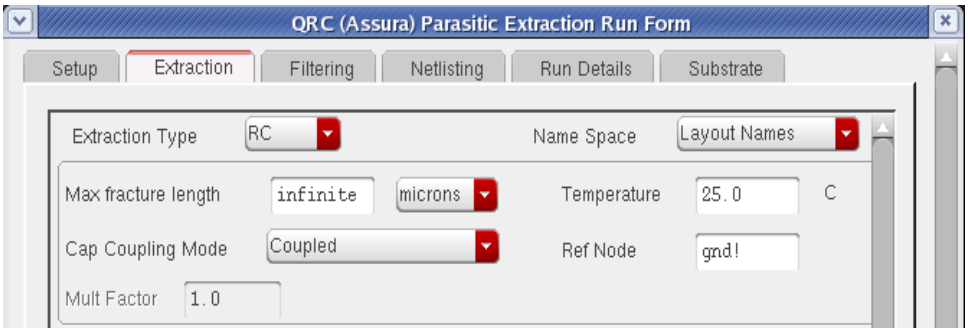
In this section we will extract the RC values from the layout and perform analog circuit simulation on the designs extracted with RCX. Before using RCX to extract parasitic devices for simulation, the layout should match with schematic completely to ensure that all parasites will be backannoted to the correct schematic nets.

Running RCX

1. From the layout window execute **Assura – Run RCX**.
2. Change the following in the "**Assura parasitic extraction run form"**. Select **Output** type under **Setup** tab as **Extracted View**.



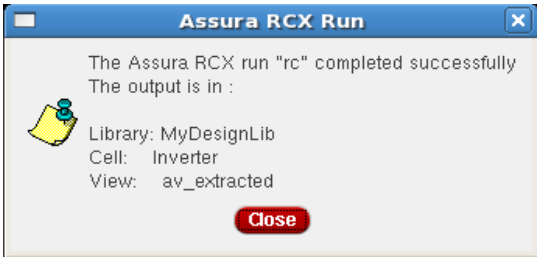
3. In the **Extraction** tab of the form, choose Extraction type, Cap Coupling Mode and specify the Reference node for extraction.



4. In the **Filtering** tab of the form, **Enter Power Nets** as **vdd!, vss!** and **Enter Ground Nets** as **gnd!**

5. Click **OK** in the Assura parasitic extraction form when done. The RCX progress form appears, in the progress form click **Watch log file** to see the output log file.

6. When RCX completes, a dialog box appears, informs you that **Assura RCX run Completed successfully.** Click on **close** to terminate the RCX run

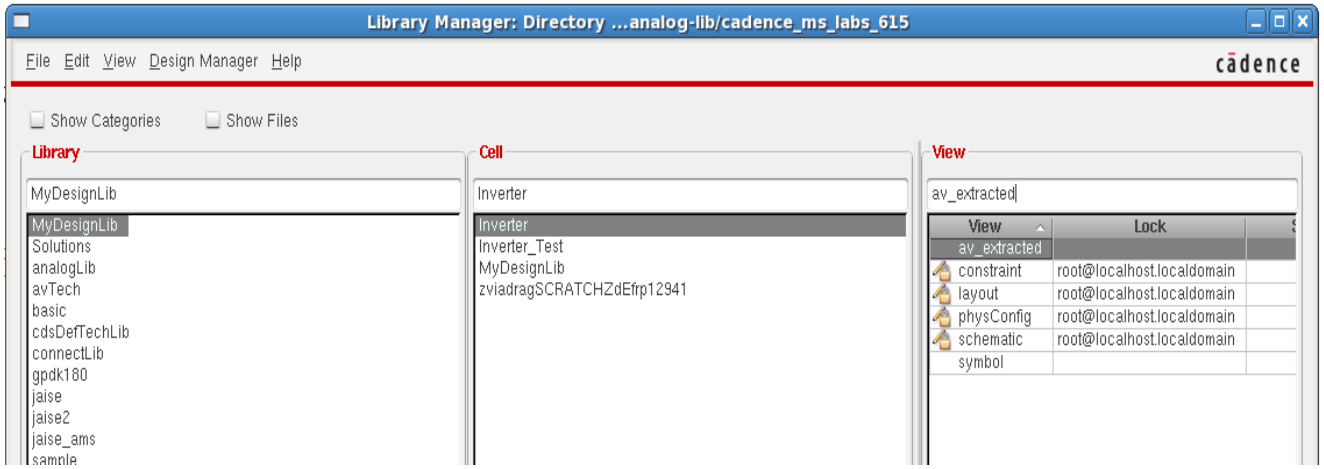


7. To view the av_extracted design, execute the following steps from the CIW window **Tools – Library Manager**, select the following

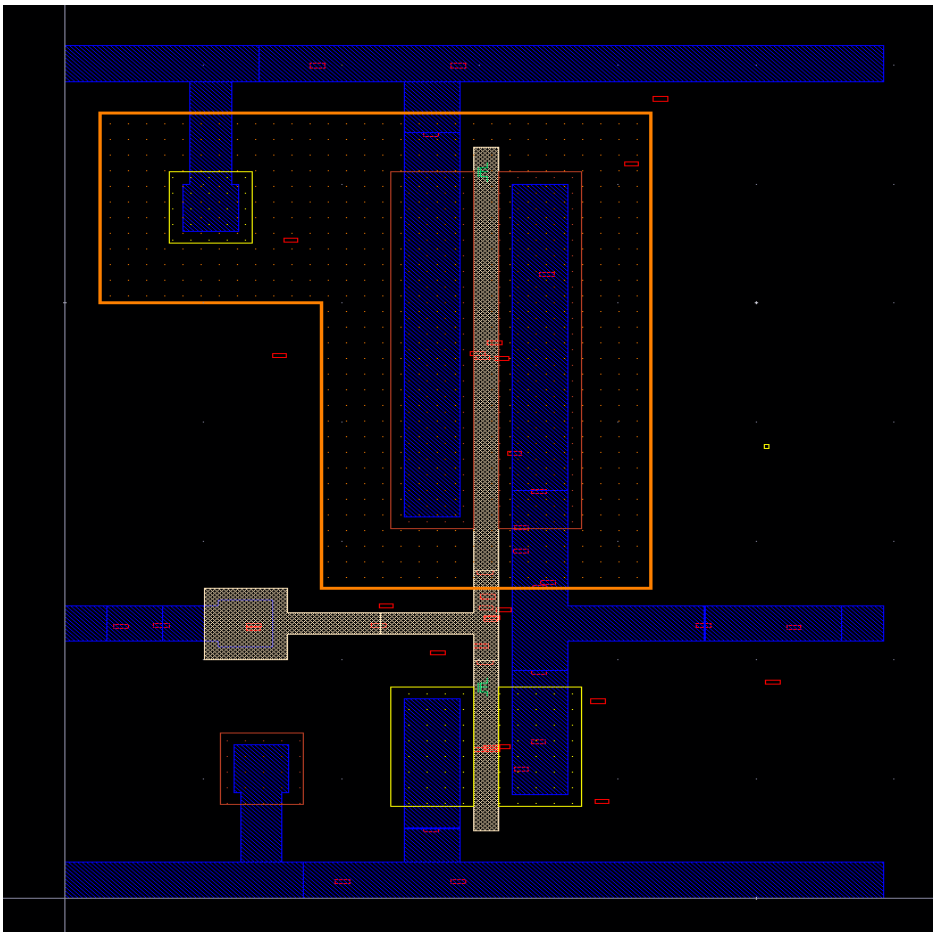
Library ⟶ MyDesignLib

Cell ⟶ Inverter

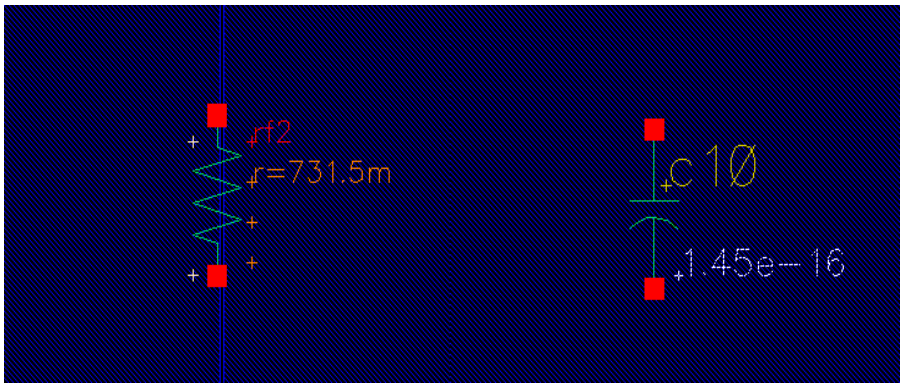
Double click on **av_extracted** option under **View** field. The av_extraced view of designwill pop up.



The av_extracted view of the inverter design looks like this



Note: - Press **shift-f** to view values of the extracted resistance and capacitance in the av_extracted view

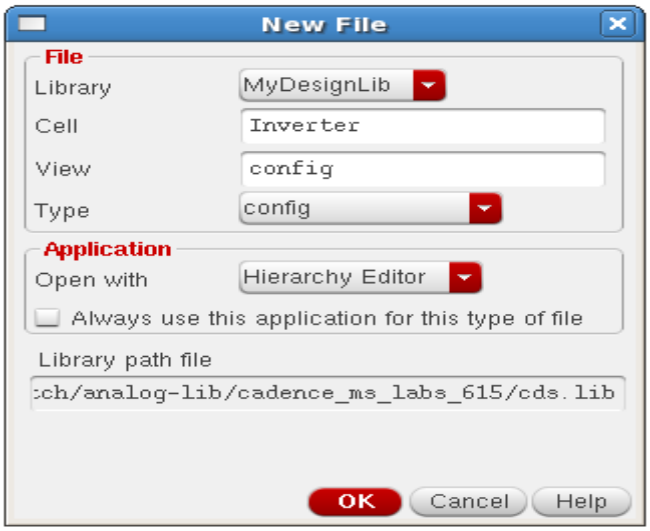


Creating the Configuration View

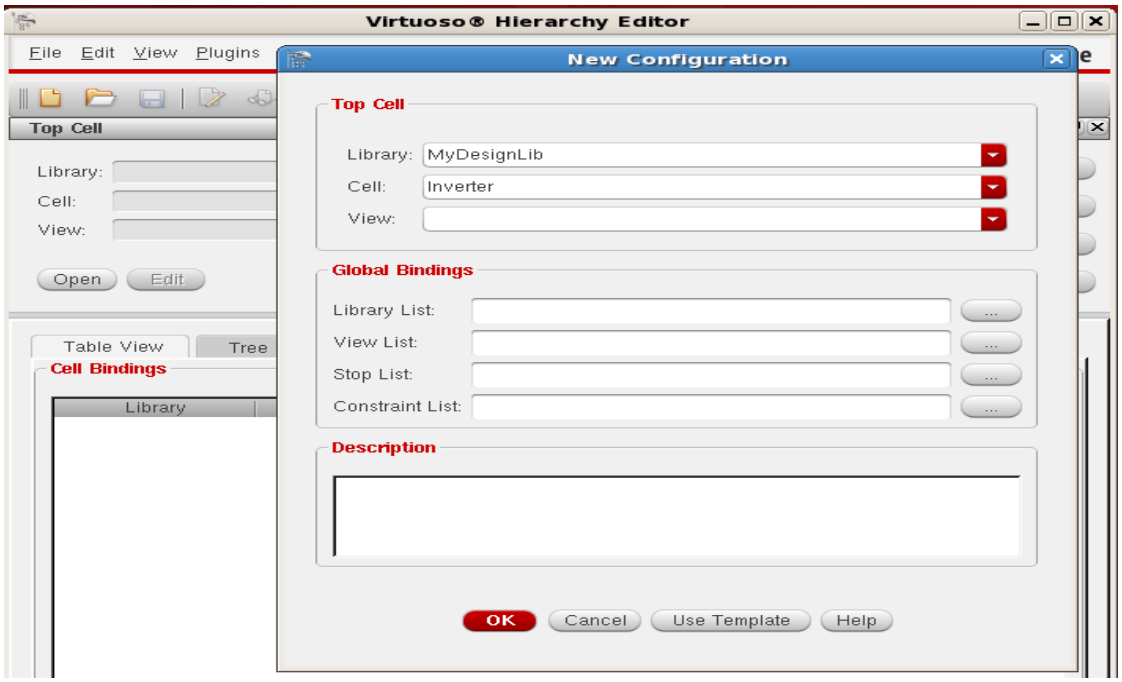
In this section we will create a config view and with this config view we will run the simulation with parasitic components.

1. In the CIW or Library Manager, execute **File – New – Cellview.**

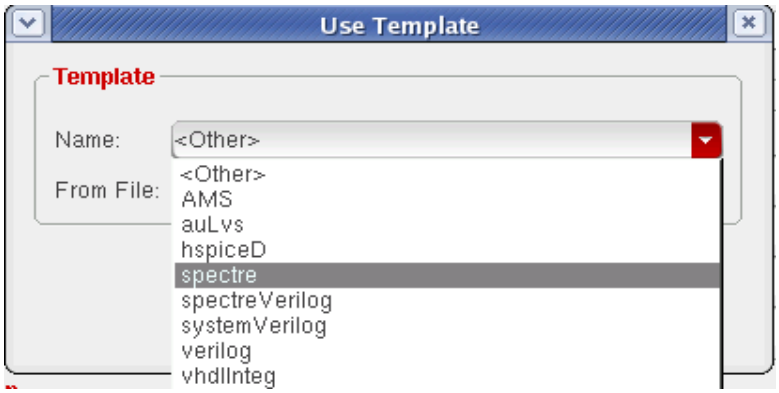
2. In the Create New file form, set the following:



3. Click **OK** in create **New File** form. The "**Hierarchy Editor"** form opens and a "**New Configuration"** form opens in front of it.

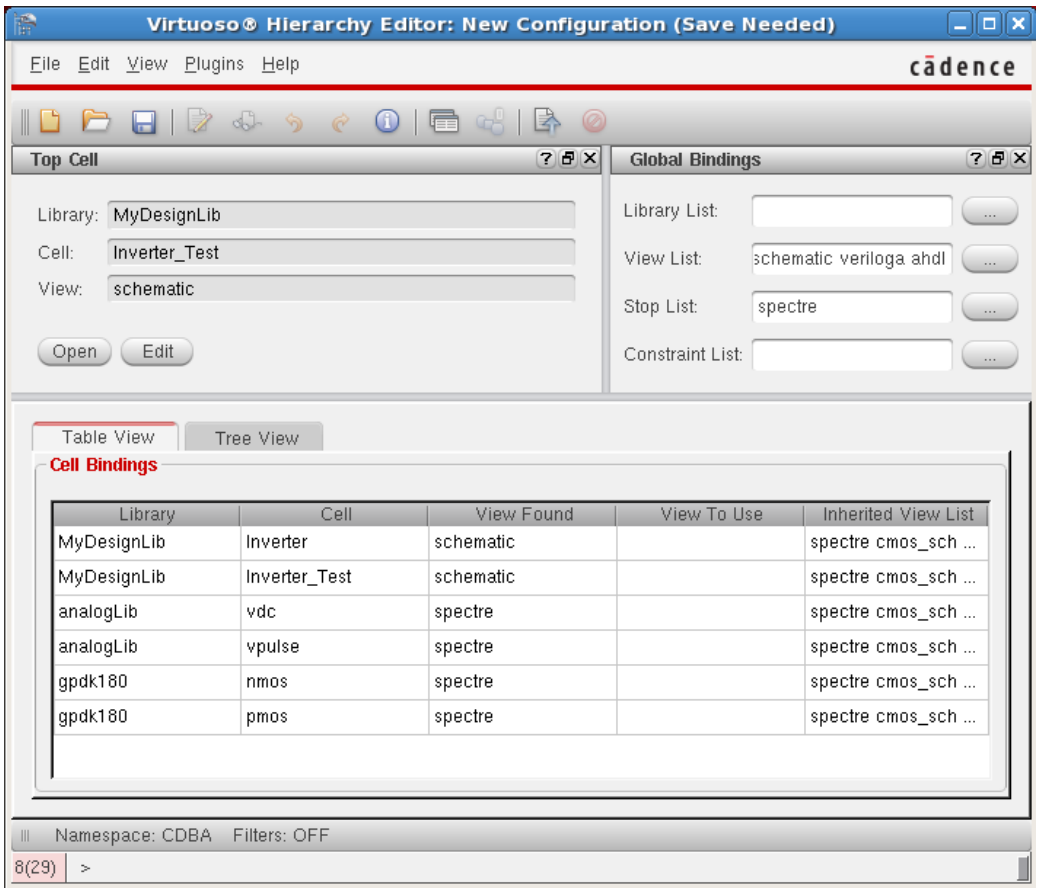


4. Click **Use template** at the bottom of the **New Configuration** form and select **Spectre** in the cyclic field and click **OK**.

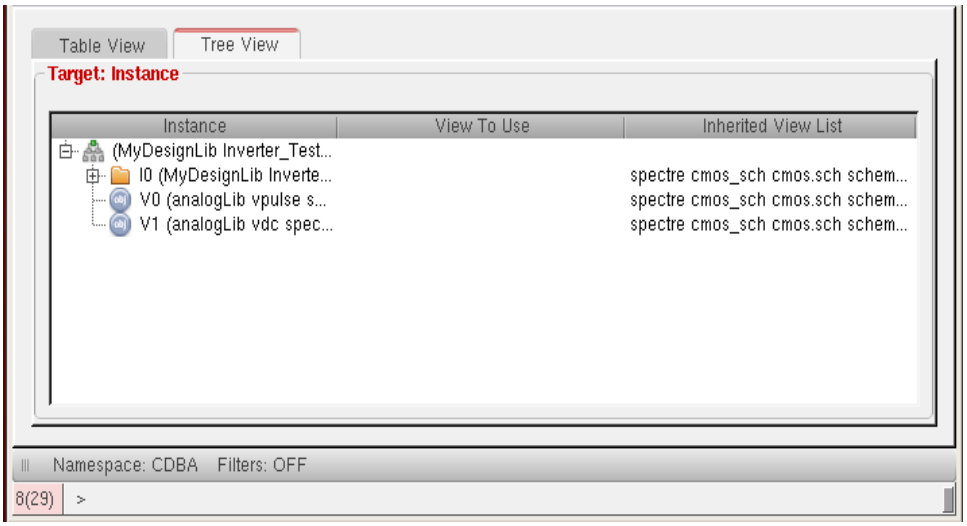


5. Change the **Top Cell - View** to **schematic** and remove the default entry from the **Library List** field and Click **OK** in the New Configuration form.

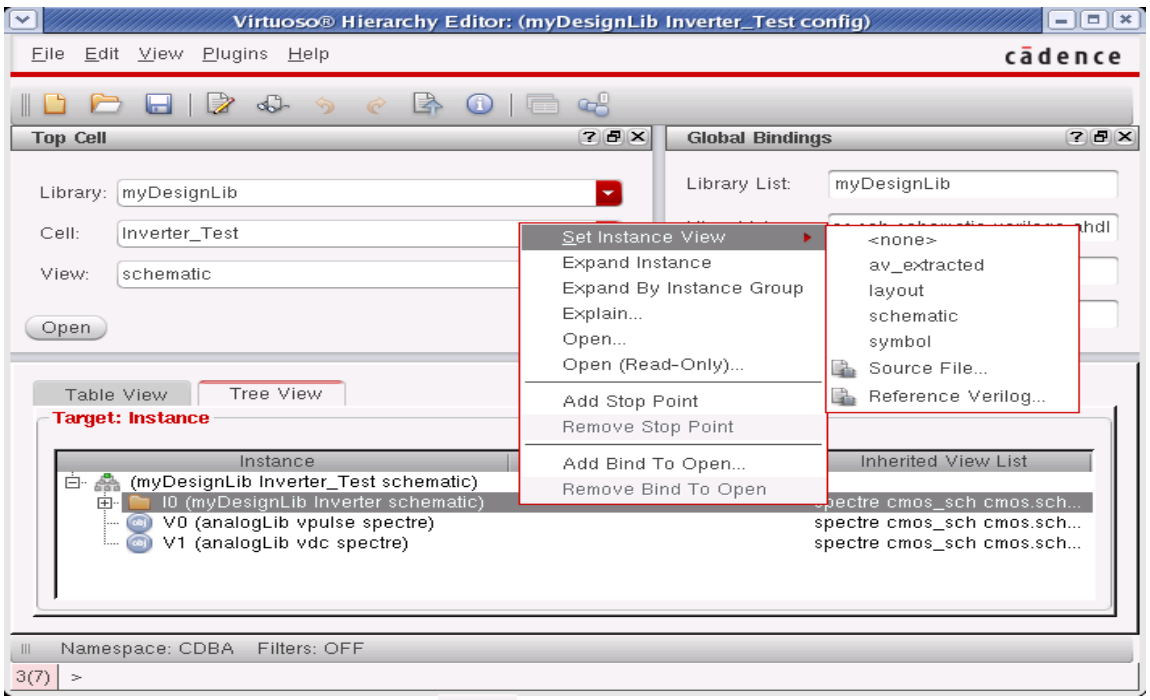
The hierarchy editor displays the hierarchy for this design using table format.



6. Click the **Tree View** tab. The design hierarchy changes to tree format. The form should look like this



7. Click on the **I0 (MyDesignLib..)** folder icon and click right, a set of option arises, click on **Set Instance View** and choose **av_extracted.**



8. **Save** the current configuration  and Close the Hierarchy Editor window. Execute **File – Close Window**.

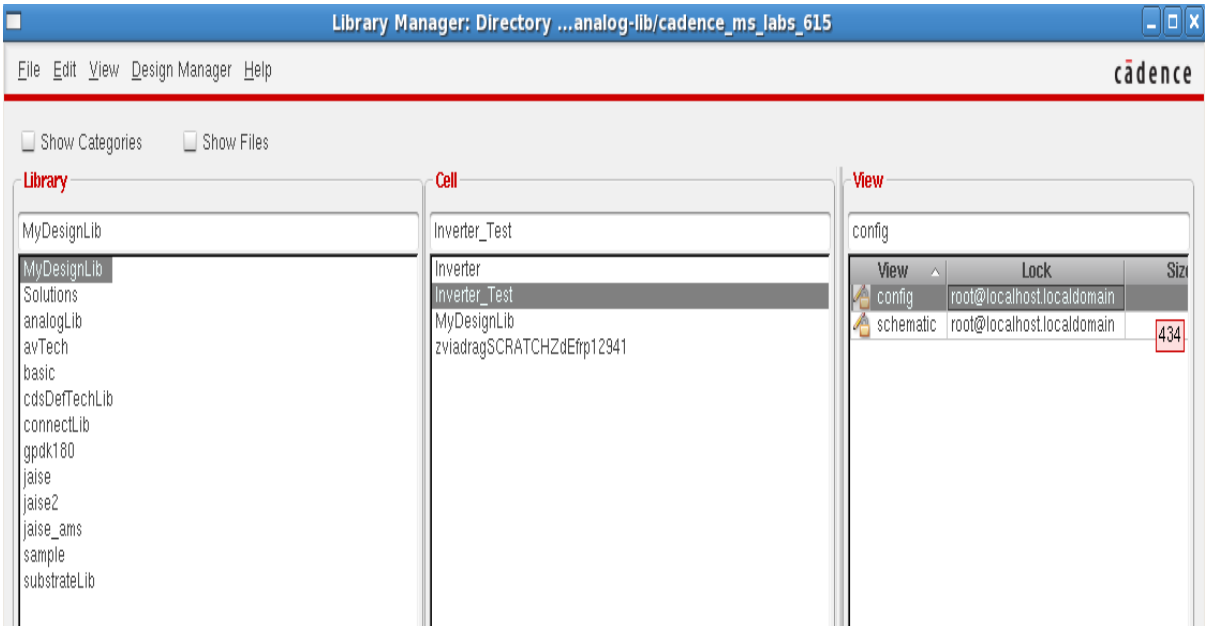
9. From CIW, execute **Tools – Library Manager.**

10. In the **library Manager** window, select the following

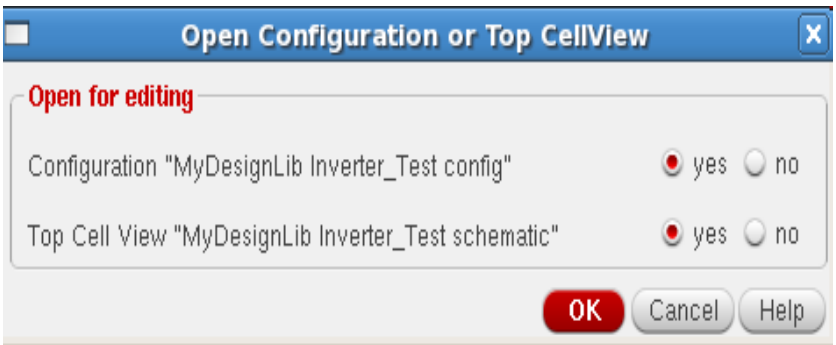
Library → **MyDesignLib**

Cell → **Inverter_Test**

Double click on **config** under **View**



11. A new **"Open Configuration or Top CellView"** form appears. Choose **yes** in both the cyclic fields and click **OK**.



The Inverter_Test schematic and Inverter_Test config window appears. Notice the window banner of schematic also states **Config: MyDesignLib Inverter_Test config.**

Simulation of config view with Spectre

1. Execute **Launch – ADE L** from the schematic window.

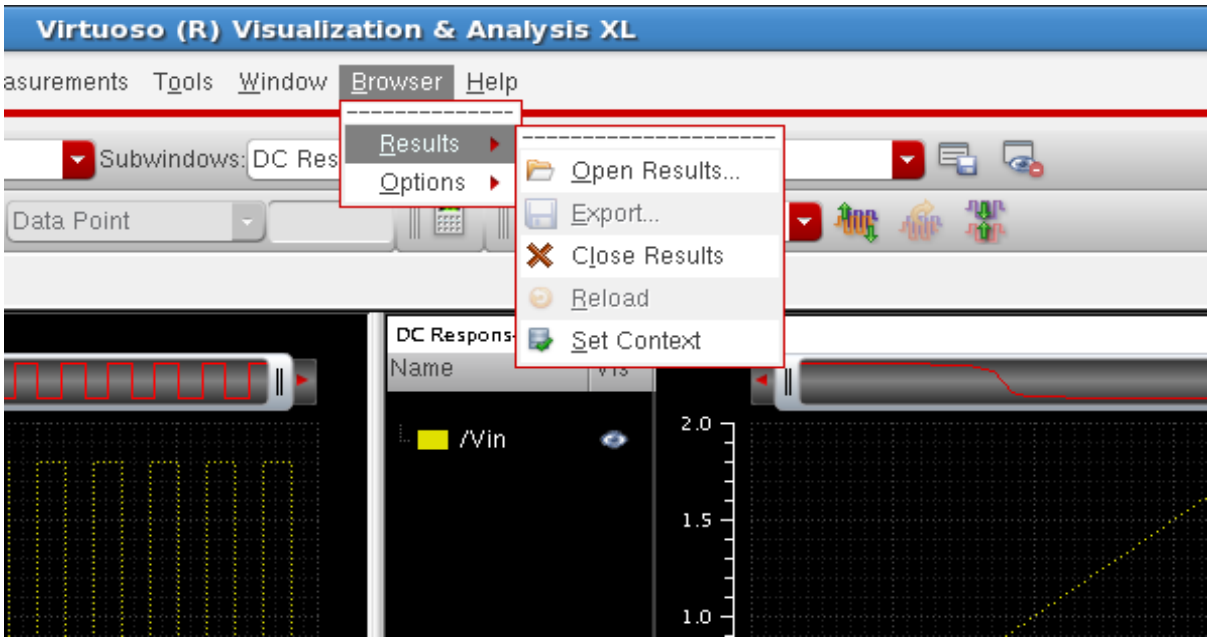
2. Now you need to follow the same procedure for running the simulation. Executing **Session–Load state,** the Analog Design Environment window loads the previous state.

3. Click **Netlist and Run** icon to start the simulation. 

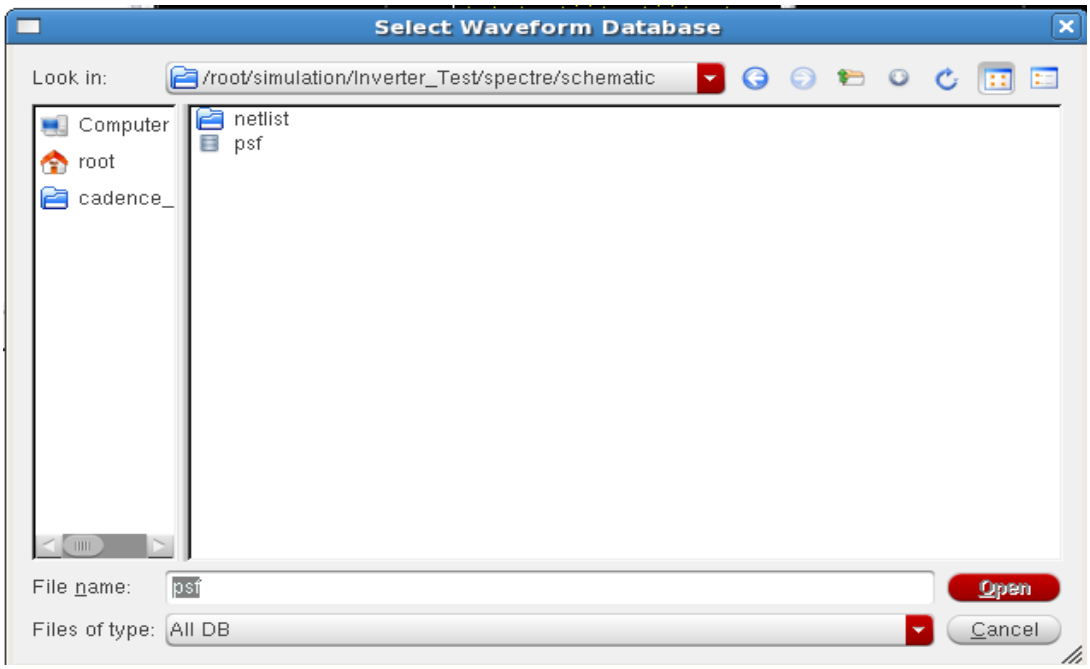
The simulation takes a few seconds and then waveform window appears.

Measuring Power, Voltage and Current Level

1. In the waveform window, execute **Browse – Results –Open results.**

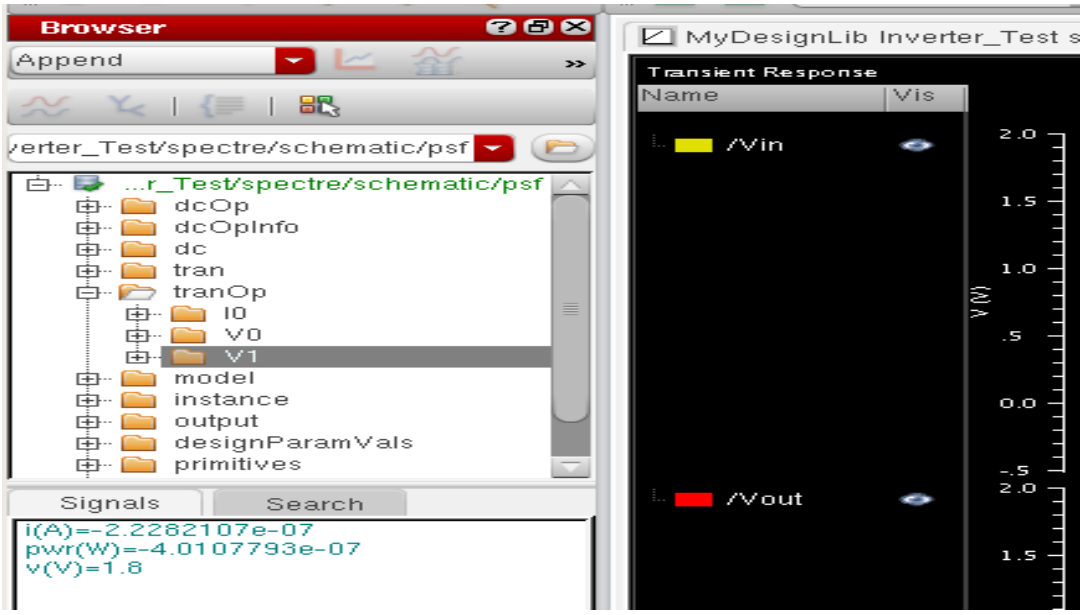


2. A **"Select Waveform Database"** form appears. Double click on the psf option.



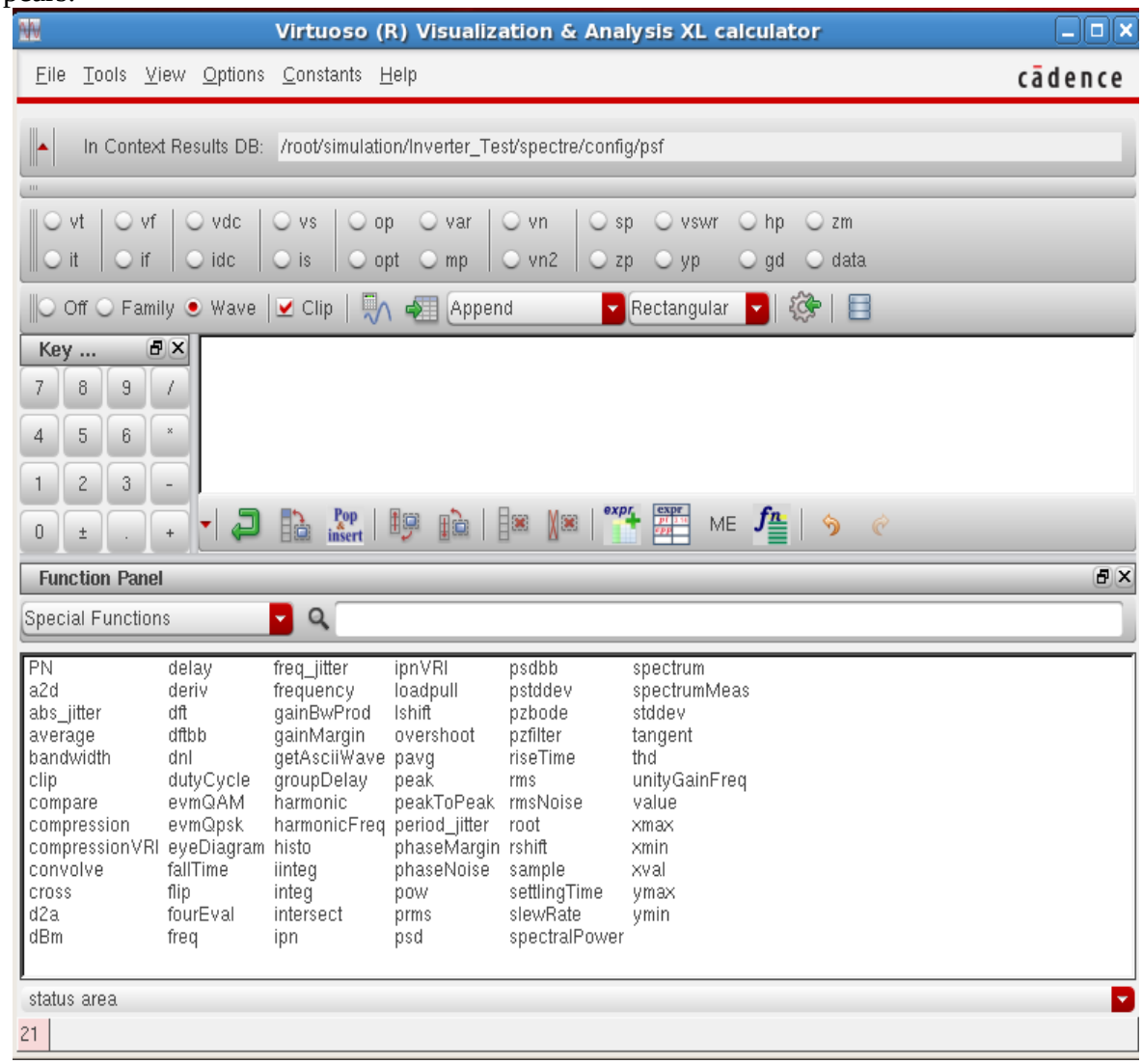
3. A **Brower** form appears on left side of the waveform window. Open **tranOp – V1** (supply signal).

We can find the values for current, power and voltage level under **signals** field below browser form.



Measuring the Propagation Delay

1. In the waveform window execute **Tools – Calculator.**  The calculator window appears.



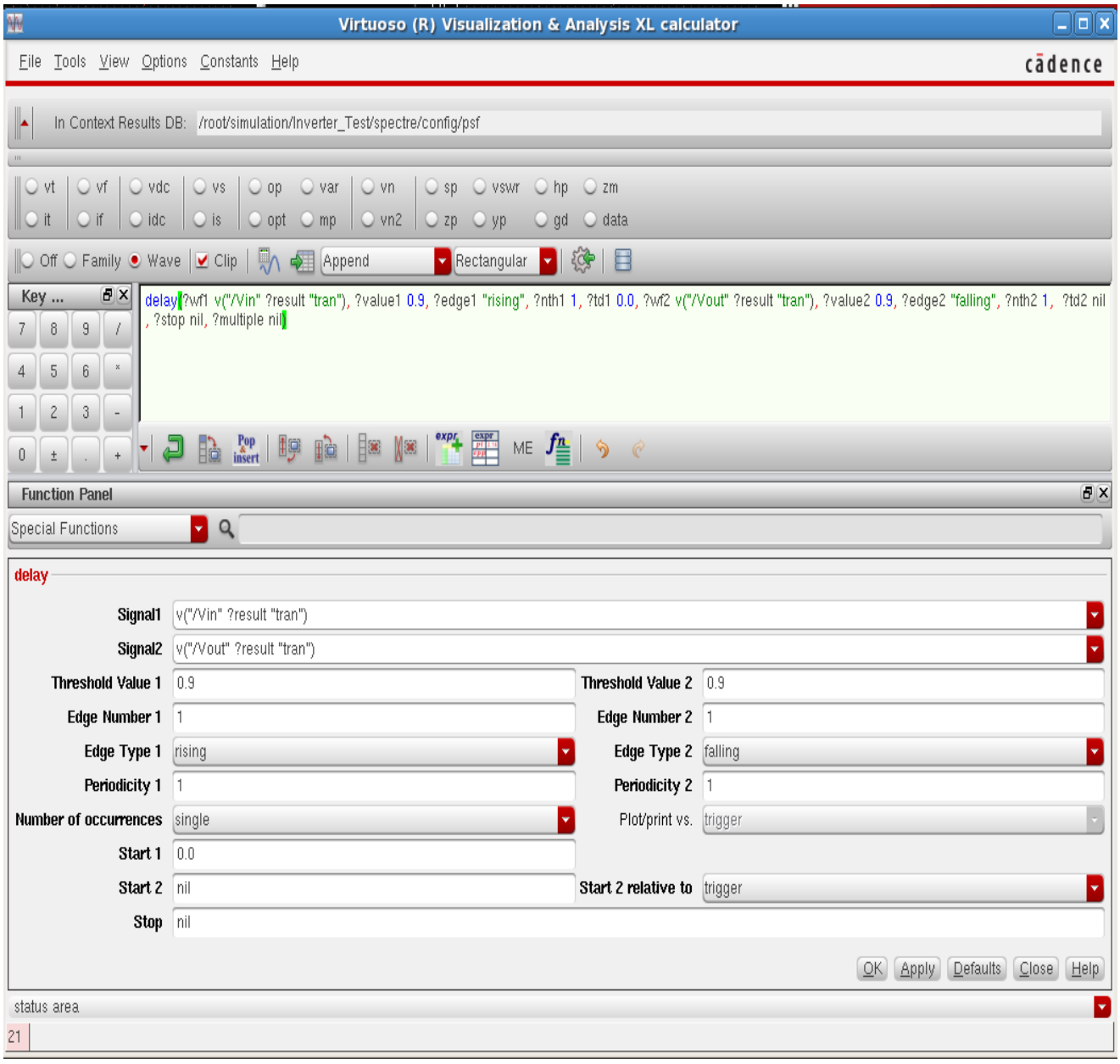
2. From the functions select **delay,** this will open the delay data panel.

3. Place the cursor in the text box for Signal1, select the **wave** button and select the input waveform from the waveform window.

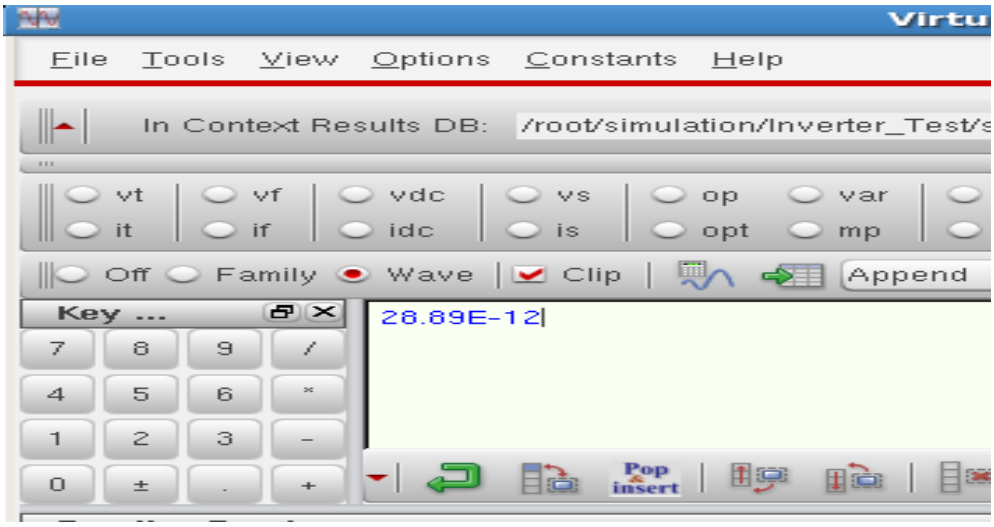
4. Repeat the same for Signal2, and select the output waveform.

5. Set the **Threshold value 1** and **Threshold value 2** to 0.9; this directs the calculator to calculate delay at 50% i.e. at 0.9 volts.

6. Execute **OK** and observe the expression created in the calculator buffer.



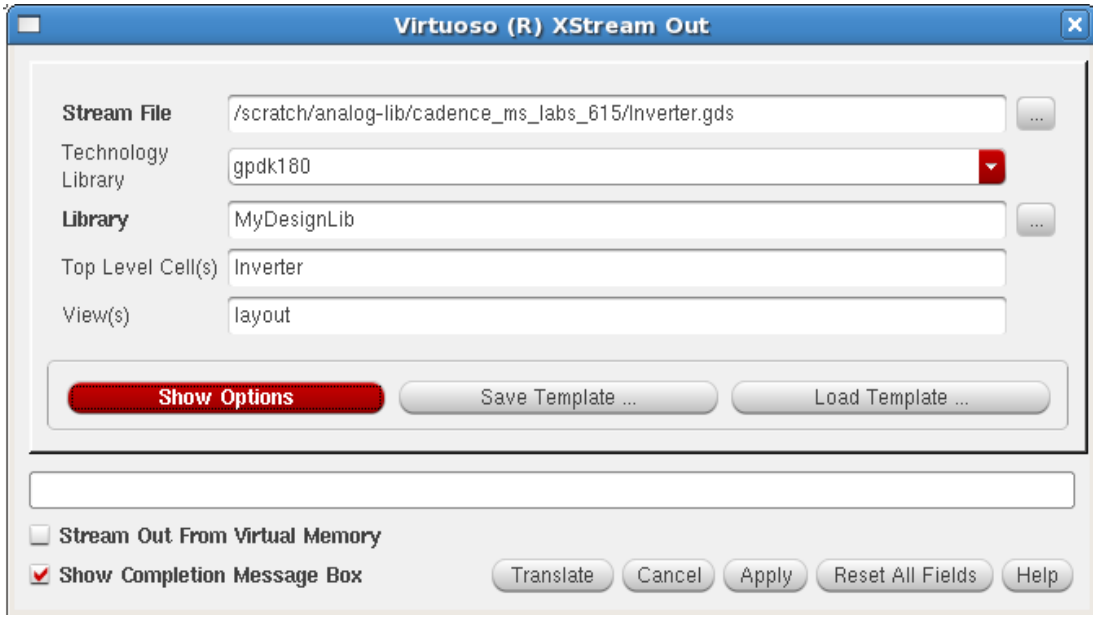
7. Click on **Evaluate the buffer icon**  to perform the calculation, note down the value returned after execution and close the window.



Generating Stream Data

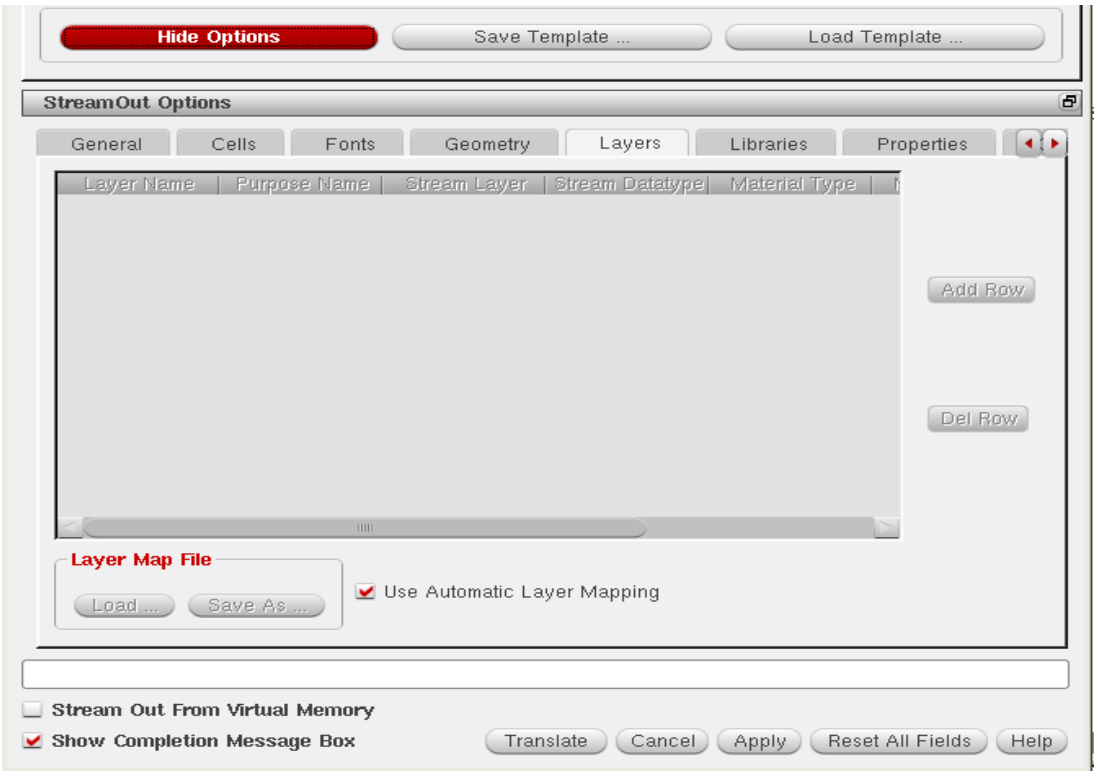
Streaming Out the Design

1. Select **File – Export – Stream** from the **CIW** menu and **Virtuoso Xstream Out** form appear. Make changes in Xstream Out window as show below.



1. Click the **Show Options** field.

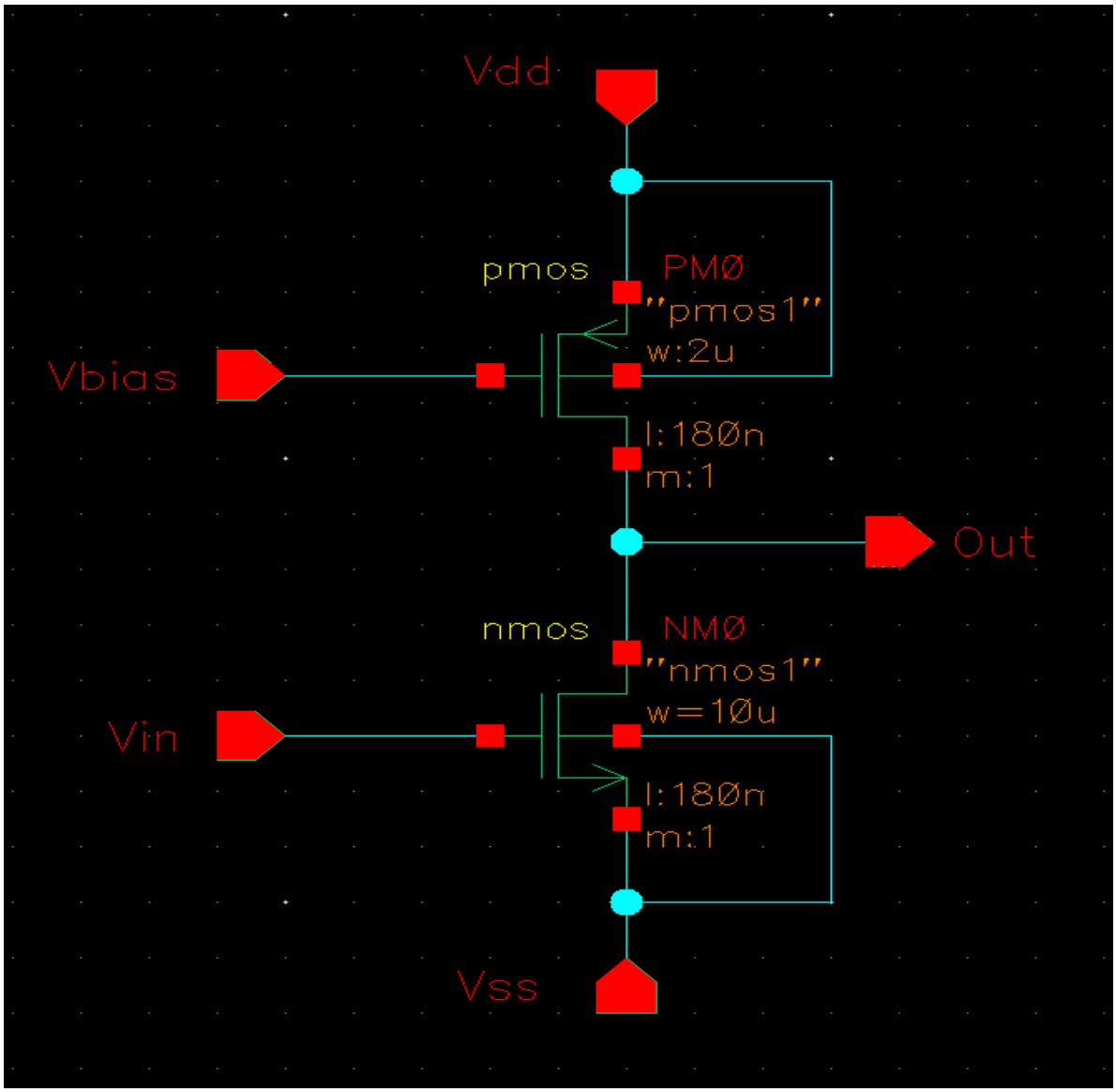
2. Click the **layers** field and enable **Use Automatic Layer Mapping** option.



3. Click **Translate** option and the generation of stream out for inverter starts.
4. The stream out will be ready in a few seconds with the log the log file.
5. The stream out file for inverter can be viewed by opening the file from its location using **vi Editor**.

Lab 2: CS Amplifier in CIC Flow

Schematic Capture



Schematic Entry

Objective:To create a schematic view for Common Source amplifier

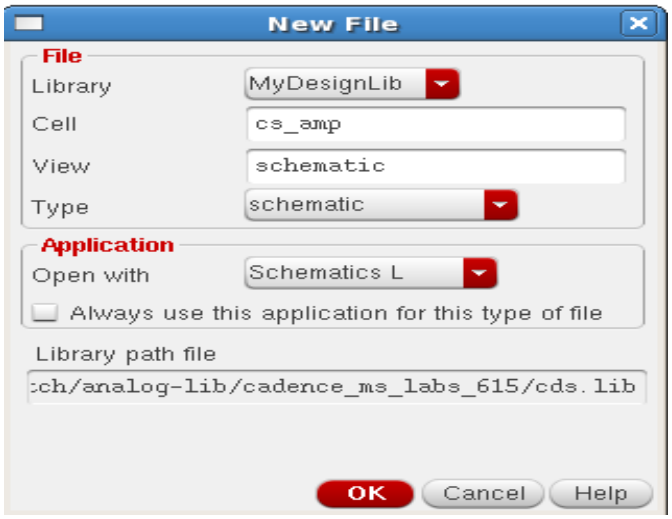
We create the cellview for Comon Source Amplifier in same directory **MyDesignLib,** which we created for Inverter

Creating a Schematic Cellview

In this section we will learn how to open new schematic window in the "**MyDesignLib**" library and build the schematic for CS amplifier as shown in the figure at the start of this lab.

1. In the CIW or Library manager, execute **File – New – Cellview**.

2. Set up the **"New File"** window as follows:

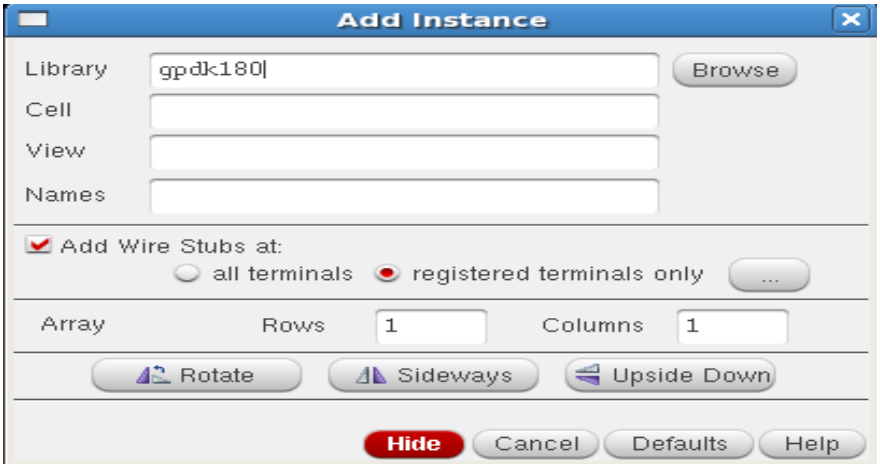


Note: Do not edit the Library path file and the one above might be different from the path shown in your window.

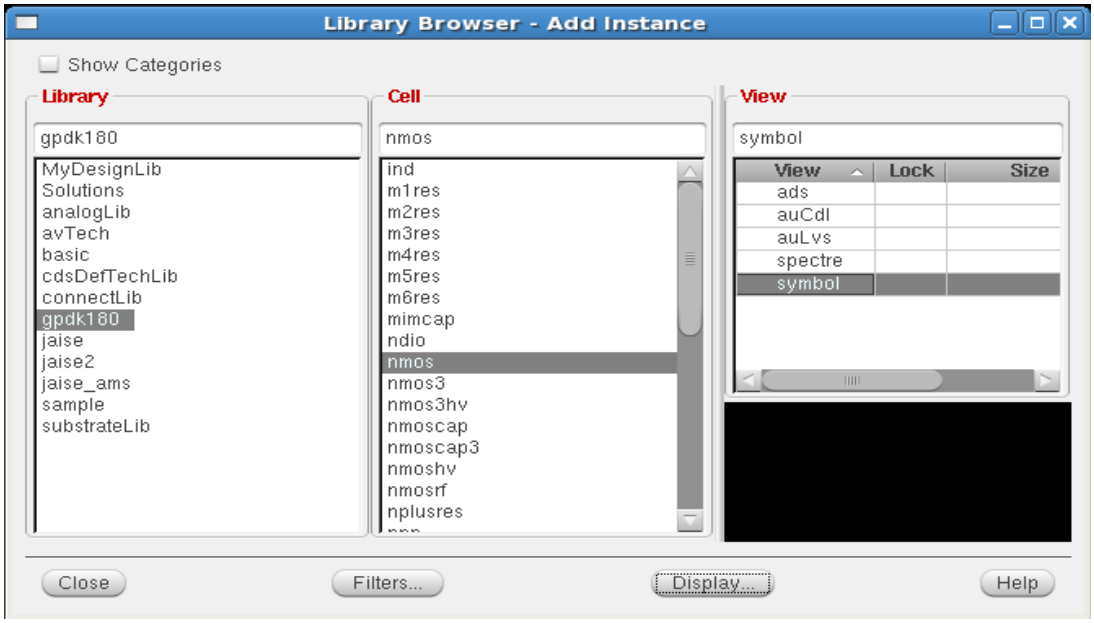
3. Click **OK** when done the above settings. A blank schematic window for the **cs_amp** design appears.
Note: Make sure the Library name is same as what we created earlier, **"MyDesignLib".**

Adding Components to schematic

1. In the cs_amp schematic window, click the **Instance** fixed menu icon  to display the Add Instance form.
Tip: You can also execute **Create — Instance** or press **i**.

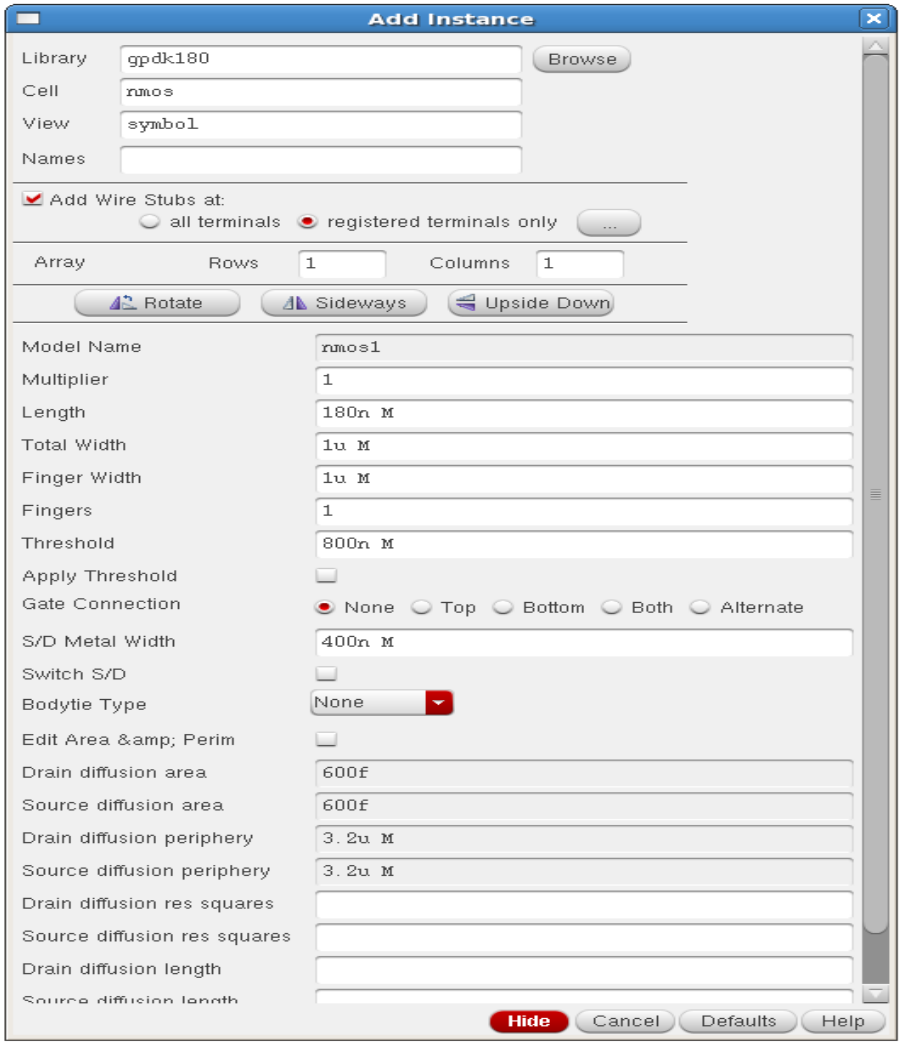


2. Click on the **Browse** button. This opens up a Library browser from which you can select components and the **symbol** view.



You will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.

Instantiating the nmos symbol is shown below as an example



3. After you complete the Add Instance form, move your cursor to the Schematic window and **left click** to place a component.

4. After entering components, click **Cancel** in the Add Instance form or press ***Esc***.
This is a table of components for building the cs_amp schematic.

Library name	Cell Name	Properties
gpdk180	pmos	Total Width= 2u, Length=180n
gpdk180	nmos	Total Width = 10u, Length=180n

If you place a component with the wrong parameter values, use the **Edit— Properties— Objects** command to change the parameters.

Use the **Edit— Move** command if you place components in the wrong location.

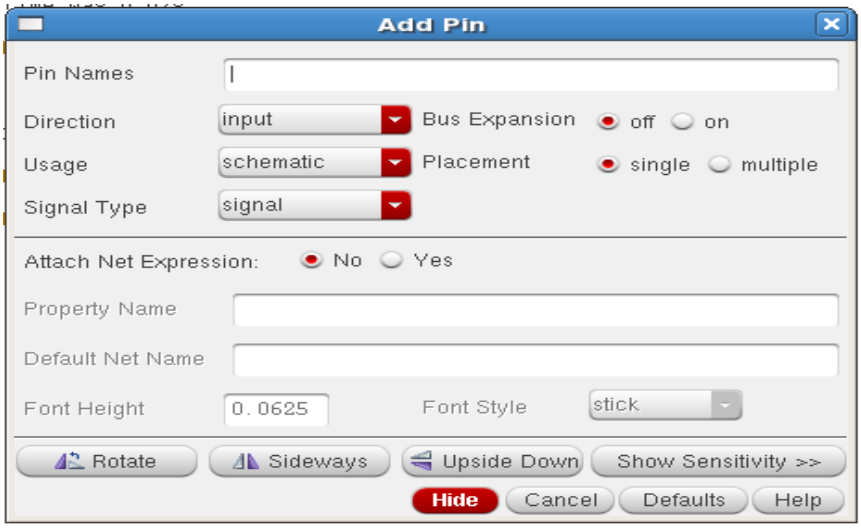
You can rotate components at the time you place them, or use the **Edit— Rotate** command after they are placed.

Adding pins to Schematic

1. Click the **Pin** fixed menu icon in the schematic window. 

Tip: You can also execute **Create — Pin** or press **p**.

The Add pin form appears.



2. Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Names	Direction
Vin, Vbais, Vdd, Vss	input
Out	output

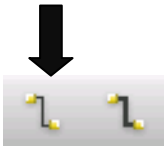
Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to **schematic**.

3. Select **Cancel** from the Add – pin form after placing the pins.

In the schematic window, execute **Window— Fit** or press **f** to fit all the components to the schematic editor window.

Adding Wires to a Schematic

Add wires to connect components and pins in the design.



1. Click the **Wire (narrow)** icon in the schematic window.

Tip: You can also press the **w** key, or execute **Create — Wire (narrow).**

2. In the schematic window, click on a pin of one of your components as the first point for your wiring. A diamond shape appears over the starting point of this wire.

3. Follow the prompts at the bottom of the design window and **left click** on the destination point for your wire. A wire is routed between the source and destination points.

4. Complete the wiring as shown in figure and when done wiring press ***Esc*** key in the schematic window to cancel wiring.

Note: A single node cannot have more than 3 branches.

Saving the Design

1. Click the **Check and Save** icon in the schematic editor window.

2. Observe the CIW output area for any errors.

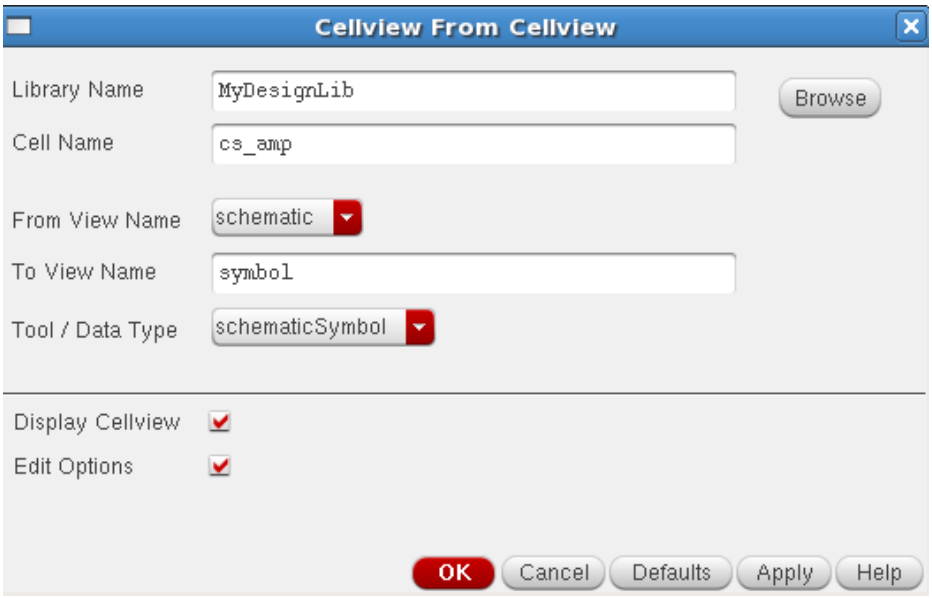
Symbol Creation

Objective: To create a symbol for the cs_amp

In this section, you will create a symbol for your cs_amp design so you can place it in a test circuit for simulation. A symbol view is extremely important step in the design process. The symbol view must exist for the schematic to be used in a hierarchy. In addition, the symbol has attached properties (cdsParam) that facilitate the simulation and the design of the circuit.

1. In the cs_amp schematic window, execute **Create — Cellview— From Cellview**.

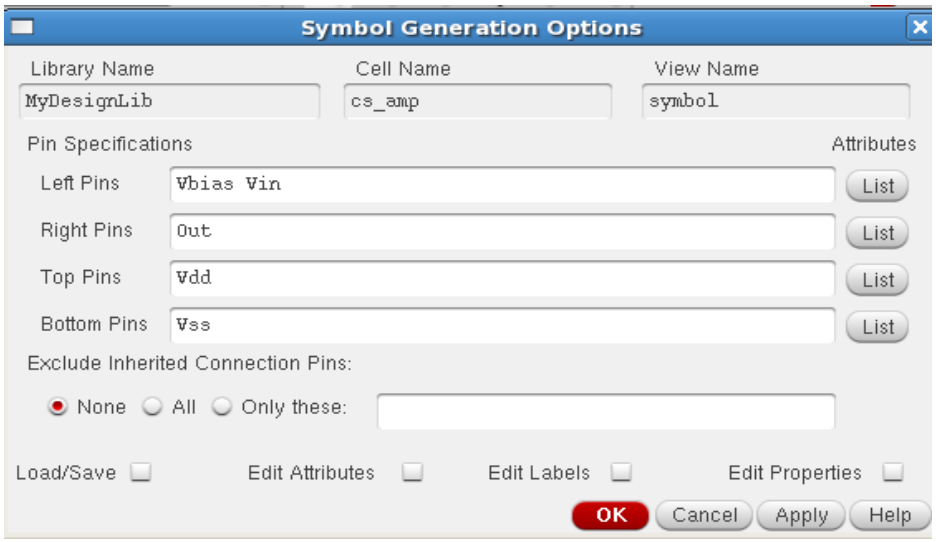
The "**Cellview From Cellview"** window appears. With the Edit Options function active, you can control the appearance of the symbol to generate.



2. Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **schematicSymbol**.

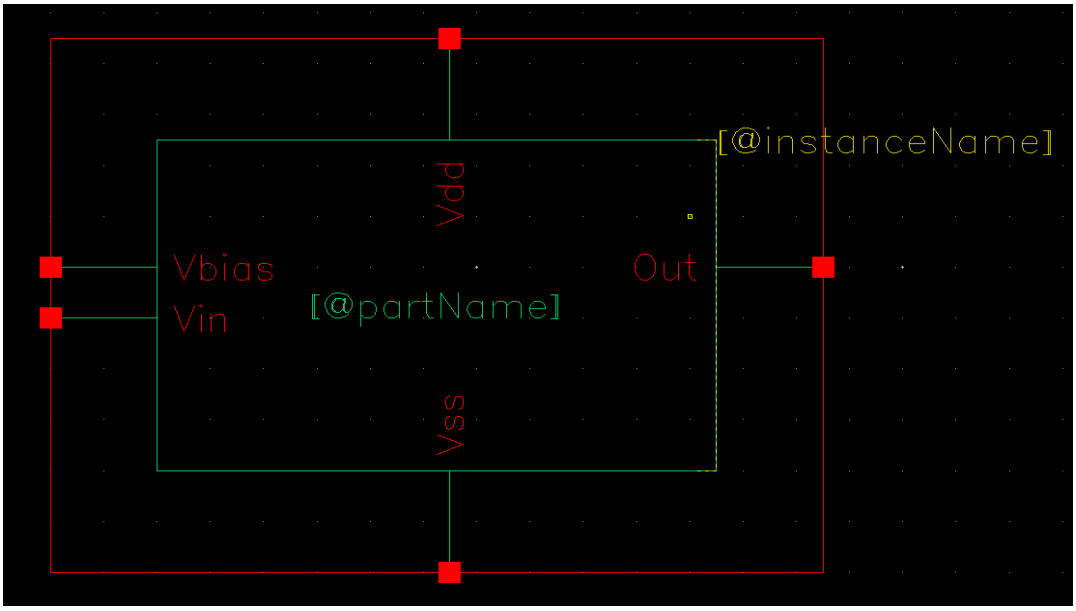
3. Click **OK** in the **"Cellview From Cellview"** form.

4. The **"Symbol Generation options"** window appears. Arrange the pins the way the symbol should have them.



5. Click **OK** in the **"Symbol Generation Options"** form.

6. A new window displays with an automatically created Cs_amp symbol as shown here.



Editing a Symbol

In this section we will modify the cs_amp symbol to look like an cs_amp gate symbol.

1. Move the cursor over the automatically generated symbol, until the green rectangle is highlighted, **left click** to select it.

2. Click **Delete** icon in the symbol window, similarly select and delete the outer red rectangle.

3. Execute **Create – Shape – polygon**, and draw a shape similar to triangle.

4. After creating the triangle press ***Esc*** key.

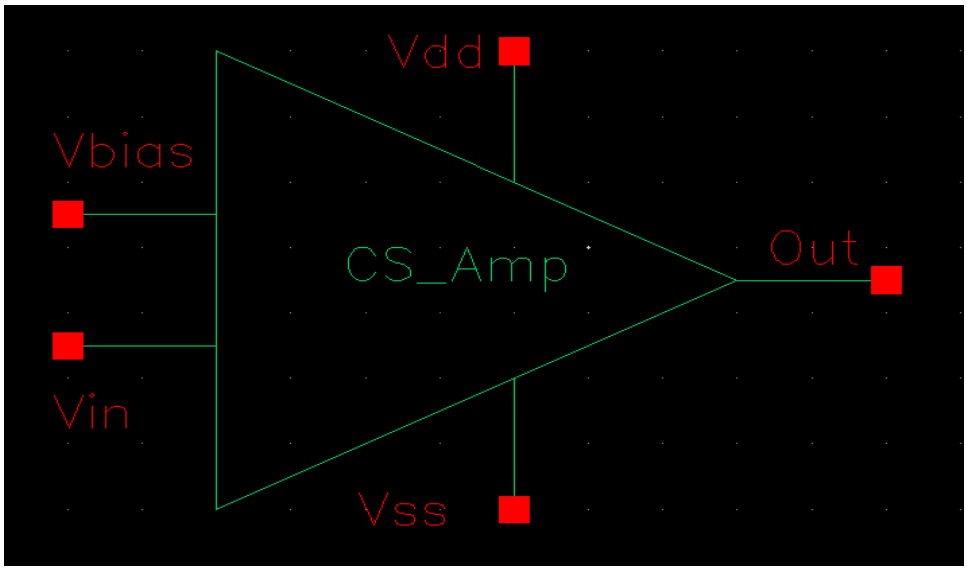
5. Execute **Create – Shape – Circle** to make a circle at the end of triangle.

6. You can move the pin names according to the location.

7. Execute **Create – Selection Box**. In the Add Selection Box form, click **Automatic**. A new red selection box is automatically added.

8. After creating symbol, click on the **save** icon in the symbol editor window to save the symbol.

9. In the symbol editor, execute **File – Close** to close the symbol view window.



Building the Test Design

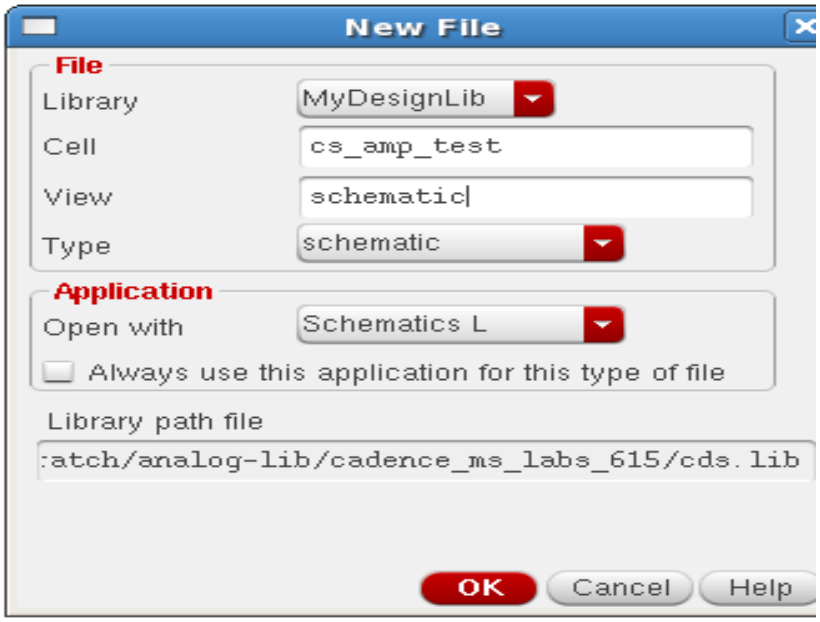
Objective: To build a test circuit using cs_amp symbol

We will create the **cs_amp_test** cellview that will contain an instance of the cs_amp cellview.

1. In the CIW or Library Manager, execute **File – New – Cellview**.

2. Set up the **New File** form as shown.

3. Click **OK** when done. A blank **Schematic Editor** window for the **cs_amp_test** design appears.



Building the Circuit

1. Using the component list and Properties/Comments in this table, build the **cs_amp_test** schematic.

Library name	Cellview name	Properties
MyDesignLib	cs_amp	Symbol
analogLib	Vsin (for Vin)	AC Magnitude= 1; DC Voltage= -1.8; Offset Voltage= 0; Amplitude= 5m; Frequency= 1K
analogLib	Vdc	DC Voltage = 2.5 (for Vdd) DC Voltage = -2.5 (for Vss) DC Voltage = 1 (for Vbias)
analogLib	gnd	

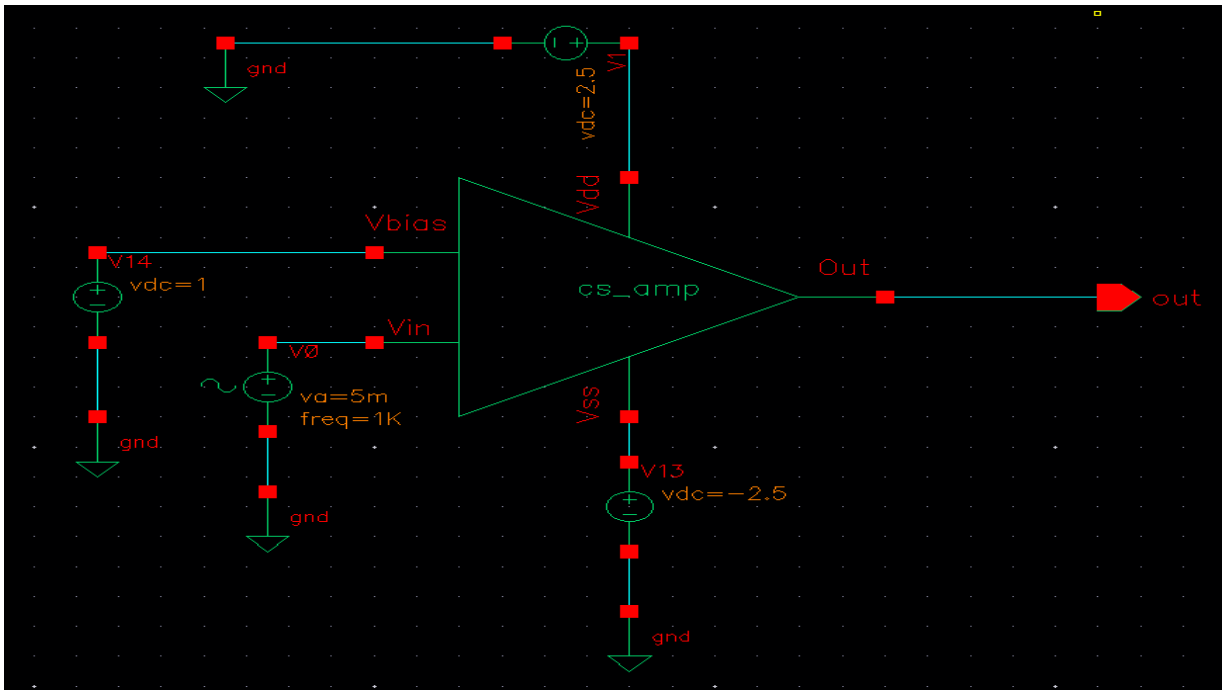
2. Add the above components using **Create — Instance** or by pressing **i**. 

3. Click the **Wire (narrow)** icon and wire your schematic. 

4. Click **Create — Wire Name** or press **L** to name the input **(Vin)** and output **(Vout)** wires as in the below schematic. 

5. Click on the **Check and Save** icon to save the design. 

6. Leave your **cs_amp_test** schematic window open for the next section.



Analog Simulation with Spectre

Objective: To set up and run simulations on the cs_amp_test design

In this section, we will run the simulation for CS Amplifier and plot the transient; DC characteristics and we will do Parametric Analysis after the initial simulation.

Starting the Simulation Environment

1. In the **cs_amp_test** schematic window, execute **Launch – ADE L**
The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

Choosing a Simulator

Set the environment to use the **Spectre® tool**, a high speed, highly accurate analog simulator. Use this simulator with the **cs_amp** design, which is made-up of analog components.

1. In the simulation window (ADE), execute **Setup— Simulator/Directory/Host**.

2. In the Choosing Simulator form, set the Simulator field to **Spectre** (Not spectreS) and click **OK**.

Setting the Model Libraries

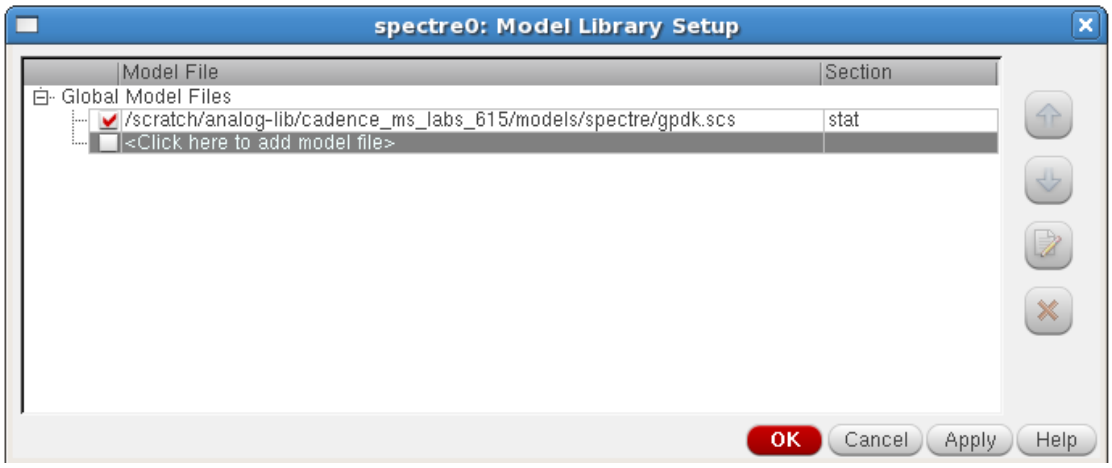
The Model Library file contains the model files that describe the nmos and pmos devices during simulation.

1. In the simulation window (ADE L), execute **Setup - Model Libraries.**

The Model Library Setup form appears. Click the **browse** button  to add **gpdk.scs** if not added by default as shown in the **Model Library Setup** form.

Remember to select the section type as **stat** in front of the gpdk.scs file.

The Model Library Setup window should looks like the figure below.



To view the model file, highlight the expression in the **Model Files** field and Click **Edit File**.

2. To complete the Model Library Setup, move the cursor and click **OK.**

Choosing Analysis

This section demonstrates how to view and select the different types of analysis to complete the circuit when running the simulation.

1. In the Simulation window (ADE), execute **Analysis - Choose Analysis** or click the 

Choose - Analysis icon.

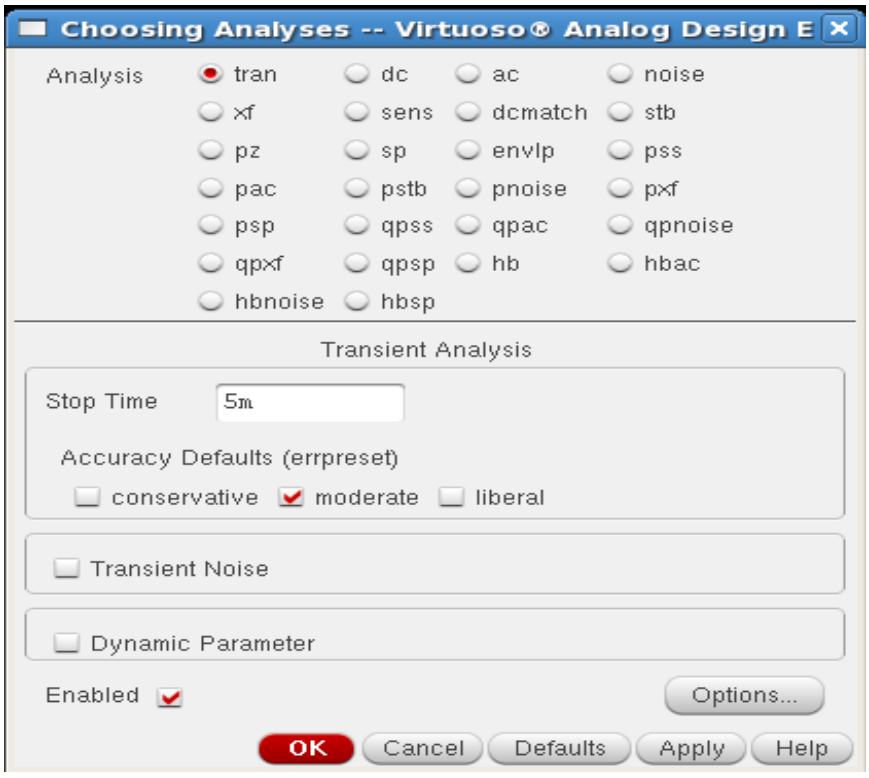
The Choosing Analysis form appears. This is a dynamic form, the bottom of the form changes based on the selection above.

2. To setup for transient analysis

   a. In the Analysis section select **tran**.

   b. Set the stop time as **5m**.

   c. Click at the **moderate** and **Enabled** buttons at the bottom, and then click **Apply**.



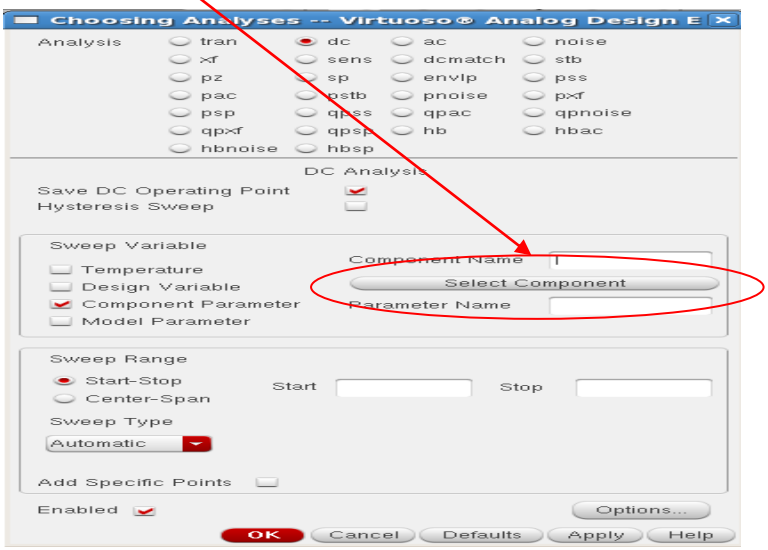
3. To set up for DC Analysis:

   a. In the Analysis section, select **dc**.

   b. In the DC Analysis section, turn on **Save DC Operating Point.**

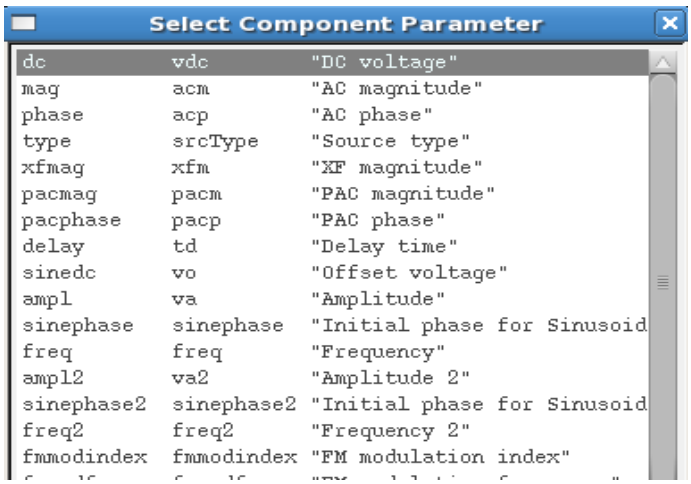
   c. Turn on the **Component Parameter**.

   d. Click the **Select Component**, Which takes you to the schematic window.



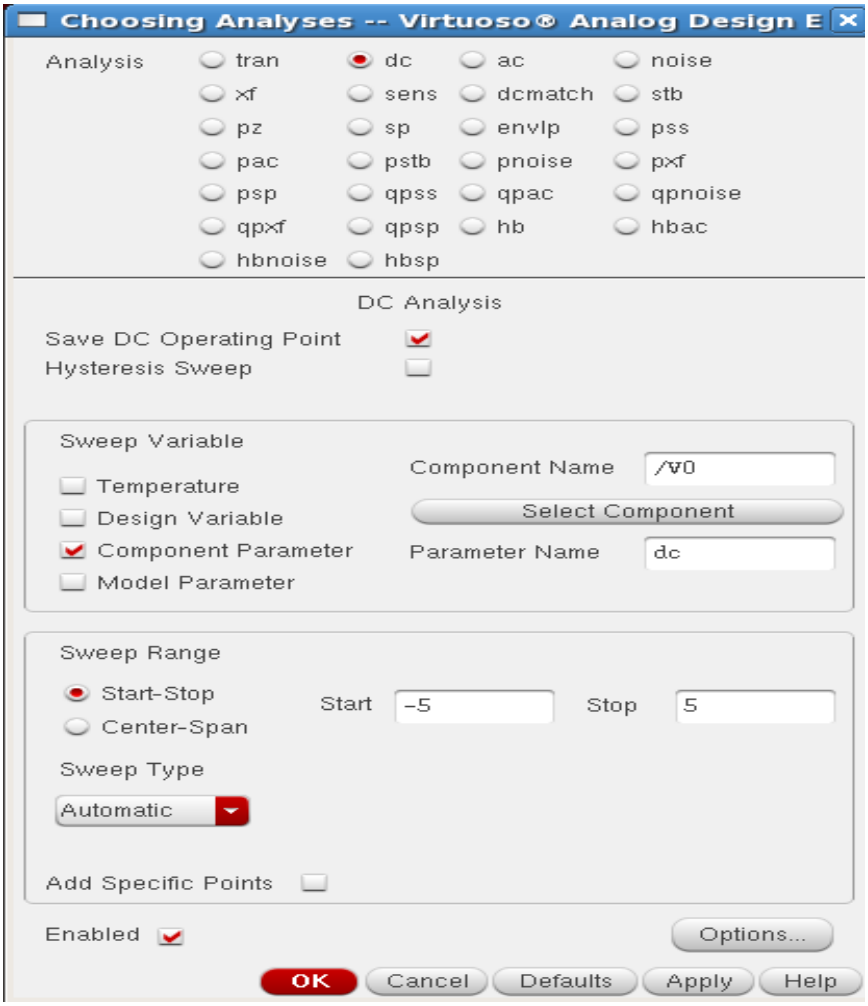
   e. Select input signal **vsin source** in the test schematic window.

   f. Select **DC Voltage** in the "**Select Component Parameter"** window and click **OK**.

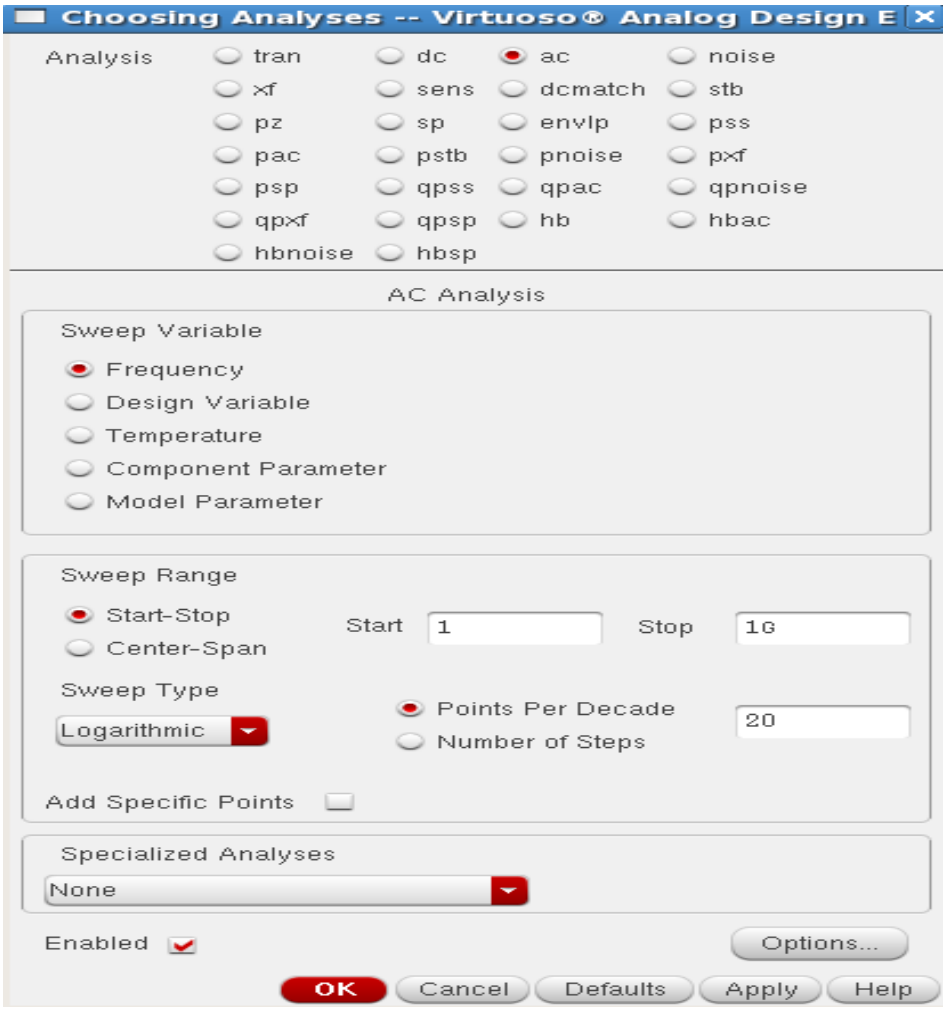


   g. In the analysis form, enter **start** and **stop** voltages as **-5** to **5** respectively.

   h. Check the enable button and then click **Apply.**



4. To Set up for **AC** analysis
    a. In the Analyses section, select **ac**.
    b. In the AC Analyses section, turn on **Frequency.**
    c. In the Sweep Range section select **start** and **stop** frequencies as **1** to **1G.**
    d. Select Sweep type as **Logarithmic** and set **Points Per Decade** as **20**.
    e. Check the enable button and then click **Apply**.



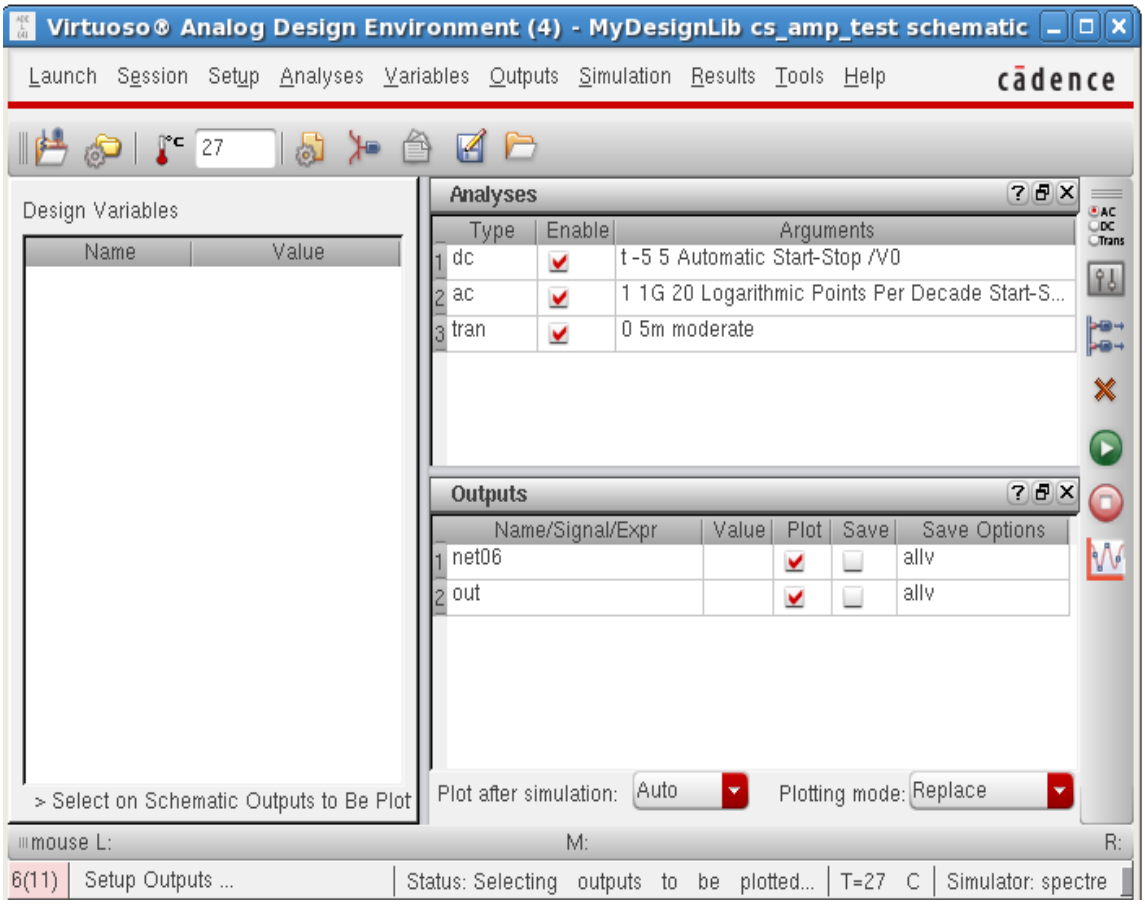
5. Click **OK** in the **Choosing Analysis** form.

Selecting Signals for Plotting

1. Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.

2. Follow the prompt at the bottom of the schematic window, Click on input and output net of the cs_amp_test. Press ***Esc*** with the cursor in the schematic after selecting it.

After setting the transient and DC analysis and also the signals for wave plotting, the ADE L window will look like the figure below.

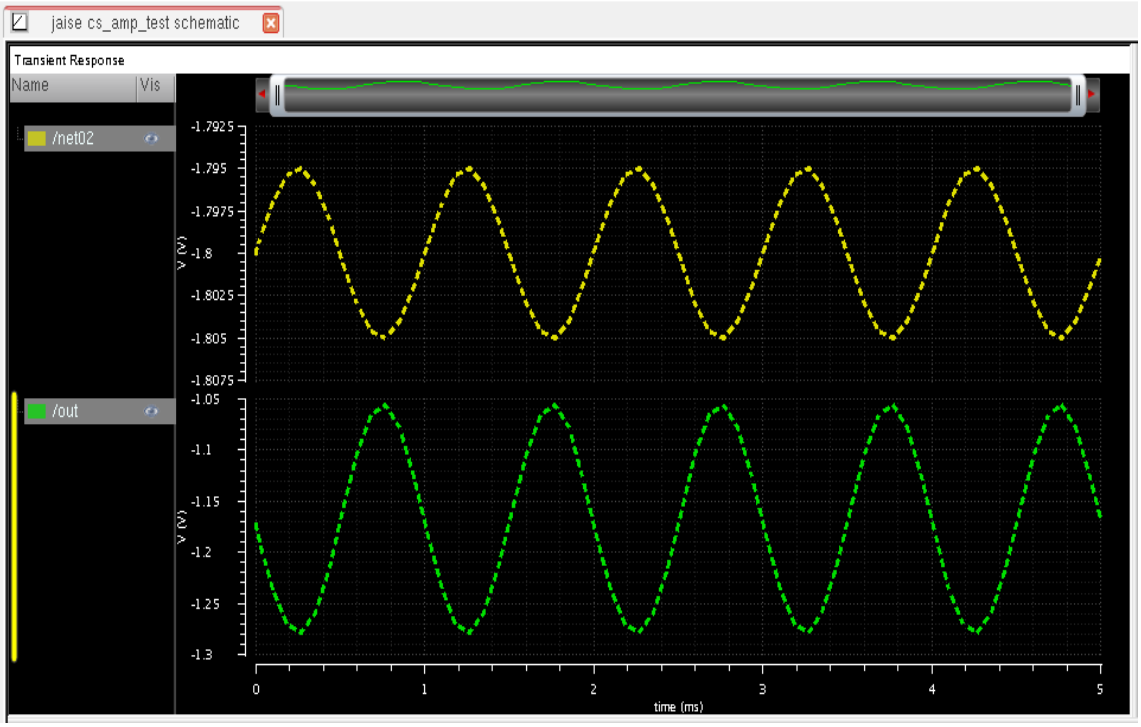


Running the Simulation

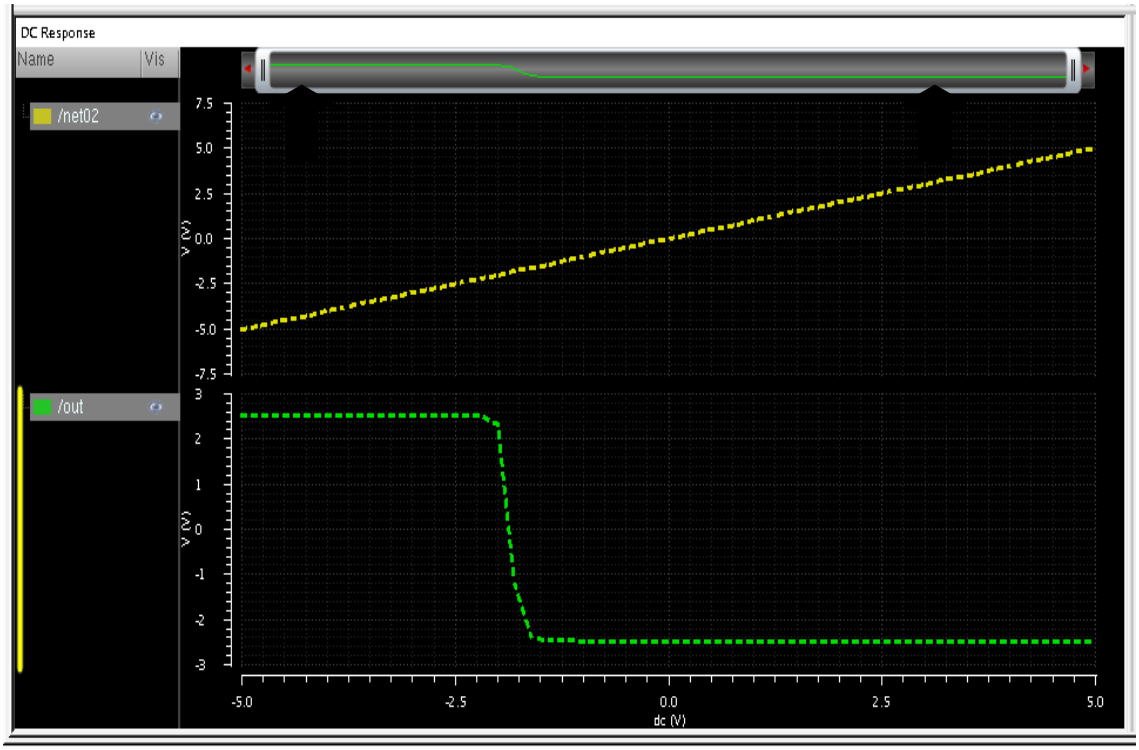
1. Execute **Simulation – Netlist and Run** in the simulation window to start the Simulation or the  **Netlist and Run** icon present in the ADE L window, this will create the netlist as well as run the simulation.

2. When simulation finishes, the Transient, DC plots automatically will be popped up along with log file.

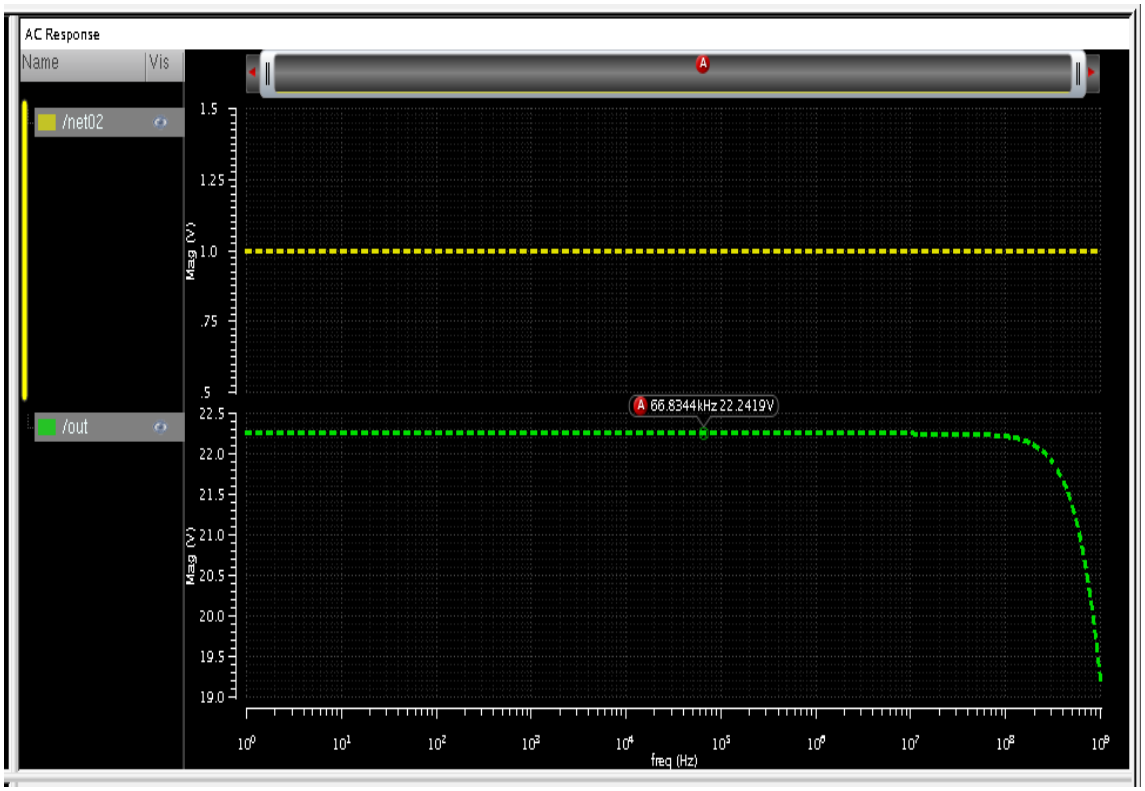
3. Click on the **Split Current Strip** icon  to separate the wave plots.



Transient Analysis



DC Analysis



AC Analysis

Saving the Simulator State

We can save the simulator state, which stores information such as model library file, outputs, analysis, variable etc. This information restores the simulation environment without having to type in all of setting again.

1. In the Simulation window, execute **Session – Save State**. The Saving State form appears.

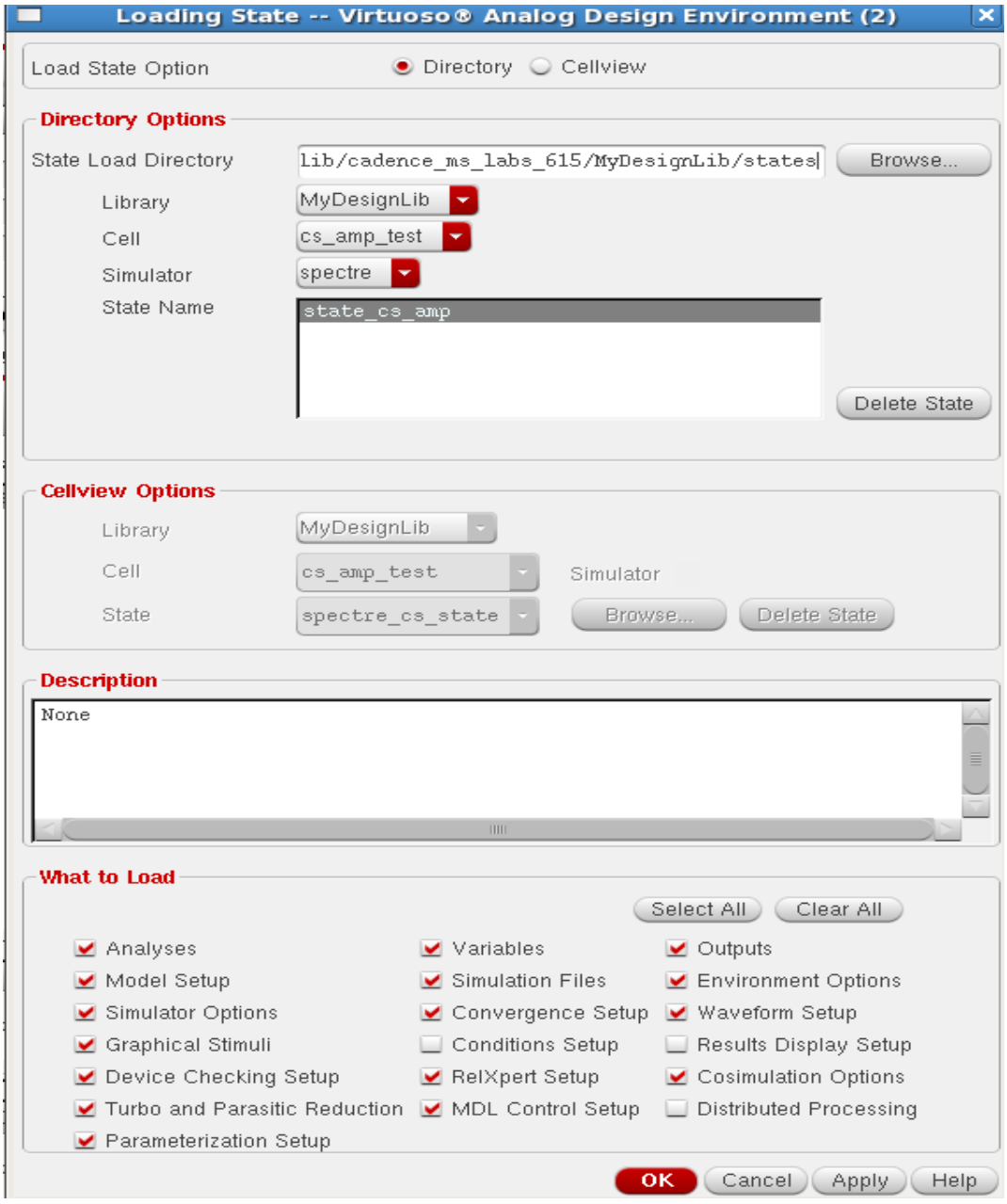
2. Set the **Save State Directory** field to the directory in which the state should be saved. Change the **Save as** field to **state_cs_amp** (any valid identifier) and make sure all options are selected under **What to save** field.

3. Click **OK** in the saving state form. The Simulator state is saved.

Loading the Simulator State

1. From the ADE window execute **Session – Load State.**

2. In the Loading State window, set the State name to **state_cs_amp** as shown



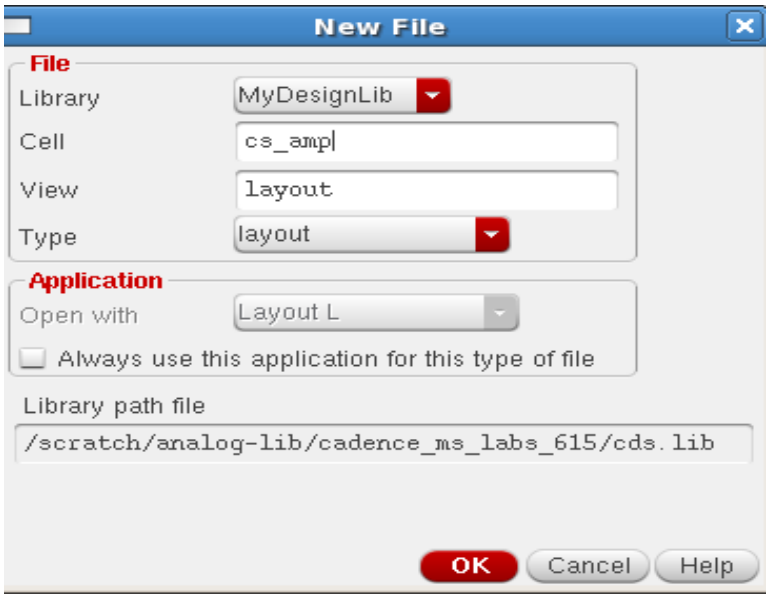
3. Click **OK** in the Loading State window.

Creating Layout View of cs_amp

1. From the **cs_amp** schematic window menu execute **Launch – Layout XL**. A "**Startup Option"** form appears.

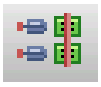
2. Select **Create New** option and click **OK.**

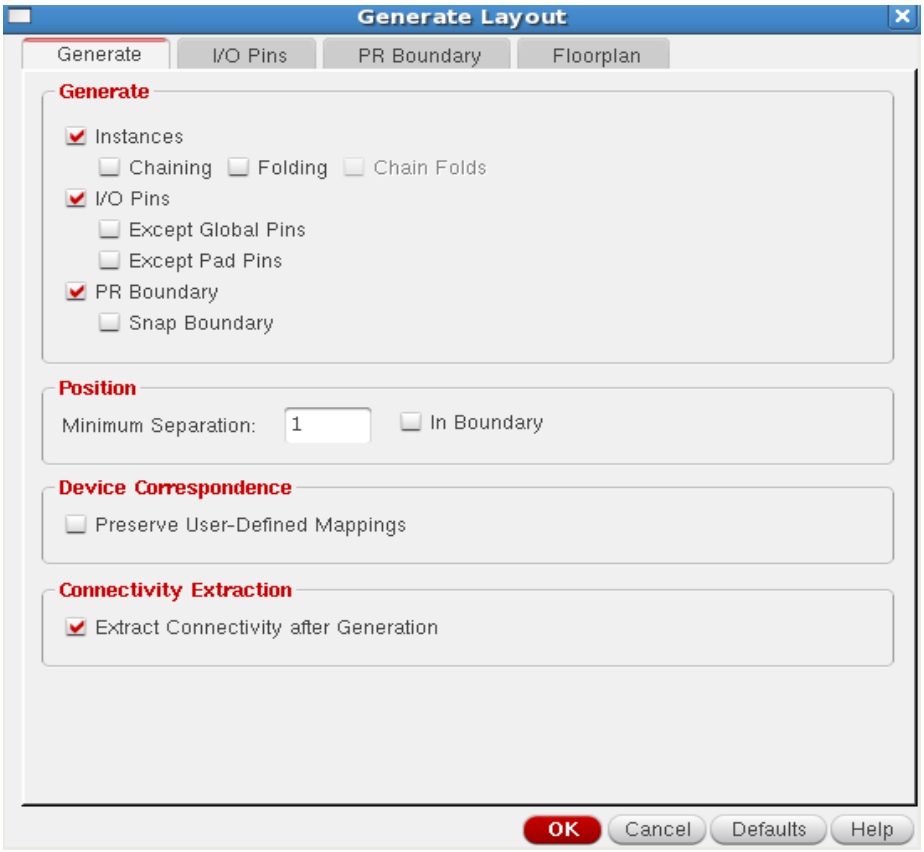
3. A **"New File"** form appears, Check the Library (**MyDesignLib**), Cellname (**cs_amp**) and Viewname **(layout).**



4. Click **OK** from the **"New File"** Window. **LSW** (Layer Select Window) and a blank layout window appear along with schematic window.

Adding Components to Layout

1. Execute **Connectivity – Generate – All from Source** or click the icon  in the **"Layout Editor window"**, **Generate Layout** form appears. Click **OK** which imports the schematic components in to the Layout window automatically.



2. Re arrange the components with in PR-Boundary as shown in the next page.

3. We can stretch the PR-Boundary to our requirement by executing **Edit-stretch** or click the stretch icon  and them the PR-Boundary. Press ***Esc*** after stretching. We can also use this feature to stretch Wire and routing elements.

Tip: Press **S** to stretch.

4. To move the components, execute **Edit-Move** or click the **Move** icon  and then click on the component which is to be moved. . Press ***Esc*** after moving.

Tip: Press **M** to move.

5. To rotate a component, Select the component and execute **Edit –Properties**. Now select the degree of rotation from the property edit form.

6. To know the distance between different components, or to measure the area consumed by the design, execute **Tools - Create Ruler.** Press ***Esc*** after measurements.

Tip: Press **K** for ruler.

Making interconnection

1. Execute **Connectivity –Nets – Show/Hide selected Incomplete Nets** or click  the icon in the Layout Menu.

2. Try to move a device to get the connectivity information, which shows the guide lines (or flight lines) for the inter connections of the components.

3. From the layout window execute **Create – Shape – Path** or **Create wire or click**  or **Create – Shape – Rectangle (**for vdd and gnd bar**)** and select the appropriate Layers from the **LSW** window and Vias for making the inter connections.

Creating Contacts/Vias

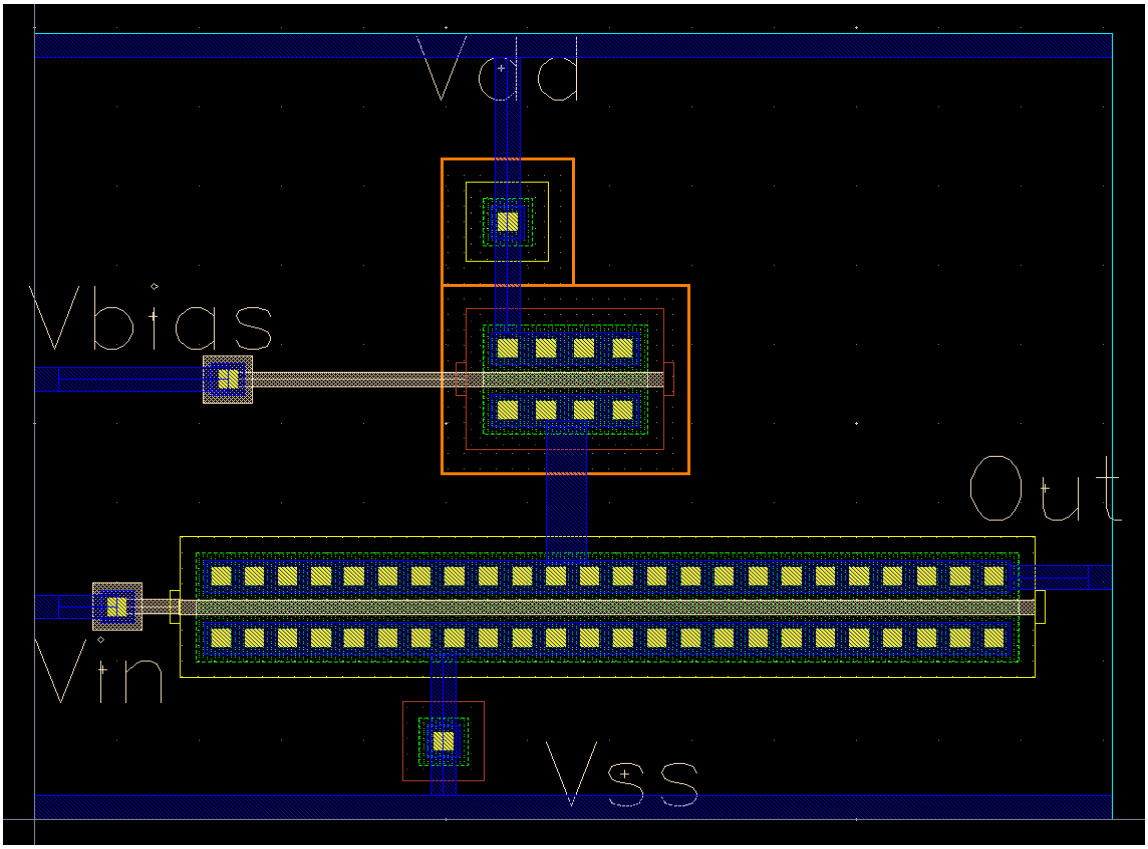
We will use the contacts or vias to make connections between two different layers.

Execute **Create — Via** or click  icon to place different Contacts, as given in below table.

Connection	Contact Type
For Metal1- Poly Connection	Metal1-Poly
For Metal1- Psubstrate Connection	Metal1-Psub
For Metal1- Nwell Connection	Metal1-Nwell

Saving the design

1. Save your design by selecting **File — Save** or click  to save the layout and layout should appear as below



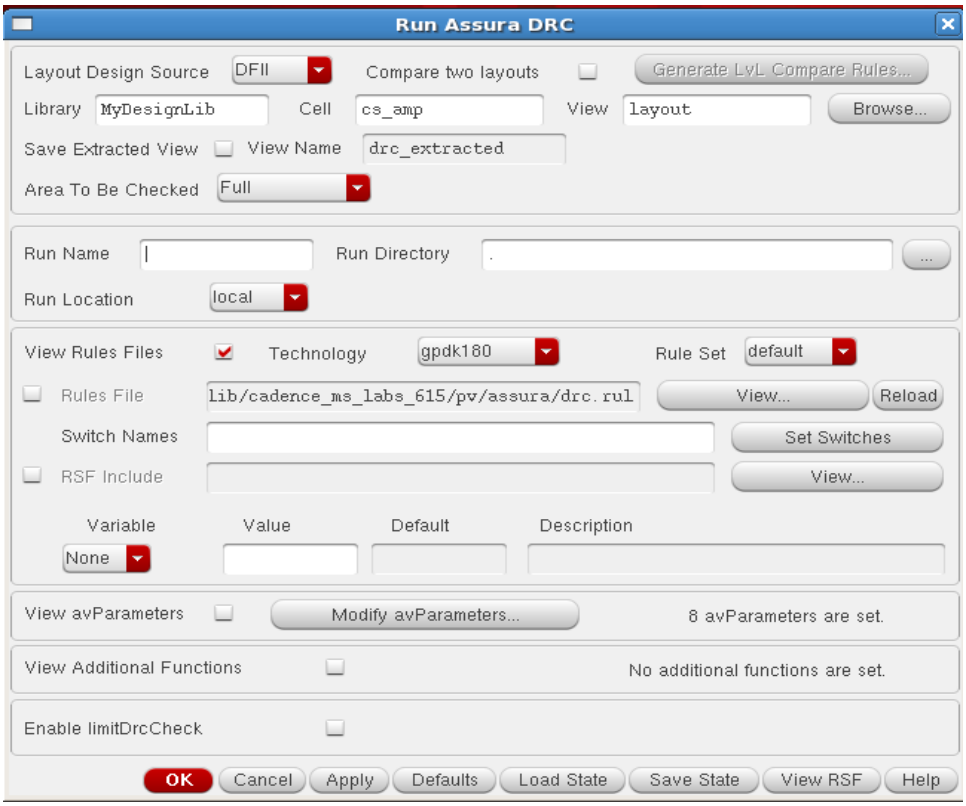
Physical Verification

Assura DRC

Here we check whether our design obeys the design rules.

Running a DRC

1. Select **Assura - Run DRC** from layout window. The DRC form appears. The Library and Cellname are taken from the current design window, but rule file may be missing. Select the Technology as **gpdk180.** This automatically loads the rule file.



3. Click **OK** to start DRC.

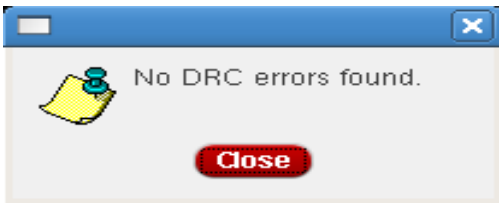
4. A Progress form will appears. You can click on the watch log file to see the log file.

5. When DRC finishes, a dialog box appears asking you if you want to view your DRC results, and then click **Yes** to view the results of this run.

6. If there any DRC error exists in the design, **View Layer Window** (VLW) and **Error Layer Window** (ELW) appears. Also the errors highlight in the design itself.

7. You can refer to rule file also for more information, correct all the DRC errors and **Re – run** the DRC.

8. If there are no errors in the layout then a dialog box appears with **No DRC errors found** written in it, click on **close** to terminate the DRC run.

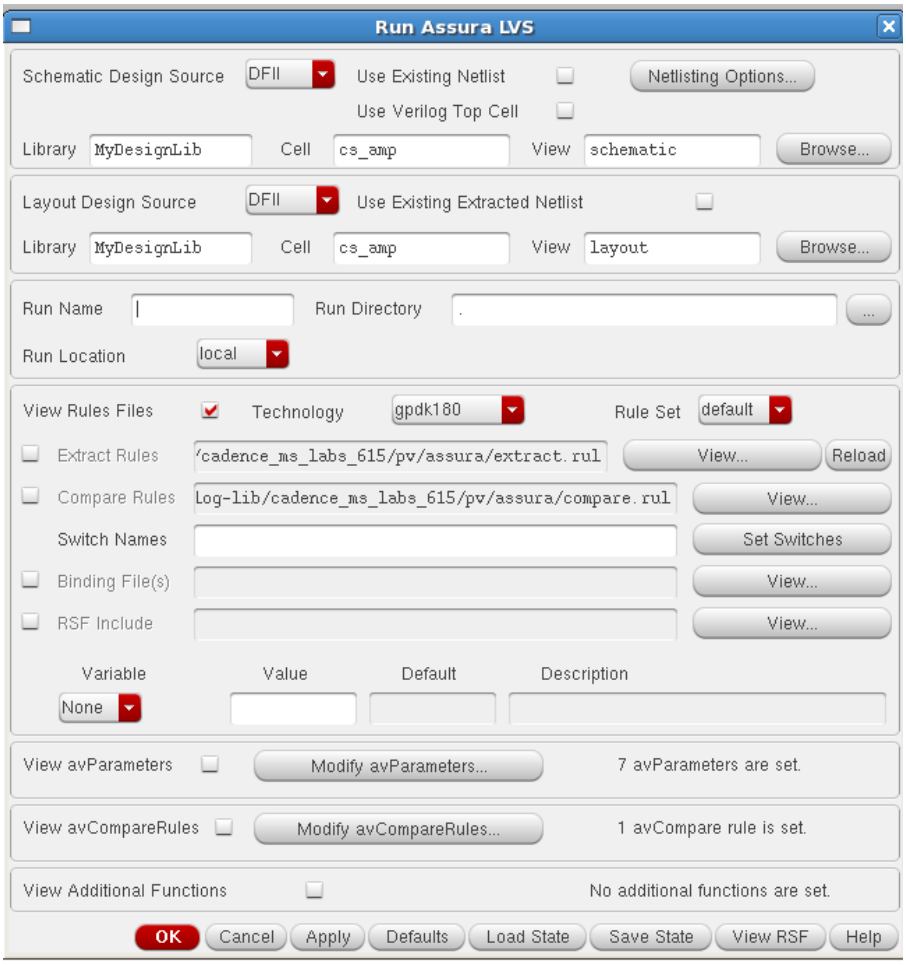


Assura LVS

In this section we will perform the LVS check that will compare the schematic netlist and the layout netlist.

Running LVS

1. Select **Assura – Run LVS** from the layout window. The **"Run Assura LVS"** form appears. It will automatically load both the schematic and layout view of the cell.



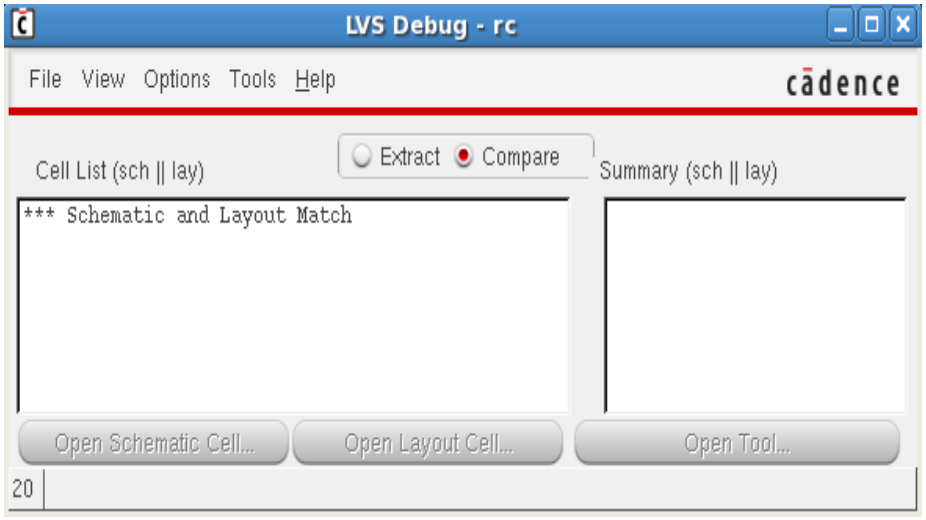
2. Click **OK** to run LVS.

3. Once the LVS is completed, a window informs that the LVS completed successfully and asks if you want to see the results of this run. Click **Yes** in the window.

4. If the schematic and layout do not matches, **LVS Debug** window appears, and you are directed into **LVS Debug Environment.**

5. In the **LVS Debug** window you can find the details of mismatches and you need to correct all those mismatches and **Re – run** the LVS till you will be able to match the schematic with layout.

6. If the schematic and layout matches completely, you will get a window displaying **Schematic and Layout Match.** Close the window to terminate the LVS run.

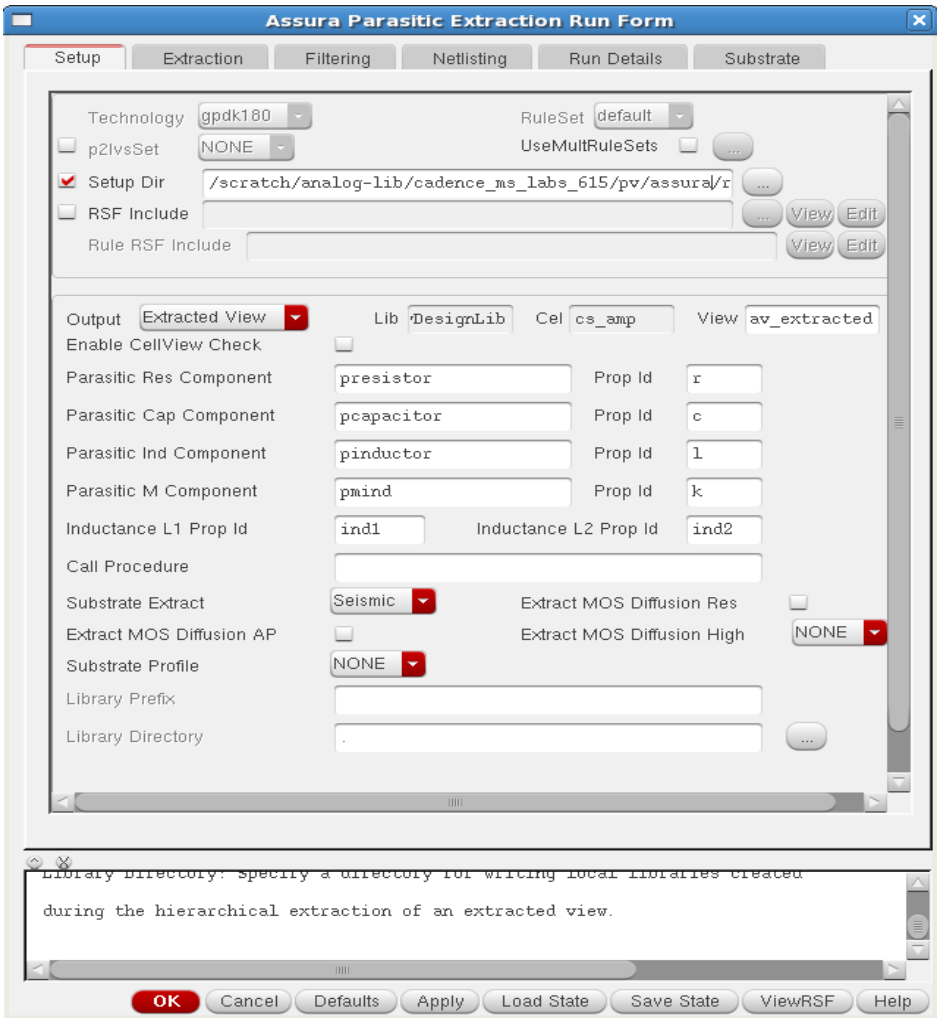


Assura RCX

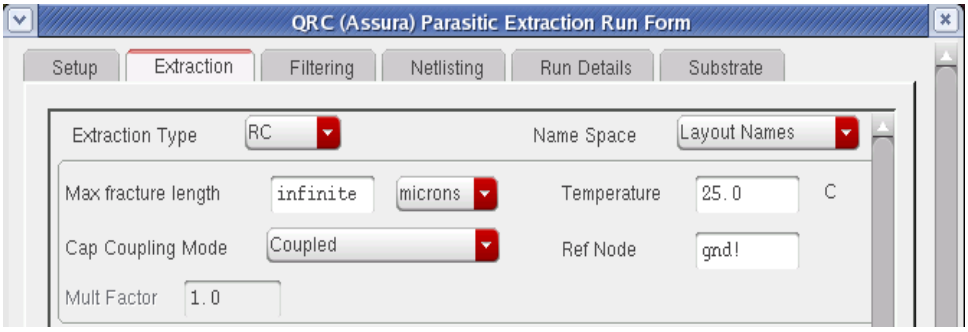
In this section we will extract the RC values from the layout and perform analog circuit simulation on the designs extracted with RCX. Before using RCX to extract parasitic devices for simulation, the layout should match with schematic completely to ensure that all parasites will be backannoted to the correct schematic nets.

Running RCX

1. From the layout window execute **Assura – Run RCX**.
2. Change the following in the "**Assura parasitic extraction run form"**. Select **Output** type under **Setup** tab as **Extracted View**.



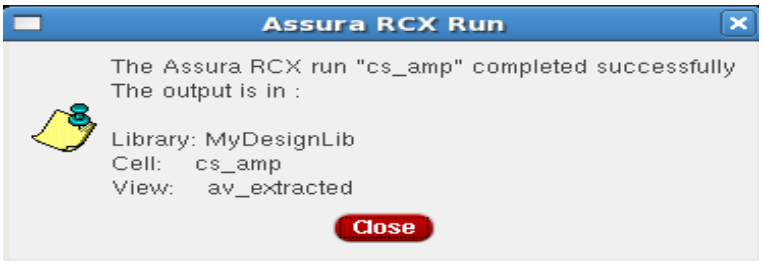
3. In the **Extraction** tab of the form, choose Extraction type, Cap Coupling Mode and specify the Reference node for extraction.



4. In the **Filtering** tab of the form, **Enter Power Nets** as **vdd!, vss!** and **Enter Ground Nets** as **gnd!**

5. Click **OK** in the Assura parasitic extraction form when done. The RCX progress form appears, in the progress form click **Watch log file** to see the output log file.

6. When RCX completes, a dialog box appears, informs you that **Assura RCX run Completed successfully.** Click on **close** to terminate the RCX run

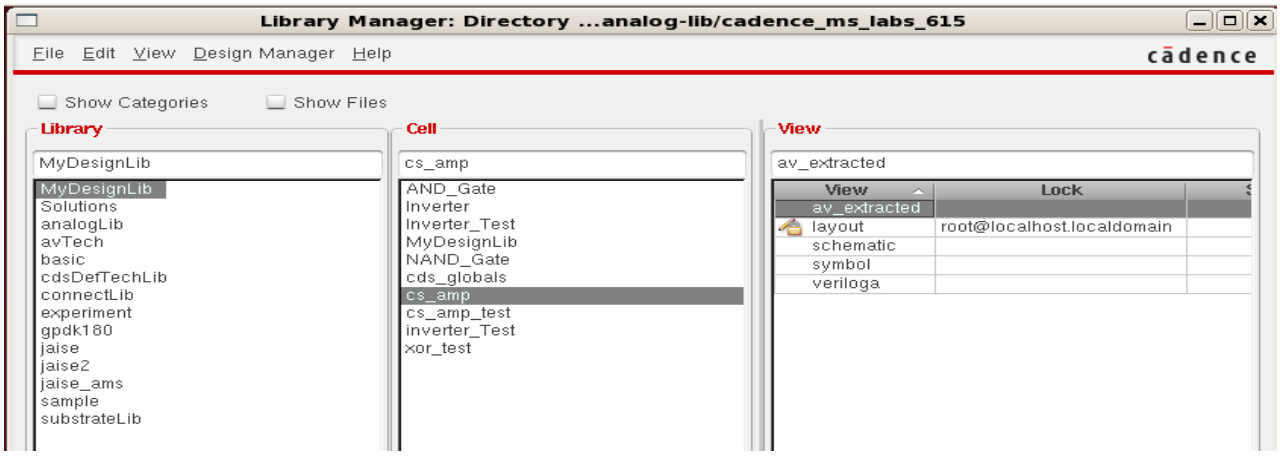


7. To view the av_extracted design, execute the following steps from the CIW window **Tools – Library Manager**, select the following

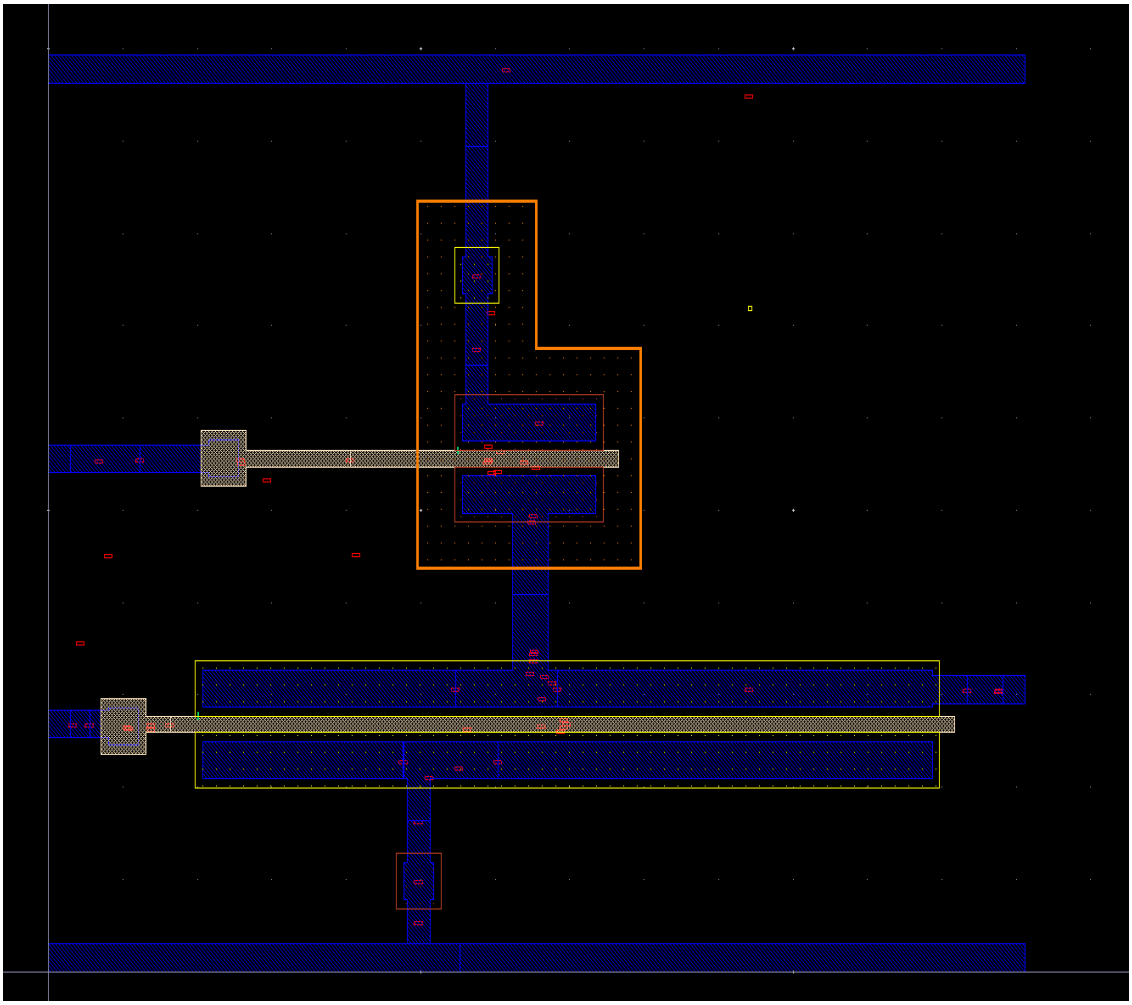
Library ⟶ MyDesignLib

Cell ⟶ cs_amp

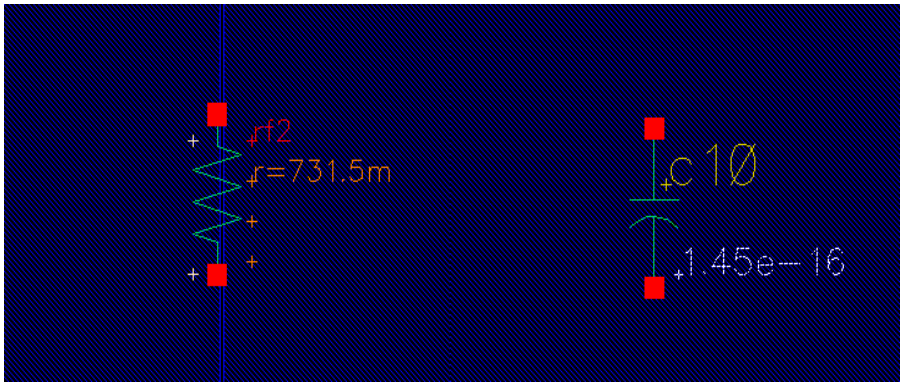
Double click on **av_extracted** option under **View** field. The av_extraced view of design will pop up.



The av_extracted view of the cs_amp design looks like this



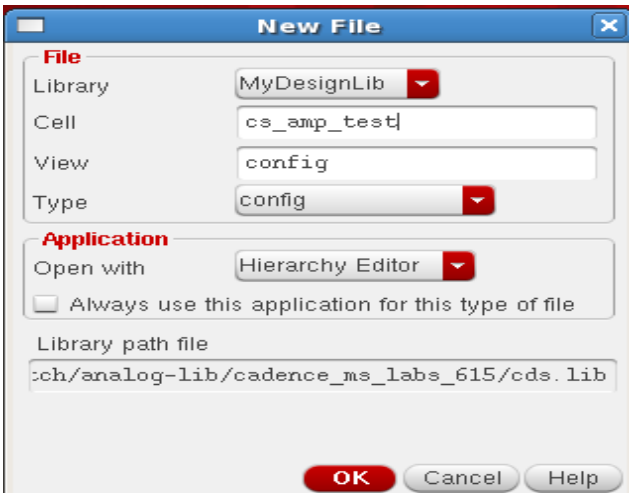
Note: - Press **shift-f** to view values of the extracted resistance and capacitance in the av_extracted view



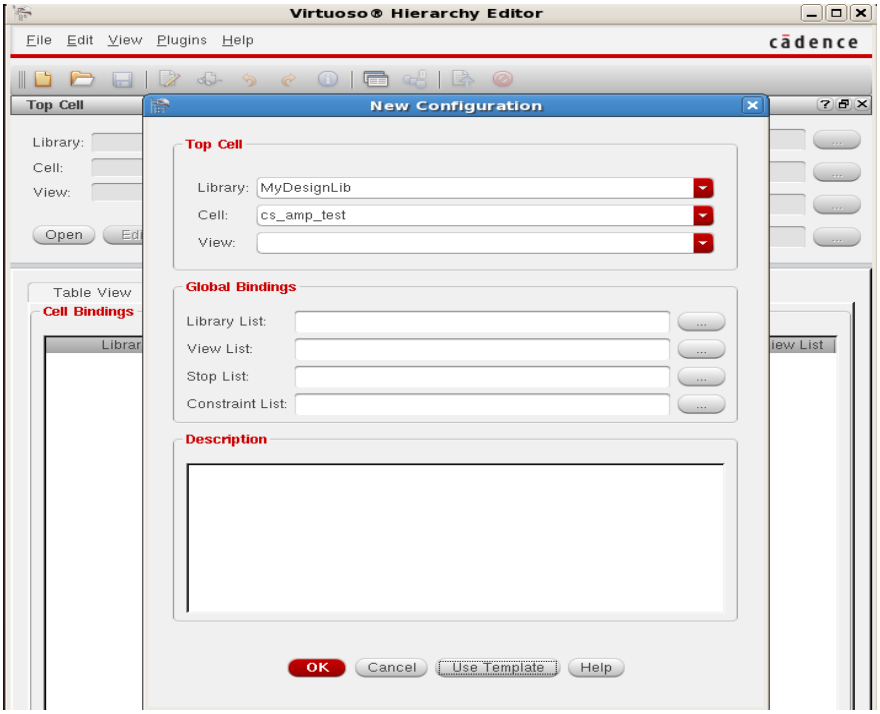
Creating the Configuration View

In this section we will create a config view and with this config view we will run the simulation with parasitic components.

1. In the CIW or Library Manager, execute **File – New – Cellview.**
2. In the Create New file form, set the following:



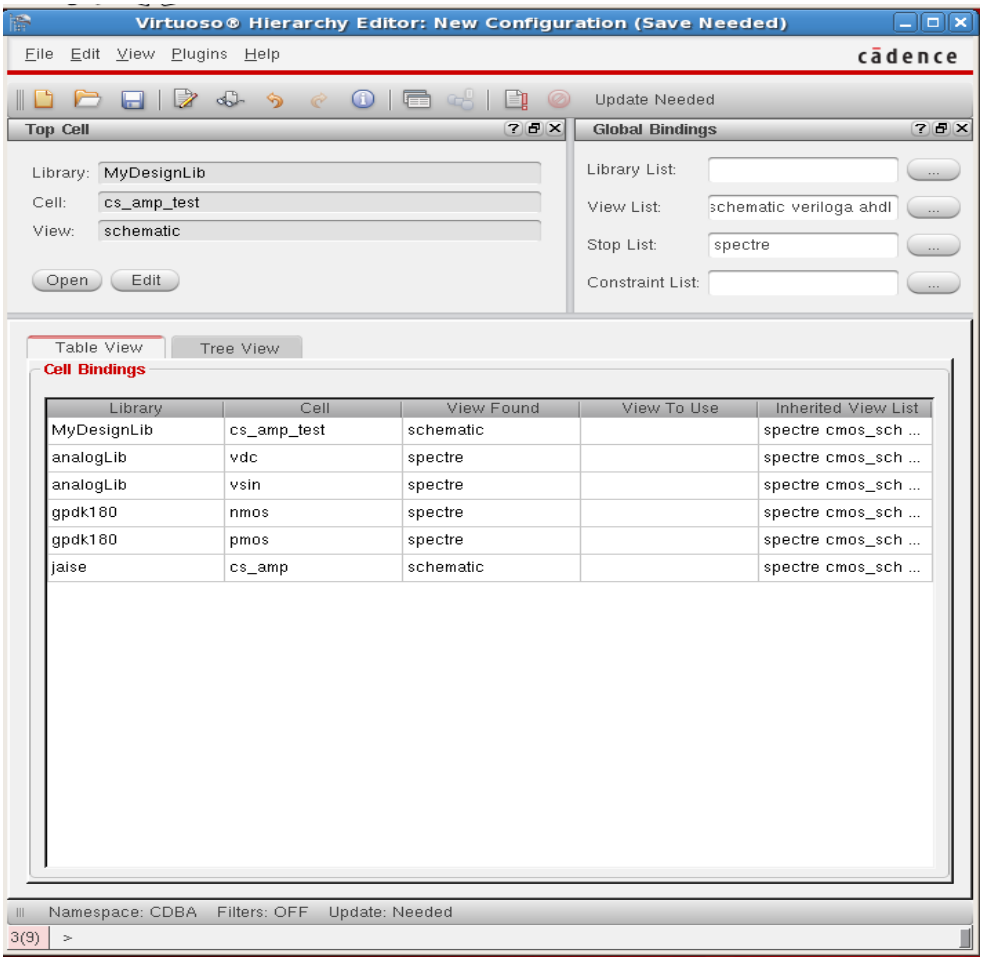
3. Click **OK** in "**New File"** form. The "**Hierarchy Editor"** form opens and a "**New Configuration"** form opens in front of it.



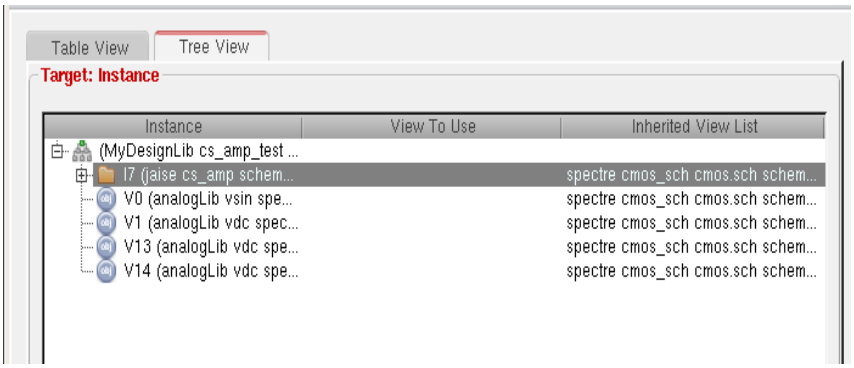
4. Click **Use template** at the bottom of the **New Configuration** form and select **Spectre** in the cyclic field and click **OK**.

5. Change the **Top Cell - View** to **schematic** and remove the default entry from the **Library List** field and Click **OK** in the New Configuration form.

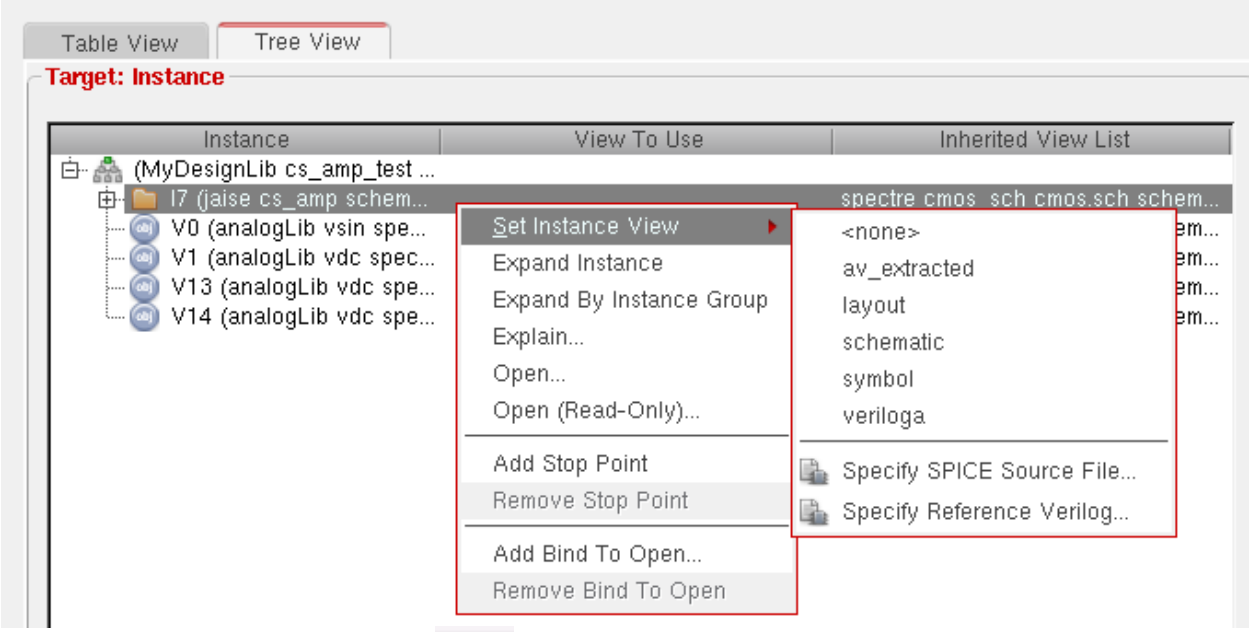
The hierarchy editor displays the hierarchy for this design using table format.



6. Click the **Tree View** tab. The design hierarchy changes to tree format. The form should look like this



7. Choose the **cs_amp schematic** folder icon and right click, a set of option arises, click on **Set Instance View** and choose **av_extracted.**



8. **Save** the current configuration  and Close the Hierarchy Editor window. Execute **File – Close Window**.

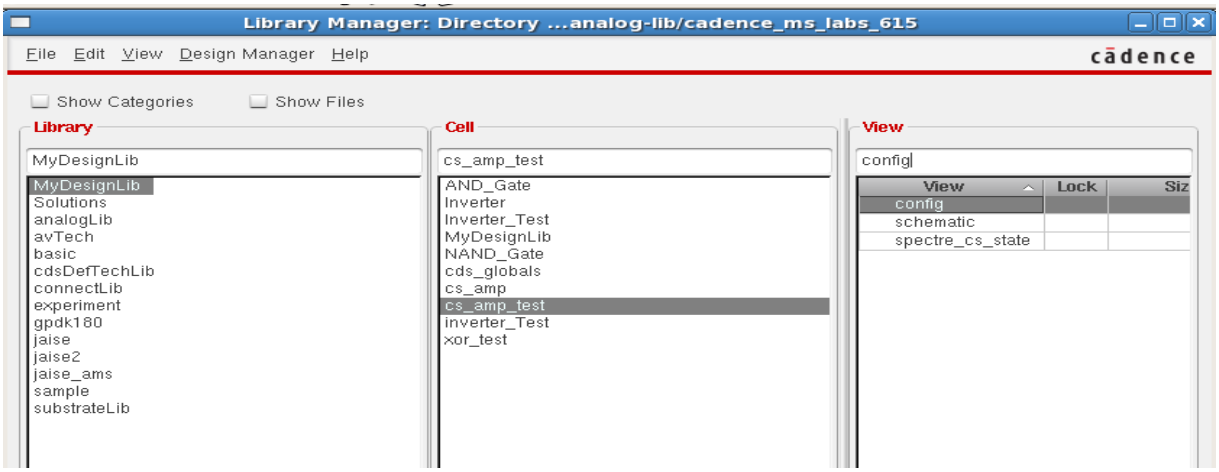
9. From CIW, execute **Tools – Library Manager.**

10. In the **library Manager** window, select the following

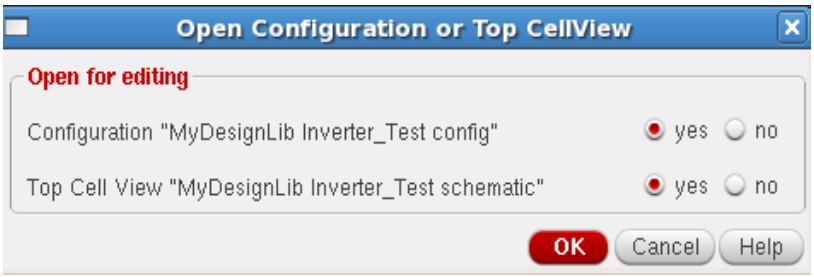
Library → **MyDesignLib**

Cell → **cs_amp_test**

Double click on **config** under **View**



11. A new **"Open Configuration or Top CellView"** form appears. Choose **yes** in both the cyclic fields and click **OK**.



The cs_amp_test schematic and cs_amp_test config window appears. Notice the window banner of schematic also states **Config: MyDesignLib cs_test config.**

Simulation of config view with Spectre

1. Execute **Launch – ADE L** from the schematic window.

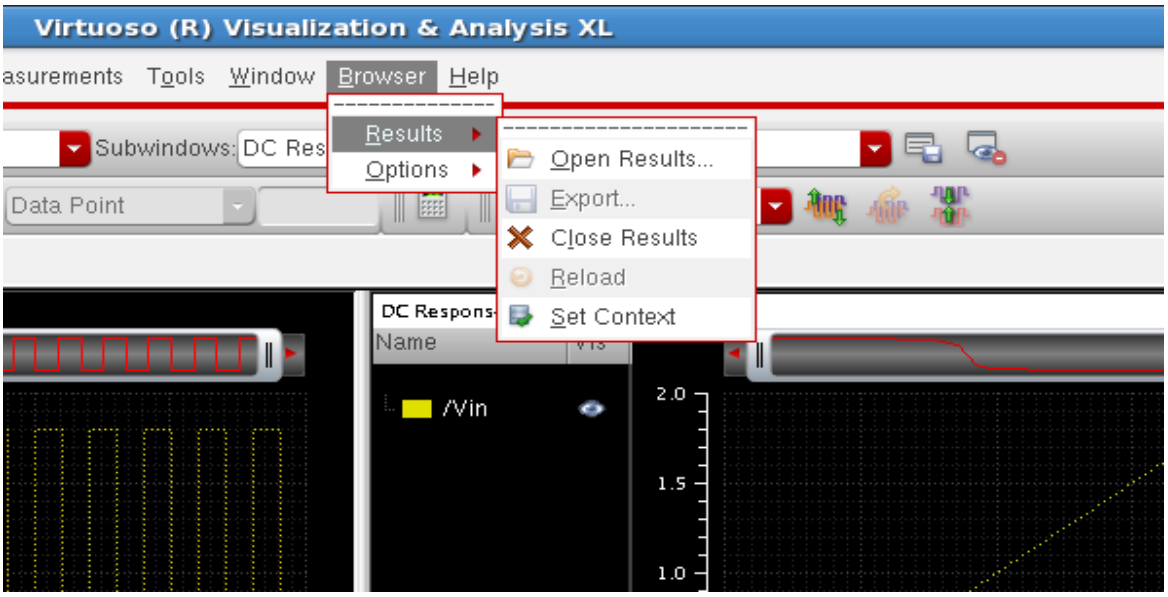
2. Now you need to follow the same procedure for running the simulation. Executing **Session–Load state,** the Analog Design Environment window loads the previous state.

3. Click **Netlist and Run** icon to start the simulation. 

The simulation takes a few seconds and then waveform window appears.

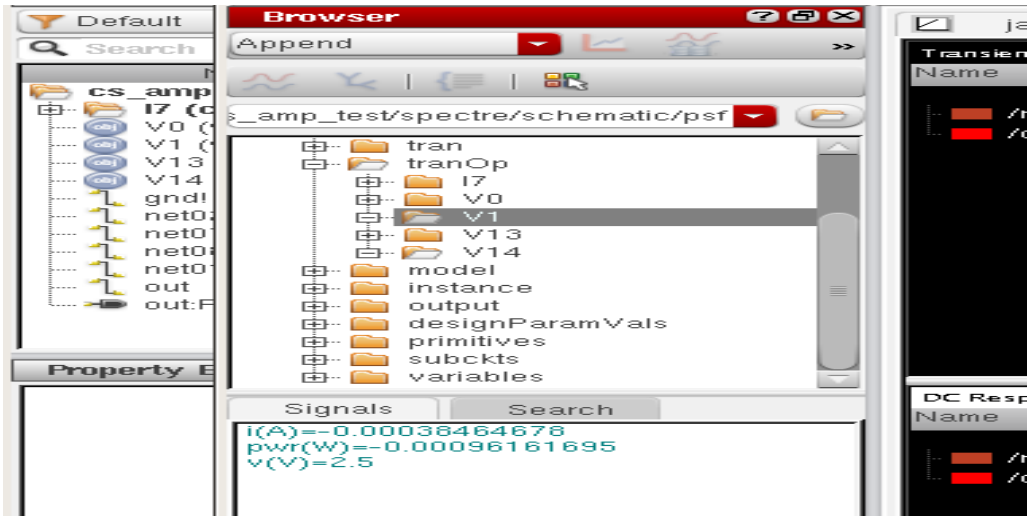
Measuring Power, Voltage and Current Level

1. In the waveform window, execute **Browse – Results –Open results.**



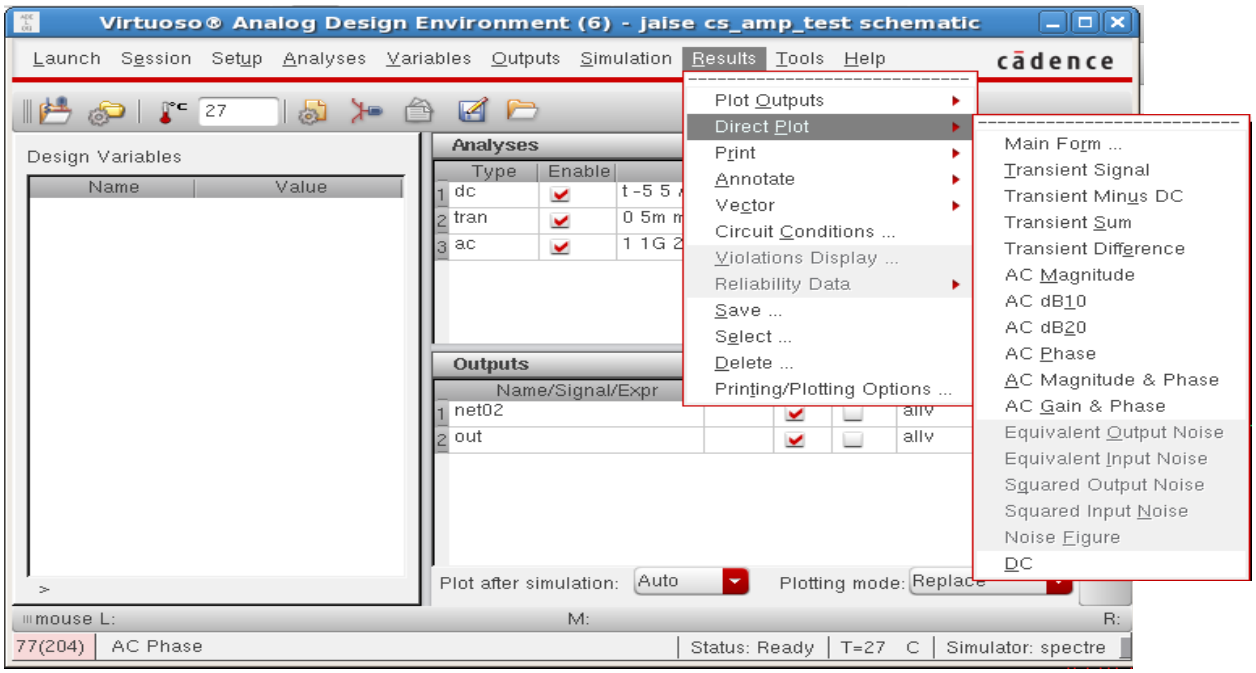
2. A **"Select Waveform Database"** form appears. Double click on the psf option.

3. A **Brower** form appears on left side of the waveform window. Open **tranOp – V1** (supply signal).
We can find the values for current, power and voltage level under **signals** field below browser form.



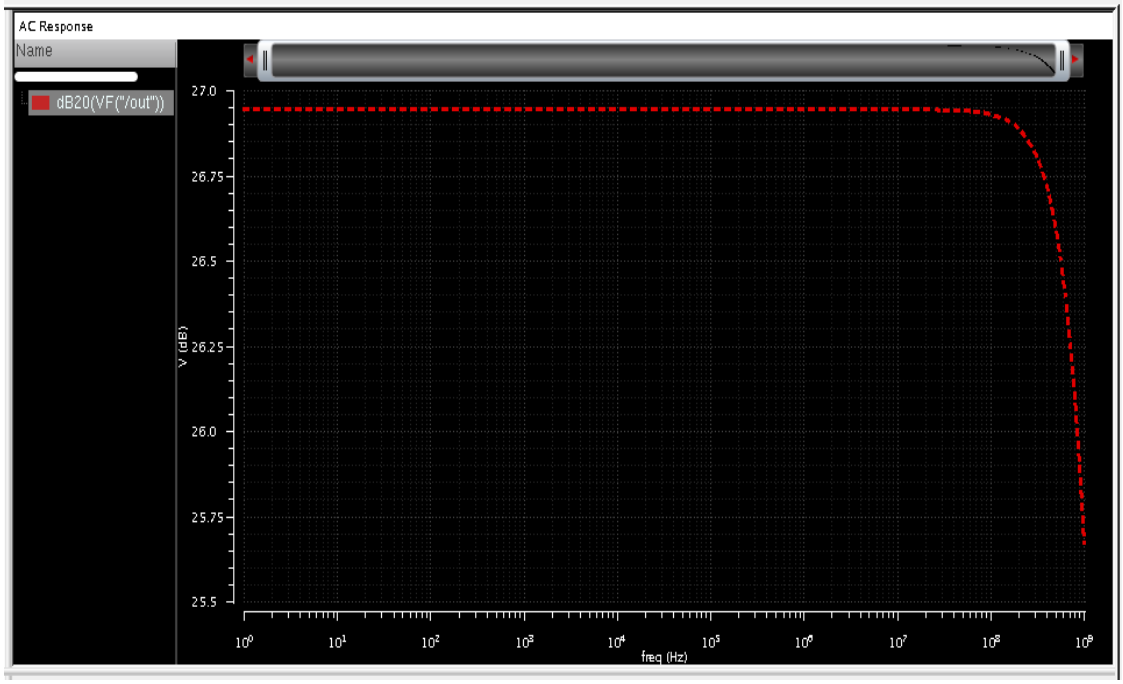
Measuring Gain of the Circuit

1. After simulation, execute **Results- Direct Plot- AC dB20** from the **ADE** window.



2. The **Test Design** opens and click on the output net and press ***Esc***.

3. The plot for gain in dB appears. Place the mouse pointer on the plot to get the value for gain.



Gain in dB

Measuring Bandwidth of the Circuit

1. In the waveform window, execute **Tools- Calculator**, The calculator window appears.

2. Click on the **Clear buffer** icon  to remove the previously calculated value from the tool buffer.

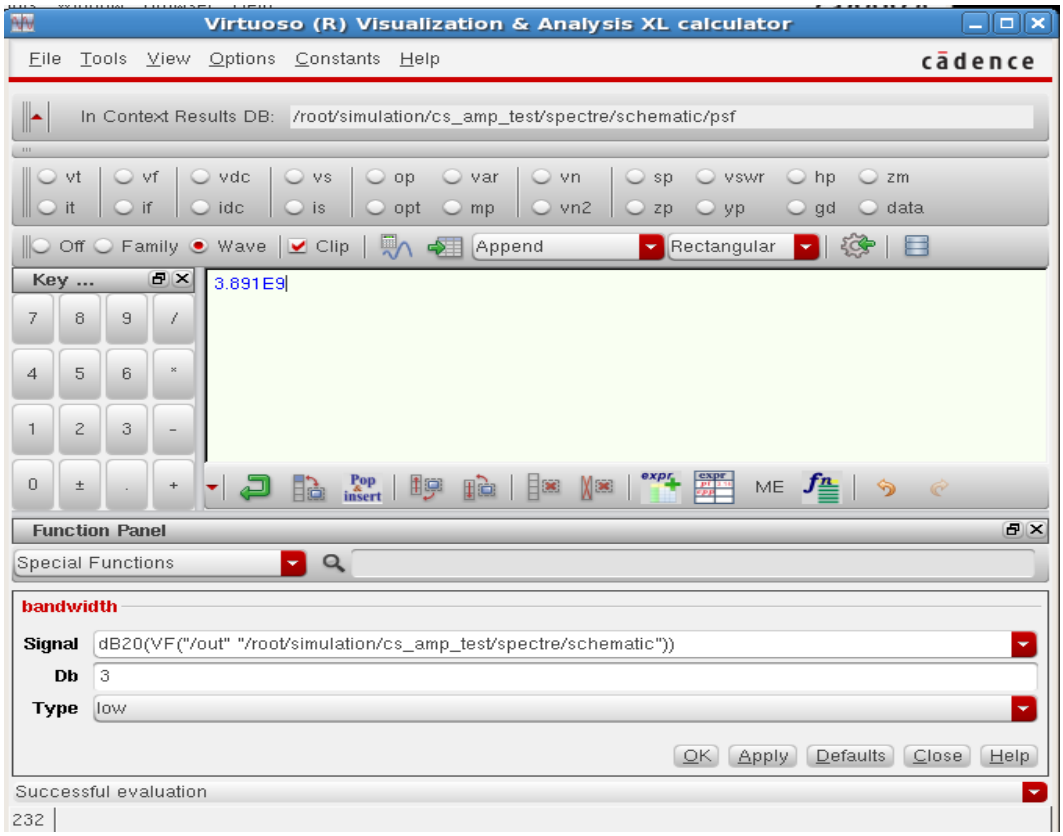
3. From the functions select **bandwidth,** this will open the bandwidth data panel.

4. Place the cursor in the text box for Signal, select the **wave** button and select the **Gain** waveform from the waveform window.

5. Execute **OK** and observe the expression created in the calculator buffer.

6. Click on **Evaluate the buffer icon**  to perform the calculation, note down the value returned after execution.

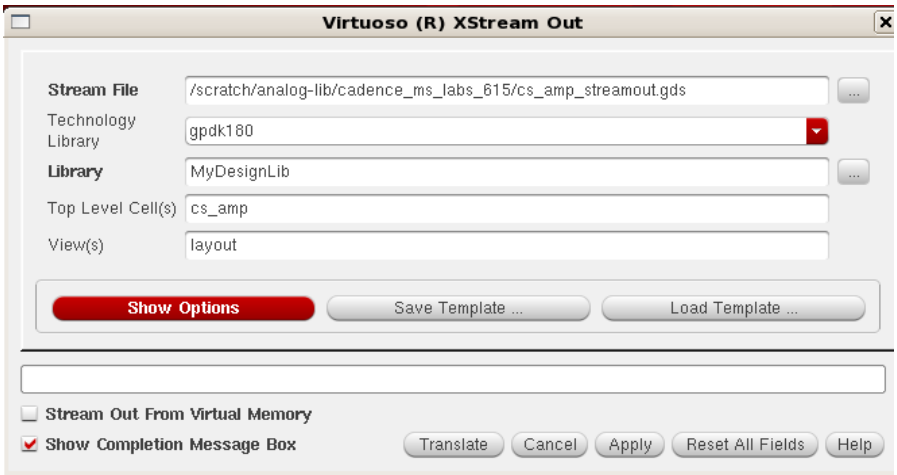
7. Close the calculator window.



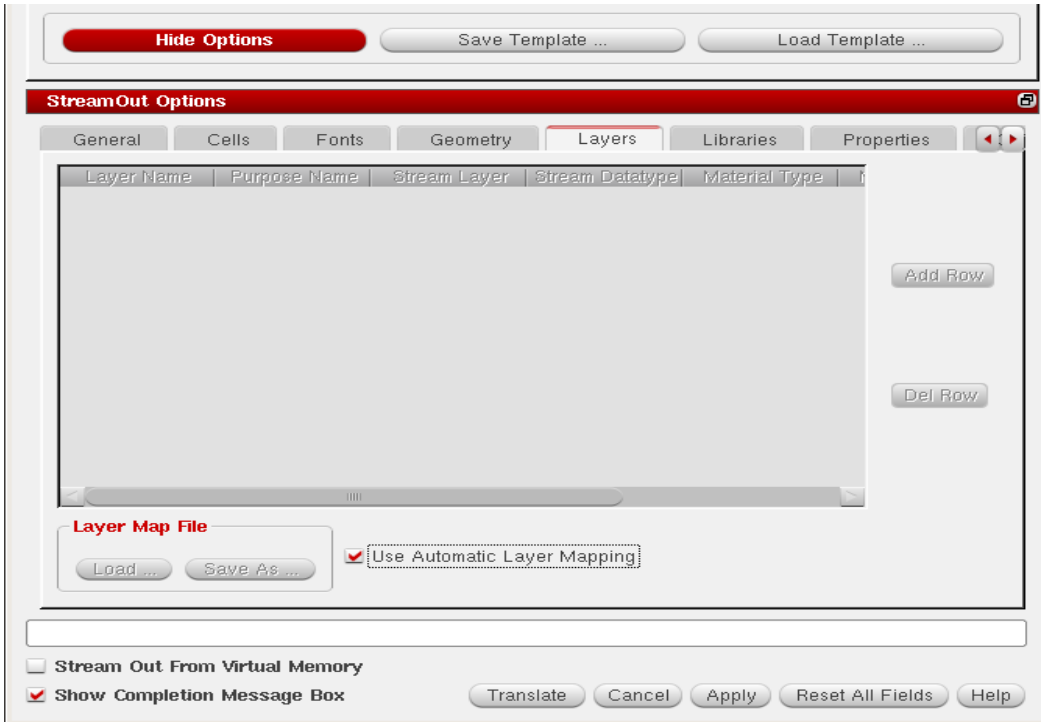
Generating Stream Data

Streaming Out the Design

1. Select **File – Export – Stream** from the **CIW** menu and **Virtuoso Xstream Out** form appear. Make changes in Xstream Out window as show below.



6. Click the **Show Options** field



7. Click the **layers** field and enable **Use Automatic Layer Mapping** option.
8. Click **Translate** option and the generation of stream out for cs_amp starts.
9. The stream out will be ready in a few seconds with the log the log file.
10. The stream out file for cs_amp can be viewed by opening the file from its location using **vi Editor**.