1) Using only AND gate, a) our harand is possible

A Doud

B out

If A dranger from 1 to 0 B danger from 0 to 1 In intermediale, we get a spike. i.e. ouo -> static hazad

b) For lul hazard,

CA: a combinational circuit

CA: a combinational circuit

CB: mother combinational

CB: mother c

CA: a combinational circuit

i. A and B are results of AND operations.

Fox out to have ful hazard,

It can happen ONLY if A: I all and B: Ital.

But since A and B are themselves results of

AND operations, they can be I'll only if their

imputs are lul.

If we propagate this back to the Primary Inputs, out can be tul ONLY if P.I are tul volvide is not possible as P.Is countouly be be undefined. Huce I'll hatard is NOT possible

3) Advantages og Event Driver Sim over Pavallel Sin all, i) Parallel sim has to evaluate the WHOLE circuit everytime but Event driven zin only execut enstrates a portion of the circuit based on the current events (FASTER Simulation time)

ii) Parallel Sim requires a lot of memory for it's 4 n-bit values per wire (n= num of circuits) Event laiver sin requires lesse memory storage. For huge circuits, parallel sin may not be

Faults > { gisal, aisao, viisary La = {a: Sa-0} Lb=23 Lc=29 La=Le=L+={3 Ly= la: s-a-o} (as a is controlling) Ly = La: s-a-o} Lr = {a: s-a-o} (o: s-a-l) (cout detected) Lu=Lg=29 Lx=Lo, V Luv()={a:s-a-o} Lg, = Lg U {g,: s-a-o} = 2 g,: s-a-o} Lg = Lg U { 3 = { 3 Le=(Lo2 1 Lx 1 Lg) U 13 = 23 Lm = (Le - Lg2) = 29 Lm = 23 no faults detected.

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