CS6330: DSTTD

Mid-Semester

Weightage: 25%. Duration: 50 mts.

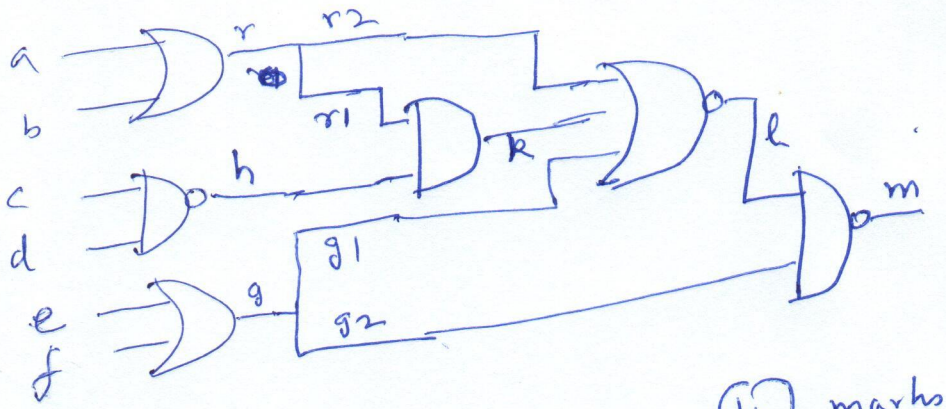
(1) Given a combinational Circuit with only AND gate is it possible to generate

(a) an 0^* hazard (Static hazard)

(b) an 1^* hazard (Static hazard)

If yes, show an example. If no, prove the same. — (8) marks.

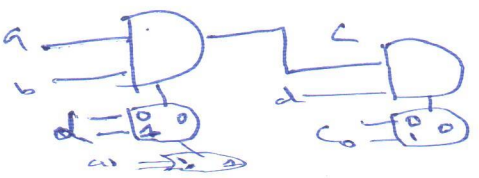
(2) Perform Deductive Simulation for the test vector (a=1, b=0, c=1, d=0, e=1, f=1) and the fault g_1: s-a-0, a: s-a-0, r1: s-a-1



— (16) marks.

(3) State the advantages of Event driven Simulation over Parallel Simulation — (2) marks.

(4) When (a=1, b=0, d=0) is applied on the following Circuit, find the new Concurrent list of faults.



— (5) marks