* Digital Electronics and Logic Design (DELD) - Practical Number - 13

Name :- Kaustubh Shrikant Kabra.
Class :- Second Year Engineering.
Div :- A Roll Number :-
Batch :-
Department :- Computer Department
College :- AISSMS's IOIT.

Title :-
Shift Registers.

Aim :-
Study of Shift Registers [SISO, SIPO, PISO, PIPO]

Objective :-
The study the working of shift registers.

Theory :-
Mode of operation of a shift register: The various mode in which a shift register can operate are as follows :-

1. Serial input Serial Output [SISO]
2. Serial Input Parallel Output [SIPO]
3. Parallel Input Serial Output [PISO]
4. Parallel Input Parallel Output [PIPO]

1) Serial In Serial Out [SISO] :-

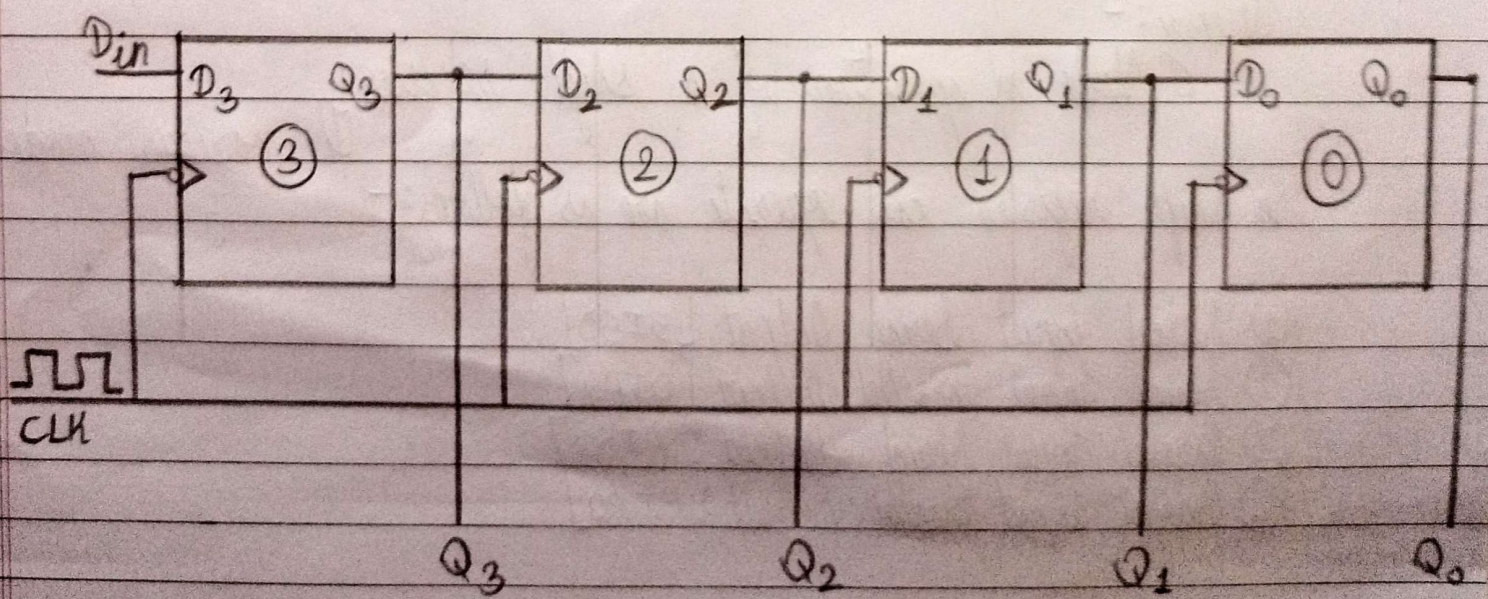
C.P	Q_3	Q_2	Q_1	Q_0	D_{in}
Initially	0	0	0	0	1
↓1	0	0	0	1	1
↓2	0	0	1	1	1
↓3	0	1	1	1	1
↓4	1	1	1	1	1

Shift Left Register

C.P	D_{in}	Q_3	Q_2	Q_1	Q_0
Initially	1	0	0	0	0
↓1	1	1	0	0	0
↓2	1	1	1	0	0
↓3	1	1	1	1	0
↓4	1	1	1	1	1

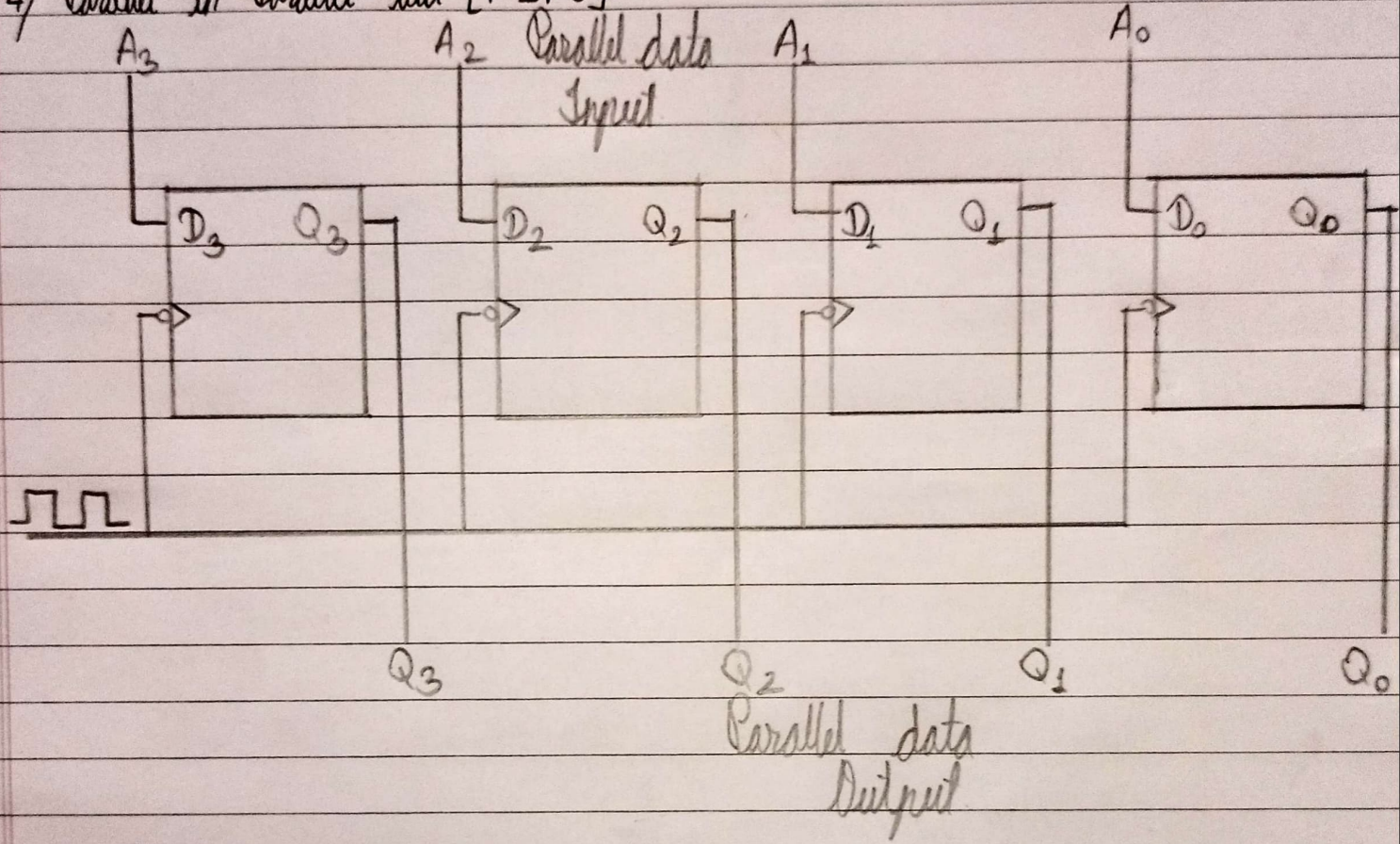
Shift Right Register

2) Serial In Parallel Out [SIPO] :-



CP	Q_3	Q_2	Q_1	Q_0
–	NC	NC	NC	NC
↓	D_3	D_2	D_1	D_0

4) Parallel in Parallel Out [PIPO]:-



Application of Shift Register:-

1. Temporary data storage.
2. Delay line
3. Serial-to Parallel Converter
4. Parallel-to Serial Converter
5. Counter
6. Sequence Generator

Conclusion:-

Hence, we have studied the shift register and its different types.