UNIT I
MINIMIZATION TECHNIQUES AND LOGIC GATES

1. **What are basic properties of Boolean algebra?**

The basic properties of Boolean algebra are 1.commutative property, 2.associative property, 3.distributive property and 4.idem potency.

2. **What is meant by bit?**

A binary digit is called a bit.

3. **Define byte**.

Byte is defined as a group of 8 bits.

4. **State the associative property of Boolean algebra.**

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is illustrated as follow:

A+ (B+C) = (A+B) +C

5. **State the commutative property of Boolean algebra.**

The commutative property states that the order in which the variables are OR ed when changed does not make any difference in the characteristics. The commutative property is illustrated as follow:

A+B=B+A

6. **State the distributive property of Boolean algebra.**

The distributive property states that AND ing several variables and OR ing the result with a single variable is equivalent to OR ing the single variable with each of the several variables and then AND ing the sums. The distributive property illustrated as follow is:

A+BC= (A+B) (A+C)

7. **Write the absorption law of Boolean algebra.**

The absorption law of Boolean algebra is given by X+XY=X.

8. **Simplify A.A'C.**

A.A'C = 0.C

[A.A' = 0]

= 0

9. **Simplify A(A + B)**

A(A + B) = AA + AB

= A(1 + B) [1 + B = 1]

= A.

10. **Reduce A'B'C' + A'BC' + A'BC**

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A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C
= A'C' + A'BC

[A + A' = 1]

= A'(C' + BC)
= A'(C' + B)

[A + A'B = A + B]

11. State and prove Demorgan's theorem.

i. (AB)'= A'+B'
ii. (A+B)'= A'B'

12. Reduce AB + (AC)' + AB'C(AB + C)

AB + (AC)' + AB'C(AB + C) = AB + (AC)' + AAB'BC + AB'CC
= AB + (AC)' + AB'CC

[A.A' = 0]

= AB + (AC)' + AB'C

[A.A = 1]

= AB + A' + C' + AB'C [(AB)' = A' + B']
= A' + B + C' + AB'C [A + AB' = A + B]
= A' + B'C + B + C' [A + A'B = A + B]
= A' + B + C' + B'C
=A' + B + C' + B'
=A' + C' + 1
= 1

[A + 1 =1]

13. Simplify the following expression Y = (A + B)(A + C')(B' + C')

Y = (A + B)(A + C')(B' + C')
= (AA' + AC +A'B +BC)(B' + C')

[A.A' = 0]

= (AC + A'B + BC)(B' + C')
= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'
= AB'C + A'BC'

14. Show that (X + Y' + XY)(X + Y')(X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X)(X + Y')(X' + Y) [A + A'B = A + B]
= (X + Y')(X + Y')(X'Y) [A + A = 1]
= (X + Y')(X'Y) [A.A = 1]
= X.X' + Y'.X'.Y
= 0 [A.A' = 0]

15. Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

ABC + ABC' + AB'C + A'BC=AB(C + C') + AB'C + A'BC
=AB + AB'C + A'BC

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=A(B + B'C) + A'BC
=A(B + C) + A'BC
=AB + AC + A'BC
=B(A + C) + AC
=AB + BC + AC
=AB + AC +BC

Hence proved.

16. Apply De Morgan's theorem for the function $((A + B + C)D)'$. [Nov /Dec – 08]

$$F = \left((A + B + C)D\right)'$$

= (A+B+C)' + D'
= A'. B'. C' + D'

17. Define – Duality Property

Duality property is defined as; every algebraic expression deducible from the postulates of Boolean algebra remains valid, if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we have to simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

18. Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x(y'z' + yz). By applying De-Morgan's theorem.

F1 = x'yz' + x'y'z

Complement of F1 = F1' = (x'yz' + x'y'z)'
= (x'yz')'(x'y'z)'
= (x + y' + z)(x + y +z')

Complement of F2 = F2' = [x(y'z' + yz)]'
= x' + (y'z' + yz)'
= x' + (y'z')'(yz)'
= x' + (y + z)(y' + z')

19. Convert the given expression in canonical SOP form Y = AC + AB + BC

Y = AC + AB + BC
=AC(B + B') + AB(C + C') + (A + A')BC
=ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC
=ABC + ABC' +AB'C + AB'C' [(A + A) =1]

20. Write the names of basic logical operators.

The names of the basic logic operators are
1. NOT / INVERT
2. AND
3. OR

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21.State the two canonical forms of Boolean algebra. [Apr. / May – 07]

The two canonical forms of Boolean algebra are:

i. Sum of products

Products of Sum

22.What are the methods adopted to reduce Boolean function?

There are four methods used to reduce the Boolean function. They are

i. Algebraic method
ii. Karnaug map
iii. Tabulation method or Quine Mc-Cluskey method
iv. Variable entered map technique.

23. What is a Karnaugh map?

A Karnaugh map or K map is a pictorial form of truth table, in which the map diagram is made up of squares called cells, with each cell representing one minterm of the function. The number of cells in the map depends upon the number of variable (literal) in the minterm or maxterm of the functions.

24. **State the limitations of Karnaugh map**.

The limitations of Karnaugh map are:

i. If the number of variables increases it is difficult to make judgments about grouping of cell and it is generally limited to six variables.
ii. The K – Map simplification is manual technique and linearly depends upon human abilities.
iii. It can not be programmed to run on a computer as it is not algorithmic.

21. Find the minterms of the logical expression Y = A'B'C' + A'B'C + A'BC + ABC'

Y = A'B'C' + A'B'C + A'BC + ABC'
= m0 + m1 + m3 + m6
= m(0, 1, 3, 6)

22. Write the maxterms corresponding to the logical expression.

Y = (A + B + C')(A + B' + C')(A' + B' + C)
= (A + B + C')(A + B' + C')(A' + B' + C)
=M1.M3.M6
= M(1,3,6)

23. What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not

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defined, it can be either high or low. These output levels are indicated by 'X' or 'd' in the truth tables and are called don't care conditions or incompletely specified functions.

24. Define implicant.

A product term is said to be an implicant of a Boolean function if the function implies the product term. In other words a product term in SOP form of a function is an implicant.

25. Define prime implicant.

An implicant is called a prime implicant if it is not a subset of another implicant of the function.

26. What is an essential prime implicant?

It is defined ast a prime implicant which includes a '1' cell that is not included in any other implicant is called an essential prime implicant.

27. Define implicate.

A sum term is said to be an implicate of a Boolean function if the function implies the sum term.

A	B	F

28. State the basic properties of Boolean algebra.

The basic properties of Boolean algebra are:

i. An identity element with respect to +, designated by 0: A + 0 = 0 + A = A
An identity element with respect to . (dot), designated by 1: A . 1 = 1 . A = A

ii. Commutative with respect to + : A + B = B + A
Commutative with respect to . (dot) : A . B = B . A

iii. Distributive property of . (dot) over + : A . (B + C) = (A . B) + (A . C)
Distributive property of + over . (dot) : A + (B . C) = (A + B) . (A + C)

iv. Associative property of + (dot): A + (B + C) = (A + B) + C
Associative property of . (dot): A . (B . C) = (A . B) . C

29. Define prime implicate.

A prime implicate of a complete Boolean function is a sum term that is implied by the function with the additional property that if any literal is removed from the term, then the resulting sum term no longer is implied by the function.

(or)

An implicate is called a prime implicate if it is not a subset of another implicate of the function.

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0	0	0
0	1	1
1	0	1
1	1	0

30. Minimize the function using Boolean algebra f= x(y+w'z)+wxz.

f= x(y+w'z)+wxz.
f= xy+w'xz+wxz
f= xy+xz(w'+w)
f= xy+xz
f= x(y+z)

31. What is an essential prime implicate?

Essential prime implicates are those implicates which contains at least one 'o' cell which is not included in any other implicates.

32. Write the Boolean function of XOR gate and give its truth table.(Nov–Dec-08)

The Boolean function of the XOR gate is given below

F = A ⊕ B = A'B + AB'

33. List out the methods adopted to reduce Boolean function.

The methods adopted to reduce Boolean function are:

i. Karnaug map
ii. Tabular method or Quine Mc-Cluskey method
iii. Variable entered map technique

34. What is the complement of $(A + BC + AB)$? [Nov / Dec – 08]

F = (A+ BC+ AB)
F' = (A+ BC+ AB)'

= A'. (BC)'. (AB)'
= A'. (B'+ C'). (A'+ B')

35. Convert the given expression to canonical Sum of products form:

$$Y = (AC + AB + BC)$$

Y = AC + AB + BC
=AC (B + B') + AB(C + C') + (A + A')BC
=ABC + AB'C + ABC + ABC' + ABC + A'BC

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=ABC + AB'C + A'BC

36. What is meant by propagation delay? [Apr /May – 09]

The propagation delay, or gate delay, is the length of time which starts when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is table and valid. Often this refers to the time required for the output to reach from 10% to 90% of its final output level when the input changes. Reducing gate delays in digital circuits allows them to process data at a faster rate and improve overall performance.

37. List out the advantages of CMOS logic. [Apr /May – 09]

The advantages of CMOS logic are:

i. Low power consumption: CMOS process provides lower power consumption and is easy to scaling down.
ii. High input impedance: Gate of CMOS needs much lower driving current than base current of bipolar.
iii. Reduced silicon area: Scaling down increases CMOS speed and reduces the area of the chip.
iv. Mature technology: CMOS processes are well established and continue to become more mature. The powerful trust by leading edge digital memory and processors has led to continuous improvement and down scaling of CMOS processes.

38. Which gates are called as universal gates? What are its advantages?

The NAND and NOR gates are called as the universal gates. These gates are used to perform all logic operations. (i.e. AND, OR, NOT, EX-OR & EX – NOR etc operations.

The advantages are:

1. Only one type of gate is required to implement the functions.
2. Minimum number of IC's required.
3. Reduces the printed board size, reduction in costs.
4. As number of IC's reduced the probability of occurrence of troubles becomes less.

39. Mention the important characteristics of digital IC's?

The important characteristics of digital IC's are

1. Fan out
2. Fan In
3. Power dissipation
4. Propagation Delay
5. Noise Margin
6. Operating temperature
7. Power supply requirements

40. Define Fan-out?

Fan out is defined as the number of standard loads that the output of the gate can

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drive without impairment of its normal operation.

41. Define fan in?

Fan in is the number of inputs connected to the gate without any degradation in the voltage level.

42. Show that a positive logic NAND gate is a negative logic NOR gate.

Logic expression for NAND gate is F=(X.Y)'

F= (X.Y)'= X' + Y' …DeMorgan's theorem

F= X' + Y' is the logic expression for negative logic NOR gate.

43. Define power dissipation?

Power dissipation is defined as a measure of power consumed by the gate when fully driven by all its inputs.

44. What is propagation delay?

Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in nano seconds(ns).

45. Define noise margin?

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the output. It is expressed in milli volts(mV).

46. What is Operating temperature?

All the gates or semiconductor devices are temperature sensitive in nature. The maximum temperature at which the performance of the IC is not affected is called as operating temperature. Operating temperature of the IC generally vary from 0^0 C to 70^0 C.

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49. (X + Y)' = X' . Y', These can be proved by the use of truth tables.

Proof of (X + Y)' = X' . Y'

X	Y	X+Y	(X+Y)'
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

X	Y	X'	Y'	X'.Y'
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

The two truth tables are identical, and so the two expressions are identical.

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50.

State and prove De Morgan's theorem. [Nov /Dec – 10]

De Morgan suggested two theorems that form important part of Boolean algebra.
They are:

i. The complement of a product is equal to the sum of the complements.

(AB)' = A' + B'

ii. The complement of a sum term is equal to the product of the complements.

(A + B)' = A'B'

Apply De Morgan's theorem for the function $((A+B+C)D)'$. [Nov / Dec – 08]

$$F = \left((A+B+C)D\right)'$$

= (A+B+C)' + D'
= A'. B'. C' + D'

51. Simplify the following using De Morgan's theorem $((AB)'C)'D'$.

$$F = ((AB)'C)'D'$$

= ((AB)' + C'). D'
= (A'+B'+C').D'

52. State the two canonical forms of Boolean algebra. [Apr. / May – 07]

The two canonical forms of Boolean algebra are:

ii. Sum of products
iii. Products of Sum

53. Simplify: $(X + X'Y)$ **[Apr. /May – 10]**

Z= X + X'Y = X + XY + X'Y since X + XY = X
Z= X + Y (X + X') since X + X' = 1
Z = X + Y

53. What is the complement of $(A + BC + AB)$? [Nov / Dec – 08]

F = (A+ BC+ AB)
F' = (A+ BC+ AB)'

= A'. (BC)'. (AB)'
= A'. (B'+ C'). (A'+ B')

54. List out the advantages of CMOS logic. [Apr /May – 09]

The advantages of CMOS logic are:

v. Low power consumption: CMOS process provides lower power consumption and is easy to scaling down.
vi. High input impedance: Gate of CMOS needs much lower driving current than base current of bipolar.
vii. Reduced silicon area: Scaling down increases CMOS speed and reduces the area of the chip.
viii. Mature technology: CMOS processes are well established and continue to become more mature. The powerful trust by leading edge digital memory and processors has led to continuous improvement and down scaling of CMOS processes.

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UNIT -2

COMBINATIONAL CIRCUITS

1. What are arithmetic circuits?

Arithmetic circuits are the circuits that perform arithmetic operations.

2. What is a half-adder?

A half adder is an arithmetic circuit that adds two binary digits. It has two inputs and two outputs only (sum and carry)

3. What is a full-adder?

A full adder is an arithmetic circuit that adds two binary digits and a carry, i.e.

Three bits. It has three inputs and two outputs (sum and carry)

4. What is the disadvantage of realizing a full –adder using two half-adder?

The disadvantage of realizing a full-adder using two half-adder is that, in this, the bits must propagate through several gates in succession, which makes the propagation delay greater than that of the full- adder circuit.

5. What is a half-subtractor?

A half-subtractor is an arithmetic circuit that subtracts one binary digit form another. It has two inputs and two outputs (difference and borrow)

6. What is a full-subtractor?

A full-subtractor is an arithmetic circuit that subtracts one binary digit form Another considering a borrow. It has three inputs and two outputs (Difference and Borrow)

7. Why are subtractor ICs not available?

Since subtraction is performed using adders by making use of 1's and 2's complement methods, separate subtraction ICs are not available.

8. What is parallel adder?

A parallel adder is an arithmetic circuit that adds two numbers in parallel form.

9. What is carry propagation delay of a full-adder?

The carry propagation delay of a full-adder in a parallel adder is the time between the application of the carry-in and the occurrence of the carry-out.

10. What do you mean by cascading of parallel adders? Why it required?

Connecting the parallel adders in series, i.e. connecting the carry out of one parallel adder to the carry-in of another parallel adder is called cascading them. It is required when a large number or bits are to be added.

11. How is addition of large binary numbers accomplished?

The addition of large binary numbers can be accomplished by cascading two or more parallel adder chips.

12. What is a combinational logic circuit? Write an example. [May /June – 08]

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called 'combinational logic circuit'.

A combinational circuit consists of input variables, logic gates and output variables. For example, consider following Boolean expression:

$Y = AB + BC + AC$

The combinational logic circuit for this would require 3 AND gates and 1 OR gate which are

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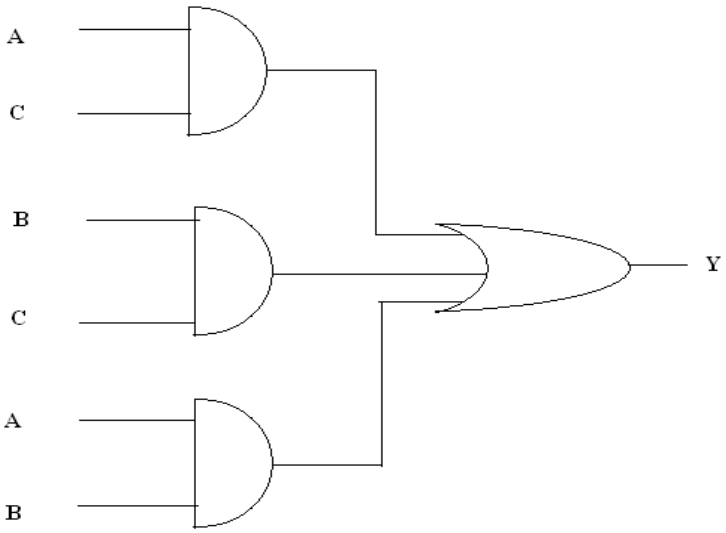
follows:



13. What is a half adder and a full adder? [Dec. /Jan. – 08]

Half adder : The logic circuit which performs the arithmetic sum of two bits is called a half adder.

Full adder : The logic circuit which performs the arithmetic sum of three bits (bit 1: input 1, bit 2:input 2, bit 3: carry from the previous addition) is called a full adder.

14. What is a ripple-carry-adder?

A ripple-carry – adder is parallel adder in which the carry-out of each full adder is the carry-in to the next most significant adder.

15. How does the look-ahead-carry speed up the addition process?

The Look-ahead-carry adder speeds up the addition process by eliminating the ripple carry delay. It examines all the input bits simultaneously and also generates the carry-in-bits for all the stages simultaneously.

16. When is carry generated and when is carry propagated in a look-ahead-carry adder?

The look-ahead-carry adder, a carry-out is generated when both the input bits are1.
A carry-in may be propagated by the full-adder when either or both of the input bits are1.

17. What is a half subtractor and a full subtractor? [May /June – 09]

Half subtractor: It is a combinational circuit that subtracts two bits and produces their difference and borrow.

Full subtractor: It is a combinational circuit that performs a subtraction between 2 bits. It also takes into account borrow of the lower significant stage.

18. What is a serial adder?

A serial adder is a sequential circuit used to add serially binary numbers.

19. Why does a serial adder require only one full-adder?

A serial adder requires only one full-adder because in this the bits are added Serially, i.e. one pair of bits at a time.

20. What is the drawback of serial adders? For which applications are they preferred?

The drawback of serial adder is the serial adders are slower than parallel adders. They are preferred for application where circuit minimization is more important than speed as in pocket calculators.

21. Why serial adders are slower than parallel adders?

Serial adders are slower than parallel adders because they require one clock pulse for each pair of bits added.

22. What are differences between serial and parallel adders?

The parallel adder uses registers with parallel load, whereas the serial adder uses shift registers. The number of full-adder circuits in the parallel adder is equal to the number of bits in the binary numbers, whereas the serial adder requires only full- adder circuits and a carry flip-flop. Excluding the registers, the parallel adder is combinational circuit, whereas the serial adder is a sequential circuit. The sequential circuit in the serial adder consist of full-adder and a flip-flop that stores the output carry.

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23. In what way is a BCD adder different form a binary adder?

While adding BCD numbers, the output is required to be corrected which is not required in the case of binary adders.

24. Compare the hardware requirements of a BCD arithmetic unit and a straight binary arithmetic unit.

Because of the need for correction circuit, the BCD arithmetic unit requires more hardware than the straight binary arithmetic unit.

25. Why is decimal 6 required to be added in a BCD adder if the sum is not a valid BCD number?

16 possible combinations are there with 4 bit number. In BCD only 10 of these are used and the other 6 are skipped. That is why 6 is required to be added.

26. What are code converters?

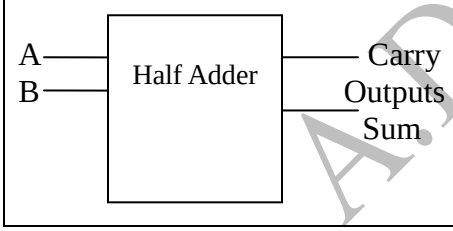
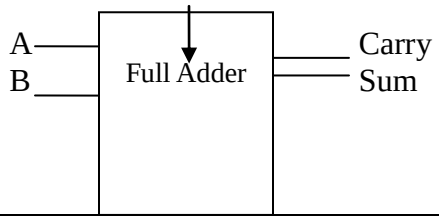
Code converters are logic circuits whose inputs are bit patterns representing numbers or characters in one code and whose outputs are the corresponding

representations in a different code.

27. Compare binary serial adder with binary parallel adder. [Dec. /Jan. – 11]

S.No	Serial Adder	Parallel Adder
1	Serial adder uses shift registers.	Parallel adder uses registers with parallel load capacity.
2	The serial adder requires only one full-adder circuit.	The number of full-adder circuits in the parallel adder equal to the number of bits in the binary numbers.
3	The serial adder is a sequential circuit.	Excluding the registers, the parallel adder is a purely combinational circuit.
4	Time required for addition depends on number of bits.	Time required for addition does not depend on the number of bits.
5	It is slower.	It is faster.

28. List the differences between a half adder and a full adder. [Dec /Jan – 07]

Half adder	**Full adder**
Half adder takes two binary-inputs i.e augend and addend bits and gives out two binary outputs as sum and carry.	Full-adder alongwith augend and addend takes third additional bit Cin as input. Cin represents the carry from the previous lower significant position.
Half-adder is not used in practice	Full-adder is used in practice.
Block diagram: 	Block diagram: 

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29. What is a parity bit generator?

A parity bit generator is a digital circuit that generators a bit called the parity bit to be added to the data bits.

30. What is the basic principle used in order to check or generate the proper parity bit in a given code word?

The basic principle used in order to check or generate the proper parity bit in a given code word is 'the modulo sum of an even number of 1s is always a 0 and the modulo sum of an odd number of 1s is always a 1'

31. How is even parity bit generated for four data bits?

To generate an even parity bit for four data bits, the four data bits are added using three X-OR gates. The sum bit will be the parity bit.

32. How is odd parity bit generated for four data bits?

To generate an even parity bit for four data bits, the four data bits are added using three X-OR gates and the sum bit is inverted.

33. What is a comparator?

A comparator is a logic circuit that compares the magnitudes of two binary numbers. The X – NOR gate(coincidence gate) is a basic comparator.

34. When are two binary numbers equal?

Two binary numbers are equal, if and only if all their corresponding bits coincide.

35. What is an encoder?

An encoder is a device whose inputs are decimal digits and/or alphabetic characters and whose outputs are the coded representations of these inputs.

36. What is an encoding?

Encoding is a process of converting familiar numbers or symbols into a coded format.

37. What is meant by carry propagation delay? [Dec. /Jan. – 09]

In parallel adders, sum and carry outputs of any stage cannot be produced until the input carry occurs. This time delay in the addition process is called carry propagation delay. This delay increases with increase in the number of bits to be added in an adder circuit.

38. What is A ripple ― carry - adder?

A ripple ― carry – adder is parallel adder in which the carry-out of each full adder is the carry-in to the next most significant adder.

39. How does the look-ahead-carry speed up the addition process?

The Look-ahead-carry adder speeds up the addition process by eliminating the ripple carry delay. It examines all the input bits simultaneously, and also generates the carry-in-bits for all the stages simultaneously.

40. Write a short note on one bit comparator. [May /June – 08]

It is a special combinational circuit designed primarily to compare the relative magnitudes of two binary numbers. An n-bit comparator receives two n-bit numbers, A and B

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outputs are: A>B, A=B and A<B. As per the magnitudes of the two numbers, one of the outputs will be high

41. Suggest a solution to overcome the limitation on the speed of an adder. [Dec /Jan – 09]

It is possible to increase speed of adder by eliminating inter-stage carry delay. This method utilizes logic gates to look at the lower – adder bits of the augend and addend to see if a higher-adder carry is to be generated.

42. Differentiate between a demultiplexer and a decoder. [Dec. /Jan. – 09]

S.No	Decoder	Demultiplexer
1	Decoder is a many inputs to many outputs device.	Demultiplexer is a one input to many outputs device.
2	There are no selection lines.	The selection of specific output line is controlled by the value of selection lines.

43. What is a data selector?

Multiplexer is a digital switch. Particularly, it has 2^n input lines and n selection lines whose bit combinations determine which input line is selected and routed onto available only single line.

Hence, multiplexer is a selector of one out of several data sources available at its input lines, to connect it to output line. Simply it is a 'Many into one' device and also called 'data selector'.

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44. List out the differences between DEMUX and MUX. [May /June – 09]

Parameter	Multiplexer	Demultiplexer
Definition	Multiplexer is a digital switch which allows digital information from several sources to be routed on to a single output line.	Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines.
Number of data inputs	2^n	1
No of data outputs	1	2^n
Relationship of input and Output	Many to one	One to many
Applications	1. Used as a data selector. 2. In time division in multiplexing at the transmitting end.	1. Used as a data distributor. 2. In time division multiplexing at the receiving end.

45. What are the applications of Multiplexer and Demultiplexer? [Dec /Jan – 08]

The application of Multiplexer are:

i. They are used in time multiplexing systems.

ii. They are used in frequency multiplexing systems.

iii. They are used in data acquisition systems.

The applications of Demultiplexer are:

i. It can be used as a decoder.

ii. It can be used as a data distributer.

iii. It can be used to implement Boolean expressions.

46. What is arbitration?

In some practical applications, priority encoders may have several inputs that are routinely high at the same time, and the principle function of the encoder in those case is to select that input with the highest priority. This function is called arbitration.

47. What is priority encoder?

A priority encoder is a logic circuit that responds to just one input, in accordance

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with some priority system, among those that may be simultaneously high.

48. The most common priority system is based on what?

The most common priority system is based on the relative magnitudes of the inputs: Whichever decimal digit is the largest is the one encoded.

49. What is a decoder?

A decoder is a logic circuit that converts an *n*-input binary code into a corresponding single numeric output code. In other words, a decoder is a device that identifies or recognizes or detects a particular code.

50. Why a binary-to-octal decoder is called a 1-of-8 decoder?

A binary-to-octal decoder is called a 1-of-8 decoder because only one of the eight outputs is activated at one time.

51. What for are enable inputs used in a decoder?

Enable inputs are used to control the operation of the decoder.

52. What is a multiplexer(MUX)?

A multiplexer or data selector is a logic circuit that accepts several data inputs and allows only one of them at a time to get through to the outputs. It is a N:1 device.

53. What is multiplexing?

Multiplexing means sharing. Selecting 1-out-of-N input data sources and transmitting the selected data to single output channel is called multiplexing.

54.How many types of multiplexing are there? Name them.

There are two types of multiplexing. They are time division multiplexing and frequency division multiplexing.

55. Why is a multiplexer called a data selector?

A multiplexer is called a data selector because it accepts several data inputs and allows only one of them at a time to get through to the output.

56. What are the applications of multiplexers?

Multiplexers are used for data selection, data routing, operation sequencing, parallel-to serial conversion, waveform generation, logic function generation, etc.

57. Can a multiplexer be used to realize a logic function?

This realization is better in the following ways.

(a) Simplification of logic function is not required.
(b) IC package count is reduced.
(c) Reliability of the system is improved because of external wired connections.
(d) It is very easy to change the logic function implemented if and when redesign of a system becomes necessary.

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58. What is the minimum number of selection lines required for selecting one out of *n* inputs lines?

The minimum number of selection lines required for selecting one out of *n* inputs lines is m=log n/ log 2.

59. Can 'strobe' or 'enable' input of a multiplexer be used to increase it size ?

Yes. A 'strobe' or 'enable' input of a multiplexer be used to increase it size .

60. Why is time multiplexing used display system?

Time multiplexing is used in display systems mainly to conserve power.

61. What is a demultiplexer (DMUX)?

A demultiplexer is a logic circuit that depending on the status of its select inputs, channels its data input to one of the several data outputs.

62. Why is a demultiplexer called distributor?

A demultiplexer can be thought of as a distributor since it takes a single input and distributes it over several outputs.

63. Compare a decoder with a demultiplexer.

A demultiplexer has one data input, *m* select lines , and output lines. A decoder, on the other hand, does not have the data input, but the select lines are used as input lines.

64. Can a demultiplxer be used as a logic element? If yes, what are its advantages over realization using gates?

Yes. A demultiplexer can be used as logic element. Its advantages over realization using gates are as follows.

(a) Simplification of logic function is not required.
(b) IC package count is reduced especially in multi-output circuits.
(c) Reliability of the system is improved.

65. What is the type of display used in calculators?

The type of display used in calculators is 7-segment LED/LCD.

66. Is the display used in a digital wristwatch LED or LCD? Why?

The display used in digital wristwatches is usually LCD. It is because LCD requires significantly less power than LED.

67. What is the maximum number of outputs for a decoder with a six bit data word? [May /June – 09]

The number of data inputs bits = 6.The maximum number of outputs for decoder 2^6=64

Unit III - SEQUENTIAL CIRCUITS

A.Devasena

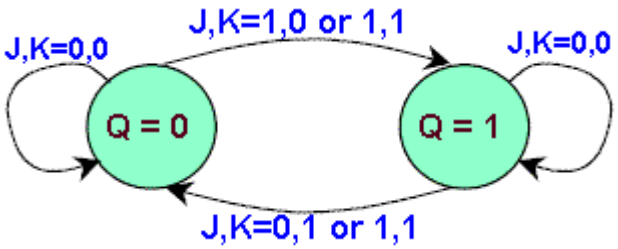
1. What are synchronous sequential circuits? [May/June – 10]

Synchronous sequential circuits are those in which signal can affect the memory element only at discrete instants of time. Clocked flip-flops are examples of synchronous sequential circuits.

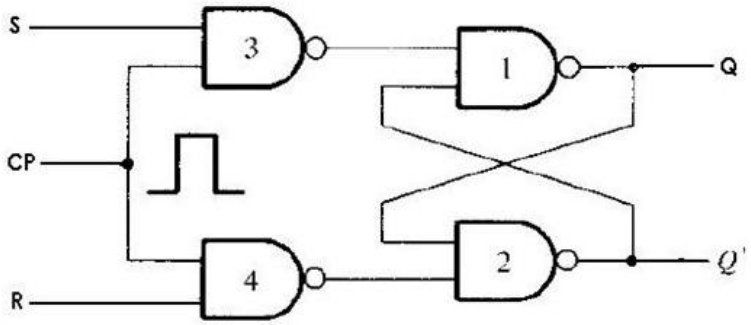
2. Write the characteristic equation and draw the state diagram of JK Flip-flop. [May/June – 10]

Characteristic equation: $Q_{n+1}= JQ'_n=KQ_n$

State Diagram:



3. Draw the logic diagram of SR Flip-flop. [May/June–



SR Flip-flop

4. Define – Sequential Logic Circuit. Write an example. [May/June – 08]

The circuits in which the output variables depend not only on the present input but they also depend upon the past outputs, which are known as sequential logic circuits. Flip-flops, counters and registers are the examples of sequential logic circuit.

5. What are the classifications of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

1) Synchronous sequential circuit.
2) Asynchronous sequential circuit.

6. Define Flip flop.

Flip flop is defined as a digital circuit which maintains its output state either at 1 or 0 until directed by an input signal to change its state.

(Or)

Flip - flop is a sequential device that normally samples its inputs and changes its outputs only at times determined by clocking signal.

7. What are the different types of flip-flop?

There are various types of flip flops. Some of them are mentioned below:

1. RS flip-flop
2. SR flip-flop
3. D flip-flop
4. JK flip-flop
5. T flip-flop

8. What is the operation of RS flip-flop?

- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

9. What is the operation of SR flip-flop?

- When R input is low and S input is high the Q output of flip-flop is Set.
- When R input is high and S input is low the Q output of flip-flop is Reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

10. What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

11. What is the operation of JK flip-flop?

- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change
- When both the inputs K and J are high it is possible to set or reset the flip-flop (ie) the output toggle on the next positive clock edge.

12.What is the operation of T flip-flop?

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T flip-flop is also known as Toggle flip-flop.

- When T=0 there is no change in the output.
- When T=1 the output switch to the complement state (ie) the output toggles.

13. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

14. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

15. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

16. What is a shift registers?

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

17.What are the different types of shift registers?

There are five types shift registers. They are,

1) Serial In Serial Out Shift Register
2) Serial In Parallel Out Shift Register
3) Parallel In Serial Out Shift Register
4) Parallel In Parallel Out Shift Register
5) Bidirectional Shift Register

18. Explain the flip-flop excitation table for RS FF.

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

0 0 transition: This can happen either when R=S=0 or when R=1 and S=0.

0 1 transition: This can happen only when S=1 and R=0.

1 0 transition: This can happen only when S=0 and R=1.

2 1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

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19.Explain the flip-flop excitation table for JK flip-flop.

In JK flip-flop also there are four possible transitions from present state to next state. They are,

0 0 transition: This can happen when J=0 and K=1 or K=0.

0 1 transition: This can happen either when J=1 and K=0 or when J=K=1.

1 0 transition: This can happen either when J=0 and K=1 or when J=K=1.

1 1 transition: This can happen when K=0 and J=0 or J=1.

20. Explain the flip-flop excitation tables for D flip-flop.

In D flip-flop the next state is always equal to the D input and it is independent of the present state. Therefore D must be 0 if Qn+1 has to 0,and if Qn+1 has to be 1 regardless the value of Qn.

21. Explain the flip-flop excitation tables for T flip-flop.

When input T=1 the state of the flip-flop is complemented; when T=0,the state of the flip-flop remains unchanged. Therefore, for 0 0 and 1 1 transitions T must be 0 and for 0 1 and 1 0 transitions must be 1.

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22. Define sequential circuit.

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

23. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits	Sequential circuits
1. Memory unit is not required 2. Parallel adder is a combinational circuit	1. Memory unity is required Serial adder is a sequential circuit

24. What do you mean by present state?

The information stored in the memory elements at any given time defines the present state of the sequential circuit.

25. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

26. What is synchronous sequential circuit?

In synchronous sequential circuits, signals can affect the memory elements only at

discrete instant of time.

27.What is asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

28.Give the comparison between synchronous & Asynchronous sequential circuits.

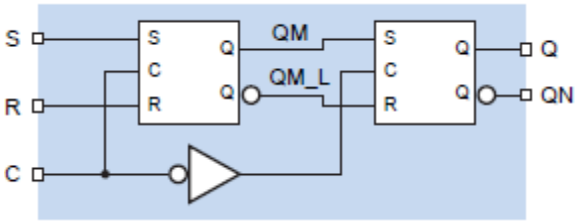
Synchronous sequential circuits	Asynchronous sequential circuits.
1. Memory elements are clocked flip-flops	1. Memory elements are either unlocked flip flops or time delay elements.
2. Easier to design	2.More difficult to design

29.Define – Race Around Condition

In a JK flip-flop , when J = K = 1 and for every clock pulse applied the output changes its state.ie. the output toggles for every clock pulse applied. This condition is called as 'race around condition'.

29. What is a master-slave flip-flop? Write an example.

` A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave. When c = 1, the first flip flop is enabled and thus the master is enabled. When c = 0, the slave flip flop (second one) is enabled.



Master slave S-R flip flop

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30. Write the excitation table for RS FF.

The excitation table for RS FF:

Q_n	Q_{n+1}	R	S
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

31. Write the excitation table for JK flip-flop.

The excitation table for JK flip-flop:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

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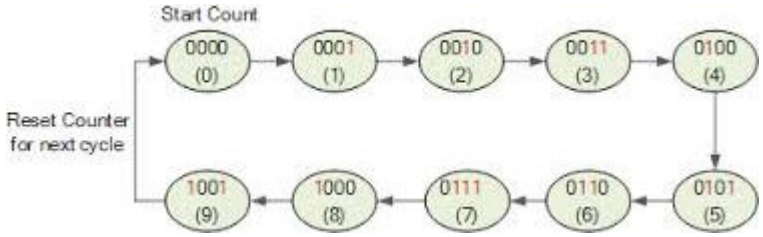
32. Write the excitation table for T flip-flop.

The excitation table for T flip- flop:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

33.Draw the state diagram of MOD-10 counter. [Dec/Jan– 08]



State diagram for mod-10

33. What is synchronous counter? [Dec/Jan– 06]

When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called synchronous counter.

34. **What is a self starting counter? [May/June – 10]**

In a counter, if the next state of some unused state is again an unused state and if by chance, the counter happens to find itself in the unused states and never arrived at a used state, then the counter is said to be in the lockout conditions. The counter which never goes in lockout condition is called self starting counter

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35. What is a shift register? List its types. (D/J – 10)

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

There are five types. They are:

i. Serial in serial out shift register
ii. Serial in parallel out shift register
iii. Parallel in serial out shift register
iv. Parallel in parallel out shift register
v. Bi─ directional shift register

36. **What is the difference between serial transfer and parallel transfer? What is the type of register used in each case? (D/J – 07)**

When data is transferred one bit at a time, the process of transfer is known as serial transfer. When multiple bits are transferred at a time, the process is known as parallel. For parallel transfer, we can use parallel in and parallel out register. For serial transfer we can use left shift or right shift register.

37. What are the basic building blocks of an Algorithmic State Machine? (M/J – 11)

The basic building blocks of an ASM chart are:

i. State box
ii. Decision box and
iii. Conditional box

UNIT4
MEMORY DEVICES

A.Devasena

1. What is a PLD?

A PLD (programmable logic device) is an IC that contains a large number of gates, flip-flops and registers that are interconnected on the chip. Many of the connections, however, are fusible links which can be broken.

2. What is the principal advantage of a PLD?

The principal advantage of PLDs is that in many applications, they can replace a number of the circuits.

3. What is programming?

The fuse blowing process is called programming.

4. What are the advantages of PLDs over fixed function ICs are:

(a) Low development cost (b) Less space requirement
(c) Less power requirement (d) High reliability
(e) Easy circuit testing (f) Easy design modification
(g) High design security (h) Less design time

5. What is a ROM?

A ROM (Read only Memory) is essentially a memory device in which permanent information is stored, Data can only be read from it.

6. What are the technologies used for the fabrication of ROMs?

ROMs and PROMs can be fabricated using bipolar or MOS technology but EPROMs and EEPROMs are possible only with MOS technology.

7. How is the memory size specified?

The memory size is specified as M x N bits where M is the number of locations and N is the number of bits in each location.

8. Is there no provision of entering information in the read only memory? If no what can be read from the memory and if yes why it is called as read only memory.

There is a provision of entering information is ROM. This process is known as programming. In case of programmable ROMs, the ROM is removed form the circuit and is programmed using a PROM programmer, In the case of non-programmable ROM, the information is entered as a part of the fabrication process itself. Because of the requirement of programming it is known as read only memory.

9. A memory has 16 bit address bus. How many locations are there in this?

The number of memory locations in the memory with 16-bit address but = 2^{16} – 65,536-64k.

10. What for is the letter 'K' used in memories?

The k is used in memories to represent 2^{10} memory locations ie 1024 locations.

11. What happens to the information stored in memory location after it has been read?

The reading operation is non-destructive, which means the stored information remains intact after it has been read and can be read any number of times.

12. Explain the programming of ROM.

A ROM is programmed at the time of manufacturing . The information be entered is supplied by the user. The contents of this are fixed at the time of its fabrication and these can never be changed. That means it cannot be erased.

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13. Is the ROM a volatile memory? Explain.

Programming of ROM involves making of the required interconnections at the time of fabrication and, therefore, its contents are unaffected even when the power is off. Thus it is a non-volatile memory.

14. What is a PROM?

A PROM is a ROM which can be programmed.

15. What does a 32 x 8 ROM contain?

A 32 x 8 ROM contains 32 words(addresses)of 8 bits each..

16. Which decoder is contained in a 32 x 8 ROM?

A 32 x 8 Rom contains a 5 x 32 decoder.

17. How many OR gates are there in a 32 x 8 ROM and how many inputs are does each OR gate of a 32 x 8 Rom have ?

A 32 x 8 ROM contains 8 Or gates and each OR gate has 32 inputs

18. What should be the size of a ROM to produce the square of a 3-bit input

The size of the ROM to the square of a 3-bit input .

19. What is the size of decoder in a 32 x 4 ROM?

A 32 x 4 ROM contains a 5 x 32 decoder.

20. What is the size of the decoder in a 8 x 4 ROM?

A 8 x 4 ROM contains a 3 x 8 decoder.

21. What are the types of ROMs?

The various type of ROMs are:

(a) The mask programmed ROMs (MROMs)
(b) Programmable read only memories (PROMs)
(c) Erasable programmable read only memories (EPROMs)
(d) Electrically erasable programmable read only memories(EEPROMs)

22. What is an MROM?

An MROM is a ROM which has its storage locations written into(programmed) by the manufacturer during the last fabrication process of the unit according to the customer's specification . a major disadvantage of MROM is that it cannot be reprogrammed in the event of a design change requiring modification of stored data .

23. What is a PROM?

A PROM is a field programmable ROM. It is not programmed during the manufacturing processes but is custom programmed by the user. Once programmed, the date cannot be altered. PROMs are manufactured with fusible links.

24. Is the PROM volatile or Non-volatile?

It is Non-volatile similar to the ROM.

25. What are the technologies used for the fabrication or ROMs

MROMs and PROMs can be fabricated sung bipolar or MOS technologies, but EPROMs and EEPROMs are possible only with MOS technology.

26. How can a ROM device be considered as a combinational circuit?

A ROM device has M locations and N bits are stored at each location. Each location has its unique address, Therefore, it the signals corresponding to the input variables are applied at the address input pins or ROM, then the contents stored at that location are available at output pins. Thus, it operates as a combinational circuit.

27. Is it possible to locate any ROM location at random?

Any ROM location can be selected for reading (or accessed) at random by applying the corresponding input variables at the address input pins.

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28. Is it possible to design multiple output circuits using ROM?

Multiple output circuits can be designed using ROM by selecting a ROM which has the number of bits at each location at least equal to the number of outputs desired.

29. What is an EPROM?

An EPROM is a Rom whose contents can be erased and reprogrammed enabling the device to be used repeatedly. Its contents can be erased by exposing it to ultraviolet light. Selective erasure is not possible.

30. Differentiate between PROM and EPROM .

A PROM can be programmed only once whereas an EPROM can be programmed any number of times.

31. In an EPROM chip, is it possible to erase the contents of only some of the locations? If not, Why?

No, When the chip is exposed to UV radiation, all the contents get erased simultaneously. It is not

32. Some information is stored in EPROM which is required to be modified. How will you do it?

First, whatever is stored should be erased by exposing the EPROMs UV radiation and then it is programmed to store the new information.

33. What is an EEPROM?

An EEPROM or EAROM is a ROM whose contents can be electrically erased and reprogrammed enabling the device to be used repeatedly . Selective erasure is possible.

34. What are the two major disadvantages of EPROM ?

The two major disadvantages of EPROM are as follows:

(a) They have to be removed form their sockets in order to be erased and reprogrammed.
(b) The erasure remove the complete memory contends. This necessitates complete reprogramming even when one memory word has to be changed.

35. What a combinational PLD?

A combinational PLD is an IC with programmable gates divided into an AND array and an OR array to provide an AND-OR sum of products implementation.

36. What is a combinational PLDs?

There are three major types of combinational PLDs and they differ in the placement of the programmable connection in the AND-OR array. The various PLDs used are PAL (programmable array logic), PLAs(programmable logic Arrays'), and PROMs (programmable read only memories) .

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37. What is a PAL?

BVVC` A PAL is a combinational PLD with a programmable AND array and fixed OR array.

39. What is a PLA?

A PLA is a combinational PLD with both programmable AND and OR array.

40. What is a FPLA ?

FPLA is a field programmable logic array. It can be programmed by the user by means of certain recommended procedures.

41. What is the programming table of a PLA?

The programming table of PLA is a table specifying the fuse map of a PLA.

42. How is the size of a PLA is specified ?

The size of a PLA is specified by the number of inputs, the number of product terms and the number of outputs.

43. What is a fuse map?

A fuse map is a map that shows which fuses to blow.

44.What is the basic architecture of a PLA?

A PLA consists of an array of programmable AND and OR gates. The number of inputs to every AND gate is twice the number of input variables possible for a chip, and the number of inputs to every OR gate is equal to the number of AND gates. The outputs of the OR gates give the output of the realized logic functions.

45. How is the capacity of a PLA specified?

The Capacity of a PLA is specified as the number of inputs product terms and outputs.

46. Are PLAs and FPLAs are non-volatile.

PLAs and FPLAs are non-volatile.

47. Are erasable and programmable PLAs available?

A. No. Erasable and programmable PLAs are not available.

48. Is it possible to share the product terms between different outputs in a PLA? If yes, how?

Yes, Since each OR gate may be connected to all the product terms, the output of the AND gate with product terms required for different output functions can be connected to corresponding OR gates.

49. Is it possible to share the product terms between different outputs in a PAL? Justify your answer.

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No. In a PAL the OR gates are non-programmable. Every AND gate can supply input to only one OR gate. Therefore, it is not possible to share the product terms between different outputs.

50. What are the advantages and disadvantages of using a PROM as a PLD?

The advantages of using a PROM as a PLD are as follows:

(a) Ease of design since no simplification or minimization of logic function is required.

(b)Design can be changed, modified rapidly,

(c) It is usually faster than discrete SSI/MSI circuit.

(d) Cost is reduced.

The disadvantages of using ROM based circuits as PLDs are as follows:

(a)Non-utilization of complete circuit.

(b) Increase of power requirement and enormous increase in size with increase in the number of input variables making it impractical.

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UNIT V
SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS

1. What is sequential machine?

A sequential machine is nothing but a sequential circuit represented by a block or

a module with inputs and outputs indicated. Digital computers and digital communication systems are examples of synchronous sequential machines.

2. What are finite state machines?

Finite state machines are those machines whose past histories can affect their future behavior only in a finite number of ways, i.e they are machines with a finite number of states. They are abstract models describing the synchronous sequential machines.

3. List the various memory elements used in sequential machines.

The various memory elements used in sequential machines are D flip-flop, T flip-flop, SR flip-flop, and J-K flip-flop.

4. How is the state of the memory element specified?

The memory element has two states. Its state is specified by the value of its output which may assume either a 0 or a 1. It is represented by a state variable.

5. What do you mean by the term 'state diagram'? What do the vertices, the directed arcs, and the labels on the arcs of a state diagram represent?

The state diagram or state graph is a pictorial representation of the relationships between the present state, the input ,the next state, and the output of the finite state sequential machine. The vertices (nodes) of the graph represent the states of the machine. The directed arcs emanating from each vertex indicate the state transitions caused by various input symbols (i.e.the direction of arrows point to the next state that the machine will go after the input is applied). The label on the directed arc indicates the input symbol that causes the transition, and the output symbol that is to be generated.

6. What is state assignment?

The process of assigning the states of physical devices to the states of a sequential machine is known as state assignment.

7. What do you mean by the term 'state table'? What does each row, column and entry of the state table represent?

The state table is a tabular representation of the relationship between the present state, the input, the next state and the output. Each column of the state table corresponds to one input symbol, and each row of the state table corresponds to one state. The entries corresponding to each combination of the input symbols and the present state specify the output that will be generated and the next state to which the machine will go.

8. Compare the state diagram and the state table.

Both the state diagram and the state table contain the same information and the choice between the two representations is a matter of convenience. Both have the advantage of being precise, unambiguous, and thus more suitable for describing the

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operation of a sequential machine than that by any verbal description. The succession of states through which a sequential machine passes and the output sequence which it produces in response to a known input sequence are specified uniquely by the state diagram or by the state model and the initial state.

9. What do you mean by initial state and final state?

The initial state refers to the state of the machine prior to the application of the input sequence and the final state refers to the state of the machine after the application of the input sequence.

10. What is an excitation table? What information does it give?

An excitation table is a table which lists the present states, the excitations and the next states. It gives information about the excitations or inputs required to be applied to the memory elements in the sequential circuit to bring the sequential machine from the present state to the next state. It also gives information about the outputs of the machine after application of the present inputs.

11. What is transition and output table?

The transition and output table of a sequential machine is a table which lists the present state, the next state to which it will go and the output it produces. It can be obtained from the state table by modifying the entries of the state table to correspond to the states of the machine, in accordance with the selected state assignment. In this table the next state and output entries are separated into two sections. The next state part of the state table is called the transition table.

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12. Define an input alphabet and an output alphabet.

The set of all possible combinations of inputs is called an input alphabet and the set of all possible combinations of outputs is called an output alphabet.

13. What are state variables?

The output values of physical devices are referred to as state variables.

14. What is the Mealy model of the state diagram of a memory element?

In the Mealy model of the state diagram each node in the state diagram represents a particular state of the FF (0 or 1). The labels on the arcs indicate the input/output, i.e. the input that is given when the FF is in a particular state and the corresponding output. The directions of the arrows point to the next state the FF will go after the input is applied.

15. What is the Moore model of the state diagram of a memory element?

In the Moore model of the state diagram, the state code and the value of the output are written inside the circle. The directed line joining one node to the other, or looping back to the same node has the value of the input written beside the line.

16. What is a serial binary adder?

A serial binary adder is a sequential circuit which adds two binary numbers serially.

17. What is a sequence detector?

A sequence detector is a sequential machine which produces an output 1 every time the desired sequence is detected, and an output 0 at all other times.

18. What is a serial parity-bit generator?

A serial parity-bit generator is a two terminal circuit which receives coded messages, so that the resulting outcome is an error- detecting coded message.

19. By how many models are synchronous sequential circuits represented? Name them.

Synchronous or clocked sequential circuits are represented by two models.

They are:

i. Moore circuit (or model)
ii. Mealy circuit (or model)

20. What is a Mealy machine?

The Mealy machine (circuit or model) is a sequential circuit in which the output depends on both the present state of the flip-flops and on the inputs.

21. What is a Moore machine?

The Mealy machine (circuit or model) is a sequential circuit in which the output depends only on the present state of the flip-flops.

22. Compare Moore and Mealy machines.

S.No	Moore machine	Mealy machine
1	Its output is a function of present state only. $z(t)=g\{S(t)\}$	Its output is a function of present state as well as present input. $z(t)=g\{S(t),x(t)\}$
2	Input changes do not affect the output	Input changes may affect the output of the circuit.
3	It requires more number of states for implementing same function.	It requires less number of states for implementing same function.

23. What are the capabilities and limitations of finite state machine?

The capabilities and limitations of finite state machines are as follows:

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1. With an n-state machine, we can generate a periodic sequence of n states or less than n states.
2. Certain infinite sequence cannot be produced by a finite state machine.
3. The finite state machine has limited memory and due to limited memory it cannot produce certain outputs.

24. What do you mean by successor?

If an input sequence X takes a machine from state S_i to state S_j, then S_j is said to be the X- successor of S_i .

25. What do you mean by terminal state?

A terminal state is a state with no incoming arcs which start from other states and terminate on it.

26. What is a strongly connected machine?

A sequential machine M is said to be strongly connected, if for every pair of states S_i ,S_j of the sequential machine, there exists an input sequence which takes the machine M from S_i to S_j .

27. What are redundant states?

Redundant states are states whose functions can be accomplished by other states.

28. What are equivalent states?

Two states are said to be equivalent if for every possible set of inputs they generate exactly the same output and the same next state.

29. What is the advantage of having equivalent states?

When equivalent states are there, one of them can be retained and all others can be removed without altering the input-output relationship because they are redundant. This results in reduction of states which in turn reduces the number of required flip-flops and logic gates reducing the cost of the final circuit.

30. State 'state equivalence theorem'.

The state equivalence theorem states that two states S_A and S_B of a sequential machine are equivalent if and only if for possible input sequence X, the outputs are the same and the next states are equivalent. That is, if $S_A (t+1) = S_B (t+1)$ and $Z_A=Z_B$, then $S_A = S_B$.

31. What is a distinguishing sequence?

An input sequence which distinguishes two states is called a distinguishing sequence.

32. What are distinguishable states?

Two states S_A and S_B of a sequential machine are distinguishable if and only if

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there exists at least one finite input sequence which when applied to the sequential machine causes different output sequences depending on whether S_A and S_B is the initial state.

33. What are K-distinguishable states?

Two states are said to be K-distinguishable, if they have a distinguishable sequence of length K.

34. Write the Moore reduction procedure for minimization of completely specified sequential machines using the partition technique.

The procedure for minimization and determination of n-equivalence using the partition technique is:

Step1: Partition the states into subsets such that all states in the same subset are 2-equivalent.

Step 2: Partition the states into subsets such that all states in the same subset are 2-equivalent.

Step 3: Partition the states into subsets such that all states in the same subset are 3-equivalent and so on till further partitioning of states is not possible. The last partition called the equivalence partition defines the sets of equivalent states of the sequential machine.

35. What is machine equivalence?

Two machines M_1 and M_2 are said to be equivalent if and only if for every state in M_1 , there is a corresponding equivalent state in M_2 and vice versa.

36. What are incompletely specified machines?

The sequential circuits whose state transitions or output variables are not completely specified are called incompletely specified machines.

37. What is the advantage of unspecified outputs?

The advantage of leaving outputs unspecified as long as possible during the state reduction process is, this provides additional flexibility in state reduction process.

38. Define state compatibility.

Two states S_i and S_j of a sequential machine are said to be compatible states, if and only if for every input sequence that affects the two states, the same output sequence occurs whenever both outputs are specified and regardless of whether S_i and S_j is the initial state.

39. What is merger graph?

The merger graph is a state reducing tool used reduce states in the incompletely specified machine. The merger graph is defined as follows:

1. It contains the same number of vertices as the state table contains states.
2. Each compatible state pair is indicated by an unbroken line drawn between the two state vertices.

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3. Every potentially compatible state pair with outputs not in conflict but whose next states are different is connected by a broken line. The implied states are written in the line break between the two potentially compatible states.
4. If two states are incompatible, then no connecting line is drawn.

40. What are maximal compatibles?

A set of compatible state pairs which is not completely covered by any other set of compatible state pairs is called a set of maximal compatibles.

41. What are the other names of the merger table method?

The merger table method is also called the paull-Unger method or implication chart method.

42. What is merger table?

A merger table is a table in which each cell shows the compatible pairs and their implications.

43. How do you obtain the set of all maximal compatibles from the merger table?

From the merger table, the set of all maximal compatibles is obtained as follows:

1. Begin with the rightmost column in the merger table and proceed left until a column containing a compatible pair is encountered. Write the set of all compatible pairs in this column.
2. Proceed left to the next column containing at least one compatible pair. If the state to which this column corresponds is compatible with all the states in the set of previously determined compatible states, then add this state to that set of compatible states to form a larger compatible. If the state is not compatible with all the states of previously determined set, but is compatible with some other state, form a new set of compatible states.
3. Repeat step 2 until the leftmost column is reached. The sets in the leftmost column give the set of maximal compatibles.

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44. What is compatibility graph?

The compatibility graph is a directed graph whose vertices correspond to all compatible pairs, and an arc leads from vertex (S_i, S_j) to vertex (S_p, S_q) if and only if (S_i, S_j) implies(S_p, S_q). The compatibility graph can be easily drawn from the merger graph or merger table.

45. What is sub graph of a compatibility graph?

Any part of a compatibility graph is called the sub graph of the compatibility graph.

46. What is a closed subgraph?

A subgraph of a compatibility graph is said to be closed if for every vertex in the subgraph all outgoing arcs and their terminating vertices also belong to the subgraph.

Each vertex in the subgraph belongs to one state. Such a subgraph forms a closed covering for the corresponding machine.

47. What is a minimal cover table?

A minimal cover table is a table which consists of the states of a minimal state machine.

48. How does the operation of an asynchronous input differ from that of a synchronous input? (D/J – 05)

Asynchronous sequential circuits do not use clock pulses. The change of interval state occurs during the short time of the pulse transition.

Synchronous sequential circuits use clock pulses. The clock pulses determine the computational activity which should occur within the circuit.

49. What is a fundamental mode asynchronous sequential circuit? (M/J – 03)

In fundamental mode asynchronous sequential circuits, the external inputs can change at any time and a transition from one state to another state occurs only when changes in the input occur. The inputs and outputs are represented by voltage levels rather than by pulses.

50. What is a flow table in asynchronous sequential circuits? (M/J – 07)

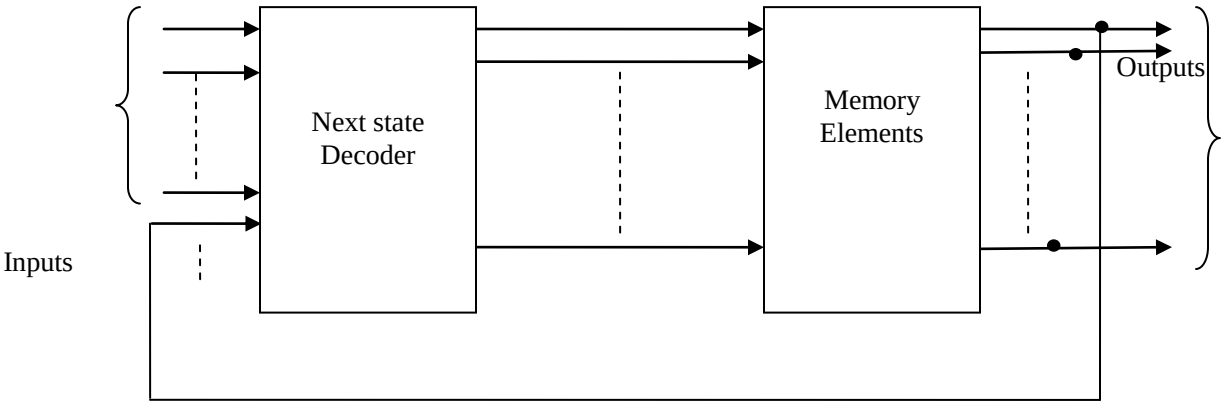
A flow table is similar to a transition table except that the internal states are symbolized with letters rather than binary numbers. The flow table includes the output values of the circuit for each stable state.

51. Define – Primitive Flow Table (D/J – 08)

It is a flow table which has exactly one stable state for each row in the table.

52. Draw the block diagram of Moore model. (M/J – 10)

Moore Circuit model



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