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1. FPGA means

a. Field Programmable Gate Array

b. Forward Programmable Gate Array

c. Forward Parallel Gate Array

d. Field Parallel Gate Array

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2. Which language could be used for programming an FPGA.

a. Verilog

b. VHDL

c. Both A and B

d. None of the above

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3. The program counter in a 8085 micro-processor is a 16-bit register, because

a. It counts 16-bits at a time

b. There are 16 address lines

c. It facilitates the user storing 16-bit data temporarily

d. It has to fetch two 8-bit data at a time

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Answer: (b).
There are 16 address lines

4. A microprocessor is ALU

a. and control unit on a single chip.

b. and memory on a single chip.

c. register unit and I/O device on a single chip.

d. register unit and control unit on a single chip.

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Answer: (d).
register unit and control unit on a single chip.

5. Basic steps of execution of an instruction is

a. fetch → execute → decode

b. decode → fetch → execute

c. execute → fetch → decode

d. fetch → decode → execute

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Answer: (d).
fetch → decode → execute

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6. A microprocessor with a 12-bit address bus will be able to access

a. 1 K bytes

b. 4 K bytes

c. 8 K bytes

d. 10 K bytes

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Answer: (b).
4 K bytes

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7. DMA is used between

a. microprocessor and I/O

b. microprocessor and memory

c. memory and I/O

d. none

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Answer: (c).
memory and I/O

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8. Which of the data transfer is not possible in microprocessor

a. memory to accumulator

b. accumulator to memory

c. memory to memory

d. I/O device to accumulator

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Answer: (c).
memory to memory

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9. Which one of the following statement is false?

a. A microprocessor has bi-directional address bus

b. A microprocessor has unidirectional address bus

c. A microprocessor has bi-directional data bus

d. A microprocessor has an ALU

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Answer: (a).
A microprocessor has bi-directional address bus

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10. In microprocessor based system DMA refers to

a. direct memory access for microprocessor

b. direct memory access for the user

c. direct memory access for the I/O device

d. none of the above

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Answer: (c).
direct memory access for the I/O device

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