

* Digital Electronics and Logic Design (DELD) - Practical Number - 9

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Title:-

Ripple Counter

Aim:-

Design of 2 bit and 3-bit ripple counter using MS-JK flip flops.

Objective:-

To design 2-bit and 3-bit ripple counter with help of MS-JK flip-flops.

Theory:-

Asynchronous counter / Ripple Counter:-

A digital counter is set of flip-flops. An ripple counter uses T flip flop to perform a counting function. In ripple counter, first flip flop is clocked with clock pulse and then each successive flip-flop is clocked by Q and \bar{Q} .

Types:-

- ① Up Counter
- ② Down Counter.

Truth Table and Logic Diagrams:-

A) 2-bit Ripple Counter.

① Up Counter ->

Counting State	Output	
	Q_A	Q_B
0	0	0
1	0	1
2	1	0
3	1	1

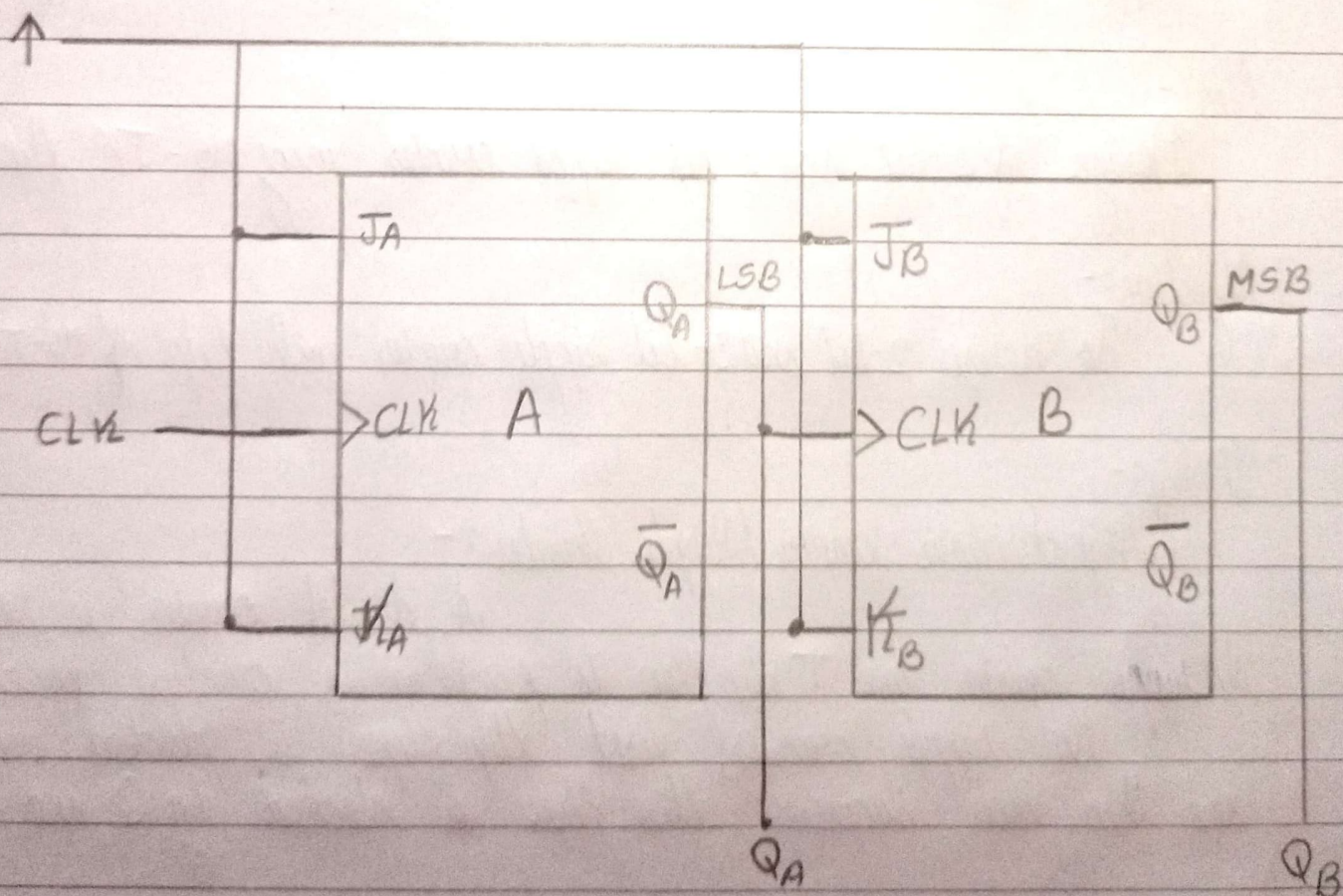


fig:- 2 bit Up counter.

② Down Counter \rightarrow

Counter State	Output	
	Q_A	Q_B
3	1	1
2	1	0
1	0	1
0	0	0

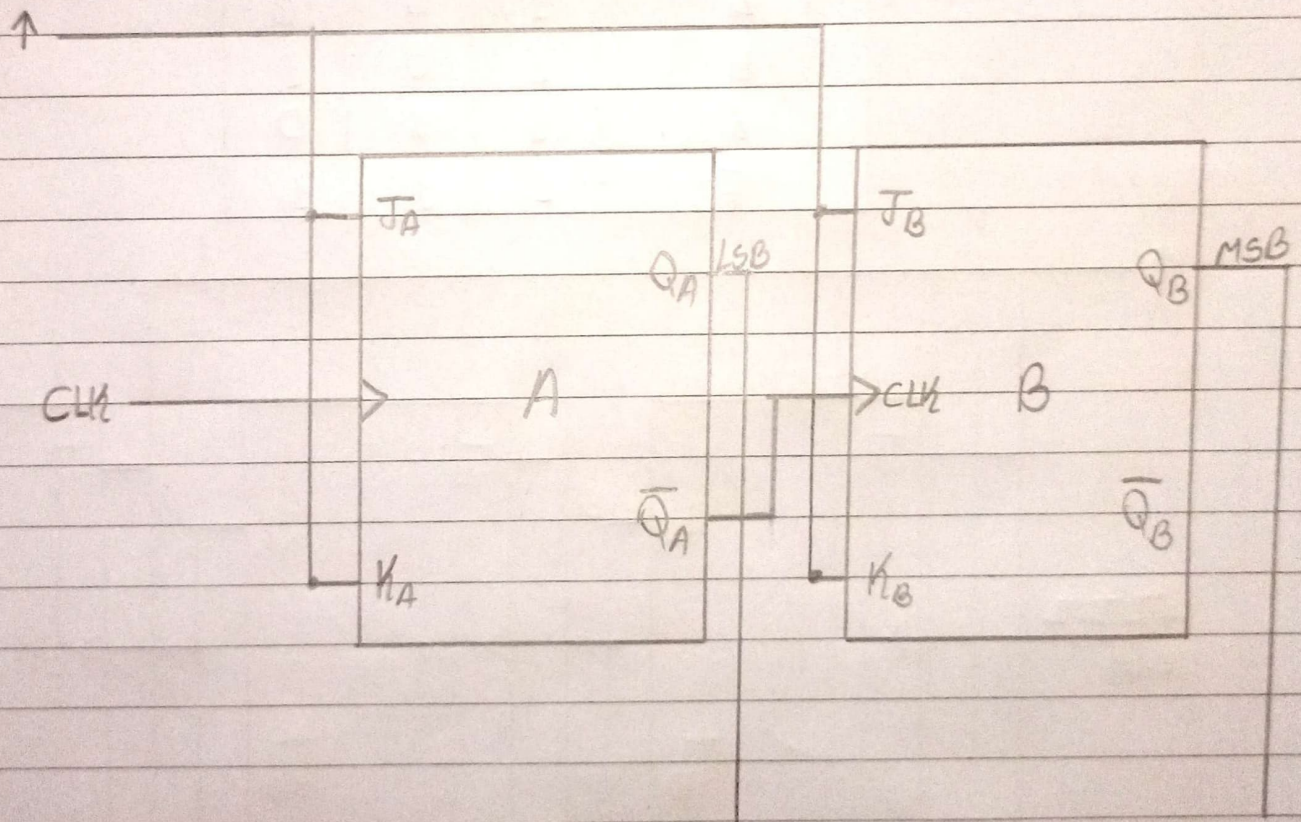


fig :- 2-bit Down counter.

B) 3-bit Ripple Counters

① Up Counter:-

Counter State	Output		
	Q_A	Q_B	Q_C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

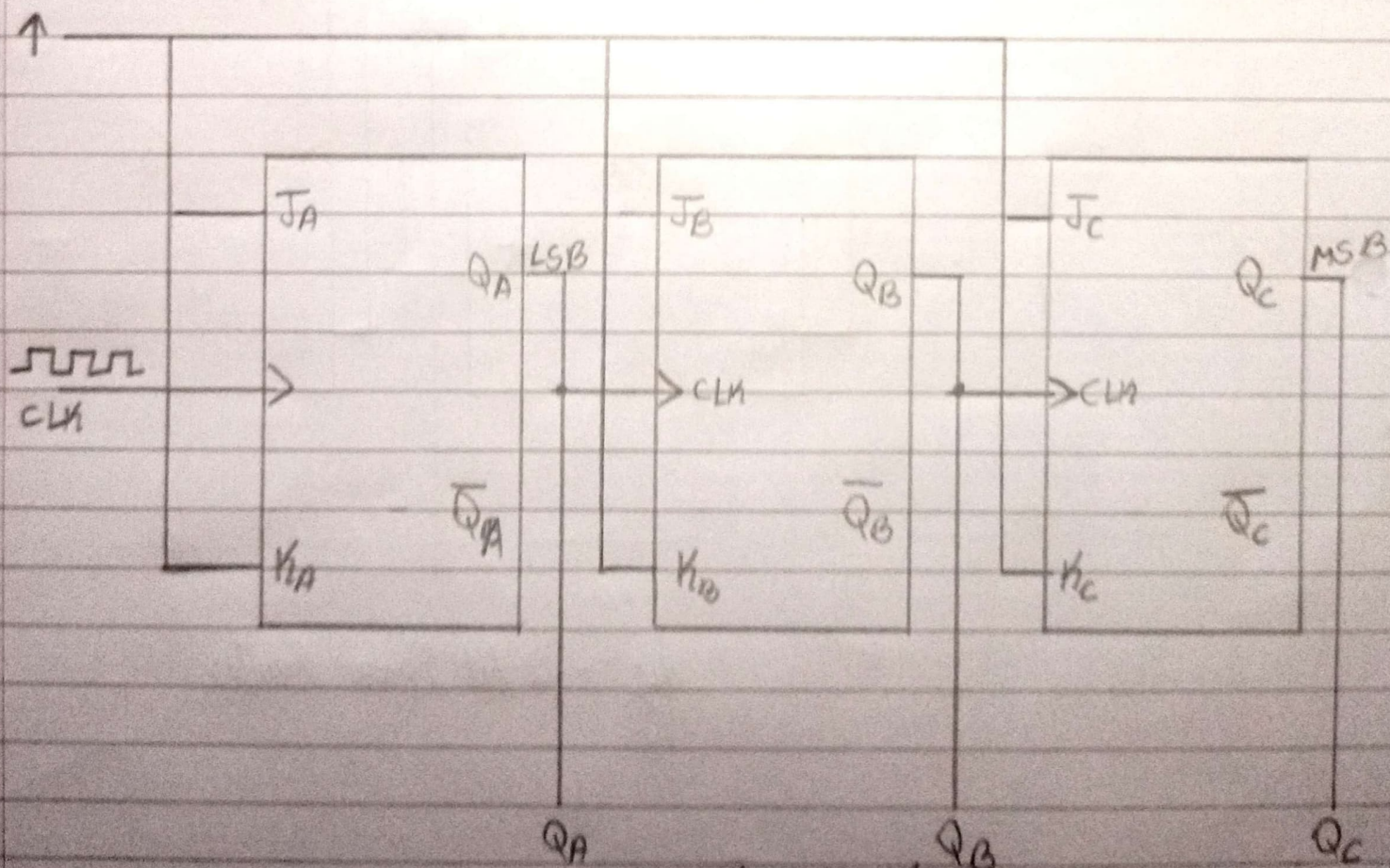


fig:- 3-bit Up Counter

② Down Counter:->

Counter State	Output		
	Q _A	Q _B	Q _C
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

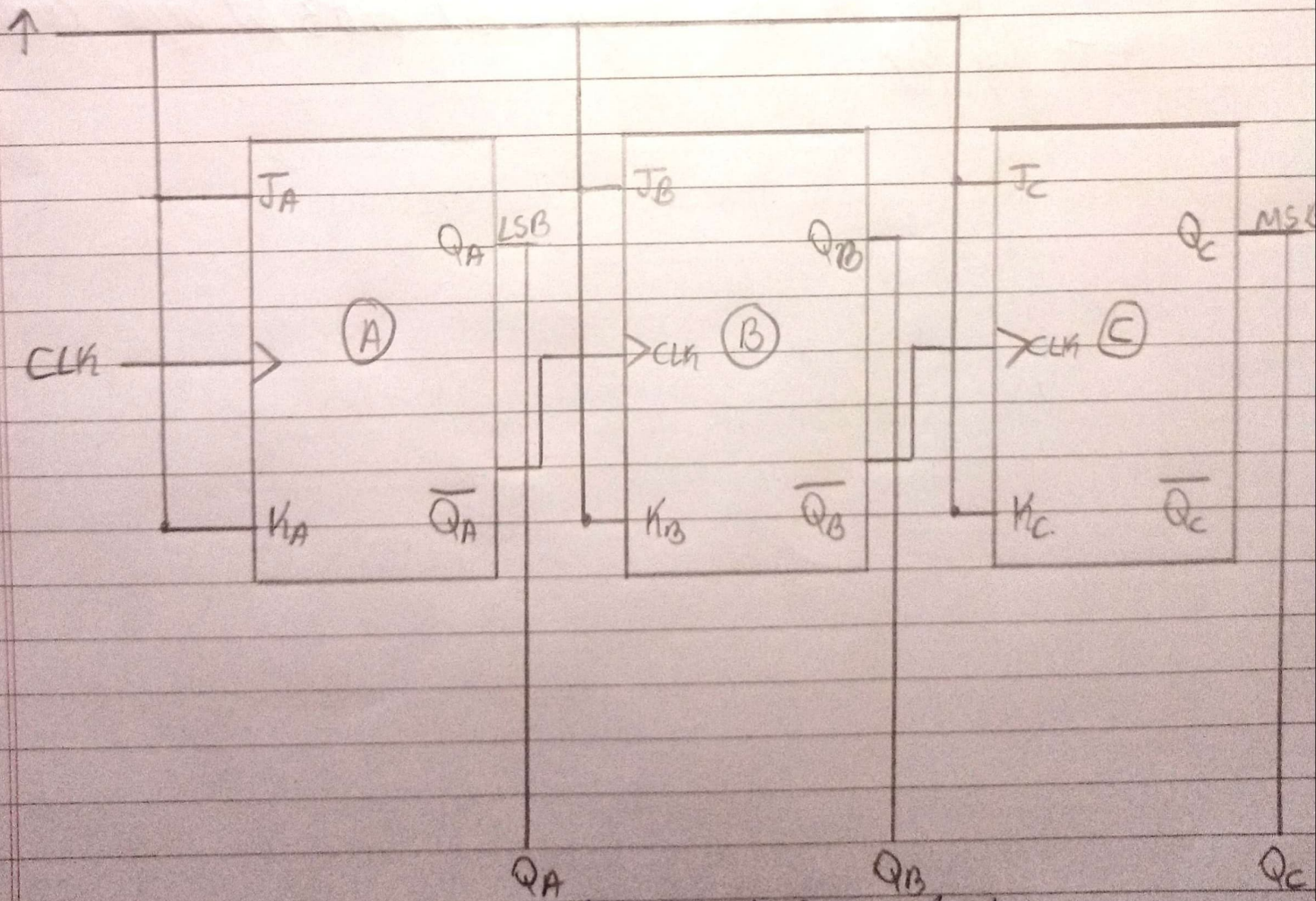


fig:- 3-bit Down Counter.

Uses:-

- ① Spinning devices
- ② Pulsed motor
- ③ Work for dividing frequency.

Outcome:-

Thus we implemented up and down ripple counter using IC 7476.

Conclusion:-

Hence, we have design 2 bit and 3 bit ripple counter using MSJK flip flop.