* Digital Electronics and Logic Design (DELD) - Practical Number - 9

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Div :- A
Batch :-
Department :- Computer Department.
College :- AISSMS's IOIT.

Title :-
Ripple Counter

Aim :-
Design of 2 bit and 3-bit ripple counter using MS-JK flip flops.

Objective :-
To design 2-bit and 3-bit ripple counter with help of MS-JK flip-flops.

Theory :-
Asynchronous counter / Ripple Counter :-
A digital counter is set of flip-flop
An ripple counter uses T flip flop to perform a counting function.
In ripple counter, first flip flops is clocked with clock pu
and then each successive flip-flop is clocked by Q and $\bar{Q}$.

Types :-
① Up Counter
② Down Counter.

Truth Table and Logic Diagrams :-

A) 2-bit Ripple counters

① Up counter →

Counting State	Output	
	Q_A	Q_B
0	0	0
1	0	1
2	1	0
3	1	1

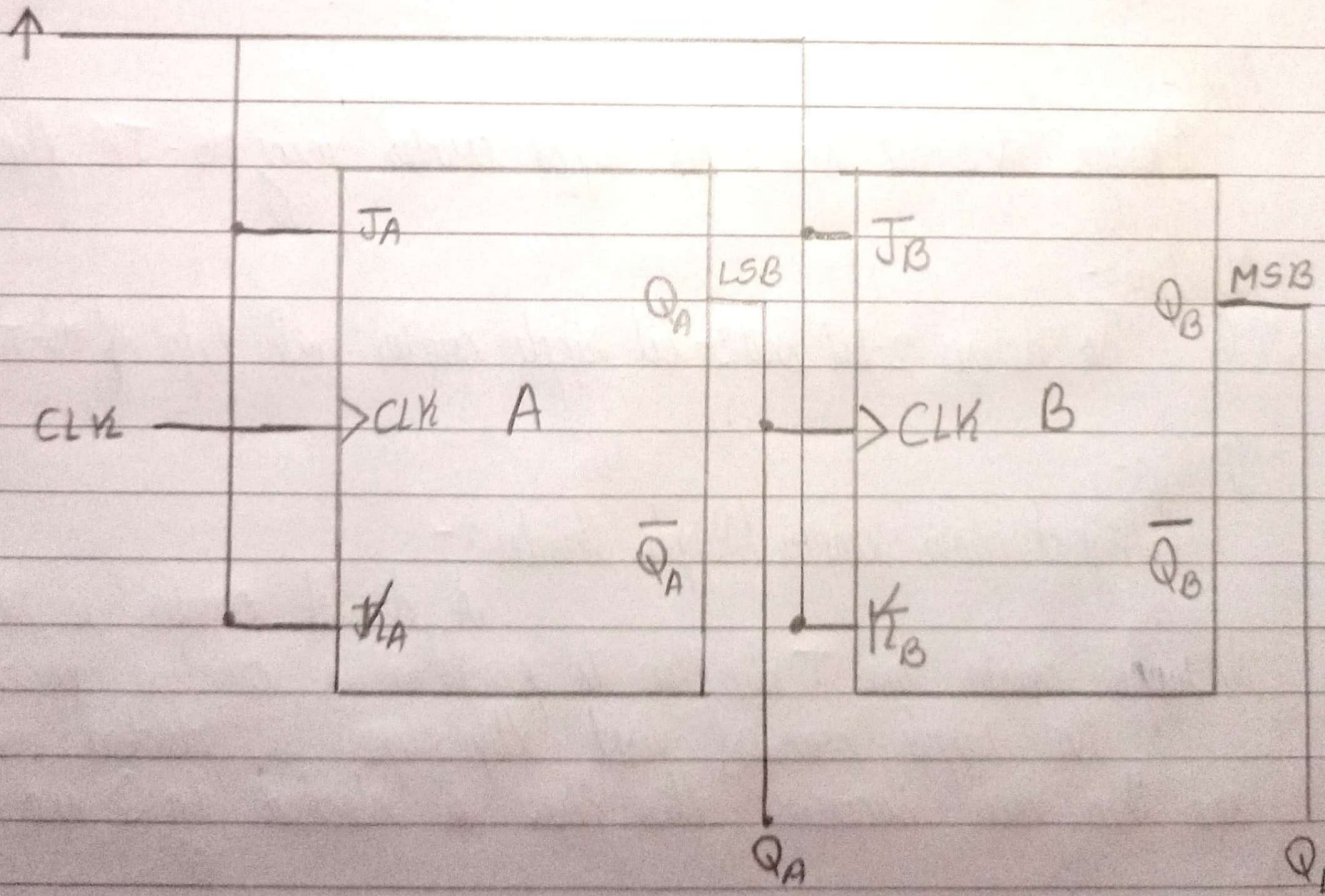
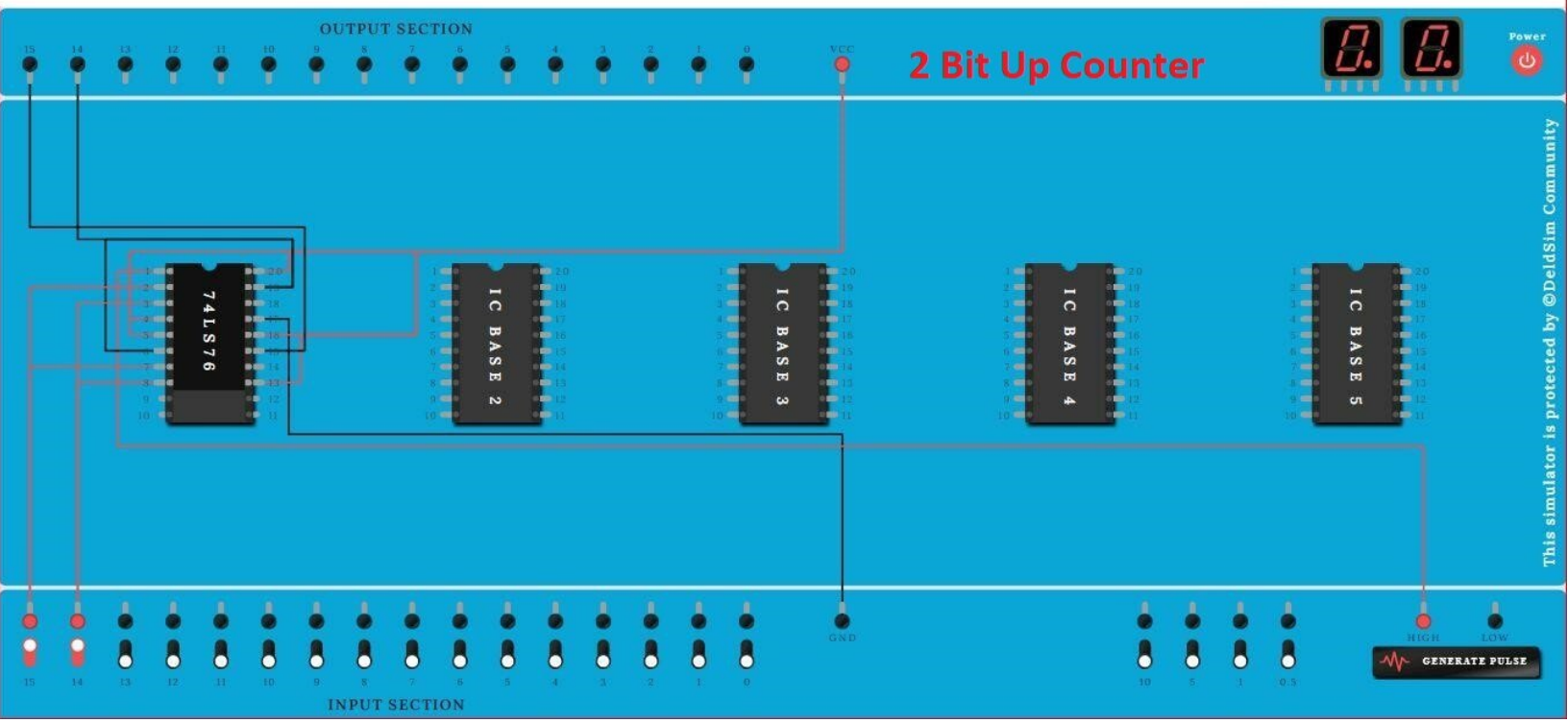


fig:- 2 bit Up counter.


OUTPUT SECTION
VCC
2 Bit Up Counter
Power
74LS76
IC BASE 2
IC BASE 3
IC BASE 4
IC BASE 5
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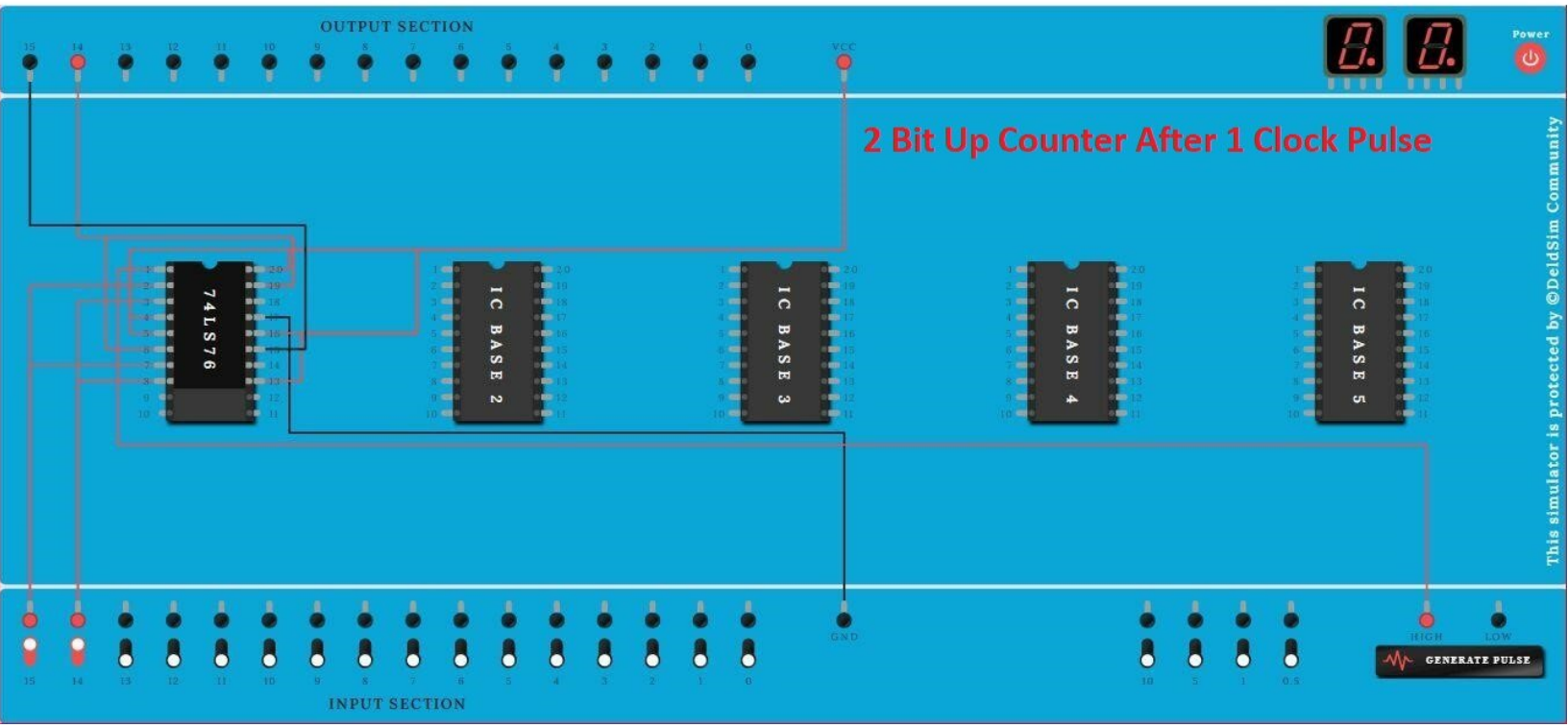
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION


OUTPUT SECTION
VCC
2 Bit Up Counter After 1 Clock Pulse
Power
74LS76
IC BASE 2
IC BASE 3
IC BASE 4
IC BASE 5
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GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION

② Down counter →

Counter State	Output Q_A	Q_B
3	1	1
2	1	0
1	0	1
0	0	0

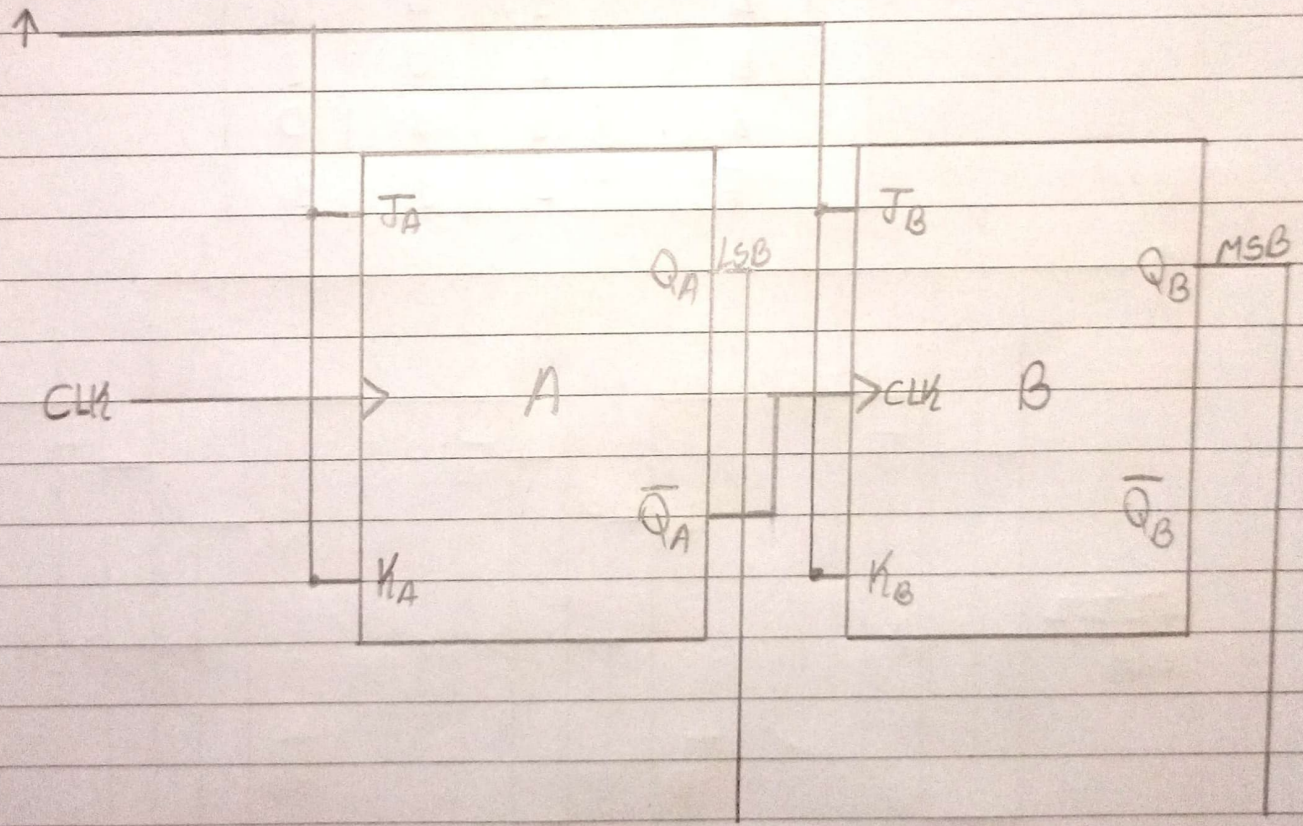
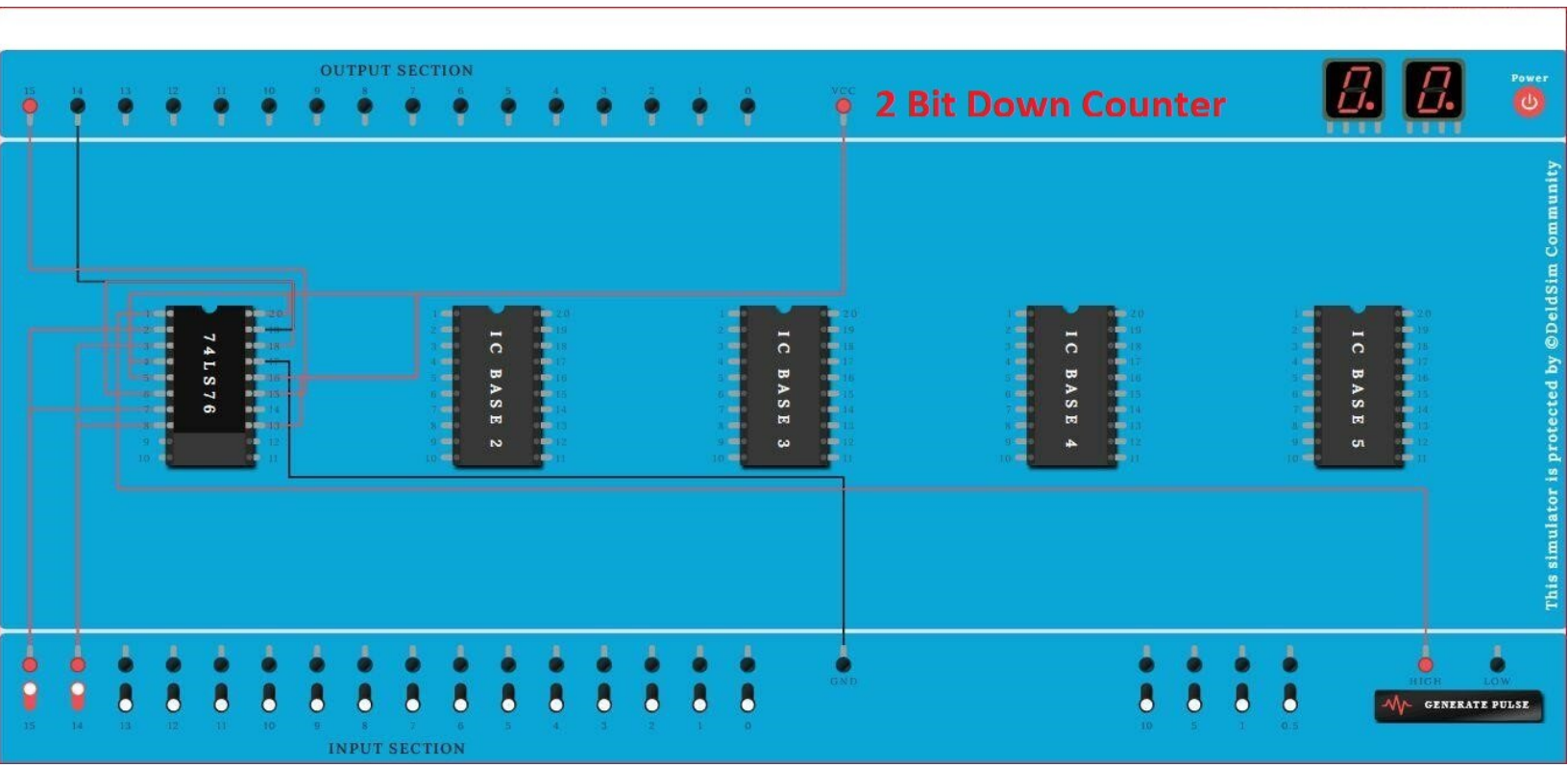


fig :- 2-bit Down counter.


OUTPUT SECTION
2 Bit Down Counter
Power
74LS76
IC BASE 2
IC BASE 3
IC BASE 4
IC BASE 5
VCC
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION
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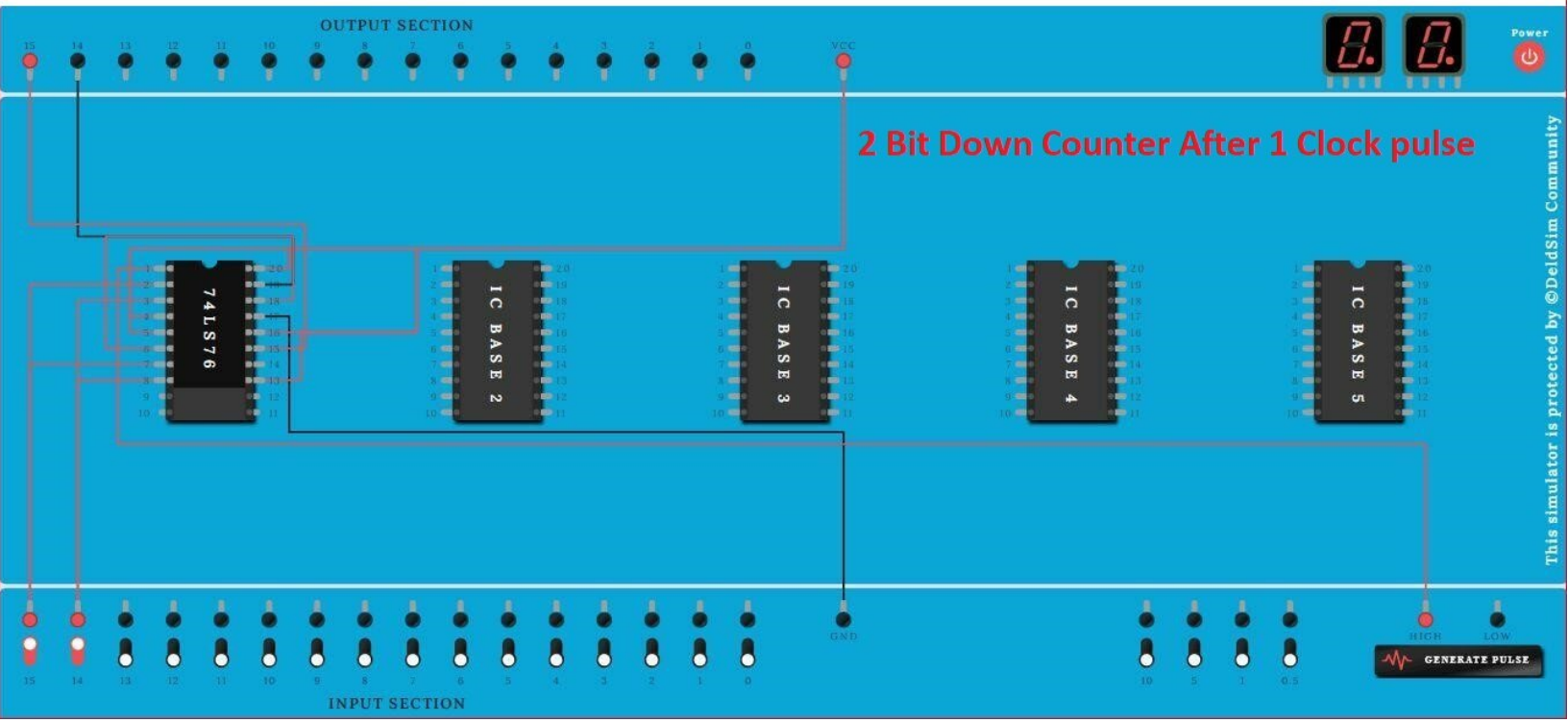
OUTPUT SECTION
2 Bit Down Counter After 1 Clock pulse
Power
74LS76
IC BASE 2
IC BASE 3
IC BASE 4
IC BASE 5
VCC
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION
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B) 3-bit Ripple counters

① Up counter :-

Counter State	Output		
	Q_A	Q_B	Q_C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1.

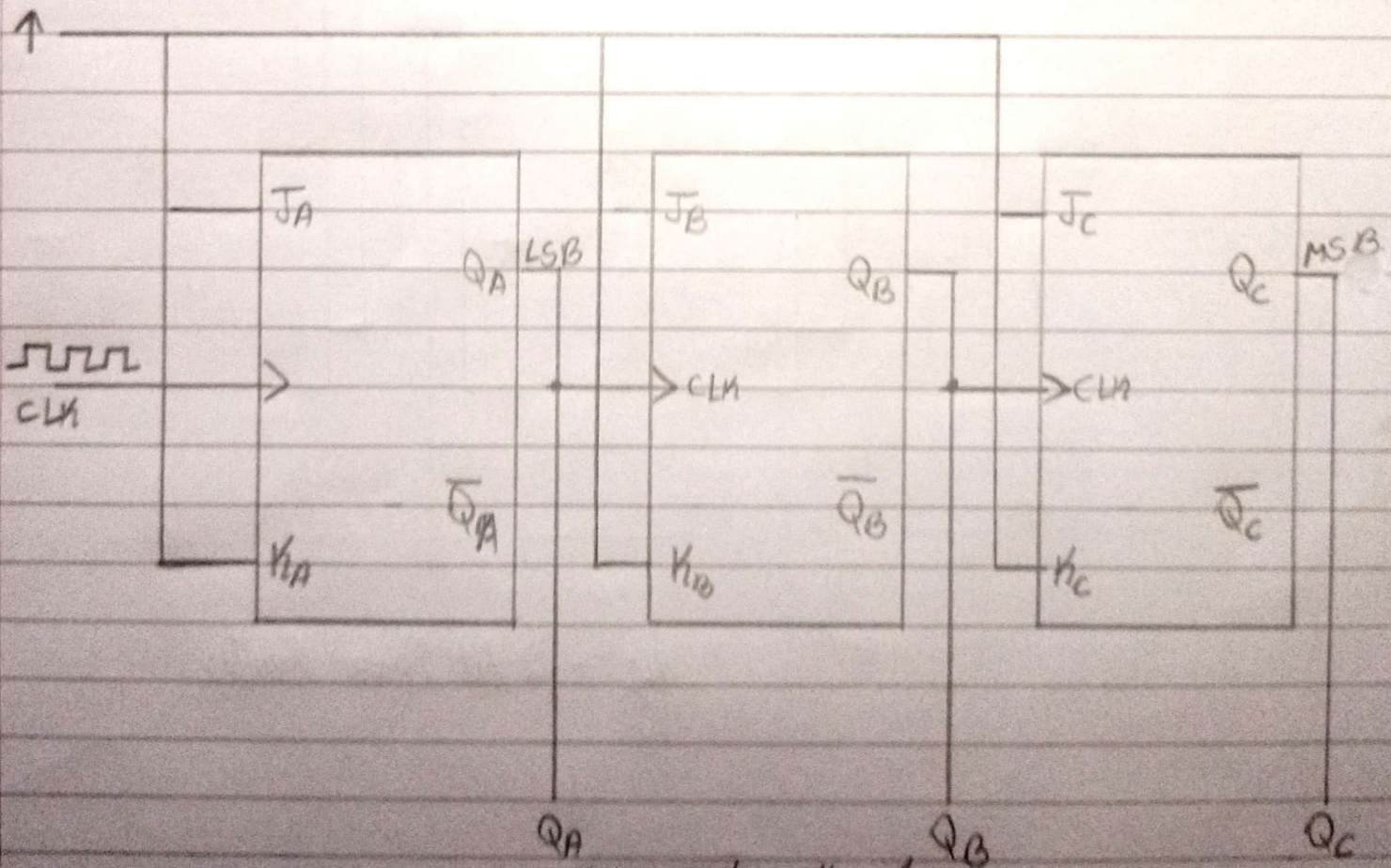
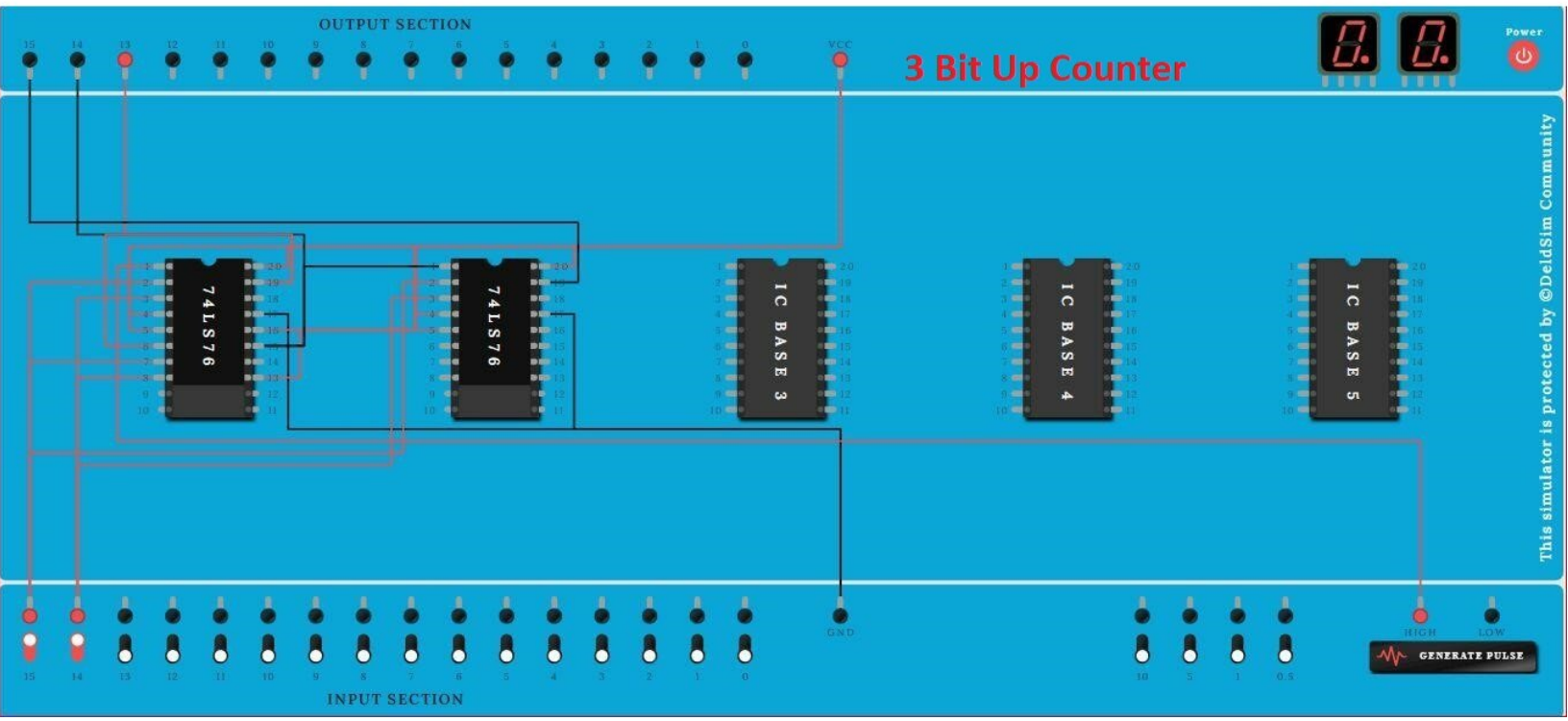


fig :- 3-bit Up counter


OUTPUT SECTION
3 Bit Up Counter
Power
74LS76
74LS76
IC BASE 3
IC BASE 4
IC BASE 5
VCC
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION
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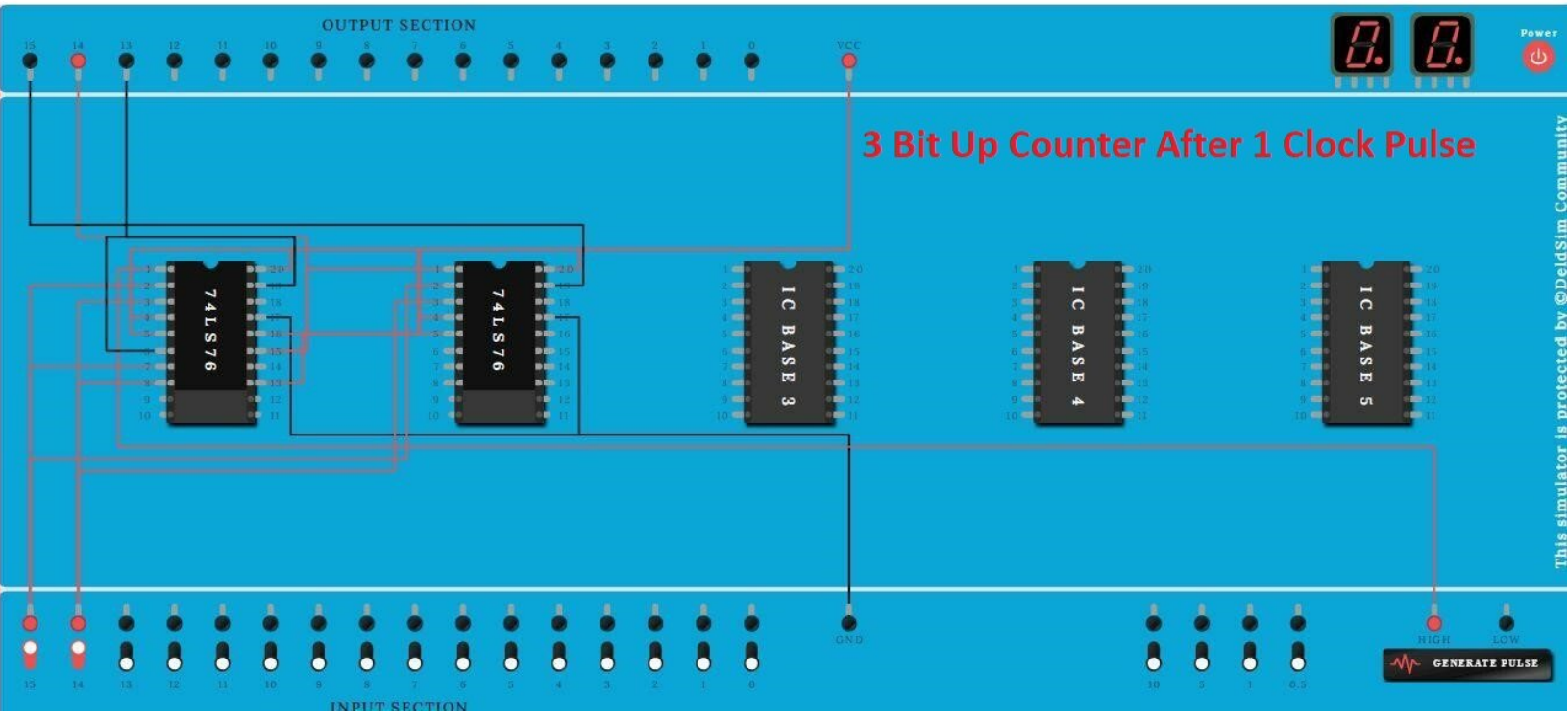
OUTPUT SECTION
3 Bit Up Counter After 1 Clock Pulse
Power
74LS76
74LS76
IC BASE 3
IC BASE 4
IC BASE 5
VCC
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION
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② Down counter :->

Counter State	Output		
	Q_A	Q_B	Q_C
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

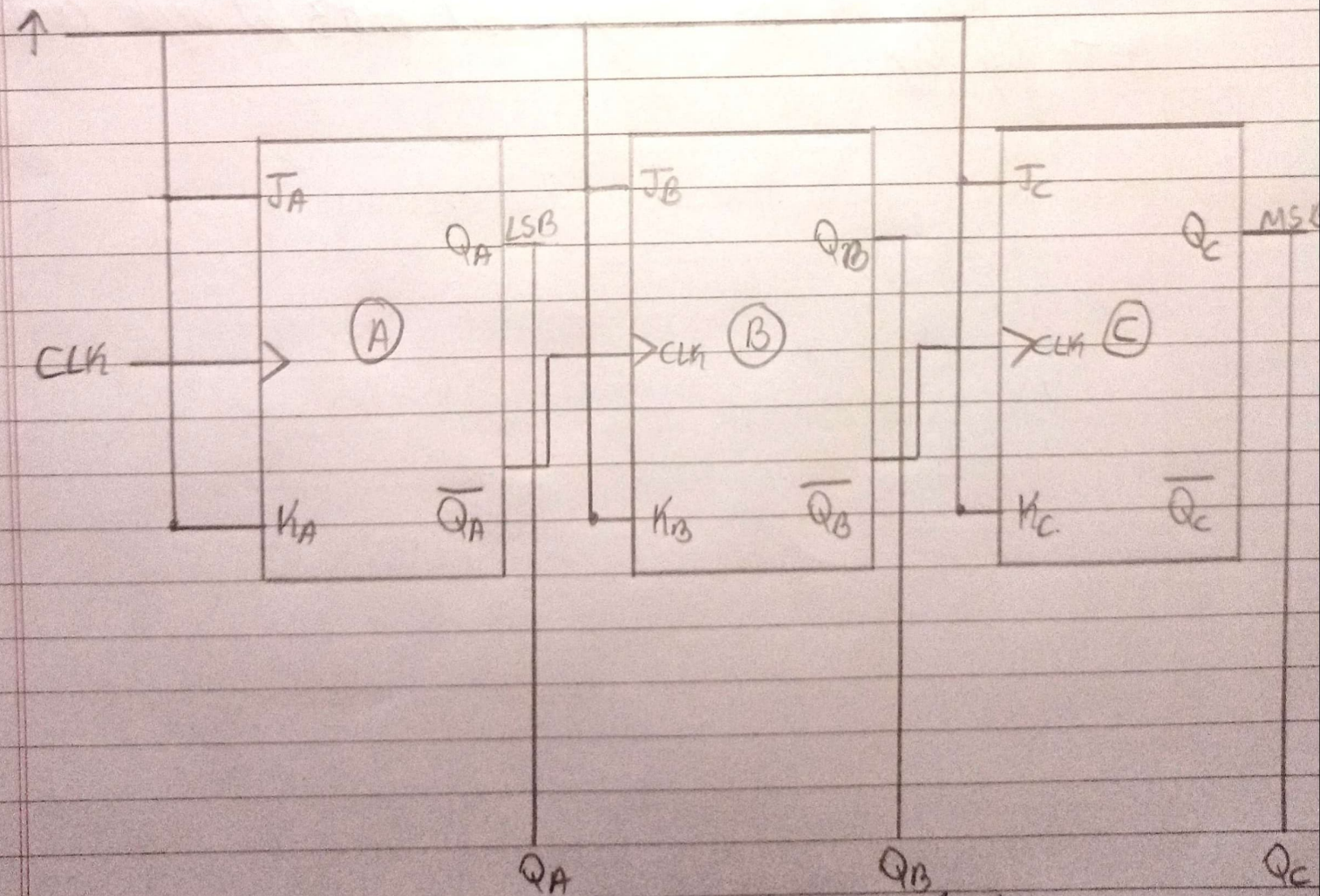
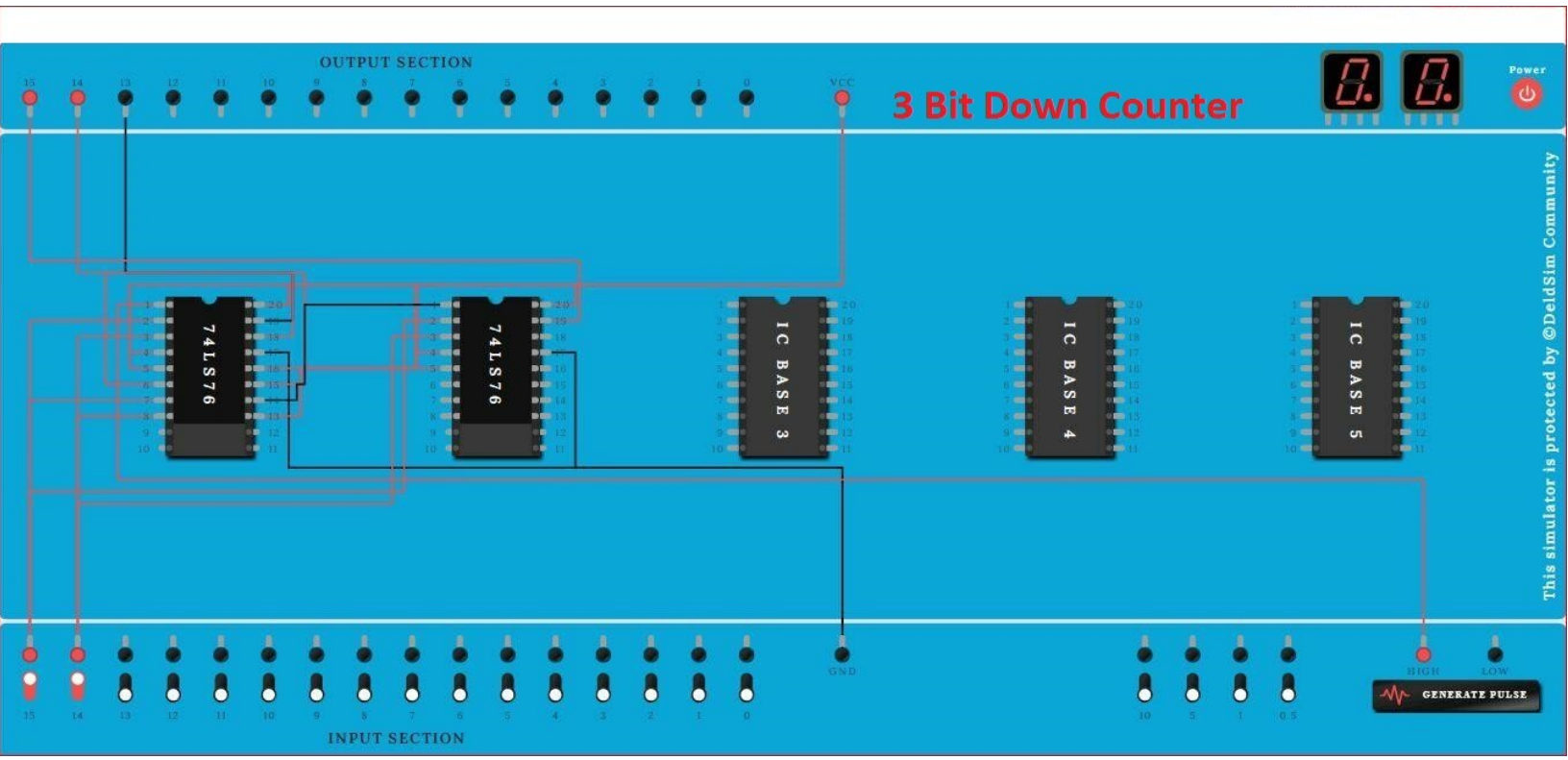


fig:- 3-bit Down counter.


OUTPUT SECTION
3 Bit Down Counter
Power
74LS76
74LS76
IC BASE 3
IC BASE 4
IC BASE 5
VCC
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION
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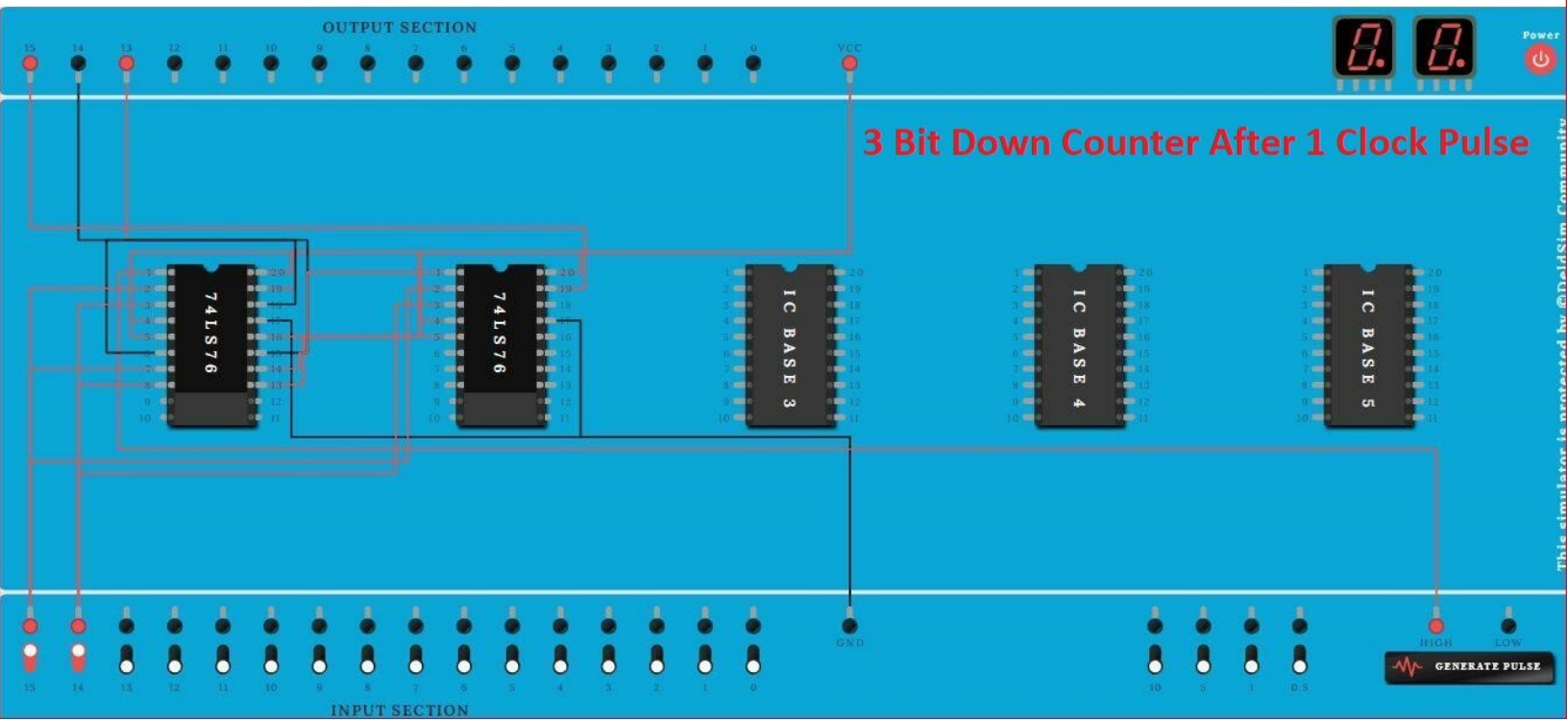
OUTPUT SECTION
3 Bit Down Counter After 1 Clock Pulse
Power
74LS76
74LS76
IC BASE 3
IC BASE 4
IC BASE 5
VCC
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION

Uses:-

1. Counting devices
2. Pulse counter
3. Used for dividing frequency

Outcome:-

Thus we implemented up and down ripple counter using IC 7476.

Conclusion:-

Hence, we have design 2 bit and 3 bit ripple counter using MSJK flip flop.