* Digital Electronics and Logic Design (DELD) - Practical Mumber - 8 Name: - Staustubh Shrikant Skabra.

Class: - Second Year Engineering.

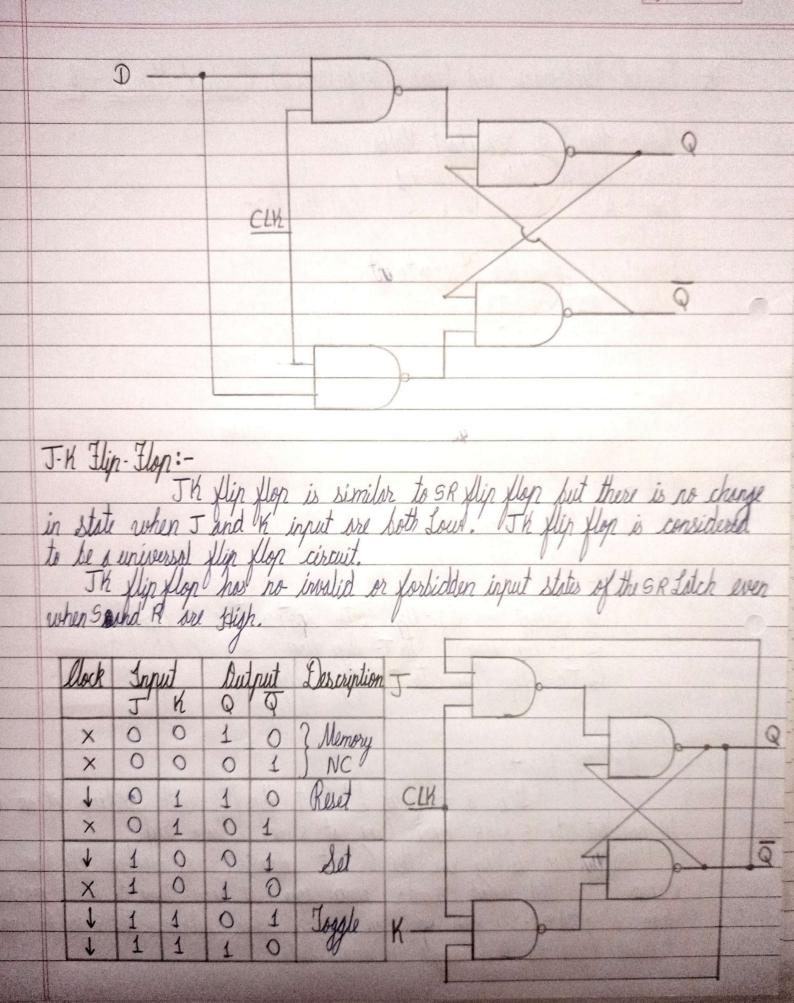
Div: - A Roll Number: -Batch:-Department: - lamputer Department lollege: - AISSMS'S IOIT. Aim: -Design and Restization: Flip-Flop Conversion Title:-Flip-Flop Conversion. Objective:

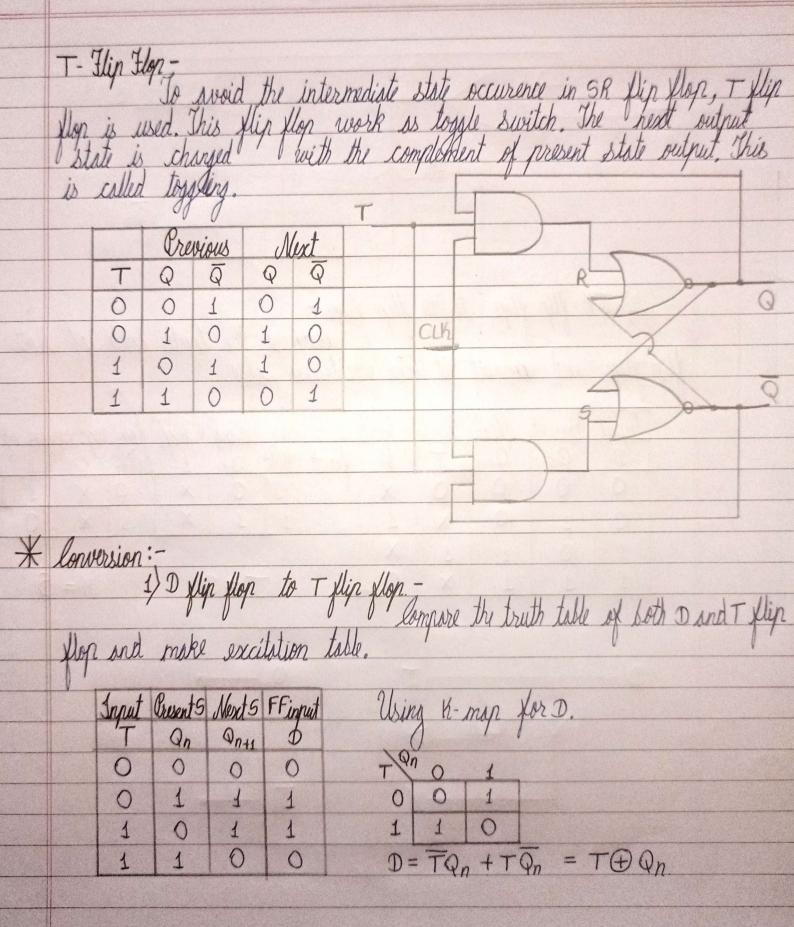
To convert one flip-flop into another type of flip-flop:

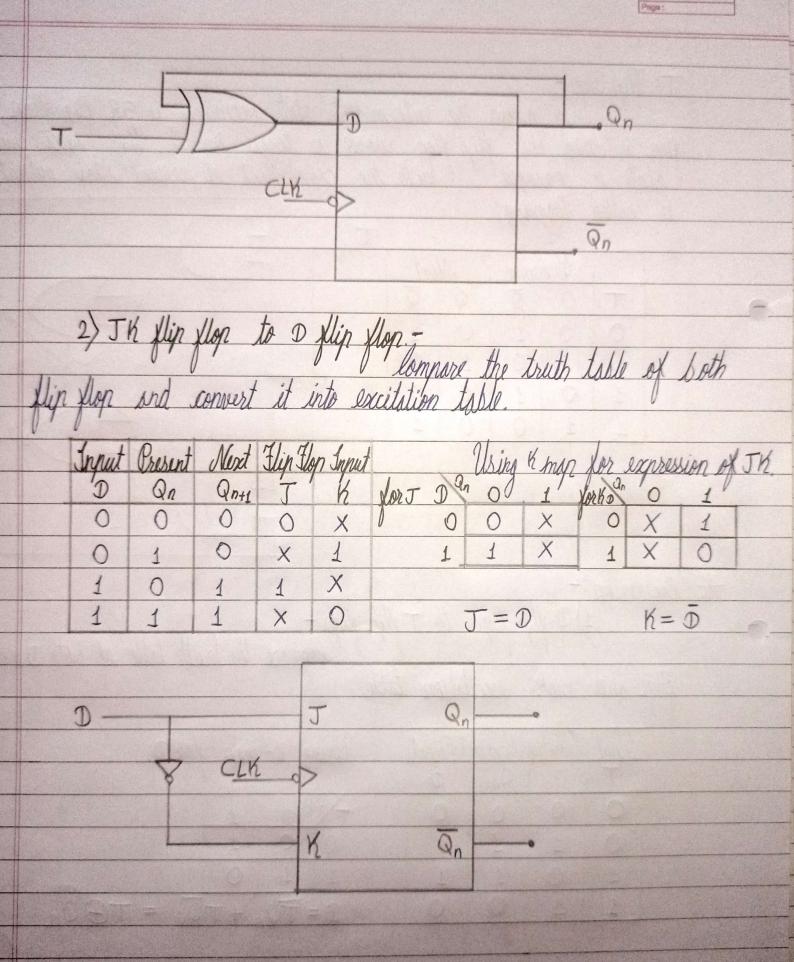
D-flip flop to D-flip flop. Theory:
1 D-Flip Flop

It is a modified Set-Ruset Alip Flop with addition of an inverter to prevent the sand R input being at same logic level.

D-flip flop is by for the most important of clocked flip flop as it answers that input sand R never equal at same time. It is constructed from a gated SR-flip flop with an inverter added between the Sand R input to allow for a single D(input) Data.







IC's Used-1 Dual Positive Edge trigered IC 7474 (D flip flop) -14 Vcc CLK, -13 CLK Clk, 3 12 D2 10 52 0,6 08 Q, GND 7

londusion:Stence, we have successfully converted the flip flop from
type to another type.