* Digital Electronics and Logic Design (DELD) - Practical Number - 10

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Div :- A Roll Number :-
Batch :-
Department :- Computer Department.
College :- AISSMS's IOIT.

Title :-
Synchronous counter.

Aim :-
Design of synchronous 3-bit up and down counter using MS-JK flip flops.

Objective :-
To design and understand 3-bit synchronous up down counter.

Theory :-
Synchronous counter -
In this counter, all the flip flop recives the external clock pulse simultaneously.

Example :- Ring counter and Johnson counter.

The gate propogation delay at reset time with not be present or we may say will not occur.

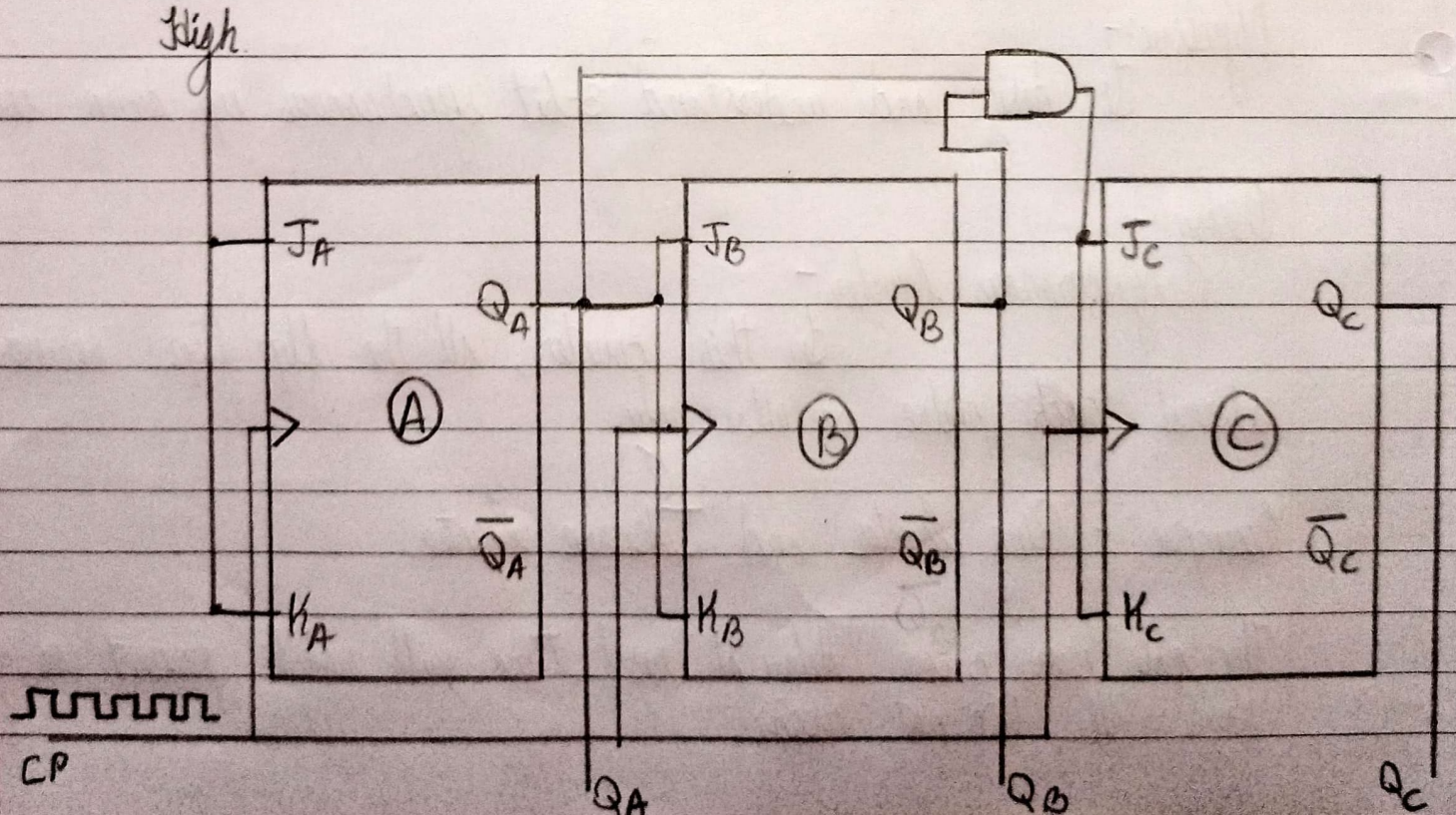
Classification of Synchronous Counter :-

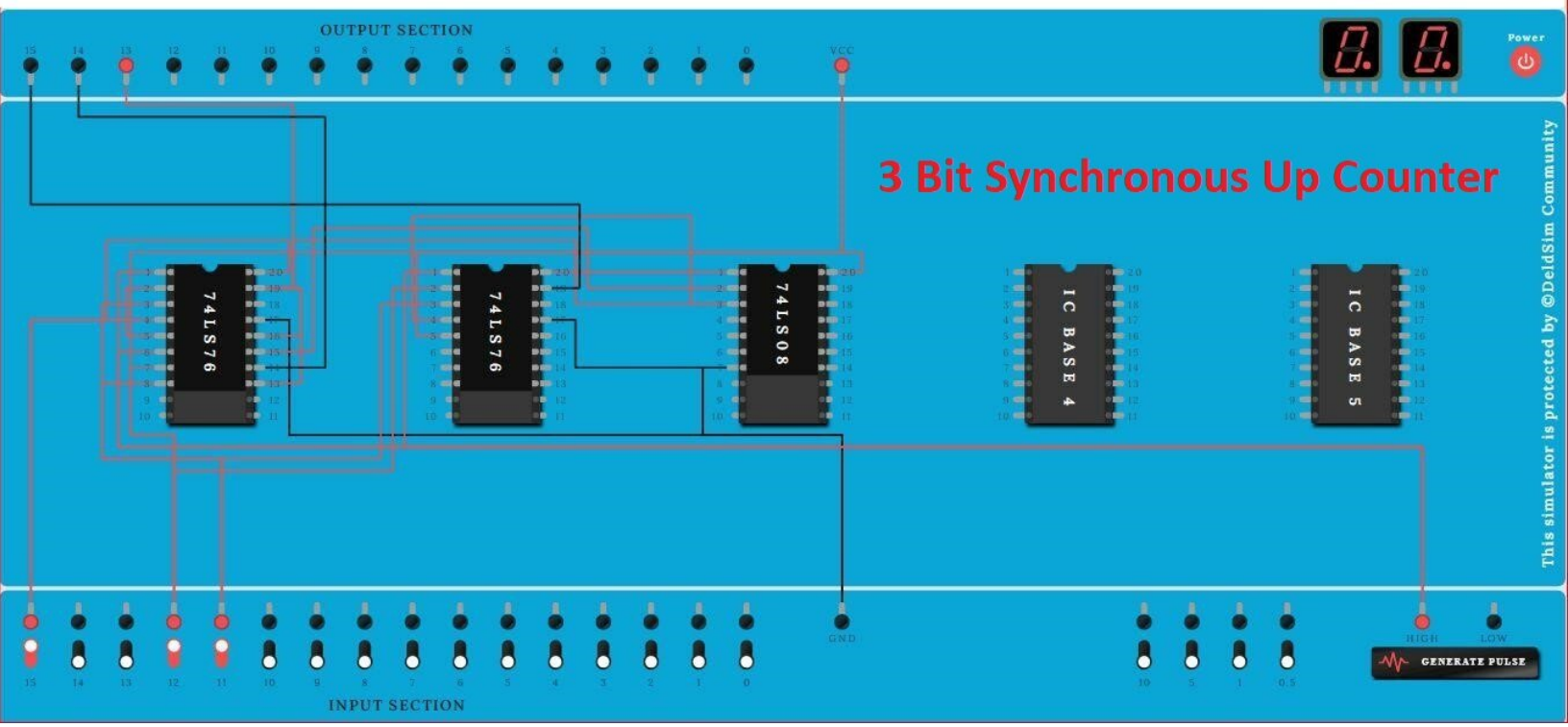
1. Up counter
2. Down counter
3. Up-down counter

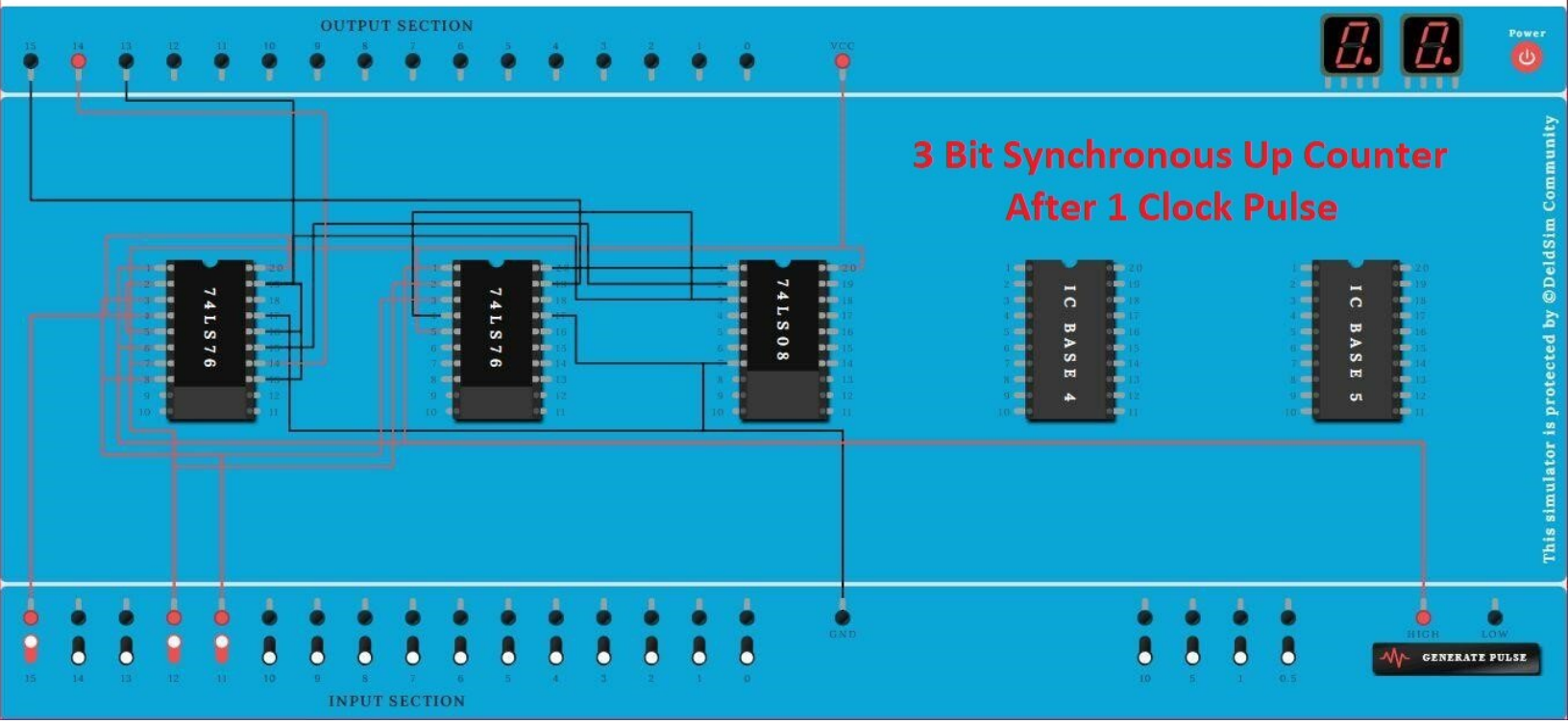
Logic Diagram and Truth Table :-

1) Up counter →

CP	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1




OUTPUT SECTION
VCC
Power
3 Bit Synchronous Up Counter
74LS76
74LS76
74LS08
IC BASE 4
IC BASE 5
This simulator is protected by ©DeldSim Community
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION


OUTPUT SECTION
VCC
Power
3 Bit Synchronous Up Counter
After 1 Clock Pulse
74LS76
74LS76
74LS08
IC BASE 4
IC BASE 5
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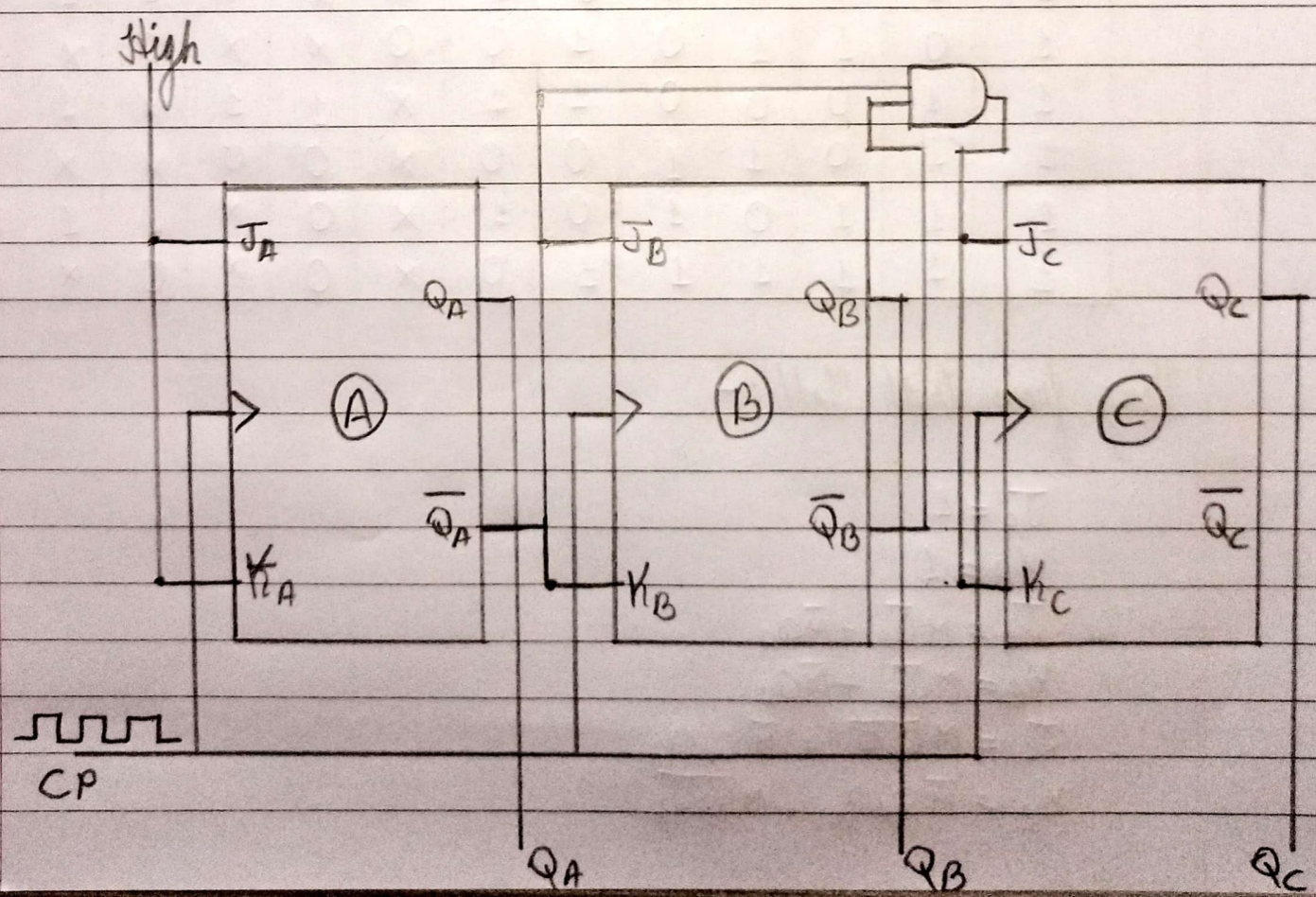
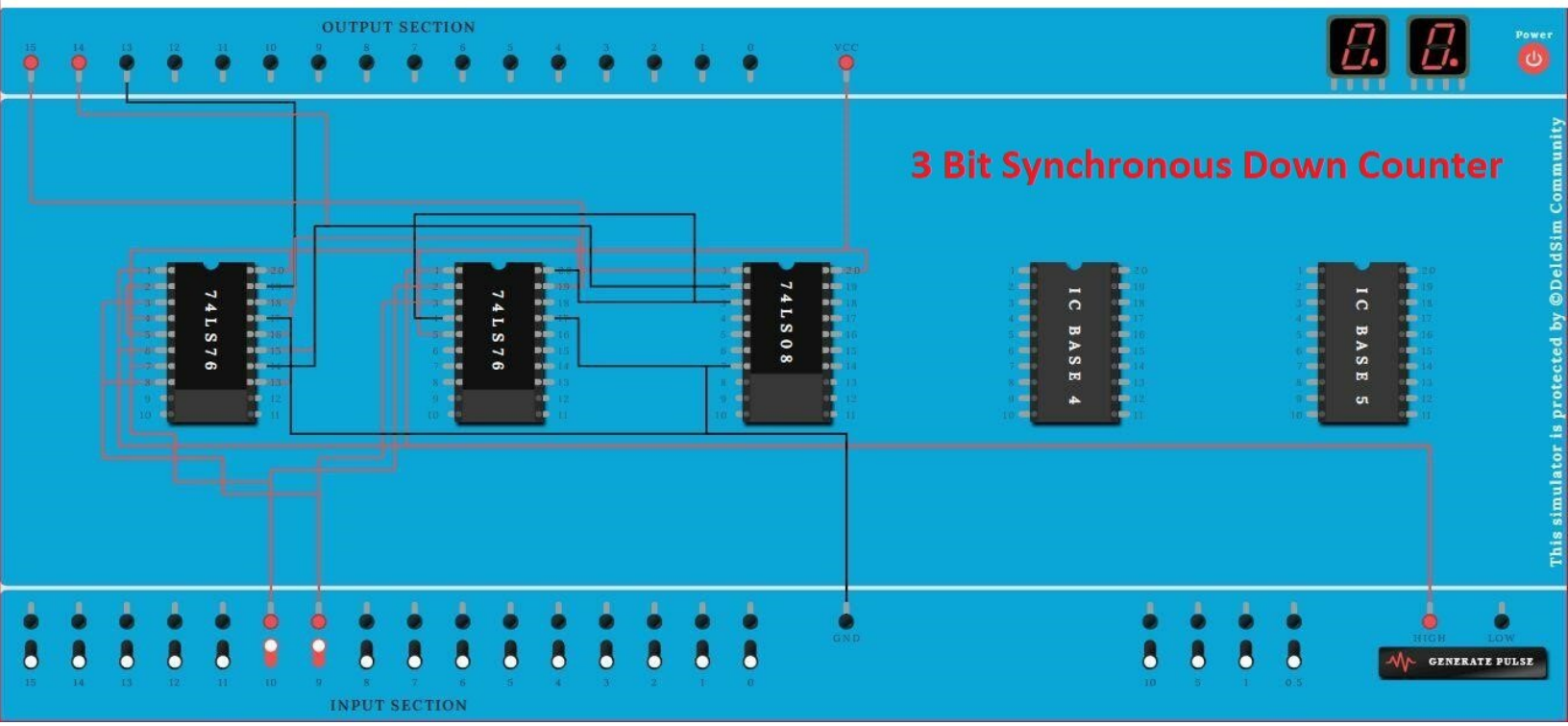
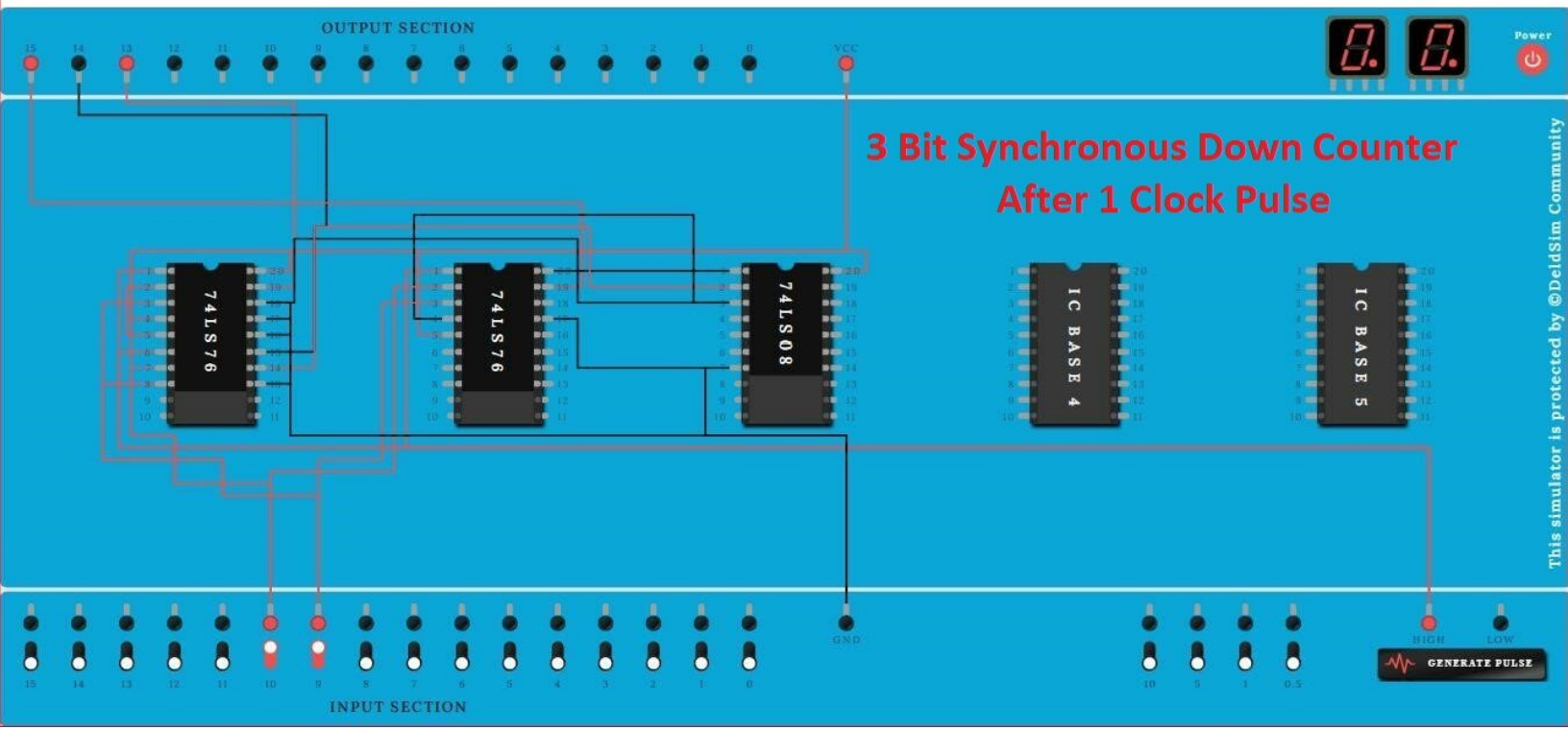
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION

2) Down counter →

CP	Q_C	Q_B	Q_A
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0




OUTPUT SECTION
VCC
Power
3 Bit Synchronous Down Counter
74LS76
74LS76
74LS08
IC BASE 4
IC BASE 5
This simulator is protected by ©DeldSim Community
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION


OUTPUT SECTION
VCC
Power
3 Bit Synchronous Down Counter
After 1 Clock Pulse
74LS76
74LS76
74LS08
IC BASE 4
IC BASE 5
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GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION

3) Up-Down counter:-

Control Input	Present			Next			Input from flip flop					
M	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	1	X	1	X
0	1	0	1	1	1	0	X	0	0	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
1	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	1
1	0	1	0	0	0	1	0	X	X	1	1	X
1	0	1	1	0	1	0	0	X	X	0	X	1
1	1	0	0	0	1	1	X	1	1	X	1	X
1	1	0	1	1	0	0	X	0	0	X	X	1
1	1	1	0	1	0	1	X	0	X	1	1	X
1	1	1	1	1	1	0	X	0	X	0	X	1

Using from truth Table:-

$J_A = 1$

$K_A = 1$

$J_B = M\bar{Q}_A + \bar{M}Q_A$

$K_B = M\bar{Q}_A + \bar{M}Q_A$

$J_C = M\overline{Q_A Q_B} + \bar{M}Q_A Q_B$

$K_C = \bar{M}Q_A Q_B + M\overline{Q_A Q_B}$.

Uses:-

1) Counting device
2) Count No. clock pulse.
3) Digital voltmeter
4) Used in digital triangular wave generator.

IC's used:-

1) Dual Master Slave JK flip flop (IC 7476)
2) AND gate (IC 7408)
3) OR gate (IC 7432).

Outcome:-

The up, down and up-down are successfully implemented, the counter are studied and output are checked. The truth table is verified.

Conclusion:-

Hence we have design 3 bit synchronous couter.