*	Digital Electronics and Logic Design (DELD) - Practical Number - 13
	Name: - Staustubh Shrikant Shabra. Class: - Second Year Engineering. Div: - A Roll Number: - Batch: -
	Div:- A O O Koll Number:- Batch:-
	Department: - longuter Department lollege: - AISSMS'S IOIT.
	Title:- Shift Registers.
	Aim:- Study of Shift Registers [SISO, SIPO, PISO, PIPO] At: 1:
	thjective:- The study the working of shift registers.
	Theory:- Node of operation of a shift register: The various mode in which a shift register can operate are as follows:- Derial input Serial Autput [5=50]
	a shift register can operate are as follows:-
	Derial input Serial Autput [5±50] Derial Input Parallel Autput [3±P0] Torallel Input Serial Autput [P±P0] Parallel Input Parallel Autput [P±P0]
	(3) Carallel Separt Serial Stutput [PI PO]

1) Serial In Serial But [5150]:-

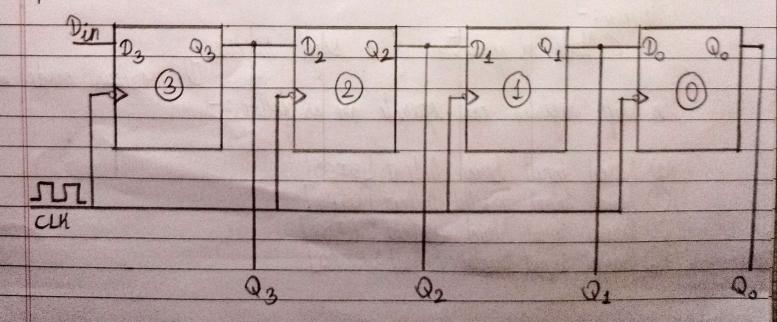
C.P.	Q ₃	Q2	Q ₁	Q.	Din	
Initially	0	0	0	0	_1	
Initially 100	04	OF	OF	15	1	
12	04	0 4	14	14	1	
13	02	14	14	15	_1	
14	15	15	15	14	1	

Shift Left Register

	C.P	Din.	Qz	Qq	Qq	Dag Q.
	Initially	01	0	0	0	0
	111	1	1	70	70	90
The state of	12	1	31	>1	30	20
	√3	1	1	>1	71	30
	↓4	1	>1	1	>1	21

Shift Right Register

2) Serial In Parallel Dut [51 PO]:-



						1		
	CP	Q ₃	THE RESERVE OF THE PERSON NAMED IN COLUMN 2 IS NOT THE OWNER.	Commence of the second	And the second second second second			
	-	NC	NC					
	1	\mathcal{D}_3	\mathbb{D}_2	$\mathcal{D}_{\mathbf{j}}$	Do			
4) Parallel in Co	rallel A	ut [PI	po]:-				*	
Az		A.2 (arallel d	ata f	1		Ao	
			Innut					
			7					
L _D	02/1	UD2	Q	, H	D,	0,1	400	00 1
3		-			1			
To To		Los			10		T	
777								
								Microsophia
	Q	3		02		01		0.
				Care	elle d	ata		
					Duta	ul		
		0 1			- 1			
Application of	Shift	Register	-					
11 0	0	/ (1) Jenno	rary da	ta sto	rage.		
		(2	Lelay.	line		0		
		(3						
		4			erial l	onverter		
		(6) lour	ter				
O Sequence generator								
		4) Carallel in Carallel de Az	4) Parallel in Parallel State [PI] A3 A2 Q D3 Q3 D2 Application of Shift Register: (2) (3)	- NC NC D ₃ D ₂ 4) Corallel in Carallel State [PIPO]:- A ₂ A ₂ Carallel d Input D ₃ D ₂ Q D ₄ D ₂ Q Q D ₅ D ₂ Q Q Delay G Delay D D D D D D D D D D D D D	- NC NC NC D ₃ D ₂ D ₁ 4) Parallel in Parallel test [PIPO]:- A ₂ Garallel data A Inquit D ₃ Q ₂ D ₂ Q ₂ Application of Shift Register:- Q Jety line	Application of Shift Register: Q3 Application of Shift Register: Q Serval - to Carallel Q Parallel - to Serval Q	- NC NC NC NC D3 D2 D1 D0 4) Carallel in Carallel data A1 A2 Carallel data A1 Application of Shift Registr:- 2 Semporary data storage. 2 Selection of Society of Carallel Converter. 2 Serial - to Carallel Converter. 3 Serial - to Carallel Converter. 4 Carallel - to Serial Converter. 5 Connerter.	- NC NC NC NC D3 D2 D4 D0 4) Cavallel in Cavallel State [PIPO]:- A2 Cavallel data A4 A0 Injust D3 D3 D2 D4 D4 D4 D4 D5 D5 D6 D7 Parallel data Dailput Application of Shift Register:- D Jennorary data storage. D Saley like D Serval - to Cavallel Converter D Lavallel - to Serial Converter D Lavallel - to Serial Converter D Lavallel - to Serial Converter

lonclusion:Hence, we have studied the shift register and its
different types.