* Digital Electronics and Logic Design (DELD) - Cractical Number - 7 Name: - Frankfuh Shrikant Habra.
Class: - Second Year Engineering.
Div: - A Roll Number: Batch: -Department: - lomputer Department lollege: - AISSMS's IOIT Title:Carity Generator and Checker. Sim:Design and Implement parity generator and checker using EX-OR gate. Itsjutive:Learn evenlodd parity generator/checker using EX-OR gate. Theory:
Revity-A term used to specify the member of one's in a digital word as odd even.

Even Carity Generator
Will produce a logic 1 at its output if the data roord contain an odd number of ones. If the data contain an even number of ones then the output of the parity generator will be low. Cority Checker- It the reciving end a logic circuit is used to check the parity

	of m	of receiving information, and determines wheather error is included in the message or not.												
	Even	Even sit Parity lode- Jotal number of one's in parity code is even.												
		soul number of ones in party code is even.												
	Add	Add bit Parity lade-												
		Add bit Parity lade- Jotal number of one's in parity code word is odd.												
	П.,	Truth Table:- © Carity Generator:- Input B2 B4 B0 P Expression for output using k-map 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0												
	Tru	n Jaou	@ Parit	Genera	tas:-									
			- water	g guillo	1) Even Par	ity Generator -								
			Input		autrut									
		β2	B1	Во	þ	Expression for output using k-mgs								
		0	0	0	0									
		0	0	1	1	B2 8,00 01 11 10								
		0	1	0	1	00000								
		0	1	1	0	1 1 0 1 0								
		1	0	0	1									
		1	0	1	0	$ \lambda = \beta_2 (EX-OR) \beta_1 (EX-OR) \beta_0. $								
		1	1	0	0									
		1	1	1	1									
	0													
	B2		E818 - 3 (C											
	B ₁													
1														
	B ₀ -													
	No -					- Even Carity Generator								
-			-	The state of the s	water and the second of the second of	- and Leadons								

@ Add Parity Generator:-

	Irrut		Output							
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1	0	0	0	10						
1	0	1	1	Y)	/= B2	(EX-NO	R) B1 (EX-NOR) B.
1	1	0	1							
1	1	1	0	10		= B2	(EX-0)	2) B1 (EX-OR)	Bo

B ₂		
B ₁		
-	4	Y
B ₀		

- Add Parity Gerator

	60	1	11 1	1		[0 -> 3 mm 7								
	(G) Cari	ity e	hurer	(A)	1 Parit	lhecker-	0 > Error 1 -> Not Error							
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		0	1	0	0	0	00	1	0	1	0			
		0	1	0	1	1	01	0	1	0	1			
		0	1	1	0	1	11	1	0	1	0			
		0	1	1	1	0	10	0	1	0	1			
		1	0	0	0	0								
		1	0	0	1	1	Y = F	EX-	OR)B	2 (EX	OR) B1 (EX-OR) Bo	
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	2 8	ven la	rity e	Shecker	-			-	0 → 1 →	Error Not	Speak		
			Jry	nut		Autrut	_ V W V V V V V						
		Parity (P)	B2 1	Bs	Во	y							
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	7/20/19/19	1	0	0	1	0							
		1	0	1	0	0	Y= P	(EX-OF	R) B2 (1	EX-OR)	B1 (EX-0	R)Bo	
		1	0	1	1	1							
		1	1	0	0	0							
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* IC's Used:-1) EX-OR yate - (IC7486) 2) NOT You (IC 7404) 7486 11 10 8 tulcomes:Thus we study parity generator and checker and their truth talls. londusion: -Hence, we have design and implemented the parity generator checker using EX-OR.

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