X	Digital Electronics and Logic Design (DELD) - Practical Mumber - 10
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	Tilli:
	Title:- Synchronous lounter.
	Aim:-
	Design of synchronous 3-bit up and down counter using MS-JK
	flip flogs.
	Objective:-
	Objective:- To design and understand 3-bit synchronous up down counter.
	Theory:
	Synchronous lounter— In this counter, all the flip flop recives the external clock phase simultaneously.
	In this counter, all the fly floor receives the.
	external clock pluse simultaneously.
	Example: - Ring bourter and Johnson bourter.
	d + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 + 1 +
	The gate propagation delay at rused time with not be present or we may say will not occur.
	say will o not occur.

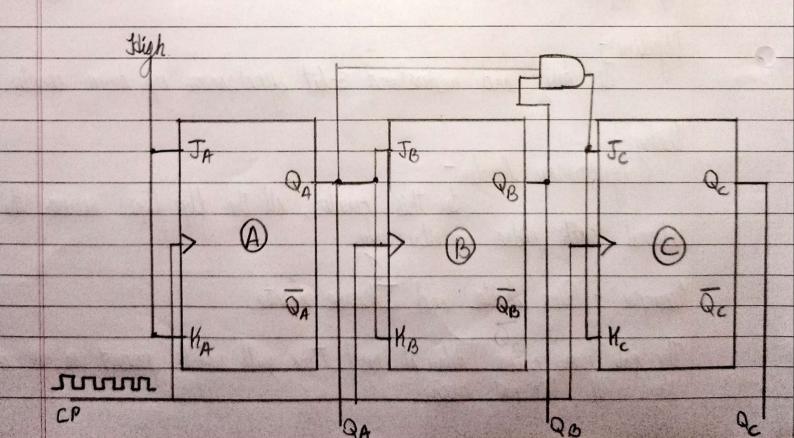
Classification of Synchronous Counter:

(2) Up Counter

(2) Down Counter

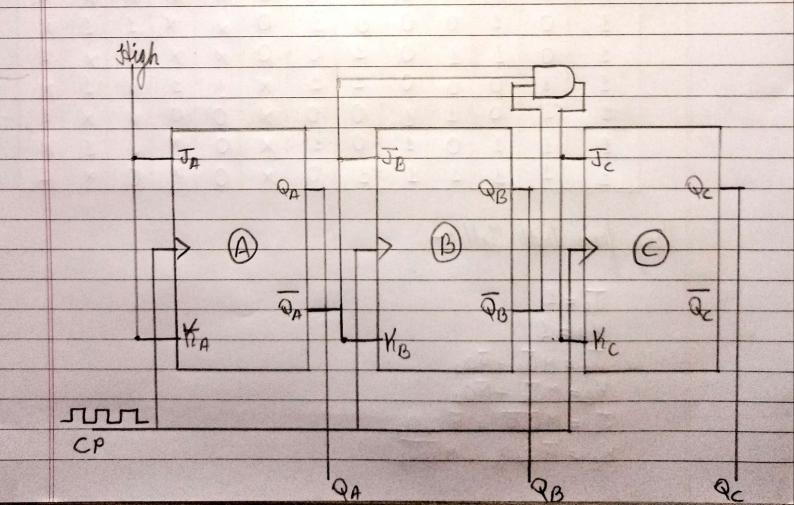
(3) Up down Counter

Logic Diagram and Truth Table:-  1> Up lounter ->									
	CP	Qc	QB	QA	1-4-11-1	7272 TO 189			
	0	0	0	0	7				
	1	0	0	1					
	2	0	1	0					
	3	0	1	1		Serie J			
	4	1	0	0					
	5	1	0	1		-			
	6	1	1	0					
	7	1	1	1		and the			



2) Down lounter ->

1	CP	Qc	QB	QA
	CP 7	1	i	1
	6	1	1	0
	6	1	0	1
	4	1	0	0
	3 2	0	1	1
	2	0	1	0
	1	0	0	1
k	0	0	0	0



3) Un-Down Counter: -

M   Qc   Q6   QA   Qc+1   Qa+1   Tc   Kc   Tg   Kig   UA   KA															
M Qc Q6 QA QcH QAH QAH TZ KC TB K6 TA KA  O O O O O O O O O O A O X A X X A  O O O O I O I O O X A X X A  O O I O O I O I O X O X A X A  O O I O O I I O I X O I X A  O I O O I I O I X O I X A  O I I O I I I I X O X O I X  O I I O I I I I X O X O I X  I O I I I I I X I X I  I O O O I O O O X A X I X I  I O O O O O O X A X I X I  I O O O O O O O O O O O O O O O O O		Part to trans	1 6	mount			Next		1	nnud	from	Slip	Slog	)	
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0 1 0 0 1 0 0 1 x 0 1 x 1 x 1 x 1 0 1 0		0	0	1	1	1	0	0	1	X	X	1	X	1	
0 1 1 0 1 1 4 X 0 X 0 1 X 0 1 1 1 0 0 0 X 1 X 1 X 1 1 0 0 0 1 1 1 1 X 1 X 1 X 1 0 0 1 0 0 0 X 0 X X 1 1 0 1 0 0 0 1 0 X X 1 1 X 1 0 1 1 0 1 0 0 X X 0 X 1 1 1 0 1 1 0 0 X X 1 X 1 X 1 1 1 0 1 1 0 0 X X 1 X 1 X		0	1	0		1	0	1	X	Bernard March	1	X	1	X	
0 1 1 0 1 1 4 X 0 X 0 1 X 0 1 1 1 0 0 0 X 1 X 1 X 1 1 0 0 0 1 1 1 1 X 1 X 1 X 1 0 0 1 0 0 0 X 0 X X 1 1 0 1 0 0 0 1 0 X X 1 1 X 1 0 1 1 0 0 0 X X 0 X 1 1 1 0 1 1 0 0 X X 1 X X 1 1 0 1 1 0 0 X X 1 X X 1 1 1 0 1 1 0 0 X X 0 X X 1 1 1 1 0 1 1 0 0 X X 0 X X 1 1 1 1 0 1 1 0 0 X X 0 X X 1		0	1	0	1	1	1	0	X	0	0	X	X	1	
1 0 0 0 1 1 1 1 X 1 X 1 X 1 0 0 1 0 0 0 0 X 0 X X 1 1 0 1 0 0 0 1 0 X X 1 1 X 1 0 1 1 0 1 0 0 X X 0 X 1 1 1 0 1 1 0 0 X 1 1 X 1 X 1 1 0 1 1 0 0 X 0 0 X X 1 1 1 1 0 1 1 0 0 X 0 X X 1		0	1	1		1	1	1	X	0	X	0	1	X	
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1 0 1 1 0 1 0 0 X X 0 X 1 1 1 0 0 0 1 1 X 1 1 X 1 X 1 1 0 1 1 0 0 X 0 0 X X 1 1 1 1 0 1 0 1 X 0 X 1 X		1	0	0	1	0	0	0	0	X	0	X	X	1	
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1 1 0 1 1 0 0 X 0 0 X X 1 1 1 1 0 1 0 1 X 0 X 1 1 X		1	0	1	1	0	1	0	0	X	X	0	X	1	
1 1 1 0 1 0 1 X 0 X 1 1 X		1	1	0	0	0	1	1	X	1	1	X	1	X	
		1	1	0	1	1	0	0	X	0	0	X	X		
1 1 1 1 1 0 X 0 X 0 X 1.		1		1	0	1	0	1	X	0		1	1	X	
		1	1	1	1	1	1	0	X	0	X	0	X	1.	

Using from truth Table: -

$$J_{A} = 1$$

$$K_{A} = 1$$

$$J_{B} = M \overline{Q}_{A} + M \overline{Q}_{A}$$

$$K_{B} = M \overline{Q}_{A} + M \overline{Q}_{A}$$

$$J_{C} = M \overline{Q}_{A} \overline{Q}_{B} + M \overline{Q}_{A} \overline{Q}_{B}$$

$$K_{C} = M \overline{Q}_{A} \overline{Q}_{B} + M \overline{Q}_{A} \overline{Q}_{B}$$

$$K_{C} = M \overline{Q}_{A} \overline{Q}_{B} + M \overline{Q}_{A} \overline{Q}_{B}.$$

Uses:
1) lounting device

2) lount No. clock pluse.

3) Digital voltmeter

4) Used in digital triangular wave generator. IC's used:
1) Dual Master Slave Tr Slip Slop (IC 7476)

2) AND gate (IC 7408)

3) OR gate (IC 7432). Dutcome: -The up, down and up-down are successfully implemented, the counter are studied and output are a checked. The truth table is verified. Sence we have design 3 bit synchronous conter