

VISVESVARAYA TECHNOLOGICAL UNIVERSITY

“Jnana Sangama”, Belagavi-590018, Karnataka



A Project Report

on

“SYNTHESIS AND PHYSICAL IMPLEMENTATION OF RAM & ROM MODULES: A COMPREHENSIVE STUDY USING CADENCE DESIGN TOOL”

Submitted in partial fulfillment of the requirements for the award of the degree of

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CERTIFICATE

Certified that the project work entitled "**SYNTHESIS AND PHYSICAL IMPLEMENTATION OF RAM & ROM MODULES: A COMPREHENSIVE STUDY USING CADENCE DESIGN TOOL**" carried out by **CHANDANA Y S [4AD20EC012], KAVANA K [4AD20EC025], KHUSHI M [4AD20EC29] and KUSUMA M [4AD20EC032]** bonafide students of ATME College of Engineering, Mysuru in partial fulfillment for the award of Bachelor of Engineering in Electronics and Communication Engineering, of the Visvesvaraya Technological University, Belagavi during the year 2023-24. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said Degree.

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- To develop highly skilled and globally competent professionals in the field of Electronics and Communication Engineering to meet industrial and social requirements with ethical responsibility.

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- To develop talented and committed human resource, by providing an opportunity for innovation, creativity and entrepreneurial leadership with high standards of professional ethics, transparency and accountability.
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ABSTRACT

This project presents the synthesis and physical implementation of Random Access Memory (RAM) and Read-Only Memory (ROM) modules using Cadence design tools. a versatile Electronic Design Automation (EDA) tool suite widely utilized in the semiconductor industry. Cadence software offers a comprehensive environment for designing and customizing memory components. In Cadence, the specification of the design is implemented using Hardware Description Languages (HDLs) such as VHDL or Verilog. The primary objective was to design, synthesize, and physically implement both RAM and ROM modules, ensuring their functionality and performance meet the desired specifications. The process involved architectural design, RTL coding, synthesis, place and route, and thorough verification. Through this project, a comprehensive understanding of memory module design and the Cadence design flow was attained. The results demonstrate successful implementation of both RAM and ROM modules, validating their correctness and functionality. This project contributes to advancing the knowledge and skills in digital design and memory system implementation using Cadence tools.

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Chapter 1

INTRODUCTION

RAM and ROM are indispensable building blocks in the development of electronic devices, from microcontrollers and smart phones to high-performance computing systems. RAM provides fast, temporary storage for data that can be read from and written to, enabling rapid processing and multitasking. ROM, on the other hand, stores essential firmware and software instructions that remain unchanged during operation. Both RAM and ROM are pivotal in ensuring the functionality and performance of electronic systems. Cadence software offers a versatile platform for designing, synthesizing, and verifying complex digital circuits, including memory components like RAM and ROM. This software suite provides a comprehensive set of tools that guide designers through each stage of the memory design process, from initial specifications to physical implementation. Key functionalities include RTL synthesis, technology mapping, timing analysis, layout generation, and power optimization.

1.1 Overview

The synthesis of RAM (Random Access Memory) and ROM (Read-Only Memory) using Cadence software typically involves a series of steps within the digital design flow. Cadence is a well-known provider of electronic design automation (EDA) tools, and its suite of software includes tools for digital design, verification, and implementation. Here's an overview of the synthesis process for SRAM and ROM using Cadence software.

RAM and ROM Synthesis using Cadence:

- **Design Entry:** Use a hardware description language (HDL) such as Verilog or VHDL to describe the SRAM circuit functionality.
- **RTL Synthesis:** Utilize Cadence's RTL synthesis tools to convert the high-level description into a Register Transfer Level (RTL) netlist.
- **Optimization:** Perform optimization to improve the design in terms of area, power, and timing using tools like Cadence Genus.
- **Technology Mapping:** Map the synthesized RTL to the target technology library, considering the specific characteristics of the SRAM cells available in that library.
- **Place and Route:** Use Cadence Innovus or Encounter tools for place and route to physically place the cells on the chip and create the detailed routing.

- **Timing Closure:** Perform timing analysis and optimization to ensure that the design meets the required timing constraints.
- **Verification:** Use Cadence simulation tools, such as Incisive, to verify the functionality and performance of the SRAM design.
- **Physical Verification:** Perform physical verification checks to ensure that the layout adheres to manufacturing rules.
- **Extraction:** Extract parasitic information from the layout for further accurate analysis.
- **Final Tape-out:** Prepare the final set of files for manufacturing (GDSII files) to create the physical SRAM chip.

1.2 Existing system

Random Access Memory (RAM) -Random Access Memory (RAM) is a type of computer memory that is used to temporarily store data that the computer is currently using or processing. RAM is volatile memory, which means that the data stored in it is lost when the power is turned off. RAM is typically used to store the operating system, application programs, and data that the computer is currently using.

Read Only Memory (ROM) is a type of computer memory that is used to permanently storedata that does not need to be modified. ROM is non-volatile memory, which means that the data stored in it is retained even when the power is turned off. ROM is typically used to store the computer's BIOS (basic input/output system), which contains the instructions for bootingthe computer, as well as firmware for other hardware devices.

1.3 Motivation

The goal is to optimize the RTL design, implement memory functionalities, and ensure successful synthesis while considering factors like power consumption, clock frequency, andtechnology constrains in the Candence environment.

1.4 Problem Statement

The problem is to design and synthesis a functional random-access memory (RAM) and readonly memory (ROM) in Candence RTL software to meet specific performance and area requirements for a digital integrated circuit.

1.5 Objectives

The aim of this project work is to:

- Design RAM and ROM using Verilog code and verify its functions using NC launcha simulation tool.
- To synthesize gate level net list for RAM and ROM.
- Explore various synthesis techniques and methodologies to design efficient RAM and ROM circuits, focusing on optimizing area, power, and performance parameters.
- Learn the process of physical implementation including floor planning, placement, routing, and optimization of RAM and ROM circuits using Cadence tools.

1.6 Organization of The Report

In Chapter 1 we have defined the overview and motivation of the project, also the objectives of the project.

In Chapter 2 gives the literature review of Synthesis and Physical Implementation of Random Access Memory and Read Only Memory.

In Chapter 3 explains about the block diagram of Random Access Memory and Read Only Memory along with the software requirements of the Project.

In Chapter 4 we have discussed the results pertaining to Synthesis of RAM and ROM with respect to area, power, slack time and number of cells utilized. Also shown the figures of floorplan and cell placement view of RAM and ROM.

Chapter 2

LITERATURE REVIEW

In this section we have discussed the papers surveyed for Synthesis and Physical implementation techniques involved in RAM and ROM . By reviewing these papers, we have designed to make efficient usage of technology.

2.1 Survey Papers

Shylashree N, Yatish D Vahvale “Design and Implementation of 64-bit SRAM and CAM on Cadence and Open-source environment” [1] the author objective is to design a power efficient SRAM cell. The traditional SRAM makes use of six transistors that consumes more power and stability for read operation is less. The author suggested carrying the work to achieve good results with respect to power using open-source tools in VLSI domain.

Ravi Kumar. K.I, Vijayalaxmi. C. Kalal, Rajani. H. P, Dr. S. Y. Kulkarni “Design and verification of low power 64-bit SRAM system using 8T SRAM: Back-End approach”[2], the author objective is to design the chip with low leakage power in memory design and to achieve low power operation he has chosen 8T SRAM cell with 64-bit memory of 8words x8bits.

Siddalingesh S. Navalgund, Prakash R Tonse “Design and Development and Implementation of ALU, RAM and ROM for 8051 Microcontroller on FPGA using VHDL” [3], the author objective is to design, development and implementation of an Arithmetic and Logic Unit (ALU), a Random Access Memory (RAM) and a Read Only Memory (ROM) for 8051 Microcontroller on Field Programmable Gate Arrays (FPGA) using VHDL.

Neelam Surana, Joycee Mekie “Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications” [4], proposed a single ended 6-T SRAM cell which has about 50% less dynamic power compared to conventional 6-T SRAM cell with the same bit error rate (BER). Since image processing applications are tolerant to errors, ultra-low voltage power-efficient embedded memories with BER can be used for storage.

Shabana Aqueel and Kavita Khare “Design and FPGA Implementation of DDR3 SDRAM Controller for High Performance” [5], the paper to address a critical aspect of modern computing systems: efficient memory access. DDR3 SDRAM is a widely used memory technology, and designing a controller for it, particularly for FPGA implementation, is both relevant and challenging. The paper likely explores various aspects such as timing constraints, data integrity, and resource utilization in FPGA implementation. It should provide insights into the design methodology employed to optimize performance while considering factors like clock frequency and routing congestion.

Sparsh Mittal, Gaurav Verma, Brajesh Kaushik, Farooq A. Khanday “SRAM-based Processing-in-Memory Techniques and Applications” [7] focuses on cutting-edge innovations in computer architecture, particularly in the domain of processing-in-memory (PIM). SRAM (Static Random-Access Memory) is a fundamental component in modern computing systems, and leveraging it for in-memory processing can lead to significant performance improvements. The paper likely delves into various techniques and methodologies for integrating processing capabilities directly into SRAM arrays, thus reducing data movement overhead and improving energy efficiency. These techniques could include specialized SRAM cell designs, circuit architectures, and algorithms tailored PIM applications.

Chapter 3

DESIGN METHODOLOGY

In this chapter will discuss about the methodology and software requirements of this project.

Architectural Design: The first step involved defining the architecture of both RAM and ROM, specifying parameters such as size, address width.

For RAM, the architecture included data input/output ports, address inputs, control signals, and memory cells. For ROM, the architecture comprised address inputs and data outputs.

RTL Coding: Using Verilog HDL, the architecture was translated into Register Transfer Level (RTL) code. RTL code for RAM included modules for memory cells, input/output ports, and control logic code for ROM consisted of a module for address decoding and data output.

Synthesis: The RTL code was synthesized using Cadence RTL Compiler to generate gate-level netlists. Synthesis optimizations were applied to improve the performance and area efficiency of the designs.

Place and Route: The gate-level netlists were subjected to place and route using Cadence Encounter to map the logic onto physical hardware resources. Constraints such as timing, area, and power were considered during place and route to meet design specifications.

Verification: Functional verification was performed using simulation tools like Cadence Incisive to ensure that the designed RAM and ROM modules operated correctly.

Block Diagram

In this section block diagram of RAM and ROM has been explained in details, both ROM and RAM are used for the storage purpose. RAM can read and write the data whereas ROM can only read the data.

3.1 Block Diagram of RAM

RAM is a form of electronic computer memory that can be read and changed in any order, typically used to store working data and machine code. RAM is a high-speed volatile memory used to store and process temporary data. It is used in CPU Cache and primary memory. The below Fig 3.1 Represents the Random Access Memory. A RAM unit stores the data and programs that the CPU uses in real time process. This data is available for different access modes including reading, writing and erasing. This hardware unit that stores the data for the utilization purpose. Fig 3.1 consists of clock, reset, write enable, read enable, data input, address signals as input and data output as output.

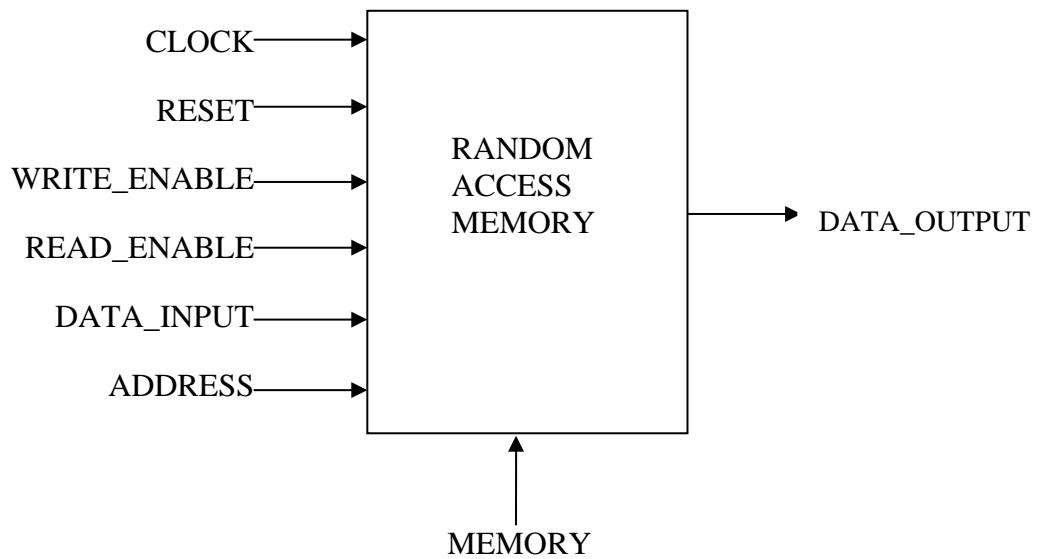


Fig 3.1 RANDOM ACCESS MEMORY

Memory is defined as a reg. The circuit works under positive clock edge. If reset signal is high no data is obtained in data output signal. To write data into the memory write enable signal should be set to one and memory address is given to address signal. In fig 3.1 To readd data from the memory read enable will be set to one and address is given to address signal. The data read from the memory is obtained in data output signal.

3.2 Block diagram of ROM

ROM stands for read only memory, it is a memory device or storage medium that stores information permanently. It is a non-volatile memory, It is also the primary memory unit of a computer along with the Random access memory.

The data that is required to be stored inside ROM is written during manufacturing phase. The figure 3.2 represents the Read only memory, which consist of clock, reset, read enable, address and memory as the input data and a data out which provides the output. The memory is defined as the Register. The circuit works under positive clock edge. If reset signal is high no data is obtained in data output signal. The circuit works under positive clock edge. If reset signal is high no data is obtained in data output signal. When read enable is high the read operations takes place.

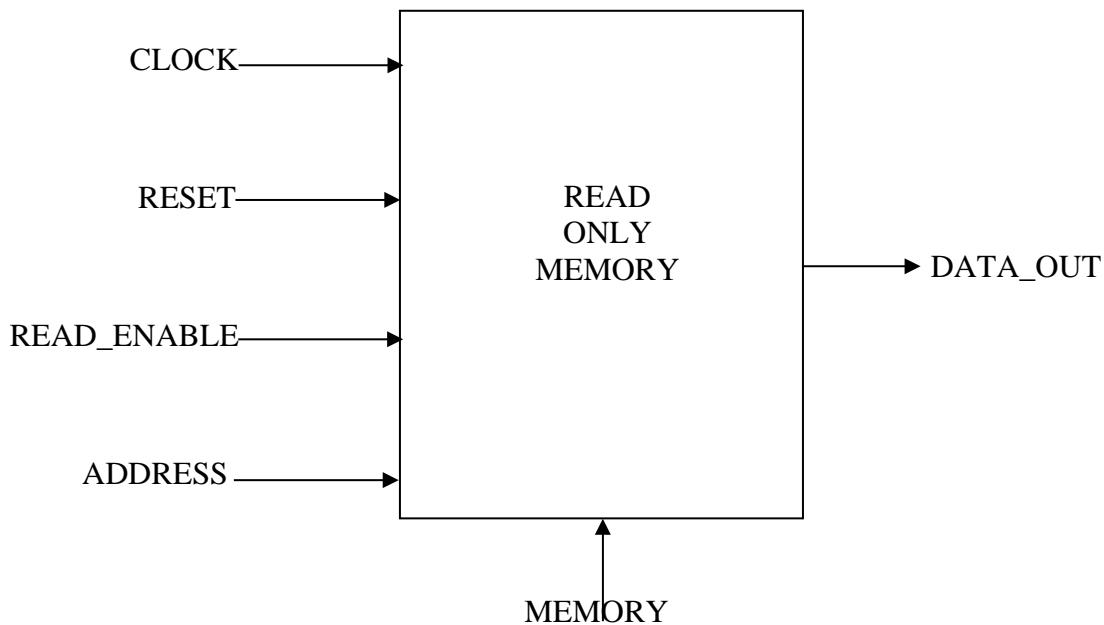


Fig 3.2 READ ONLY MEMORY

ROM is also used to store Firmware, which is a software program which remains attached to the hardware or programmed on a hardware device like a keyboard, hard drive, video cards, etc. It is stored in the flash ROM of a hardware device. It provides instructions to the device to communicate and interact with other devices.

3.3 Software specifications

The synthesis and physical implementation of RAM and ROM using Cadence typically require a suite of software tools that facilitate various stages of the design flow. Cadence provides a range of tools for digital design, synthesis, place and route, and verification. The specific tools needed include: Below are the essential software requirements for this process:

- **RTL COMPILER:** RTL Compiler will execute the instructions in the TCL file and will generate the output files and reports in the “out” folder. The generated files: “.v”: Which has the new gate level Verilog description of the synthesized system.
- **Encounter:** Cadence Encounter is a place-and-route tool that uses a Verilog netlist and generates its equivalent layout view. This tutorial describes how to use Cadence SOC Encounter to generate a layout view of the synthesized design, using standardcells library.
- **Library Files:** Standard cell libraries and technology files specific to the target process technology. These files provide essential information for synthesis and physical implementation, such as cell timing, power, and physical characteristics.

Chapter 4

RESULTS AND DISCUSSION

In this chapter will discuss about the results obtained from the project work implementation.

4.1 Results:

RAM

The below images represent the synthesized results of RAM

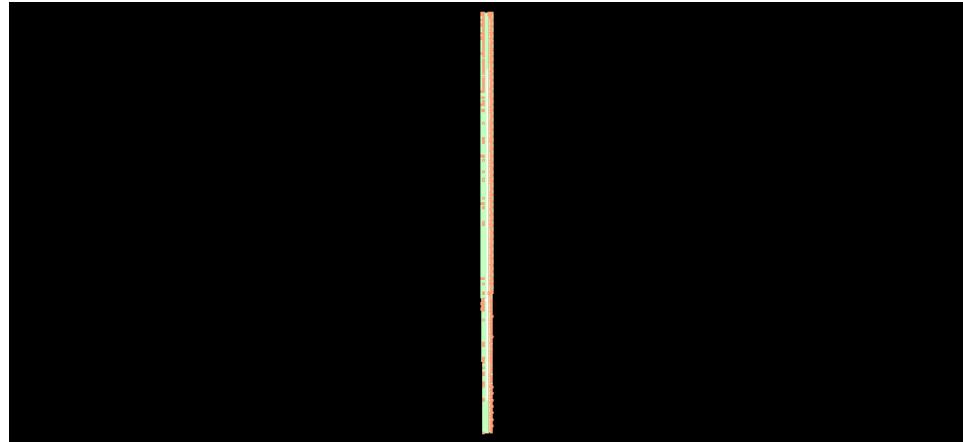


Fig 4.1. Synthesized image of RAM with memory address 2^9

The Fig 4.1 represents the synthesis of RAM of memory 2^9 consists of 7711 number of cells

, with 4104 number of sequential circuits, 58 inverter, 1 buffer and 3548 logic gates. These instances consumes leakage power of 272nw with 9380267.182 nw of dynamic power. Thenet area is 61 with slack time of 3865ps.

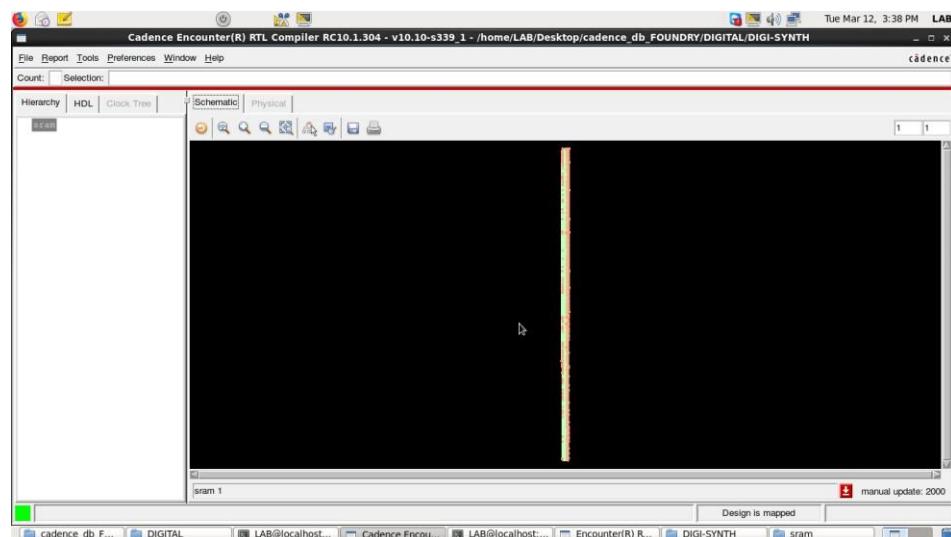


Fig 4.2 Synthesized image of RAM memory address 2^{10}

The Fig 4.2 represents the synthesis of RAM of memory 2^{10} consists of 15334 number of cells , with 8200 number of sequential circuits , 106 inverter, 10 buffer and 7018 logic gates.These instances consumes leakage power of 12.484nw with 18893960.731 nw of dynamic power . The net area is 121 with slack time of 3970ps.

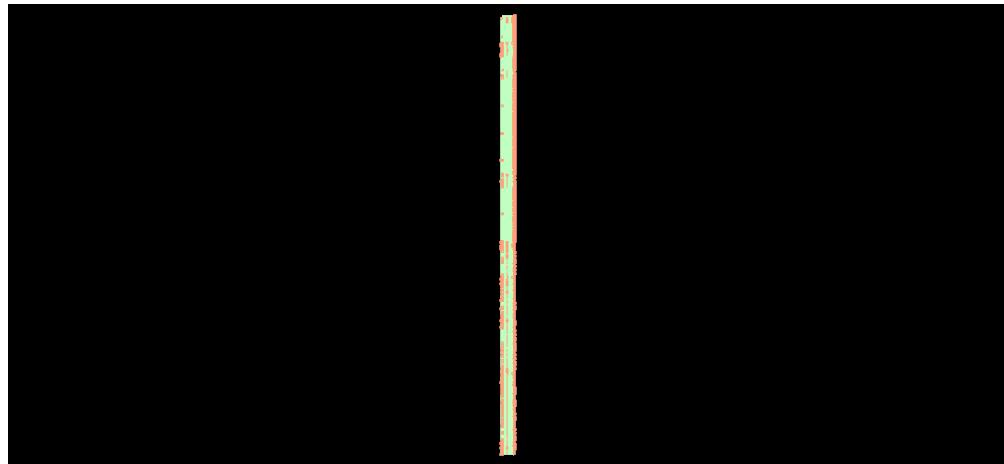


Fig 4.3 Synthesized image of RAM memory address 2^{12}

The Fig 4.3 represents the synthesis of RAM of memory 2^{12} consists of 30777 number of cells , with 16392 number of sequential circuits , 239 inverter, 110 buffer and 14036 logic gates.These instances consumes leakage power of 25.090nw with 37718533.871 nw of dynamic power . The net area is 242 with slack time of 3623ps.

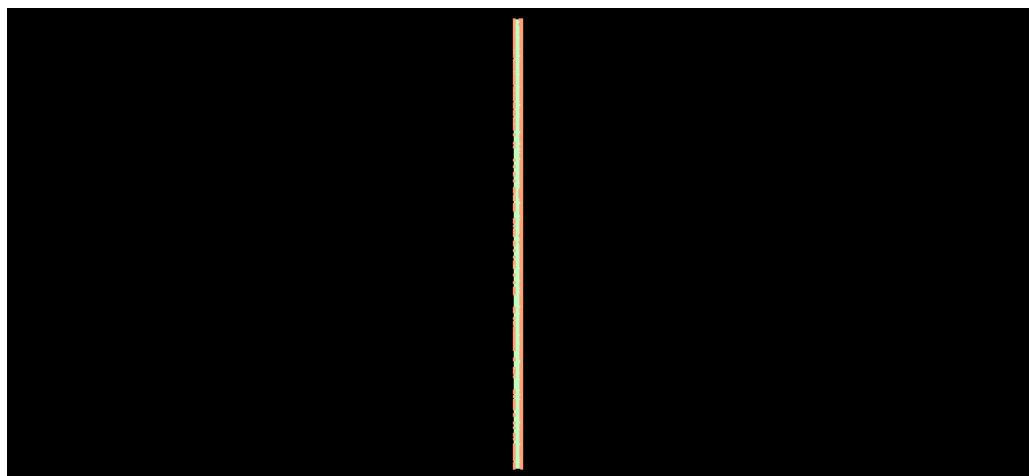


Fig 4.4 Synthesized image of RAM memory address 2^{14}

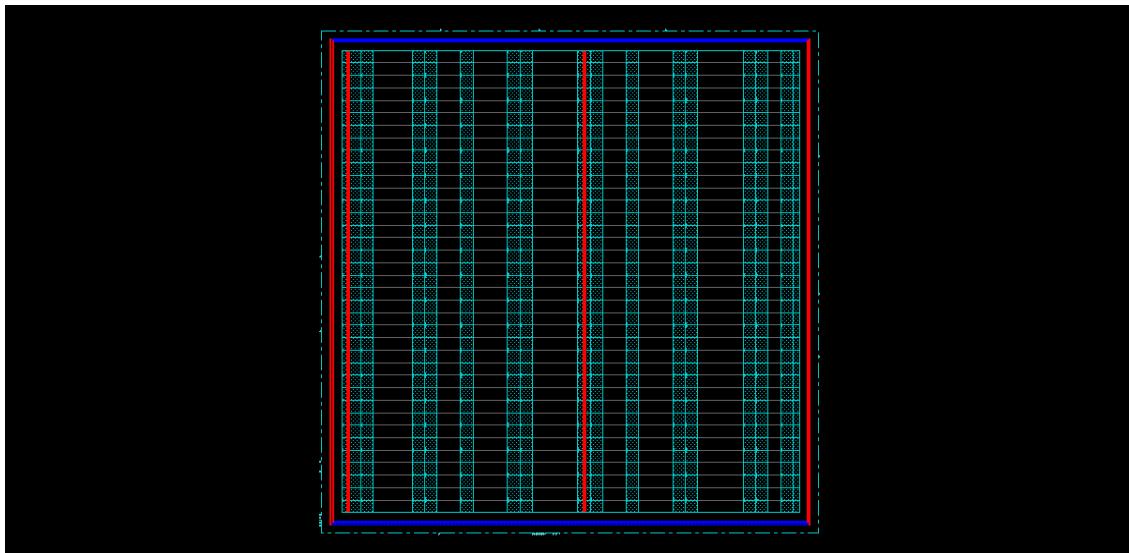
The Fig 4.4 represents the synthesis of RAM of memory 2^{14} consists of 61005 number of cells, with 32776 number of sequential circuits, 5171inverter, 195 buffer and 27836 logic gates. These instances consume leakage power of 49.983nw with 74842981.670 nw of dynamic power. The net area is 483 with slack time of 3465ps. Here the slack time reduced to other memory.

Table 4.1 Summary Report of RAM design

| MEMORY SIZE | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|-----------------|--------------|------------|-------------|-------------|
| CELLS | 7711 | 15334 | 30777 | 61005 |
| INSTANCE | SEQUENTIAL | 4104 | 8200 | 16392 |
| | INVERTER | 58 | 106 | 239 |
| | BUFFER | 1 | 10 | 110 |
| | LOGIC | 3548 | 7018 | 14036 |
| POWER | LEAKAGE (nw) | 6.272 | 12.484 | 25.090 |
| | DYNAMIC (nw) | 9380267.18 | 18893960.73 | 37718533.87 |
| | TOTAL (nw) | 9380273.45 | 18893973.21 | 37718558.96 |
| SLACK TIME (ps) | 3865 | 3970 | 3623 | 3465 |
| NET AREA | 61 | 121 | 242 | 483 |

Table 4.2 Summary report of RAM in Physical Implementation

| MEMORY SIZE | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|-------------|----------------------------|-----------|-----------|-------------|
| POWER | METAL1(um) | 177.0824 | 177.2403 | 343.4640 |
| | METAL2(um) | 335.0160 | 342.2320 | 993.0448 |
| AREA | STD.CELL(um ²) | 41001.206 | 81642.860 | 133877.621 |
| | CORE(um ²) | 36068.029 | 67168.049 | 142023.168 |
| | CHIP (um ²) | 42603.786 | 82684.184 | 4557750.534 |

Fig 4.5 Floorplan view of RAM 2^9

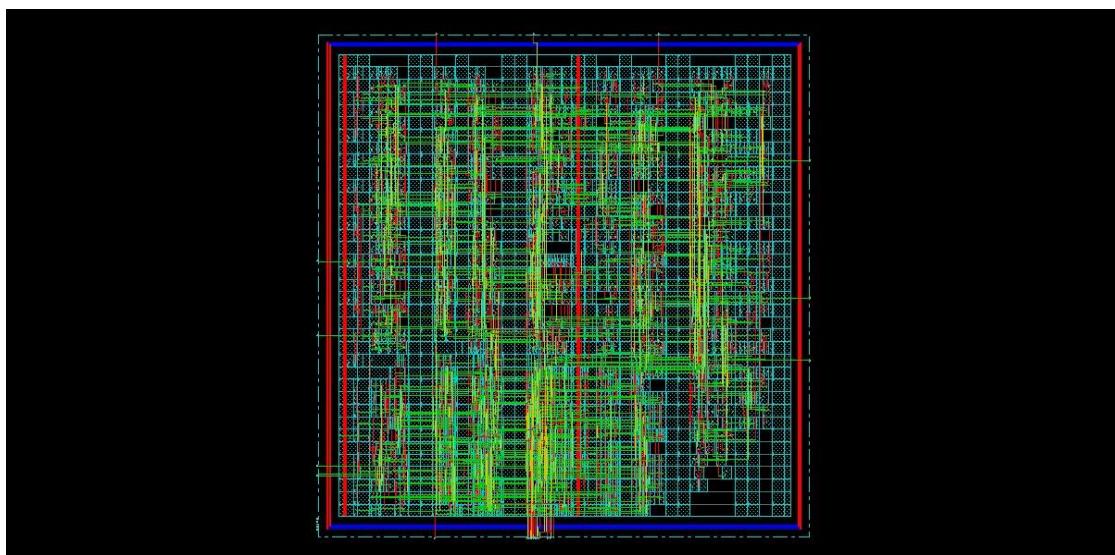


Fig 4.6 Cell Placement view of RAM 2⁹

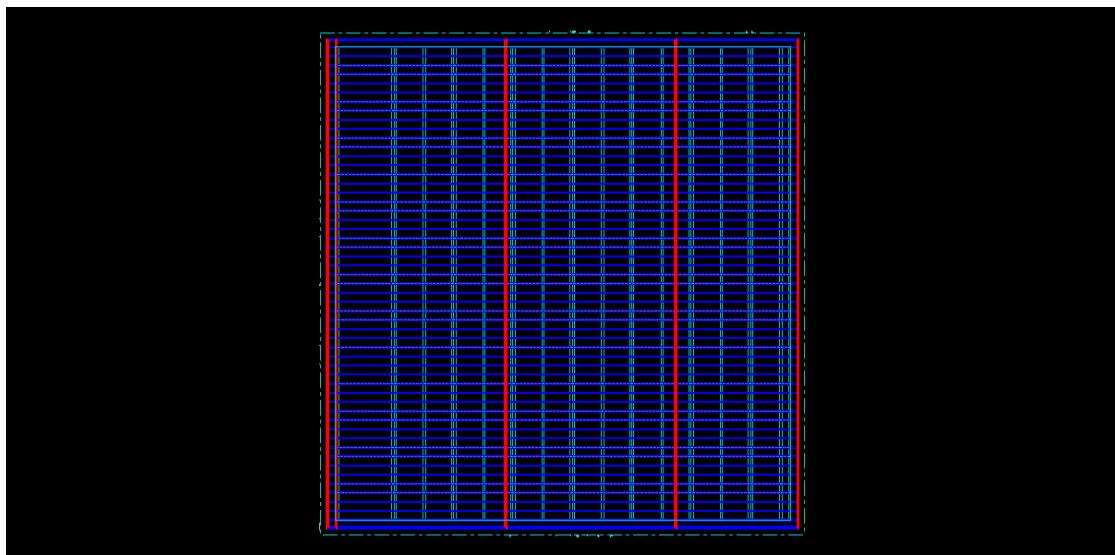


Fig 4.7 Floorplan view of RAM 2¹⁰

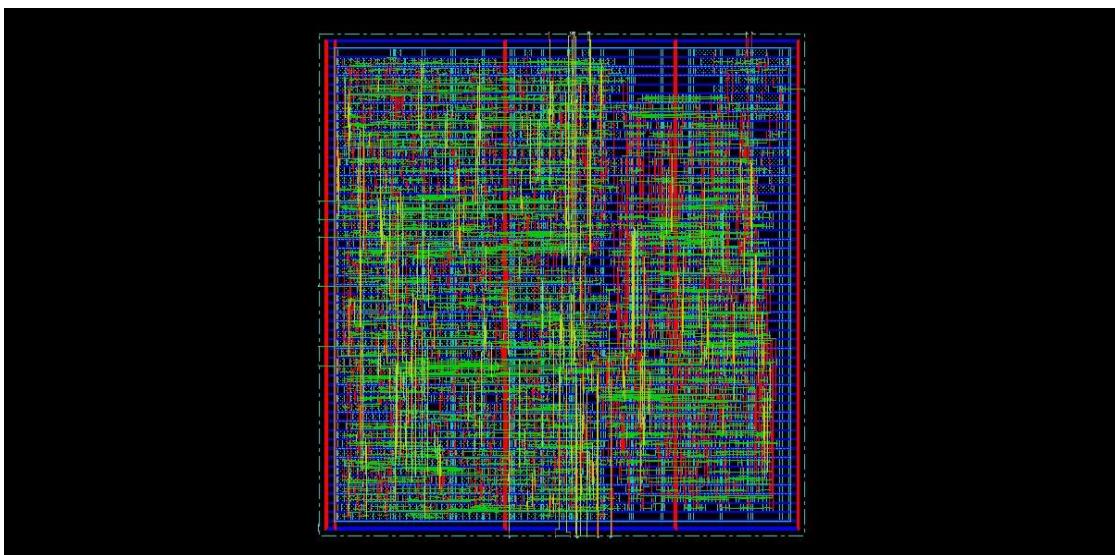


Fig 4.8 Cell Placement view of RAM 2¹⁰

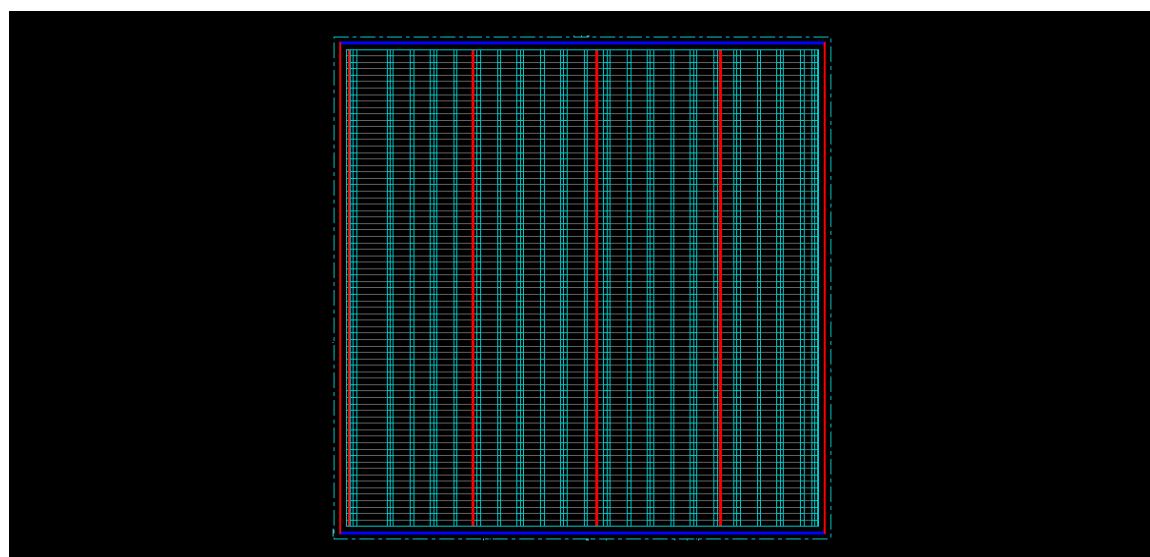


Fig 4.9 Floorplan View of RAM 2^{12}

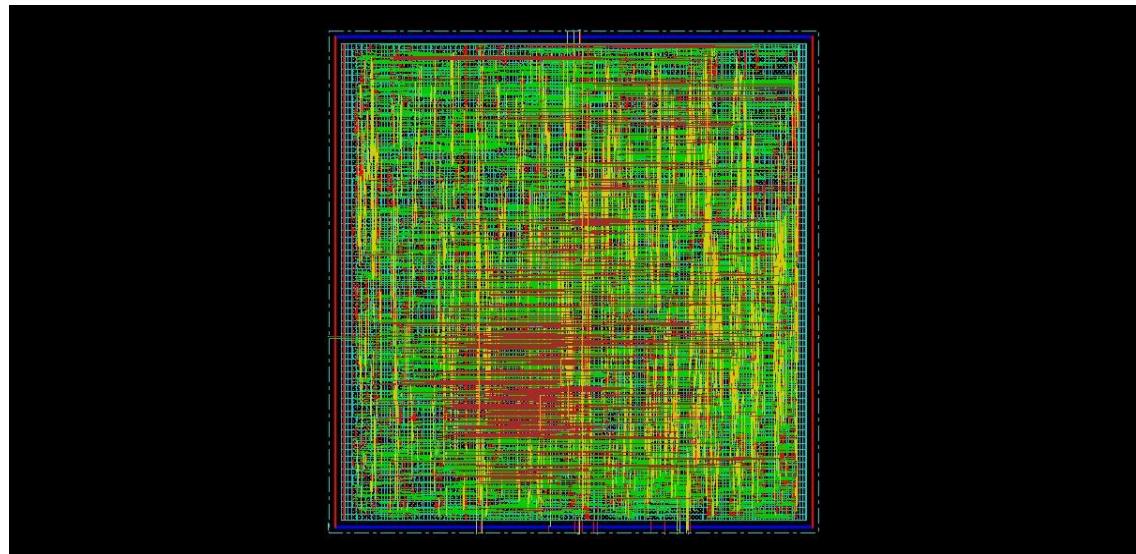


Fig 4.10 Cell Placement View of RAM 2^{12}

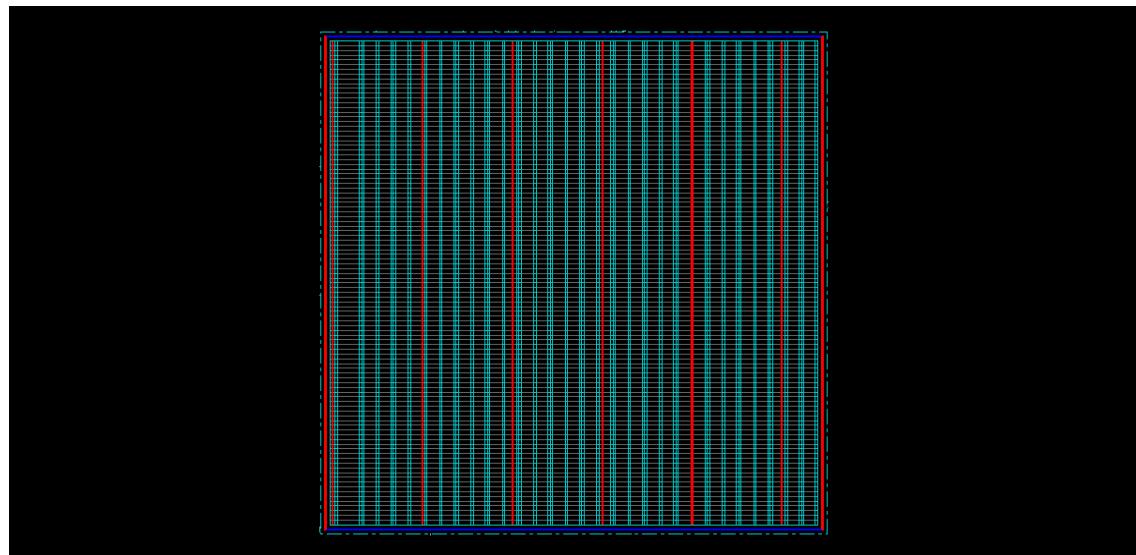


Fig 4.11 Floorplan View of RAM 2^{14}

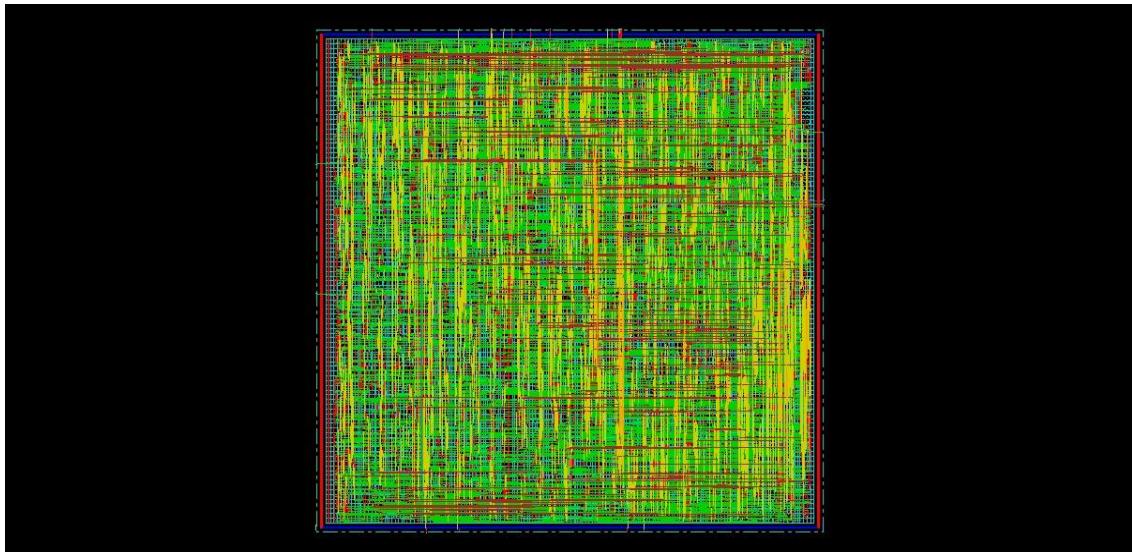


Fig 4.12 Cell Placement view of RAM 2^{14}

ROM

The below images represent the result of ROM

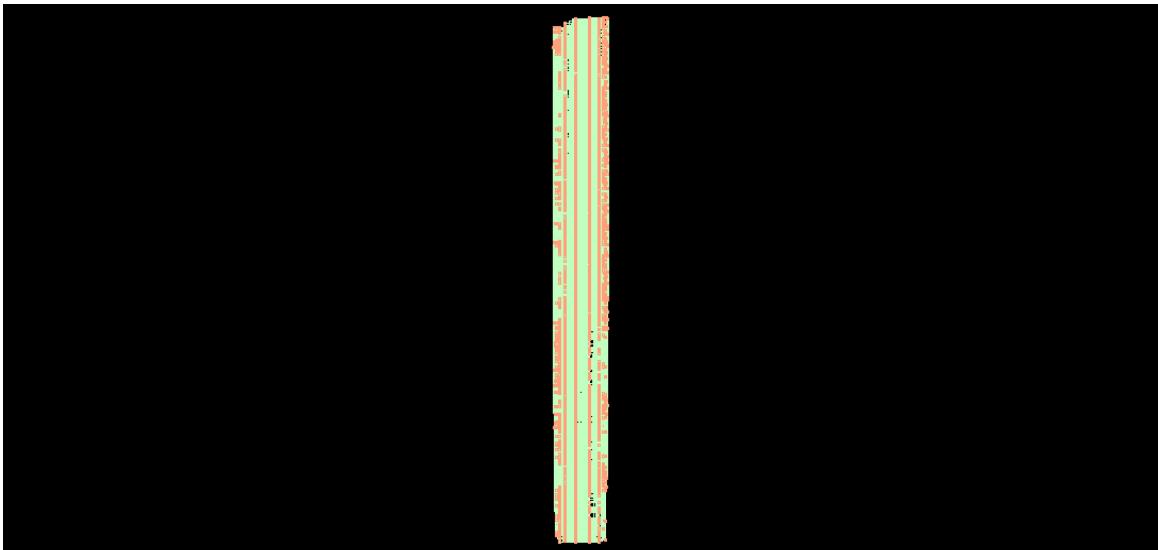


Fig 4.13 Synthesized image of ROM memory address 2^9

The Fig 4.14 represents the synthesis of rom of memory 2^9 consists of 6493 number of cells , with 8 number of sequential circuits , 1098 inverter, 46 buffer and 5341 logic gates. These instances consumes leakage power of 3.428 nw with 783463 nw of dynamic power . The net area is 26 with slack time of 128ps.

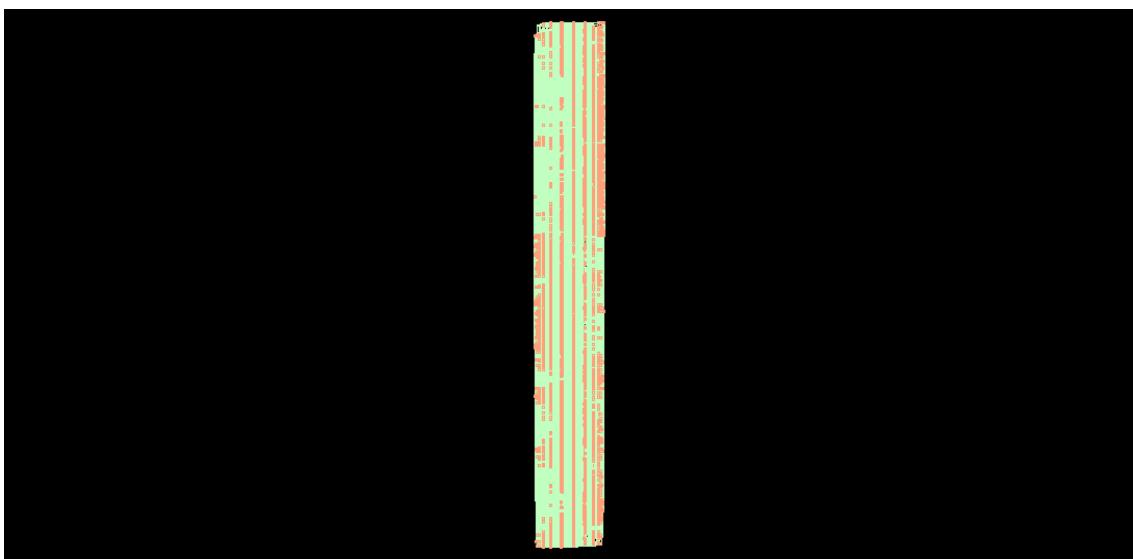


Fig 4.14 Synthesized image of ROM memory address 2^{10}

The Fig 4.15 represents the synthesis of rom of memory 2^{10} consists of 12370 number of cells , with 8 number of sequential circuits , 1684 inverter, 158 buffer and 10520 logic gates. These instances consumes leakage power of 5.393 nw with 783463 nw of dynamic power . The net area is 51 with slack time of 309ps

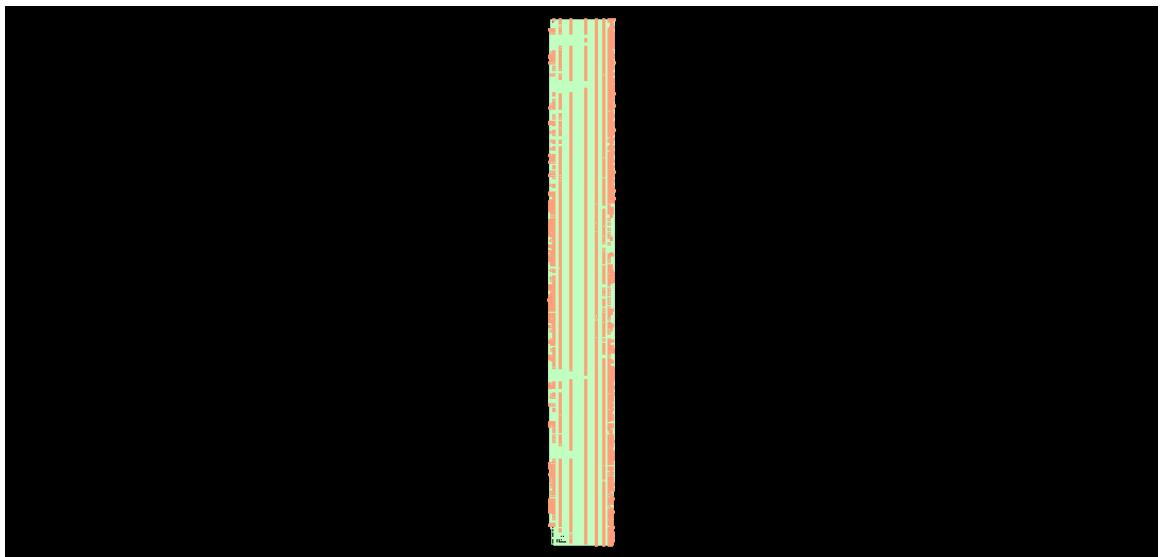


Fig 4.15 Synthesized image of ROM memory address 2^{12}

The Fig 4.16 represents the synthesis of rom of memory 2^{12} consists of 6493 number of cells , with 8 number of sequential circuits , 5494 inverter, 436 buffer and 21533 logic gates. These instances consumes leakage power of 272nw with 9380267.182 nw of dynamic power . The net area is 107 with slack time of 366 ps.

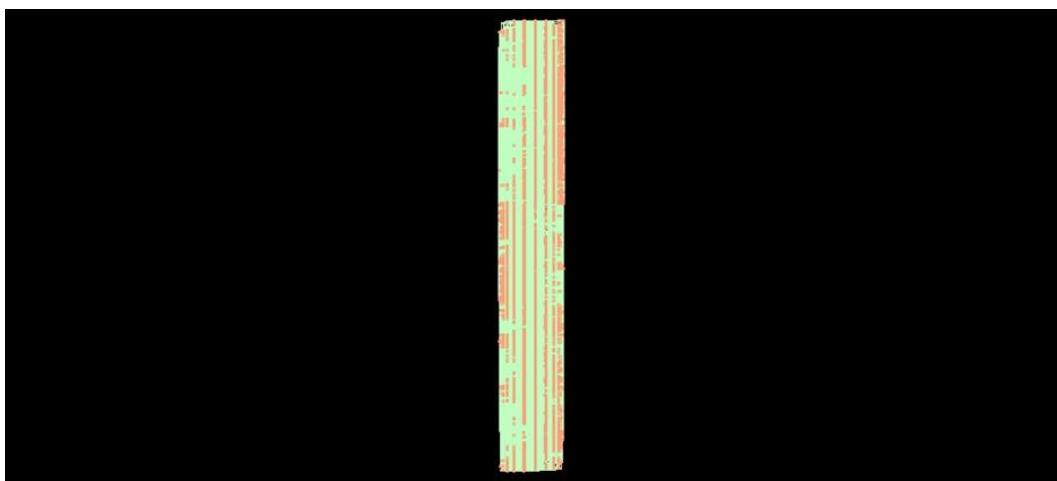


Fig 4.16 Synthesized image of ROM memory address 2^{14}

The Fig 4.1 represents the synthesis of rom of memory 2^{14} consists of 6493 number of cells , with 8 number of sequential circuits , 9649 inverter, 626 buffer and 45320 logic gates. These instances consumes leakage power of 80.191 nw with 5778829 nw of dynamic power. The net area is 216 with slack time of 511 ps

Table 4.3 Summary Report of ROM design

| MEMORY SIZE | | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|------------------------|---------------------|-------------------------|----------------------------|----------------------------|----------------------------|
| CELLS | | 6493 | 12370 | 27471 | 55603 |
| INSTANCE | SEQUENTIAL | 8 | 8 | 8 | 8 |
| | INVERTER | 1098 | 1684 | 5494 | 9649 |
| | BUFFER | 46 | 158 | 436 | 626 |
| | LOGIC | 5341 | 10520 | 21533 | 45320 |
| POWER | LEAKAGE (nw) | 3.428 | 5.393 | 12.237 | 80.191 |
| | DYNAMIC (nw) | 783463 | 1381633 | 3028347 | 5778829 |
| | TOTAL (nw) | 783469 | 1381639 | 3028359 | 5778909 |
| SLACK TIME (ps) | | 128 | 309 | 366 | 511 |
| NET AREA | | 26 | 51 | 107 | 216 |

Table 4.4 Summary report of ROM in Physical Implementation

| MEMORY SIZE | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|---|-------------------------|----------------------------|----------------------------|----------------------------|
| POWER | | | | |
| METAL1 | 177.0824 | 177.2403 | 343.4640 | 486.2308 |
| METAL2 | 335.0160 | 342.2320 | 993.0448 | 1817.9920 |
| AREA | | | | |
| STD.CELL(μm^2) | 130374.922 | 224811.418 | 485880.595 | 1044506.232 |
| CORE(μm^2) | 186251.184 | 321160.896 | 694115.730 | 1492162.560 |
| CHIP (μm^2) | 200756.032 | 340122.666 | 721864.240 | 1532720.680 |

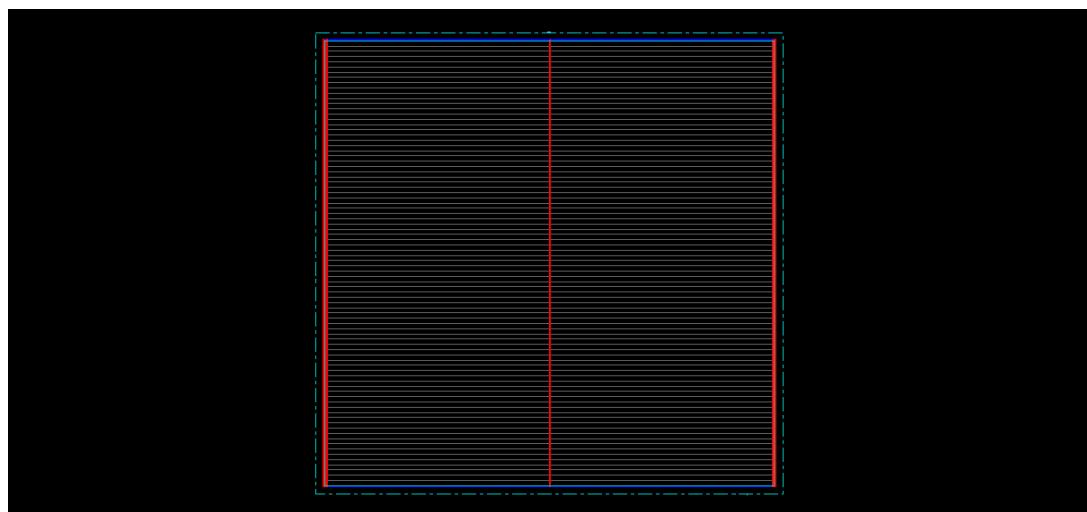


Fig 4.17 Floorplan view of ROM 2^9

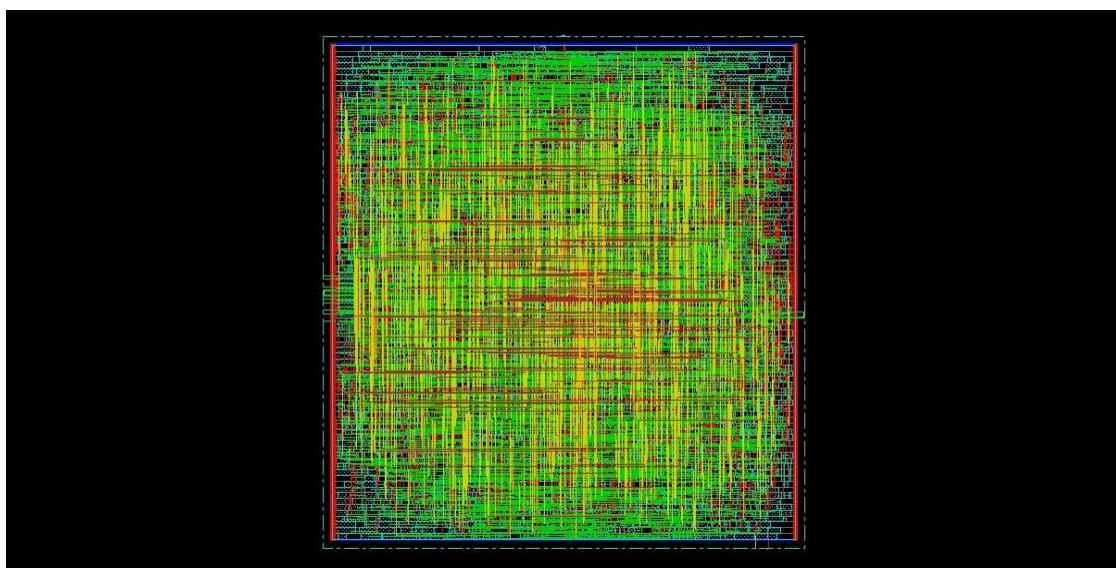


Fig 4.18 Cell Placement view of ROM 2^9

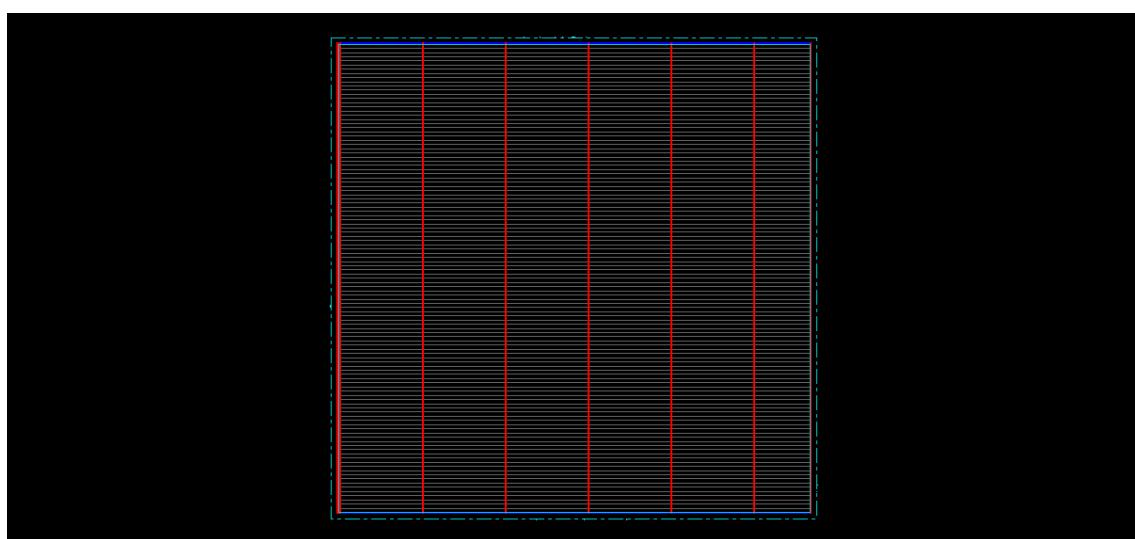


Fig 4.19 Floorplan view of ROM 2^{10}

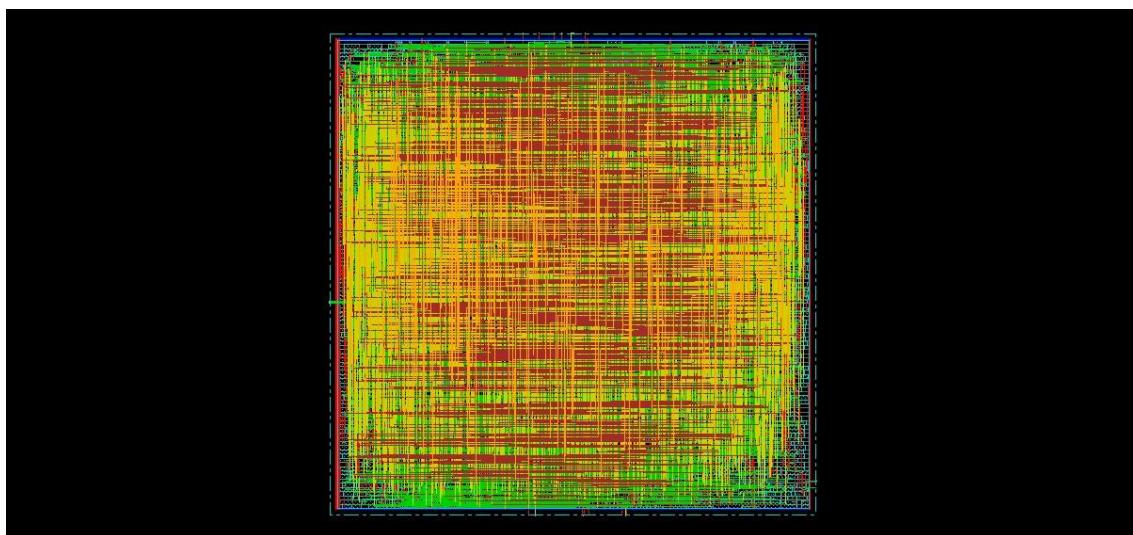


Fig 4.20 Cell Placement view of ROM 2^{10}



Fig 4.21 Floorplan view of ROM 2^{12}

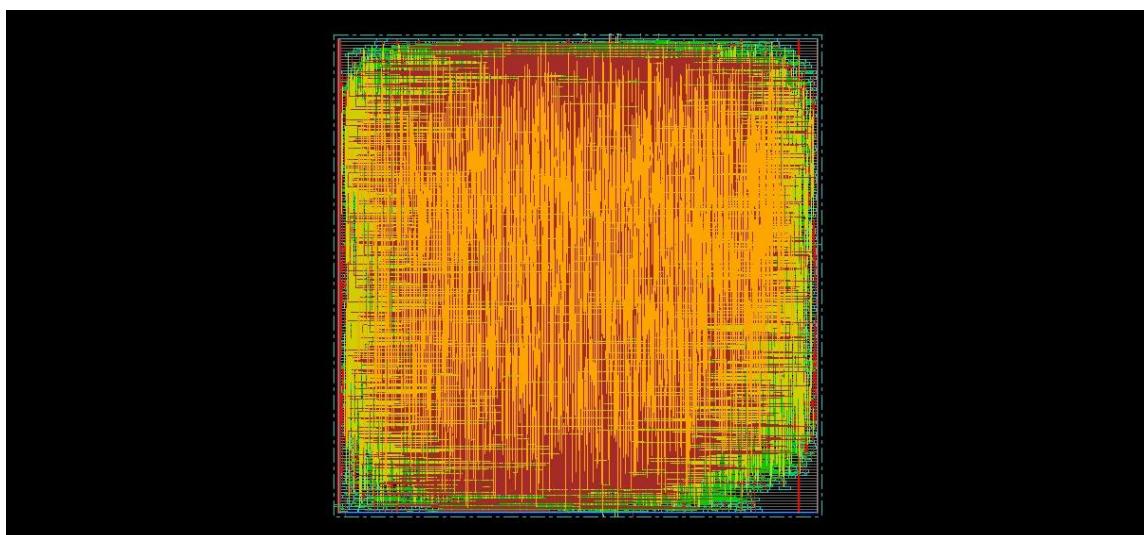


Fig 4.22 Cell Placement view of ROM 2^{12}

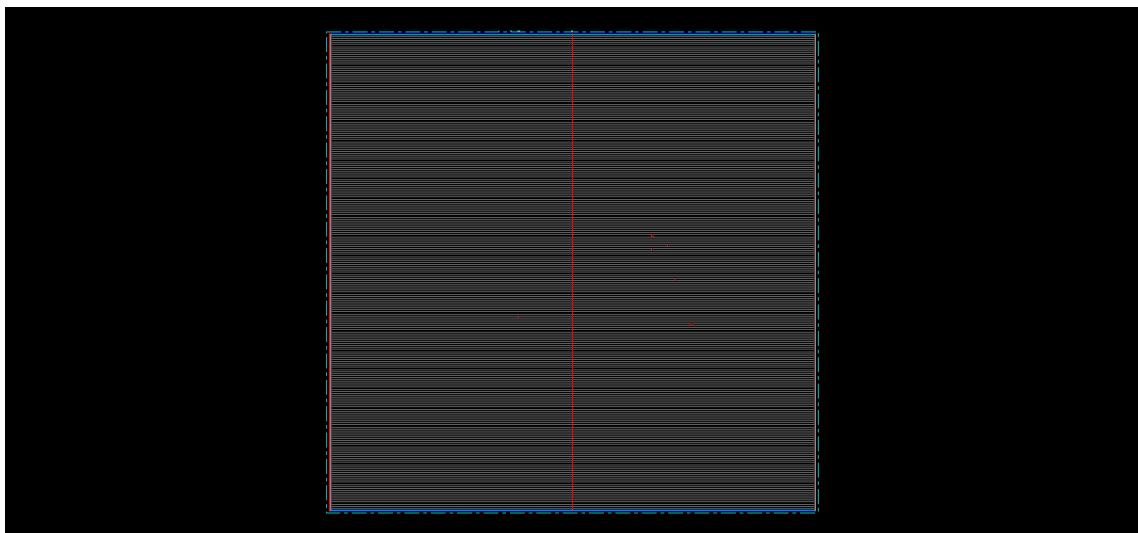


Fig 4.23 Floorplan view of ROM 2¹⁴

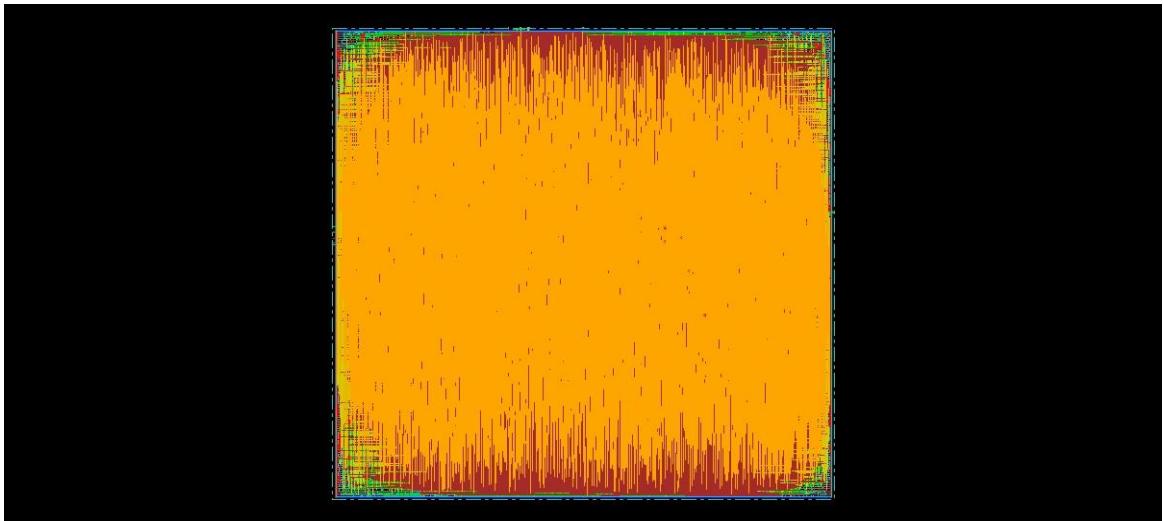


Fig 4.24 Cell Placement view of ROM 2¹⁴

4.2 Advantages

- **Efficiency:** Cadence software tools provide efficient algorithms and methodologies for synthesizing RAM and ROM components. This efficiency translates to faster design iterations and shorter time-to-market for ICs.
- **Optimization:** The synthesis process in Cadence software optimizes the design for various parameters such as area, power consumption, and performance. This optimization ensures that the RAM and ROM blocks meet the design requirements while utilizing resources effectively.
- **Integration:** Cadence tools facilitate the seamless integration of RAM and ROM blocks into larger IC designs. This integration includes connecting memory blocks to other functional units, such as processors or peripherals, ensuring compatibility and smooth operation of the entire system.

- **Customization:** Designers can customize the RAM and ROM blocks according to specific requirements using Cadence software. This customization may involve adjusting parameters such as size, speed, and organization to tailor the memory components to the application's needs.
- **Verification:** Cadence software provides robust verification capabilities, allowing designers to verify the functionality and correctness of synthesized RAM and ROM designs. This verification process helps identify and rectify any potential errors or inconsistencies early in the design cycle, reducing the risk of costly design flaws.

4.3 Disadvantages

- **Complexity:** Synthesizing RAM and ROM can be complex and require deep understanding of the memory architecture, timing constraints, and design constraints, which may pose challenges for designers.
- **Area Overhead:** The synthesis process may introduce additional area overhead compared to manually designed memories, potentially impacting overall chip size and efficiency.
- **Performance Trade-offs:** The synthesis process might not always optimize for the best performance, leading to potential trade-offs between speed, area, and power consumption.
- 4. Limited Customization: Synthesis tools may have limitations in allowing designers to fully customize the memory architecture or optimize for specific requirements, potentially constraining design flexibility.
- **Verification Complexity:** Verifying the synthesized memories can be challenging, as the generated netlists may be complex and require thorough verification to ensure functionality and reliability. Overall, while synthesis tools like Cadence offer convenience and automation, designers need to carefully consider these potential drawbacks and evaluate whether synthesizing RAM and ROM is the best approach for their specific design requirements.

4.4 Applications

RAM and ROM in Cadence software is widely used across various domains of digital design to efficiently implement memory structures and meet the performance, power, and area requirements of modern electronic systems.

Applications of RAM includes:

- **Main memory in computers:** RAM ICs are used as the primary memory for storing program instructions and data during the execution of applications.
- **Cache memory:** Some ICs incorporate RAM as cache memory to temporarily store frequently accessed data, reducing access times and improving overall system performance.

- **Buffering:** RAM ICs are often used as buffers in data-intensive applications to temporarily hold data during processing or transfer between different components.

Applications of Rom includes:

ROM integrated circuits store non-volatile data or instructions that are permanently programmed during manufacturing and cannot be altered or overwritten during normal operation.

- **Firmware storage:** Integrated circuits often incorporate ROM to store firm ware or microcode used to control various functions of electronic devices, such as embedded systems, IoT devices, and consumer electronics.
- **System configuration:** ROM ICs may contain configuration data or settings that are essential for the operation of a device or system, such as calibration values, device parameters, or lookup tables.

In summary, RAM and ROM integrated circuits are fundamental components used in electronic devices to provide temporary data storage and permanent program storage, respectively. They enable efficient operation and functionality of a wide range of electronic systems, from computers and smartphones to embedded devices and IoT endpoints.

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CONCLUSION

In conclusion, this project has successfully demonstrated the synthesis and physical implementation of Random Access Memory (RAM) and Read-Only Memory (ROM) modules using Cadence design tools. Through a systematic approach encompassing architectural design, RTL coding, synthesis, place and route, and thorough verification, both RAM and ROM modules were designed, synthesized, and physically implemented according to the specified requirements. The design and implementation of the SRAM and ROM memory is a challenging and valuable learning experience. This project will provide an opportunity to learn Cadence Virtuoso tools and also gain the knowledge and understand VLSI design. The static RAM is very widely used in CMOS systems. The project involved various stages, starting from the initial concept and requirements specification, through RTL (Register-Transfer Level) design, functional verification, synthesis, and ultimately to the generation of the final layout. Cadence's suite of tools played a vital role in facilitating these stages, providing a robust platform for designing and optimizing digital circuits. During the synthesis phase, the Cadence tools allowed for efficient mapping of the RTL description to a gate-level netlist, optimizing for factors such as area, power, and performances. Through comparative analysis, we evaluated the performance of both RAM and ROM modules, considering factors such as speed, area efficiency, and reliability. The results indicate that the design objectives were met, and the memory modules functioned effectively within the constraints of the project requirements. In summary, this project has enhanced our understanding of memory module design and the Cadence design flow. It has provided valuable insights into the synthesis and physical implementation of RAM and ROM modules, contributing to advancements in digital system design methodologies. Overall, this project signifies a significant milestone in the application of Cadence tools for memory module design and implementation.

REFERENCE

- [1]. Shylashree Nn, Yatish D Vahvale “Design and Implementation of 64-bit SRAM and CAM on Cadence and Open-source environment” in July 2021 International Journal of Circuits Systems and Signal Processing 15:586-594
- [2]. Ravi Kumar. K. I, Vijayalaxmi. C. Kalal, Rajani. H. P, Dr. S. Y. Kulkarni “Design and verification of low power 64-bit SRAM system using 8T SRAM: Back-End approach” in International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2012
- [3]. Siddalingesh S. Navalgund, Prakash R Tonse “Design and Development and Implementation of ALU, RAM and ROM for 8051 Microcontroller on FPGA using VHDL” in International Journal of Computer Applications (0975 – 8887) Volume 80 – No1, October 2013
- [4]. N. Surana and J. Mekie, "Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 1023-1027, June 2019, doi: 10.1109/TCSII.2018.2869945.
- [5]. D. Shah, E. Hung, C. Wolf, S. Bazanski, D. Gisselquist and M. Milanovic, “Yosys nextpnr: An OpenSource Framework from Verilog to Bitstream for Commercial FPGAs,” 2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing MachineS (FCCM), 2019, pp. 1-4, doi: 10.1109/FCCM.2019.00010.
- [6]. Shabana Aqueel and Kavita Khare, “Design and FPGA Implementation of DDR3 SDRAM Controller for High Performance”, International Journal of Computer

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PROJECT**

Paper Presented

- [1] Mr. Chandra Shekar P, Kusuma M, Chandana Y S “RAM Synthesis and Physical Realization in Cadence Design Environment” in April 2024 IETE Sponsored 6th National Conference on Emerging Trends in Engineering, Science and Technology (NCTEST-6).
- [2] Mr. Chandra Shekar P, Kavana K, Khushi M “Synthesis and Physical Implementation Of ROM Modules: A Comprehensive Study Using Cadence Design Tool” in April 2024 IETE Sponsored 6th National Conference on Emerging Trends in Engineering, Science and Technology (NCTEST-6).

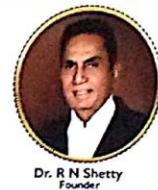


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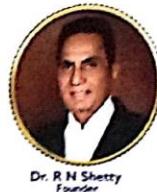


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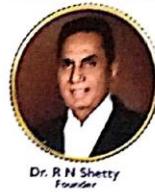


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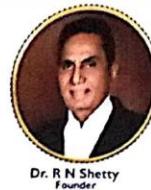
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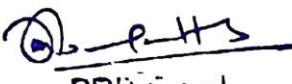
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RAM Synthesis and Physical Realization in Cadence Design Environment

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Abstract - This project presents the synthesis and physical implementation of Random Access Memory (RAM) modules using Cadence design tools. A versatile Electronic Design Automation (EDA) tool suite widely utilized in the semiconductor industry. Cadence software offers a comprehensive environment for designing and customizing memory components. In Cadence, the specification of the design is implemented using Hardware Description Languages (HDLs) such as VHDL or Verilog. The primary objective was to design, synthesize, and physically implement both RAM modules, ensuring their functionality and performance meet the desired specifications. The process involved architectural design, RTL coding, synthesis, place and route, and thorough verification. Through this project, a comprehensive understanding of memory module design and the Cadence design flow was attained. The results demonstrate successful implementation of both RAM and modules, validating their correctness and functionality. This project contributes to advancing the knowledge and skills in digital design and memory system implementation using Cadence tools.

Keywords - Random Access Memory (RAM), Cadence design tools, Electronic Design Automation (EDA), semiconductor industry, Hardware Description Languages (HDLs), VHDL, Verilog, architectural design, RTL coding, synthesis, place and route, verification, memory module design, Cadence design flow, digital design, memory system implementation.

I. INTRODUCTION

RAM is an indispensable building blocks in the development of electronic devices, from microcontrollers and smart phones to high-performance computing systems. RAM provides fast, temporary storage for data that can be read from and written to, enabling rapid processing and multitasking. ROM, on the other hand, stores essential firmware and software instructions that remain unchanged during operation. Both RAM and ROM are pivotal in ensuring the functionality and performance of electronic systems. Cadence software offers a versatile platform for designing, synthesizing, and verifying complex digital circuits, including memory components like RAM. This software

suite provides a comprehensive set of tools that guide designers through each stage of the memory design process, from initial specifications to physical implementation. Key functionalities include RTL synthesis, technology mapping, timing analysis, layout generation, and power optimization.

The synthesis of RAM (Random Access Memory) using Cadence software typically involves a series of steps within the digital design flow. Cadence is a well-known provider of electronic design automation (EDA) tools, and its suite of software includes tools for digital design, verification, and implementation. Here's an overview of the synthesis process for RAM using Cadence software.

1. Design Entry: Use a hardware description language (HDL) such as Verilog or VHDL to describe the SRAM circuit functionality.

2. RTL Synthesis: Utilize Cadence's RTL synthesis tools to convert the high-level description into a Register Transfer Level (RTL) netlist.

3. Optimization: Perform optimization to improve the design in terms of area, power, and timing using tools like Cadence Genus.

4. Technology Mapping: Map the synthesized RTL to the target technology library, considering the specific characteristics of the SRAM cells available in that library.

5. Place and Route: Use Cadence Innovus or Encounter tools for place and route to physically place the cells on the chip and create the detailed routing.

6. Timing Closure: Perform timing analysis and optimization to ensure that the design meets the required timing constraints.

7. Verification: Use Cadence simulation tools, such as Incisive, to verify the functionality and performance of the SRAM design.

8. Physical Verification: Perform physical verification checks to ensure that the layout adheres to manufacturing rules.

9. Extraction: Extract parasitic information from the layout for further accurate analysis.

10. Final Tape-out: Prepare the final set of files for manufacturing (GDSII files) to create the physical RAM chips.

II. DESIGN METHODOLOGY

Architectural Design: The first step involved defining the architecture of RAM, specifying parameters such as size, address width.

For RAM, the architecture included data input/output ports, address inputs, control signals, and memory cells.

1. RTL Coding: Using Verilog HDL, the architecture was translated into Register Transfer Level (RTL) code. RTL code for RAM included modules for memory cells, input/output ports, and control logic code for ROM consisted of a module for address decoding and data output.

2. Synthesis: The RTL code was synthesized using Cadence RTL Compiler to generate gate-level netlists. Synthesis optimizations were applied to improve the performance and area efficiency of the designs.

3. Place and Route: The gate-level netlists were subjected to place and route using Cadence Encounter to map the logic onto physical hardware resources. Constraints such as timing, area, and power were considered during place and route to meet design specifications.

III. BLOCK DIAGRAM

The below figure represents the RAM. RAM is a form of electronic computer memory that can be read and changed in any order, typically used to store working data and machine code. RAM is a high-speed volatile memory used to store and process temporary data.

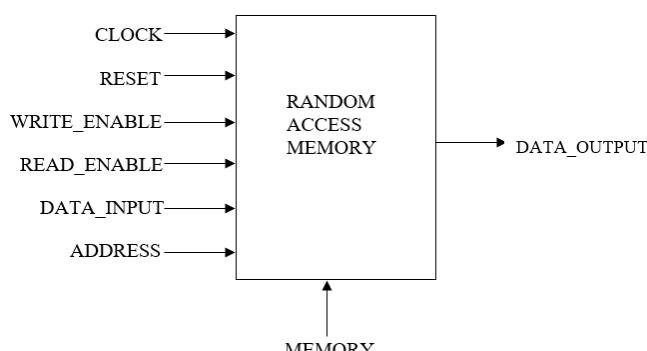


Fig 3.1: Block Diagram of RAM

It is used in CPU Cache and primary memory. A RAM unit stores the data and programs that the CPU uses in real time process. This data is available for different access modes including reading, writing and erasing. This hardware unit that stores the data for the utilization purpose. The figure shows the basic block diagram of random-access memory. It consists of clock, reset, write enable, read enable, data input, address signals as input and data output as output. Memory is defined as a reg. The circuit works under positive clock edge. If reset signal is high no data is obtained in data output signal. To write data into the memory write enable signal should be set to one and memory address is given to address signal. To read data from the memory read enable will be set to one and address is given to address signal. The data read from the memory is obtained in data output signal.

IV. SOFTWARE SPECIFICATIONS

The synthesis and physical implementation of ROM using Cadence typically require a suite of software tools that facilitate various stages of the design flow. Below are the essential software requirements for this process:

Cadence Design Tools: Cadence provides a range of tools for digital design, synthesis, place and route, and verification. The specific tools needed include:

1. RTL COMPILER: RTL Compiler will execute the instructions in the TCL file and will generate the output files and reports in the “out” folder. The generated files: “.v”: Which has the new gate level Verilog description of the synthesized system.

2. Encounter: Cadence Encounter is a place-and-route tool that uses a Verilog netlist and generates its equivalent layout view. This tutorial describes how to use Cadence SOC Encounter to generate a layout view of the synthesized design, using standard cells library.

3. Library Files: Standard cell libraries and technology files specific to the target process technology. These files provide essential information for synthesis and physical implementation, such as cell timing, power, and physical characteristics.

V RESULTS

Using Verilog HDL, the architecture was translated into Register Transfer Level (RTL) code. RTL code for RAM included modules for memory cells, input/output ports, and control logic code for ROM consisted of a module for address decoding and data output. The RTL code was synthesized using Cadence RTL Compiler to generate gate-level netlists.

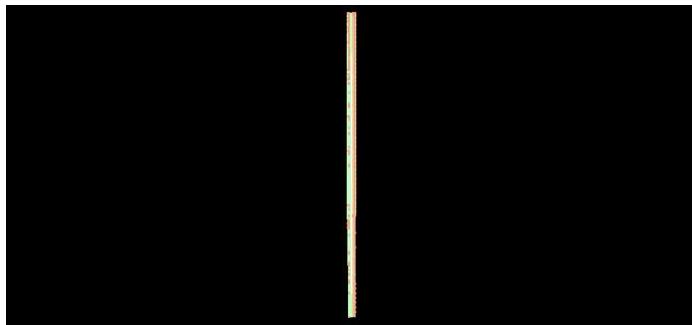


Fig 5.1: Synthesized image of RAM memory address 511

The figure represents the synthesis of sram of memory 2^9 consists of 7711 number of cells , with 4104 number of sequential circuits,58 inverter, 1 buffer and 3548 logic gates.These instances consumes leakage power of 272nw with 9380267.182 nw of dynamic power . The net area is 61 with slack time of 3865ps.

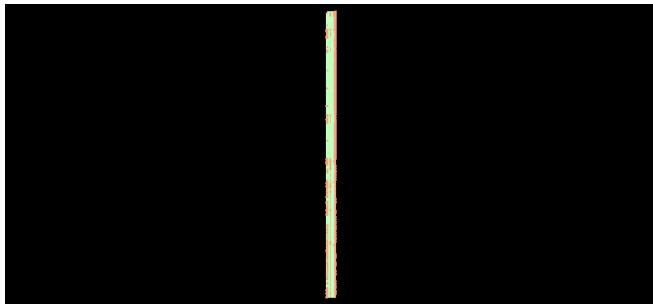


Fig 5.2: Synthesized image of RAM memory address 1K

The figure represents the synthesis of sram of memory 2^{10} consists of 15334 number of cells , with 8200 number of sequential circuits, 106 inverter, 10 buffer and 7018 logic gates.These instances consumes leakage power of 12.484nw with 18893960.731 nw of dynamic power . The net area is 121 with slack time of 3970ps.

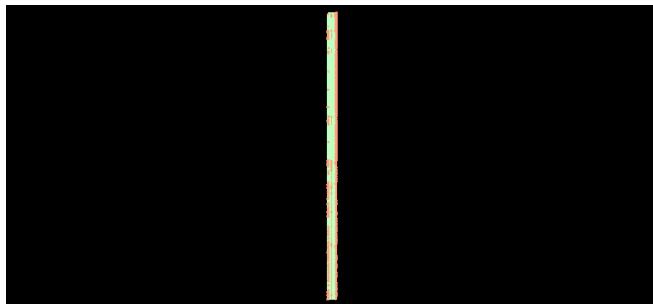


Fig 5.3: Synthesized image of RAM memory address 2K

The figure represents the synthesis of sram of memory 2^{12} consists of 30777 number of cells , with 16392 number of sequential circuits , 239 inverter, 110 buffer and 14036 logic gates.These instances consumes leakage power of 25.090nw with

37718533.871 nw of dynamic power . The net area is 242 with slack time of 3623ps.

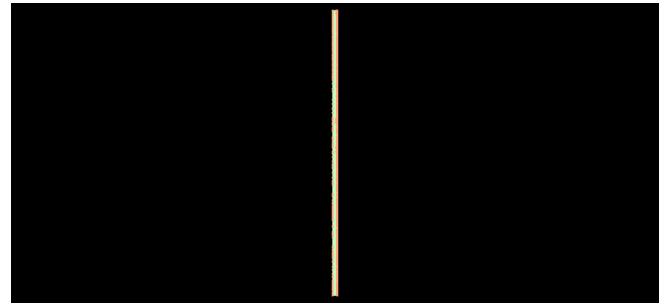


Fig 5.4: Synthesized image of RAM memory address 4K

The figure represents the synthesis of sram of memory 2^{14} consists of 61005 number of cells , with 32776 number of sequential circuits , 5171inverter, 195 buffer and 27836 logic gates.These instances consumes leakage power of 49.983nw with 74842981.670 nw of dynamic power . The net area is 483 with slack time of 3465ps.Here the slack time reduced to other memory .

Table 5.1: Summary Report of Ram Design

| MEMORY SIZE | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|-----------------|--------------|------------|-------------|-------------|
| CELLS | 7711 | 15334 | 30777 | 61005 |
| INSTANCE | SEQUENTIAL | 4104 | 8200 | 16392 |
| | INVERTER | 58 | 106 | 239 |
| | BUFFER | 1 | 10 | 110 |
| | LOGIC | 3548 | 7018 | 14036 |
| POWER | LEAKAGE (nw) | 6.272 | 12.484 | 25.090 |
| | DYNAMIC (nw) | 9380267.18 | 18893960.73 | 37718533.87 |
| | TOTAL (nw) | 9380273.45 | 18893973.21 | 74842981.67 |
| SLACK TIME (ps) | 3865 | 3970 | 3623 | 3465 |
| NET AREA | 61 | 121 | 242 | 483 |

Table 5.2: Summary on Physical Implementation

| MEMORY SIZE | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|-------------|-----------------------------|-----------|-----------|-------------|
| POWER | METAL1(um) | 177.0824 | 177.2403 | 343.4640 |
| | METAL2(um) | 335.0160 | 342.2320 | 993.0448 |
| AREA | STD.CELL(μm^2) | 41001.206 | 81642.860 | 133877.621 |
| | CORE (μm^2) | 36068.029 | 67168.049 | 142023.168 |
| | CHIP (μm^2) | 42603.786 | 82684.184 | 4557750.534 |

Floor planning is the process of creating an initial layout of the chip's functional blocks. It involves partitioning the chip area into regions for various purposes such as logic, memory, and input/output (I/O). Floor planning also includes defining the locations and approximate sizes of these blocks, considering factors like power distribution, clock distribution, and signal routing. Cell placement involves determining the precise locations of individual standard cells within the predefined regions established during floor planning. The placement process aims to optimize various objectives such as minimizing wire lengths, reducing signal delays, and meeting timing constraints. Advanced placement algorithms use

techniques like simulated annealing or analytical methods to find an optimal placement solution.

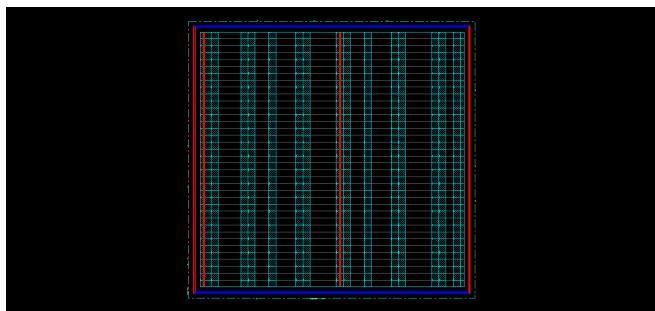


Fig 5.5: Floorplan view of RAM 511

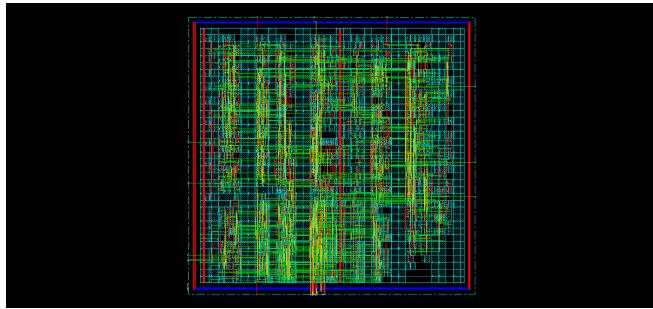


Fig 5.6: Cell Placement view of RAM 1k

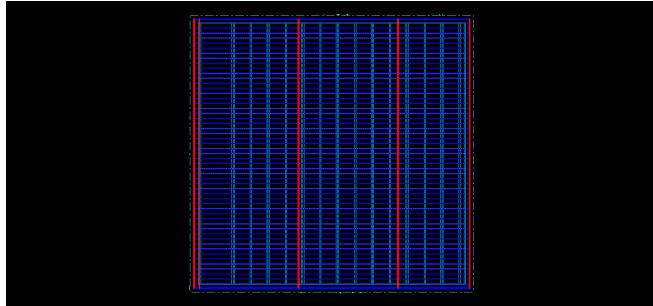


Fig 5.7: Floorplan view of RAM 1K

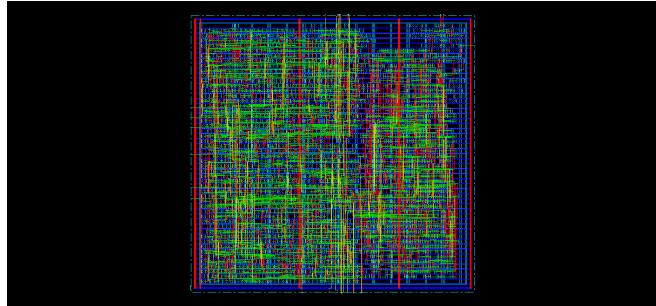


Fig 5.8: Cell Placement view of RAM 1k

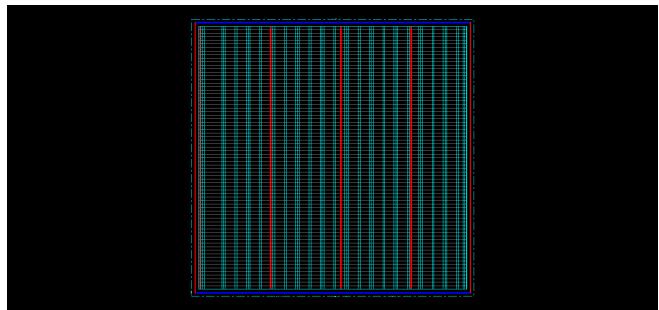


Fig 5.9: Floorplan view of RAM 2K

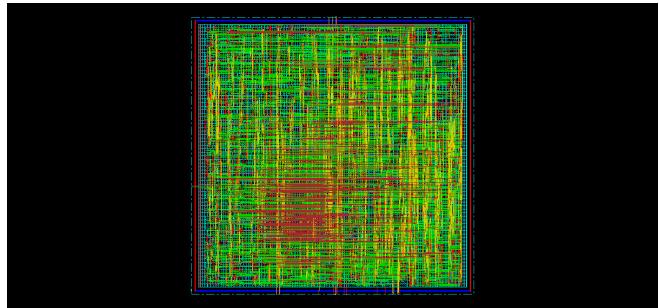


Fig 6.1: Cell Placement view of RAM 2k

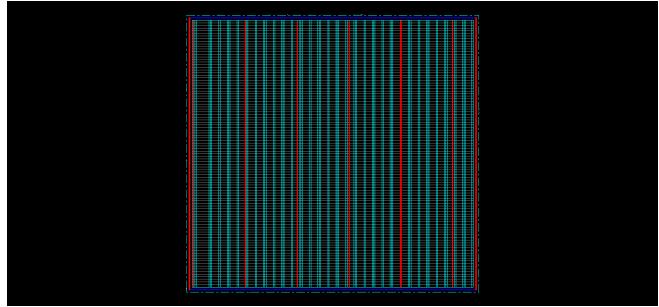


Fig 6.2: Floorplan view of RAM 4K

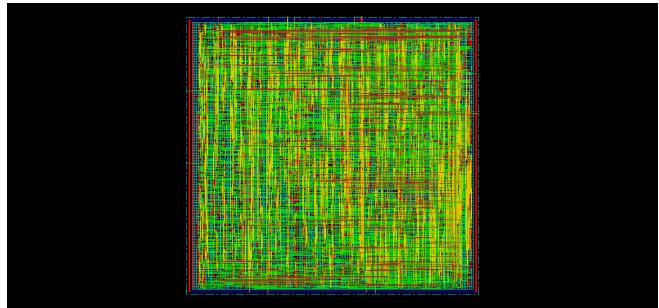


Fig 6.3: Cell Placement view of RAM 4K

VI CONCLUSION

The In conclusion, this project has successfully demonstrated the synthesis and physical implementation Random Access Memory (RAM) modules using Cadence design tools. Through a systematic approach encompassing architectural design, RTL coding, synthesis, place and route, and thorough verification, ROM modules were designed, synthesized, and physically

implemented according to the specified requirements. The design and implementation of the RAM memory is a challenging and valuable learning experience. This project will provide an opportunity to learn Cadence Virtuoso tools and also gain the knowledge and understand VLSI design. The static RAM is very widely used in CMOS systems. The project involved various stages, starting from the initial concept and requirements specification, through RTL (Register-Transfer Level) design, functional verification, synthesis, and ultimately to the generation of the final layout. Cadence's suite of tools played a vital role in facilitating these stages, providing a robust platform for designing and optimizing digital circuits. During the synthesis phase, the Cadence tools allowed for efficient mapping of the RTL description to a gate-level netlist, optimizing for factors such as area, power, and performances. Through comparative analysis, we evaluated the performance of both RAM and ROM modules, considering factors such as speed, area efficiency, and reliability. The results indicate that the design objectives were met, and the memory modules functioned effectively within the constraints of the project requirements. In summary, this project has enhanced our understanding of memory module design and the Cadence design flow. It has provided valuable insights into the synthesis and physical implementation of RAM and ROM modules, contributing to advancements in digital system design methodologies. Overall, this project signifies a significance milestone in the application of Cadence tools for memory module design and implementation.

vol. 66, no.6, pp. 1023-1027, June 2019, doi: 10.1109/TCSII.2018.2869945.

- [5] D. Shah, E. Hung, C. Wolf, S. Bazanski, D. Gisselquist and M. Milanovic, "Yosysnextpnr: An OpenSource Framework from Verilog to Bitstream for Commercial FPGAs," 2019 IEEE 27th Annual International Symposium on Field-Programmable CustomComputing MachineS (FCCM), 2019, pp. 1-4, doi: 10.1109/FCCM.2019.00010.
- [6] Shabana Aqueel and Kavita Khare, "Design and FPGA Implementation of DDR3SDRAM Controller for High Performance", International Journal of Computer.
- [7] Shekar C.P.;Kiran A.;Sougandha G.;Mamatha;Ramya N., "Design and Synthesizing of Floating Point Adder and Multiplier using Cadence RTL Compiler" 14th International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT 2023, 2023
- [8] Shekar C.P.;Dr. Basavaraj L., "Design of a Low Pass Filter for Wireless Applications" 14th International Conference on Advances in Computing, Control, and Telecommunication Technologies, ACT 2023, 2023

REFERENCES

- [1] Shylashree Nn, Yatish D Vahvale "Design and Implementation of 64-bit SRAM and CAM on Cadence and Open-source environment" in July 2021 International Journal of Circuits Systems and Signal Processing 15:586-594
- [2] Ravi Kumar. K. I, Vijayalaxmi. C. Kalal, Rajani. H. P, Dr. S. Y. Kulkarni "Design and verification of low power 64-bit SRAM system using 8T SRAM: Back-End approach" in International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2012
- [3] Siddalingesh S. Navalgund, Prakash R Tonse "Design and Development and Implementation of ALU, RAM and ROM for 8051 Microcontroller on FPGA using VHDL" in International Journal of Computer Applications (0975 – 8887) Volume 80 – No1, October 2013
- [4] N. Surana and J. Mekie, "Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs,

Synthesis and Physical Implementation of ROM Modules: A Comprehensive Study Using Cadence Design Tools

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Abstract - This project presents the synthesis and physical implementation of Read-Only Memory (ROM) modules using Cadence design tools. A versatile Electronic Design Automation (EDA) tool suite widely utilized in the semiconductor industry. Cadence software offers a comprehensive environment for designing and customizing memory components. In Cadence, the specification of the design is implemented using Hardware Description Languages (HDLs) such as VHDL or Verilog. The primary objective was to design, synthesize, and physically implement ROM modules, ensuring their functionality and performance meet the desired specifications. The process involved architectural design, RTL coding, synthesis, place and route, and thorough verification. Through this project, a comprehensive understanding of memory module design and the Cadence design flow was attained. The results demonstrate successful implementation of ROM modules, validating their correctness and functionality. This project contributes to advancing the knowledge and skills in digital design and memory system implementation using Cadence tools

I. INTRODUCTION

ROM stands for Read-Only Memory, a fundamental component of computer hardware and electronic devices. Unlike Random Access Memory (RAM), which allows for data to be read from and written to by the computer's processor, ROM is non-volatile memory. This means that the data stored in ROM remains intact even when the power is turned off. The synthesis of SRAM (Static Random Access Memory) and ROM (Read-Only Memory) using Cadence software typically involves a series of steps within the digital design flow. Cadence is a well-known provider of electronic design automation (EDA) tools, and its suite of software includes tools for digital design, verification, and implementation. Here's an overview of the synthesis process for SRAM and ROM using Cadence software.

SRAM and ROM Synthesis using Cadence:

1 Design Entry: Use a hardware description language (HDL) such as Verilog or VHDL to describe the SRAM circuit functionality.

2. RTL Synthesis: Utilize Cadence's RTL synthesis tools to convert the high-level description into a Register Transfer Level (RTL) netlist.
3. Optimization: Perform optimization to improve the design in terms of area, power, and timing using tools like Cadence Genus.
4. Technology Mapping: Map the synthesized RTL to the target technology library, considering the specific characteristics of the SRAM cells available in that library.
5. Place and Route: Use Cadence Innovus or Encounter tools for place and route to physically place the cells on the chip and create the detailed routing.
6. Timing Closure: Perform timing analysis and optimization to ensure that the design meets the required timing constraints.
7. Verification: Use Cadence simulation tools, such as Incisive, to verify the functionality and performance of the SRAM design.
8. Physical Verification: Perform physical verification checks to ensure that the layout adheres to manufacturing rules.
9. Extraction: Extract parasitic information from the layout for further accurate analysis.
10. Final Tape-out: Prepare the final set of files for manufacturing (GDSII files) to create the physical SRAM chip

II. DESIGN METHODOLOGY

Architectural Design: The first step involved defining the architecture of both RAM and ROM, specifying parameters such as size, address width.

- For RAM, the architecture included data input/output ports, address inputs, control signals, and memory cells. For ROM, the architecture comprised address inputs and data outputs.
- **RTL Coding:** Using Verilog HDL, the architecture was translated into Register Transfer Level (RTL) code. RTL code for RAM included modules for memory cells, input/output ports, and control logic code for ROM consisted of a module for address decoding and data output.

- **Synthesis:** The RTL code was synthesized using Cadence RTL Compiler to generate gate-level netlists. Synthesis optimizations were applied to improve the performance and area efficiency of the designs.
- **Place and Route:** The gate-level netlists were subjected to place and route using Cadence Encounter to map the logic onto physical hardware resources. Constraints such as timing, area, and power were considered during place and route to meet design specifications.

III. BLOCK DIAGRAM

The figure 1below represents the Read only Memory. ROM stands for read only memory, it is a memory device or storage medium that stores information permanently. It is a non-volatile memory, It is also the primary memory unit of a computer along with the Random access memory.

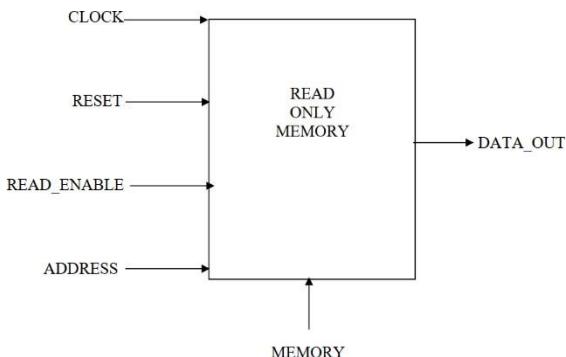


Fig 1: READ ONLY MEMORY

The figure above represents the Read only memory, which consist of clock, reset, read enable, address and memory as the input data and a data out which provides the output. The memory is defined as the Register. The circuit works under positive clock edge. If reset signal is high no data is obtained in data output signal. When read enable is high the read operations takes place. ROM is also used to store Firmware, which is a software program which remains attached to the hardware or programmed on a hardware device like a keyboard, hard drive, video cards, etc. It is stored in the flash ROM of a hardware device. It provides instructions to the device to communicate and interact with other device.

IV. SOFTWARE SPECIFICATIONS

The synthesis and physical implementation of ROM using Cadence typically require a suite of software tools that facilitate various stages of the design flow. Below are the essential software requirements for this process:

Cadence Design Tools: Cadence provides a range of tools for digital design, synthesis, place and route, and verification. The specific tools needed include:

- **RTL COMPILER:** RTL Compiler will execute the instructions in the TCL file and will generate the output files and reports in the “out” folder. The generated files: “. v”: Which has the new gate level Verilog description of the synthesized system.

- **Encounter:** Cadence Encounter is a place-and-route tool that uses a Verilog netlist and generates its equivalent layout view. This tutorial describes how to use Cadence SOC Encounter to generate a layout view of the synthesized design, using standard cells library.
- **Library Files:** Standard cell libraries and technology files specific to the target process technology. These files provide essential information for synthesis and physical implementation, such as cell timing, power, and physical characteristics.

V RESULTS

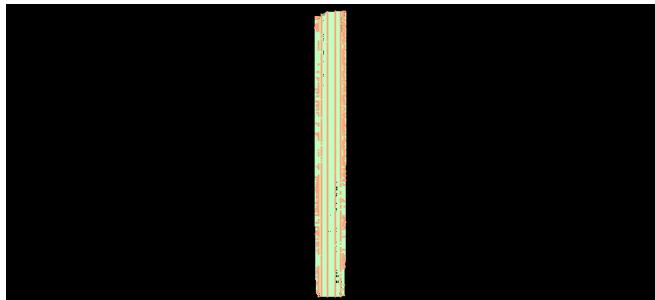


Fig 5.1 : Synthesized image of ROM memory address 511

The above figure 5.1 represents the synthesis of rom of memory 29 consists of 6493 number of cells ,with 8 number of sequential circuits , 1098 inverter, 46 buffer and 5341 logic gates. These instances consumes leakage power of 3.428 nw with 783463 nw of dynamic power . The net area is 26 with slack time of 128ps.

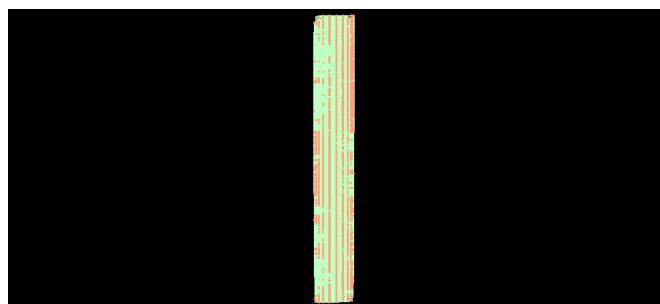


Fig 5.2 : Synthesized image of ROM memory address 1K

The figure 5.2 above represents the synthesis of rom of memory 210 consists of 12370 number of cells , with 8 number of sequential circuits , 1684 inverter, 158 buffer and 10520 logic gates. These instances consumes leakage power of 5.393 nw with 783463 nw of dynamicpower . The net area is 51 with slack time of 309ps.

The below figure 5.3 represents the synthesis of rom of memory 212 consists of 6493 number of cells , with 8 number of sequential circuits , 5494 inverter, 436 buffer and 21533 logic gates. These instances consumes leakage power of 272nw with 9380267.182 nw of dynamic power. The net area is 107 with slack time of 366 ps.

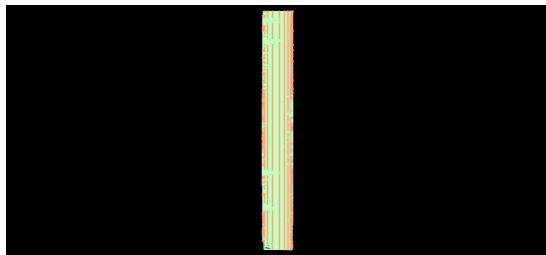


Fig 5.3: Synthesized image of ROM memory address 2K

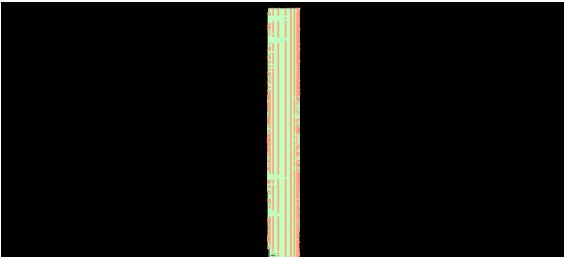


Fig 5.4: Synthesized image of ROM memory address 4K

The figure 5.4 above represents the synthesis of rom of memory 214 consists of 6493 number of cells , with 8 number of sequential circuits , 9649 inverter, 626 buffer and 45320 logic gates. These instances consumes leakage power of 80.191 nw with 5778829 nw of dynamic power. The net area is 216 with slack time of 511 ps. Below table 1 and 2 clear shows the summary report of ROM design and figure 5.5 – 6.3 shows the floorplan and cell placement view of various ROM memory sizes.

Table 1: SUMMARY REPORT OF ROM DESIGN

| MEMORY SIZE | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|-----------------|--|---------------------------|-----------------------------|------------------------------|
| CELLS | 6493 | 12370 | 27471 | 55603 |
| INSTANCE | SEQUENTIAL INVERTER BUFFER LOGIC | 8 1098 46 5341 | 8 1684 158 10520 | 8 5494 436 21533 |
| POWER | LEAKAGE (nw) DYNAMIC (nw) TOTAL (nw) | 3.428 783463 783469 | 5.393 1381633 1381639 | 12.237 3028347 3028359 |
| SLACK TIME (ps) | 128 | 309 | 366 | 511 |
| NET AREA | 26 | 51 | 107 | 216 |

Table 2: SUMMARY ON PHYSICAL IMPLEMENTATION

| MEMORY SIZE | 2^9 | 2^{10} | 2^{12} | 2^{14} |
|-------------|--|--|--|--|
| AREA | METAL1 METAL2 | 383.5216 945.8680 | 502.0048 1992.3904 | 735.4864 4032.3976 |
| POWER | STD.CELL(μm^2) CORE(μm^2) CHIP (μm^2) | 130374.922 186251.184 200756.032 | 224811.418 321160.896 340122.666 | 485880.595 694115.730 721864.240 |
| | 1086.8704 2664.5080 1532720.680 | | | |

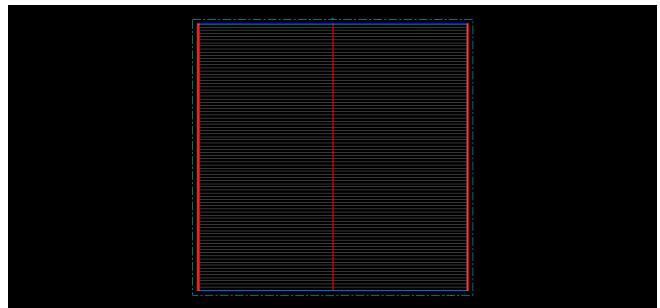


Fig 5.5: Floorplan view of ROM 511

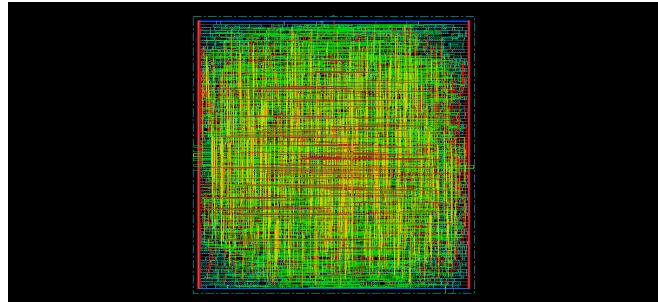


Fig 5.6: Cell Placement view of ROM 1k

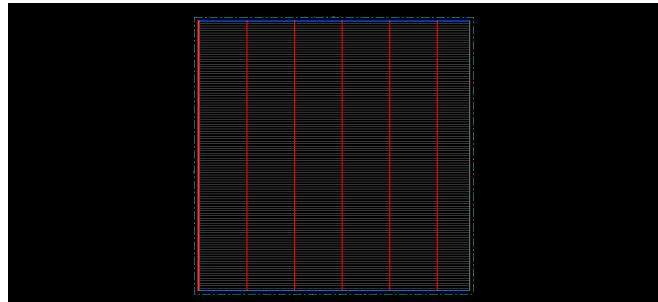


Fig 5.7: Floorplan view of ROM 1K

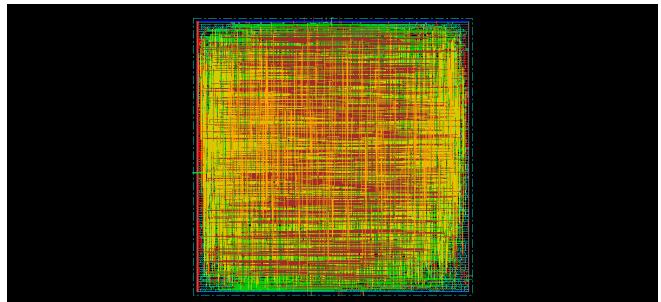


Fig 5.8: Cell Placement view of ROM 1k

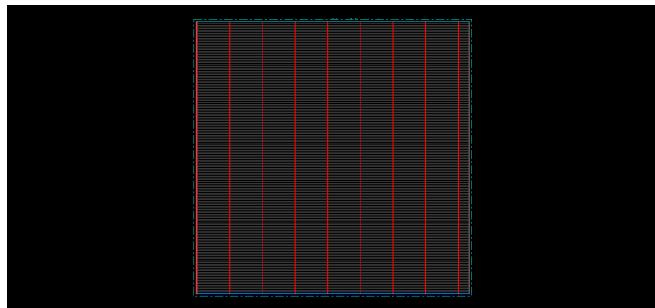


Fig 5.9: Floorplan view of ROM 2K

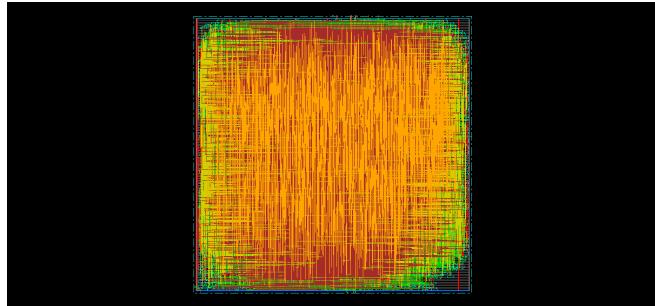


Fig 6.1: Cell Placement view of ROM 2k

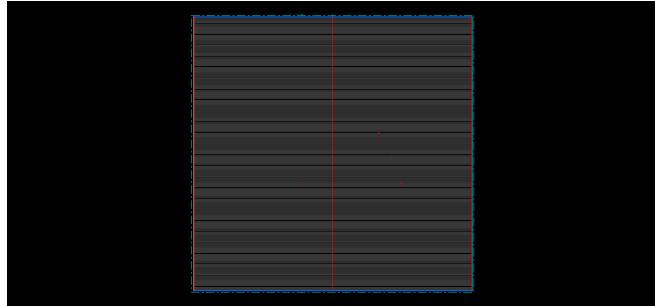


Fig 6.2: Floorplan view of ROM 4K

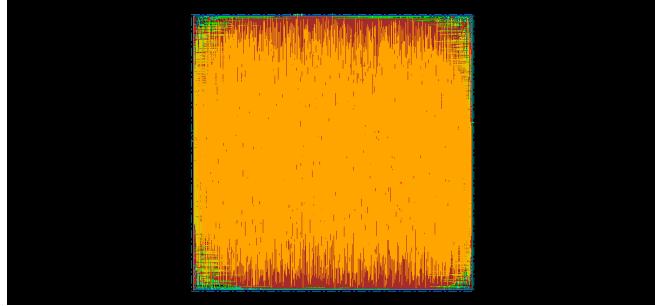


Fig 6.3: Cell Placement view of ROM 4K

CONCLUSION

This work has successfully demonstrated the synthesis and physical implementation Read-Only Memory (ROM) modules using Cadence design tools. Through a systematic approach encompassing architectural design, RTL coding, synthesis, place and route, and thorough verification, ROM modules were designed, synthesized, and physically implemented according to the specified requirements. The design and implementation of the ROM memory is a challenging and valuable learning

experience. This project will provide an opportunity to learn Cadence Virtuoso tools and also gain the knowledge and understand VLSI design. The static RAM is very widely used in CMOS systems. The project involved various stages, starting from the initial concept and requirements specification, through RTL(Register-Transfer Level) design, functional verification, synthesis, and ultimately to the generation of the final layout. Cadence's suite of tools played a vital role in facilitating these stages, providing a robust platform for designing and optimizing digital circuits. During the synthesis phase, the Cadence tools allowed for efficient mapping of the RTL description to a gate-level netlist, optimizing for factors such as area, power, and performances. Through comparative analysis, we evaluated the performance of both RAM and ROM modules, considering factors such as speed, area efficiency, and reliability. The results indicate that the design objectives were met, and the memory modules functioned effectively within the constraints of the project requirements. In summary, this project has enhanced our understanding of memory module design and the Cadence design flow. It has provided valuable insights into the synthesis and physical implementation of RAM and ROM modules, contributing to advancements in digital system design methodologies. Overall, this project signifies a significance milestone in the application of Cadence tools for memory module design and implementation.

REFERENCES

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- [2] Ravi Kumar. K. I, Vijayalaxmi. C. Kalal, Rajani. H. P, Dr. S. Y. Kulkarni "Design and verification of low power 64-bit SRAM system using 8T SRAM: Back-End approach" in International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2012
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- [4] N. Surana and J. Mekie, "Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no.6, pp. 1023-1027, June 2019, doi: 10.1109/TCSII.2018.2869945.
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- [6] Shabana Aqueel and Kavita Khare, "Design and FPGA Implementation of DDR3SDRAM Controller for High Performance", International Journal of Computer.