PHYSICAL IMPLEMENTATION AND SYNTHESIS OF RAM AND ROM MODULES USING CADENCE:-

The synthesis of SRAM (Static Random Access Memory) and ROM (Read-Only Memory) using Cadence software typically involves a series of steps within the digital design flow. Cadence is a well-known provider of electronic design automation (EDA) tools, and its suite of software includes tools for digital design, verification, and implementation. Here's an overview of the synthesis process for SRAM and ROM using Cadence software.

SRAM and ROM Synthesis using Cadence:

1 Design Entry: Use a hardware description language (HDL) such as Verilog or VHDL to describe the SRAM circuit functionality.

2. RTL Synthesis: Utilize Cadence's RTL synthesis tools to convert the high-level description into a Register Transfer Level (RTL) netlist.

3. Optimization: Perform optimization to improve the design in terms of area, power, and timing using tools like Cadence Genus.

4. Technology Mapping: Map the synthesized RTL to the target technology library, considering the specific characteristics of the SRAM cells available in that library.

5. Place and Route: Use Cadence Innovus or Encounter tools for place and route to physically place the cells on the chip and create the detailed routing.

6. Timing Closure: Perform timing analysis and optimization to ensure that the design meets the required timing constraints.

7. Verification: Use Cadence simulation tools, such as Incisive, to verify the functionality and performance of the SRAM design.

8. Physical Verification: Perform physical verification checks to ensure that the layout adheres to manufacturing rules.

9. Extraction: Extract parasitic information from the layout for further accurate analysis.

10. Final Tape-out: Prepare the final set of files for manufacturing (GDSII files) to create the physical SRAM chip.

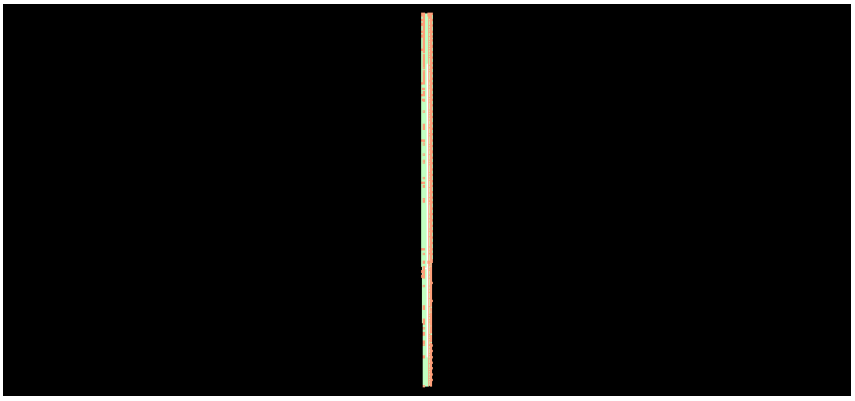
TOOLS USED:

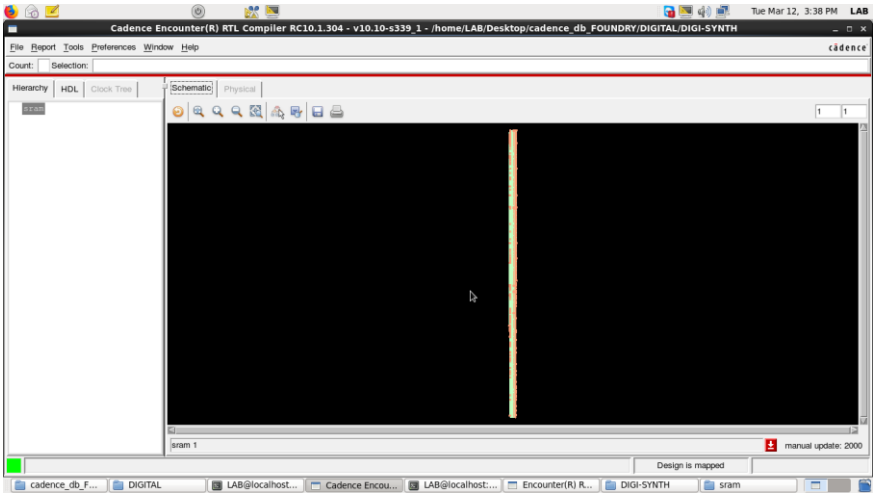
- Cadence RTL Compiler
- Encounter
- Verilog HDL

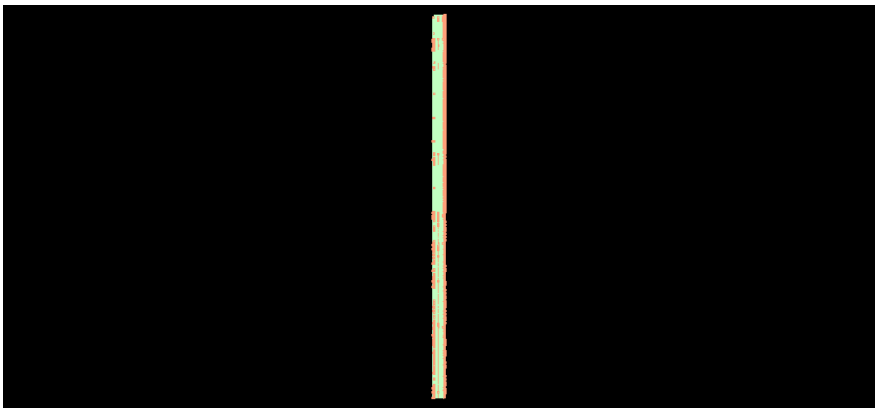
FEATURES:

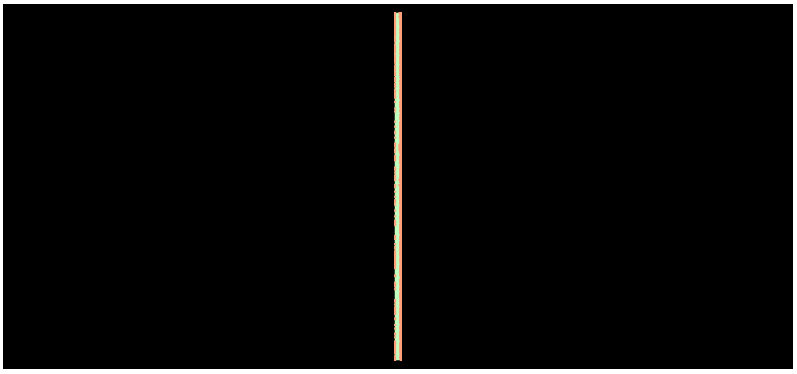
- Ram and Rom Functional and structural design.
- Synthesis and physical implementation
- Timing and area reports.

1.LAYOUTS OF SRAM WITH MEMORY OF 511, 1K,2K,4K

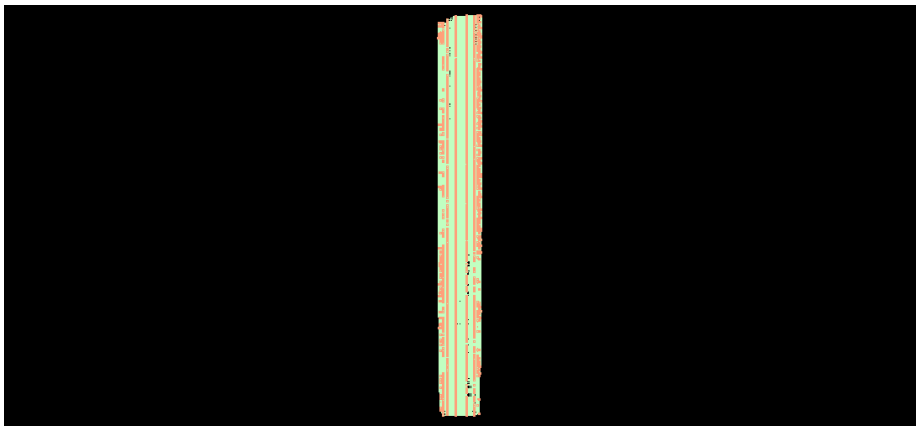


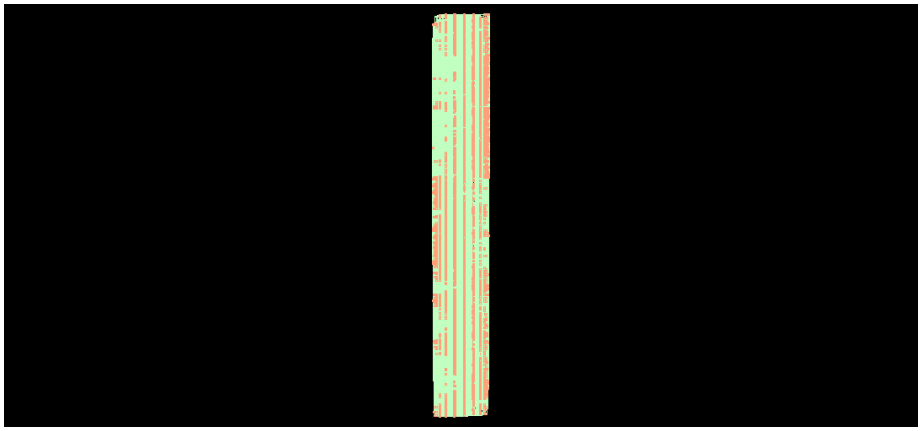


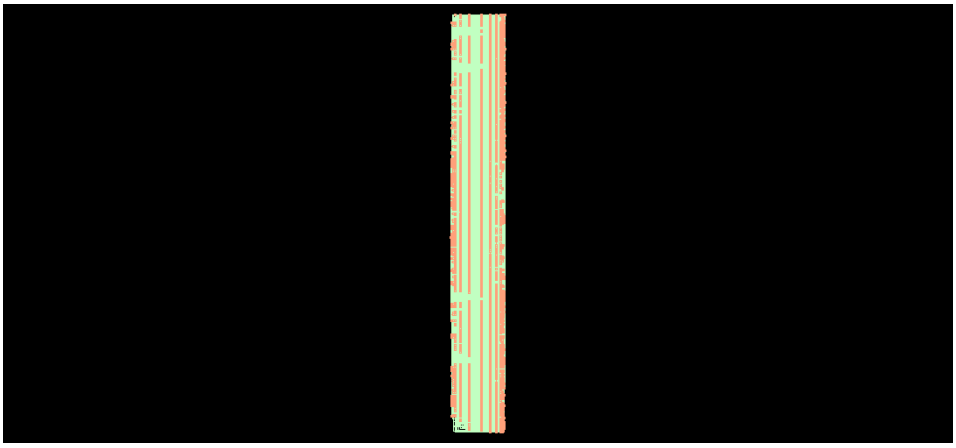




2.LAYOUT OF ROM USING THE MEMORY 511, 1K, 2K:







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