University of Oulu
521404A Digital Techniques 2
Project Report

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Version history

Version	Date	Author	Comment
1.0	16.8.2023	JL	Document template created.
	13.09.2023	Kavinda Rathnayaka	Project Started
	21.09.2023	Kavinda Rathnayaka	Module-hierarchy done
	22.09.2023	Kavinda Rathnayaka	Mux_2x16 done
	27.09.2023	Kavinda Rathnayaka	Mux_3x16 done
	01.10.2023	Kavinda Rathnayaka	Function Unit done
	15.10.2023	Kavinda Rathnayaka	Instruction Register done
	22.11.2023	Kavinda Rathnayaka	Program Counter done
	04.11.2023	Kavinda Rathnayaka	Register Bank done
	05.11.2023	Kavinda Rathnayaka	Control Unit done
	05.11.2023	Kavinda Rathnayaka	Mycpu done
	06.11.2023	Kavinda Rathnayaka	Project Report done

1 Introduction

The primary objective of this project revolves around the development of a 16-bit instruction set processor. *(see Figure 1)*

This design comprises the following key components:

1. Program Counter (PC) - Responsible for tracking the program's execution.
2. Instruction Register (IR) - Stores the current instruction being processed.
3. Control Unit (CU) - Manages and coordinates the processor's operations.
4. Register Bank (RB) - Houses registers for data storage and manipulation.
5. Function Unit (FU) - Handles various computational functions.
6. 2x16 Multiplexer (MUXM) - Used for data selection and routing.
7. 3x16 Multiplexer (MUXD) - Enables versatile data selection and control.
8. 2x16 Multiplexer (MUXB) - Facilitates flexible data routing.

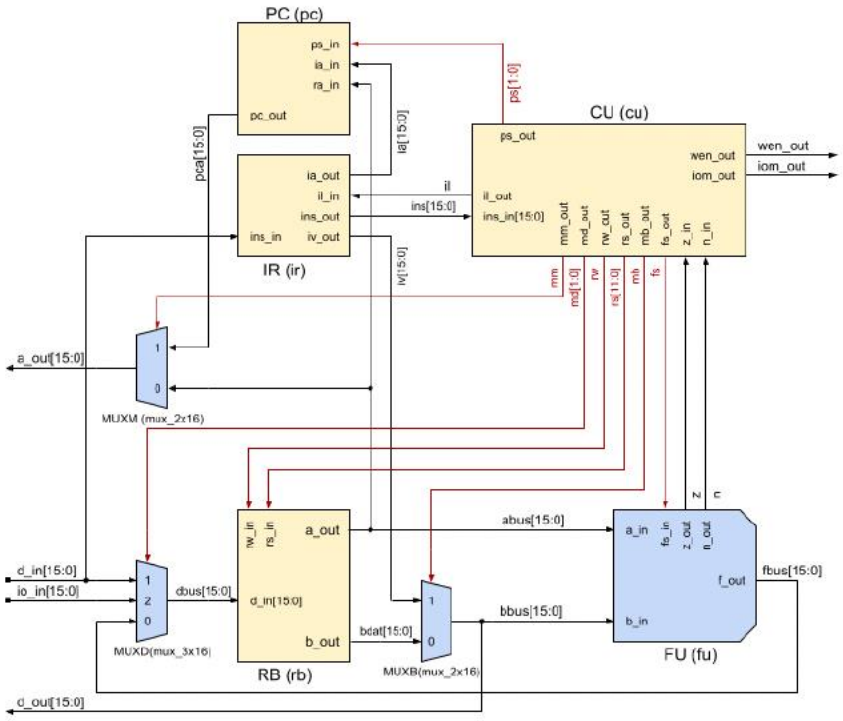


Figure 1: Processor Core Design

The architectural design of this processor core incorporates a SystemVerilog model created at the register level, which underwent synthesis using the QuestaSim Integrated Development Environment (IDE) from Siemens. To verify the functionality of each RTL (Register-Transfer Level) model, manual testbenches and test programs were written. The generated waveforms within the IDE were utilized to validate the functionality of individual RTL modules and the overall design.

Moreover, gate-level validation was utilized for specific tasks to ensure the precision of the simulation outcomes derived from RTL synthesis. Subsequently, the connectivity and potential errors within the RTL model were examined via a formality report generated by the Qautocheck wizard. At this point, an analysis of the design's cost and performance is conducted using the Synopsys Design Vision tool. The main focus of this analysis is to observe the design area, resource utilization, power consumption, and timing in order to develop an optimized version of the processor.

To Implement the XXL instruction I have used *R0 = R0 + (R1*R2)* and the CLK_PERIOD 10ns is used.

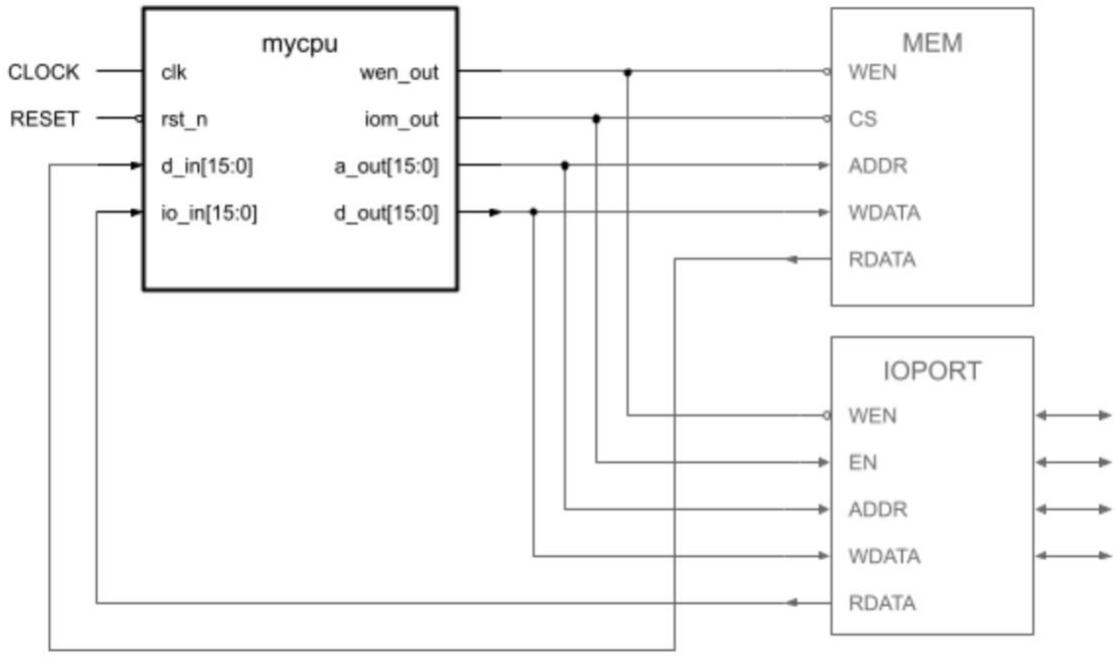


Figure 2: Overview of the Interface of the CPU core

The interface signals are:

- clk, rising edge sensitive clock signal input
- rst_n, active-low asynchronous reset input
- a_out, memory address bus
- d_out, memory data write bus
- d_in memory data read bus
- io_in, parallel input-output device (IOPORT) read bus
- iom_out, select the signal that indicates the address and write data meant for the memory or I/O devic

2. Design of the control part of the mycpu CPU

2.1. Instruction decoder implementation

The instruction decoder (CU) plays a vital role in overseeing and coordinating the retrieval and execution of instructions. In this design, the decoder is implemented as an Algorithmic State Machine, responsible for decoding control signals for both the instruction register (IR) and the program counter (PC). The instruction decoder is modeled using one sequential and one combinational process.

Primarily Instructions INF and EX0 were used to fetch and execute the instructions. Pre-defined state table was used to develop the algorithmic states within the control unit. For branch instructions zero and the negative flags were tested. Subsequentially, for the XXL instruction implementation, more than one step was implemented in the design.

2.2. Implementation of the XXL special instruction

The task is to implement a new instruction, XL1. To test the functionality, the 'xxltest.asm' code is used as random data for the registers. I have been assigned to construct the following arithmetic operation.

R0 = R0 + (R1*R2)

In this design, only one instruction can execute at a time, as the Instruction decoder uses an Arithmetic state machine and will execute only one instruction per clock cycle. Therefore, I've divided the manipulation into two stages: XXL and XL1.

I first performed the multiplication as denoted below when the XXL instruction state was loaded.

XXL:

```
begin
  ns = XL1;
  fs_out = 4'b0011;
  rs_out = {4'b1000, 4'b0001, 4'b0010};
  rw_out = 1;
  ps_out = 1;
  wen_out = 1;
end
```

In this code, R1 (0001) and R2(0010) multiply the values and store those values in the R8(1000) register in the register bank.

Then in the next clock cycle XXL's Next state XL1 will be executed.

XL1:

```
begin
  ns = INF;
  fs_out = 4'b0010;
  rs_out = {4'b0000, 4'b0000, 4'b1000};
  rw_out = 1;
  ps_out = 1;
  wen_out = 1;
end.
```

above code performs the addition part with the R8 register and saves the value in the same register R0. Once this is executed instruction decoder jumps to the next state INF.

Figure 2. ASM diagram for the XXL instruction.

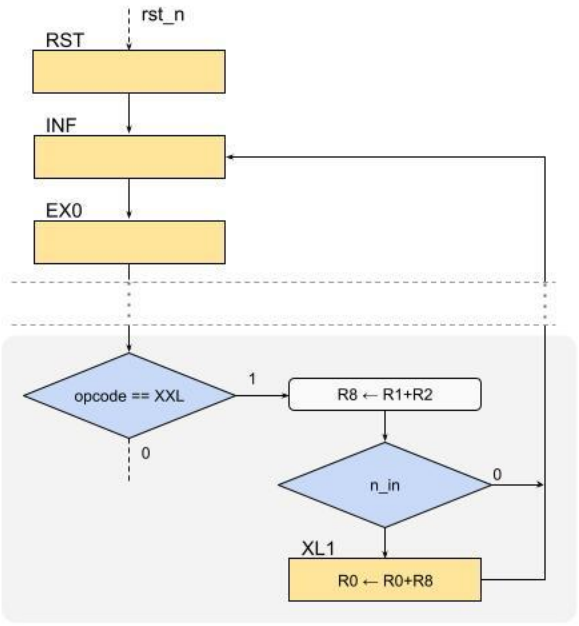


Figure 3: XXL Instruction ASM Chart

Table 1. State Table of XXL Instruction

INPUTS					OUTPUTS										
s_r	opcode	NO	z_in	n_in	ns	ps_out	it_out	rw_out	rs_out	mm_out	md_out	mb_out	fs_out	wen_out	iom_out
EX0	1111110	XXL	X	X	XL1	1	0	1	1000_0001_0010	0	0	0	0011	1	0
XL1	1111111	XXL	X	X	INF	1	0	1	0000_0000_1000	0	0	0	0010	1	0

3. mycpu verification

3.1. RTL code check results

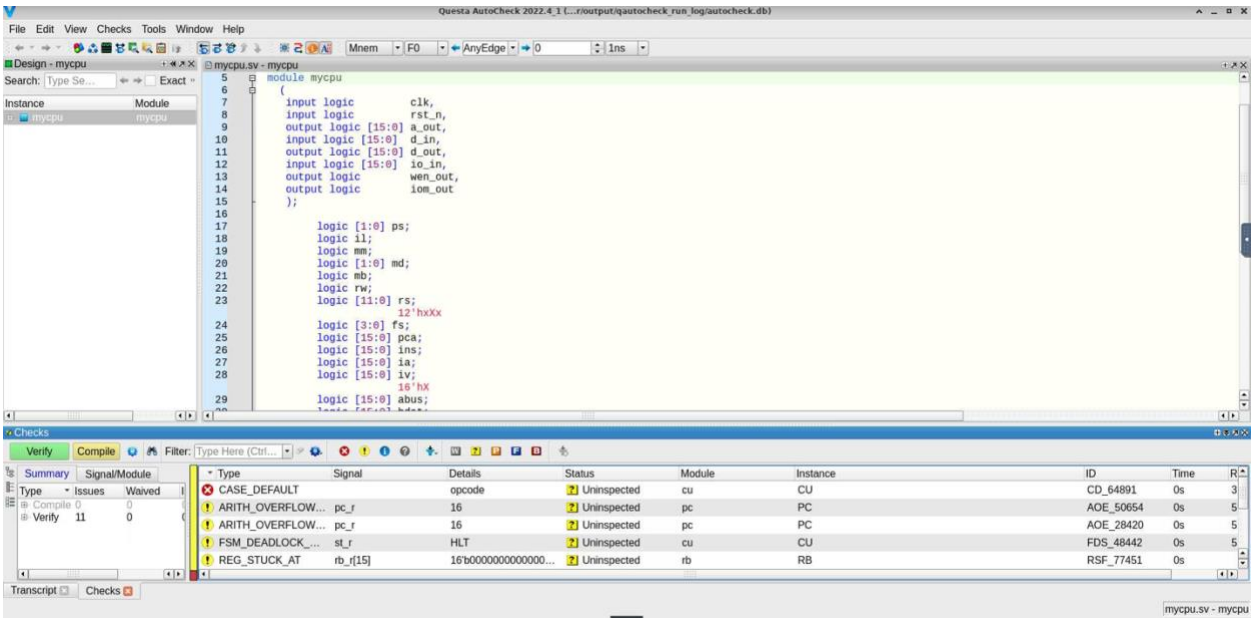


Figure 4: Questa Autocheck test report

- CASE_DEFAULT: In the control unit's "case_default" block, "ns=HLTl" causes this error. The reason for this error is that 'ns' is a logic variable and can have 'X' or 'Z' states as well. Since it is not defined for all states, it causes this kind of error.

- ARITHMETIC_OVERFLOW: This often happens with arithmetic operations when dealing with signed numbers. In this design, overflow handling is not implemented.

- FSM_DEADLOCK: The HLT instruction causes this warning. When the instruction decoder fails to fetch instructions due to a bug in PC or RB RTL models, or when there is nothing to execute.

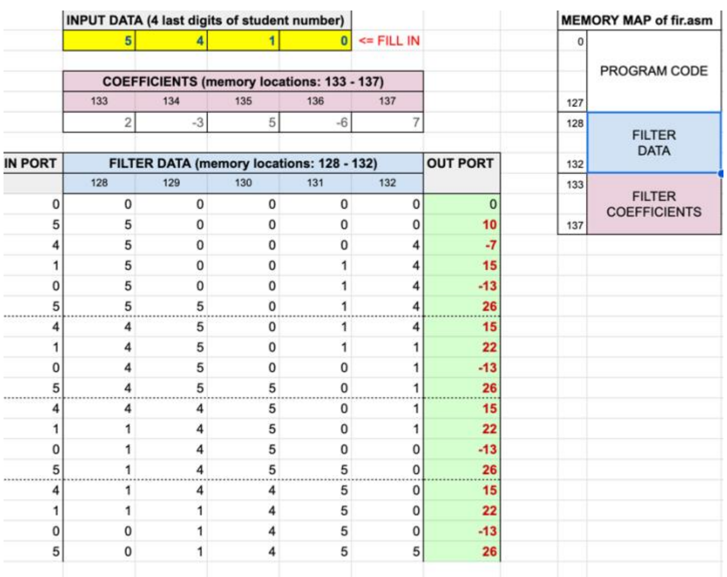
3.2. The results of the functional verification

I evaluated the following cases by decoding two .ASM files (fir.asm & xxltest.asm). The decoded data was then input into the register bank 'rb' to test the functionality of the design. After the simulation, it was verified the design simulation data against the reference data.

3.2.1. fir.asm Simulation

According to the simulation results, we can conclude that the design has worked. This also can be verified by comparing the gate-level- modal against the RTL code.

Reference page data	Simulation result

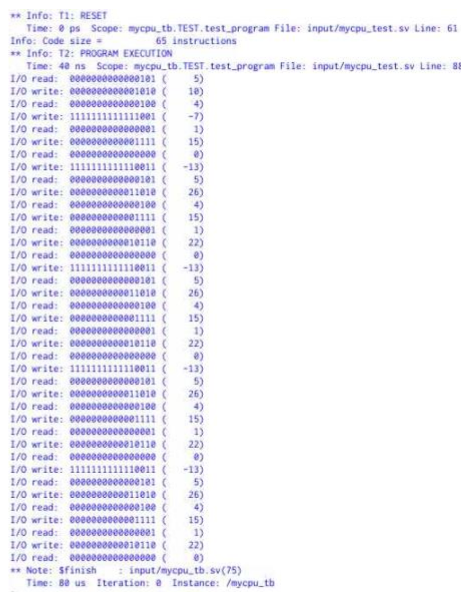


INPUT DATA (4 last digits of student number)				
5	4	1	0	<= FILL IN

COEFFICIENTS (memory locations: 133 - 137)				
133	134	135	136	137
2	-3	5	-6	7

IN PORT	FILTER DATA (memory locations: 128 - 132)					OUT PORT
	128	129	130	131	132	
0	0	0	0	0	0	0
5	5	0	0	0	0	10
4	5	0	0	0	4	-7
1	5	0	0	1	4	15
0	5	0	0	1	4	-13
5	5	5	0	1	4	26
4	4	5	0	1	4	15
1	4	5	0	1	1	22
0	4	5	0	0	1	-13
5	4	5	5	0	1	26
4	4	4	5	0	1	15
1	1	4	5	0	1	22
0	1	4	5	0	0	-13
5	1	4	5	5	0	26
4	1	4	4	5	0	15
1	1	1	4	5	0	22
0	0	1	4	5	0	-13
5	0	1	4	5	5	26

MEMORY MAP of fir.asm	
0 – 127	PROGRAM CODE
128 – 132	FILTER DATA
133 – 137	FILTER COEFFICIENTS



```
** Info: T1: RESET
   Time: 0 ps  Scope: mycpu_tb.TEST.test_program File: input/mycpu_test.sv Line: 61
Info: Code size =          65 instructions
** Info: T2: PROGRAM EXECUTION
   Time: 40 ns  Scope: mycpu_tb.TEST.test_program File: input/mycpu_test.sv Line: 88
I/O read:  0000000000000101 (     5)
I/O write: 0000000000001010 (    10)
I/O read:  0000000000000100 (     4)
I/O write: 1111111111111001 (    -7)
I/O read:  0000000000000001 (     1)
I/O write: 0000000000001111 (    15)
I/O read:  0000000000000000 (     0)
I/O write: 1111111111110011 (   -13)
I/O read:  0000000000000101 (     5)
I/O write: 0000000000011010 (    26)
I/O read:  0000000000000100 (     4)
I/O write: 0000000000001111 (    15)
I/O read:  0000000000000001 (     1)
I/O write: 0000000000010110 (    22)
I/O read:  0000000000000000 (     0)
I/O write: 1111111111110011 (   -13)
I/O read:  0000000000000101 (     5)
I/O write: 0000000000011010 (    26)
I/O read:  0000000000000100 (     4)
I/O write: 0000000000001111 (    15)
I/O read:  0000000000000001 (     1)
I/O write: 0000000000010110 (    22)
I/O read:  0000000000000000 (     0)
I/O write: 1111111111110011 (   -13)
I/O read:  0000000000000101 (     5)
I/O write: 0000000000011010 (    26)
I/O read:  0000000000000100 (     4)
I/O write: 0000000000001111 (    15)
I/O read:  0000000000000001 (     1)
I/O write: 0000000000010110 (    22)
I/O read:  0000000000000000 (     0)
I/O write: 1111111111110011 (   -13)
I/O read:  0000000000000101 (     5)
I/O write: 0000000000011010 (    26)
I/O read:  0000000000000100 (     4)
I/O write: 0000000000001111 (    15)
I/O read:  0000000000000001 (     1)
I/O write: 0000000000010110 (    22)
I/O read:  0000000000000000 (     0)
** Note: $finish    : input/mycpu_tb.sv(75)
   Time: 80 us  Iteration: 0  Instance: /mycpu_tb
```

Figure 5: Reference Data vs Simulation Results

3.2.2. xxl_test.asm Simulation

Implemented Instruction: R0 <= R0+(R1*R2)

During the first clock cycle, the instruction decoder fetches the instruction XXL. It first performs the R1 * R2 (2 * 3) multiplication and stores the result temporarily in location R8 (result: 6). When the XL1 state occurs, the stored value is then added to R0 (which is equal to 1), and the result is stored back in the same location, making it 7 in this case.

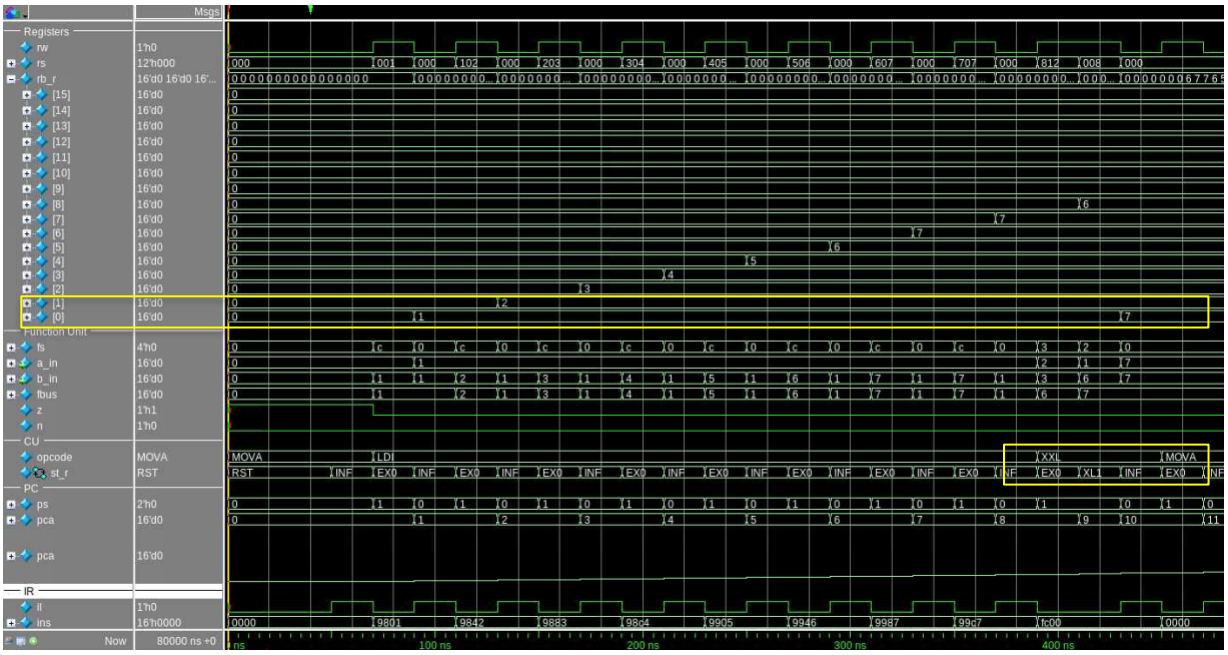


Figure 6: XXL Instruction Simulation Results

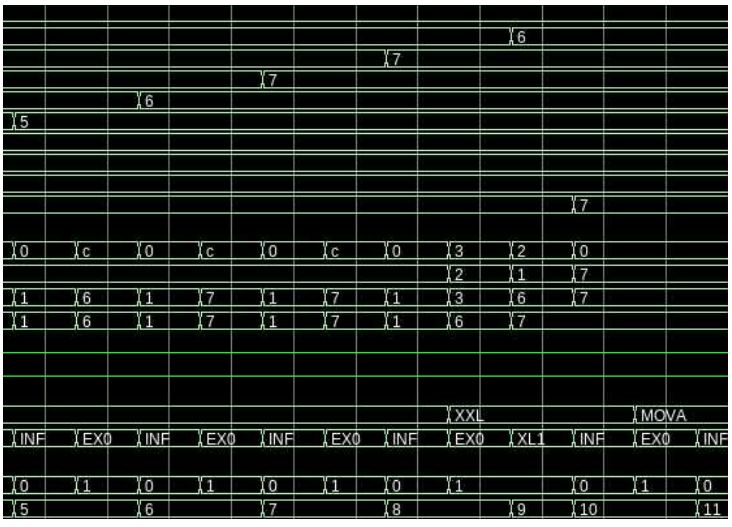


Figure 7: XXL and XL1 zoom in for clarity

4. Implementation of the mycpu design

After completing the synthesis, I conducted cost and performance optimizations. I used the Design Vision tool to analyze the power, area, and timing constraints of the design.

- POWER: Our focus was on achieving power efficiency. Design Vision generated a detailed report analyzing the expected power consumption of the RTL design.

- TIMING: Analyzing timing constraints is crucial for the data path. To ensure successful data transmission, the slack should be either 0 or slightly positive. If the initial design slack is negative, it indicates that the assigned CLOCK PERIOD was too short for the design.

- AREA: The design aimed to utilize minimal resources. The generated report provides comprehensive information about the area used.

4.1. Area results

According to the reports, there is significant difference in the data. When optimize the usage of resources gets increased. we can achieve performance optimization by adjusting the CLOCK_PERIOD to 8ns. A shorter clock period is more likely to bring the slack value closer to zero. This adjustment reduced the total cell area used in the design, but the number of flip-flops remains the same as it has no impact on the performance.

Table 3.

Feature	Cost optimized	Performance optimized
Total Cell Area	5166.747518	5420.637373
NAND2 Equivalent Area (Total Cell Area / 0.798)	6474.620	6870.262
Combinational Area	3885.861735	4139.751591
Sequential Area	1280.885782	1280.885782
Number of Flip-Flops	180	180

4.2. Timing results

CLOCK_PERIOD defined for the design was 10ns. For this setting data arrival path from the data given 9.70 data arrival delay for the critical path. Slack for the data path is slightly negative and can be improved. After setting CLOCK PERIOD to 8ns, data arrival time is reduced to 7.93 and slack is zero.

Table 4. Timing results

Feature	Cost optimized	Performance optimized
Clock Period (ns)	10	8
Critical Path Delay (ns)	data arrival time : 9.70	data arrival time : 7.93
Critical Path Slack (ns)	0.22832	0.00072
Critical path route (start- and end-point)	Startpoint:IR_ir_r_reg_15_ Endpoint:PC_pc_r_reg_15_	Startpoint:IR_ir_r_reg_11_ Endpoint:PC_pc_r_reg_9_

4.3. Power results

In many cases, when attempting to optimize design performance, power consumption tends to increase compared to the basic design settings. More power is utilized to enhance overall performance. However, in the current scenario, the total power consumption is reduced after optimization.

Table 5. Efficacy results

Feature	Cost optimized	Performance optimized
Total Power Consumption (mW)	117.5549 uW	86.4587 uW

4.4. Gate-level verification results

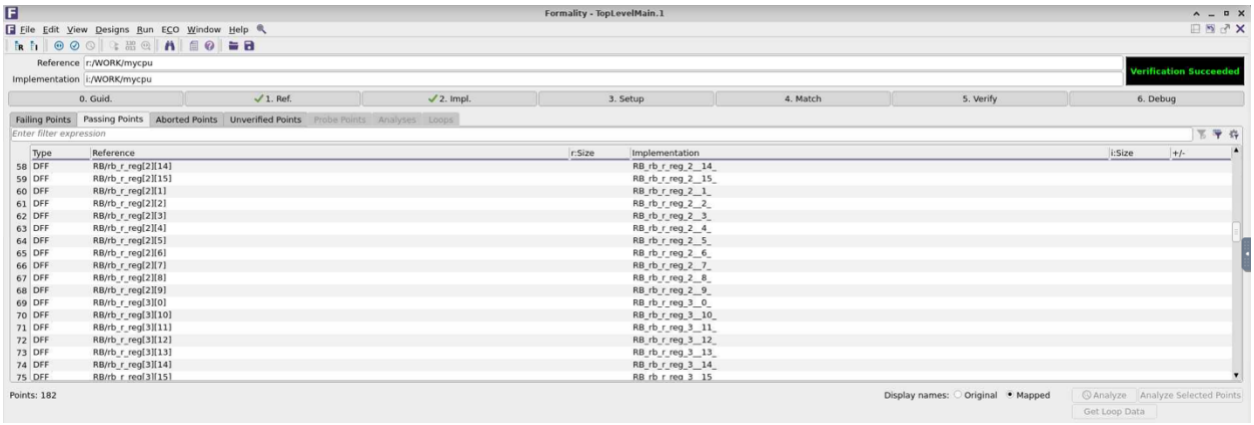


Figure 8: Formality Report

5. Discussion

The implementation of the design began with the identification of the components in the 16-bit CPU architecture. Each component was then modeled using System Verilog. To verify the functionality of each RTL design, test benches, and test programs were manually written. At the end of the design process, all components were instantiated in the main module 'mycpu.' Subsequently, a complete synthesis was performed to understand the design's functionality.

The design's functionality was analyzed using wave diagrams generated from the QuestaSim IDE. If the results were inaccurate, a sanity check was conducted to identify issues within each RTL module. Even after synthesis, certain errors such as 'case_default' violations and arithmetic overflow may remain hidden in the design. To detect such issues, the same RTL design was analyzed using Questa AutoCheck IDE and QLint for debugging. Once all tests passed successfully, design performance reports and cost optimization factors were obtained from the Design Vision IDE. The IDE also allowed the designer to identify slack time in the critical path. If the slack time was set to zero, an optimized version of the CPU was implemented.

Throughout this project, I gained experience in modeling digital circuits using system Verilog and verifying them with various high-end synthesis EDA tools like QuestaSim, Questa AutoCheck, QLint, and Design Vision.

In summary, this course provided practical training for designing digital circuits, closely resembling industry practices.

Attachments

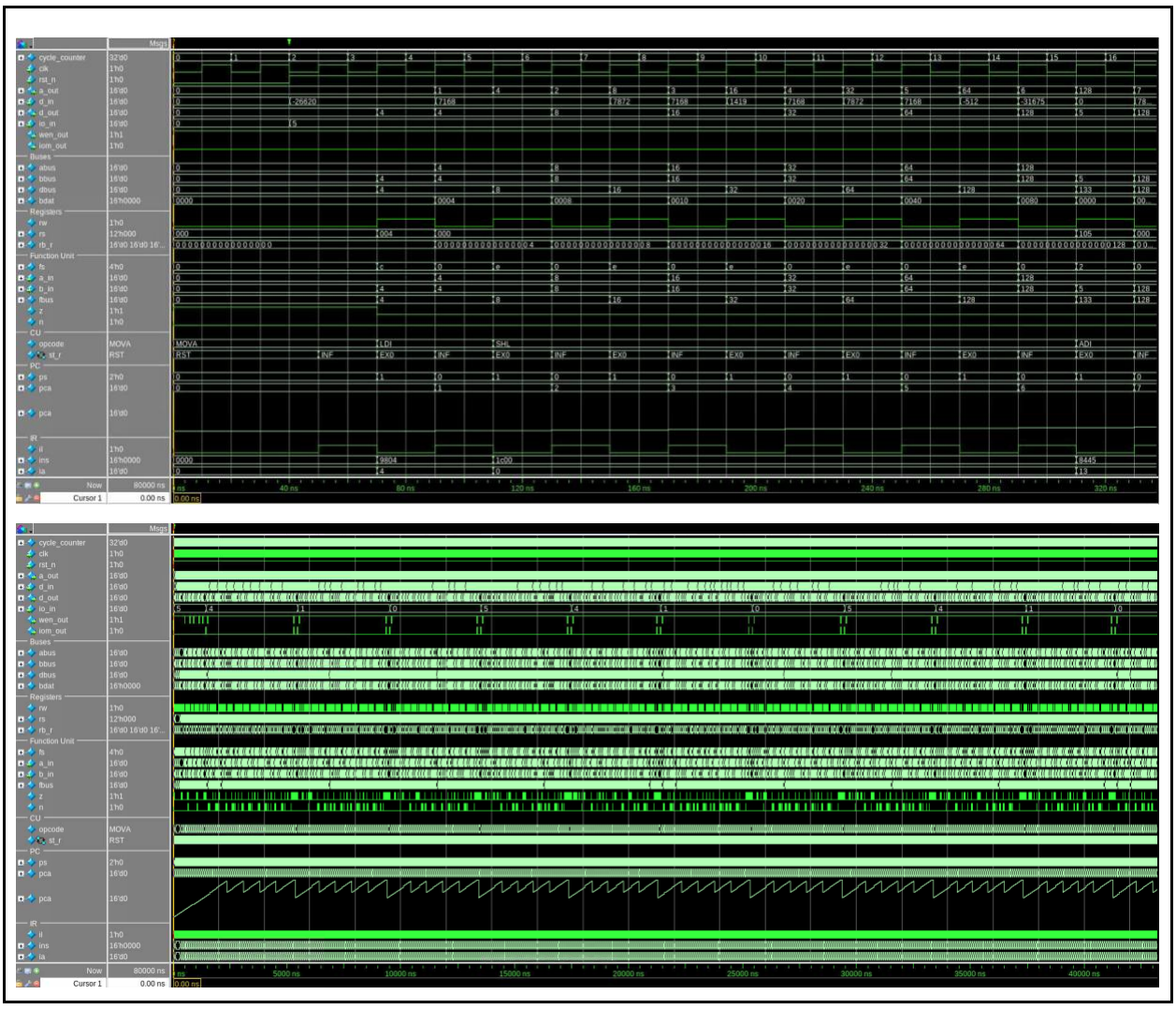
A1. Questa Autocheck Summary Report

(reports/mycpu.rtl.qautocheck_report.txt, AutoCheck Verify Summary section only)

AutoCheck Verify Summary

Check	Evaluations	Found	Waived
ARITH_OVERFLOW_SUB	0	0	0
ARITH_OVERFLOW_VAL	7	2	0
ARITH_ZERO_DIV	0	0	0
ARITH_ZERO_MOD	0	0	0
BLOCK_UNREACHABLE	72	0	0
BUS_MULTIPLY_DRIVEN	0	0	0
BUS_UNDRIVEN	0	0	0
BUS_VALUE_CONFLICT	0	0	0
CASE_DEFAULT	4	1	0
CASE_FULL	0	0	0
CASE_PARALLEL	0	0	0
FSM_DEADLOCK_STATE	5	1	0
FSM_LOCKOUT_STATE	5	0	0
FSM_STUCK_BIT	4	0	0
FSM_UNREACHABLE_STATE	5	0	0
FSM_UNREACHABLE_TRANS	7	0	0
INDEX_ILLEGAL	3	0	0
INIT_X_OPTIMISM	4	0	0
INIT_X_PESSIMISM	0	0	0
INIT_X_UNRESOLVED	0	0	0
INIT_X_UNRESOLVED_MEM	0	0	0
ONE_COLD	0	0	0
ONE_HOT	0	0	0
REG_MULTIPLY_DRIVEN	0	0	0
REG_STUCK_AT	18	7	0
REG_TOGGLE_VIOLATION	0	0	0
AC Total	134	11	0

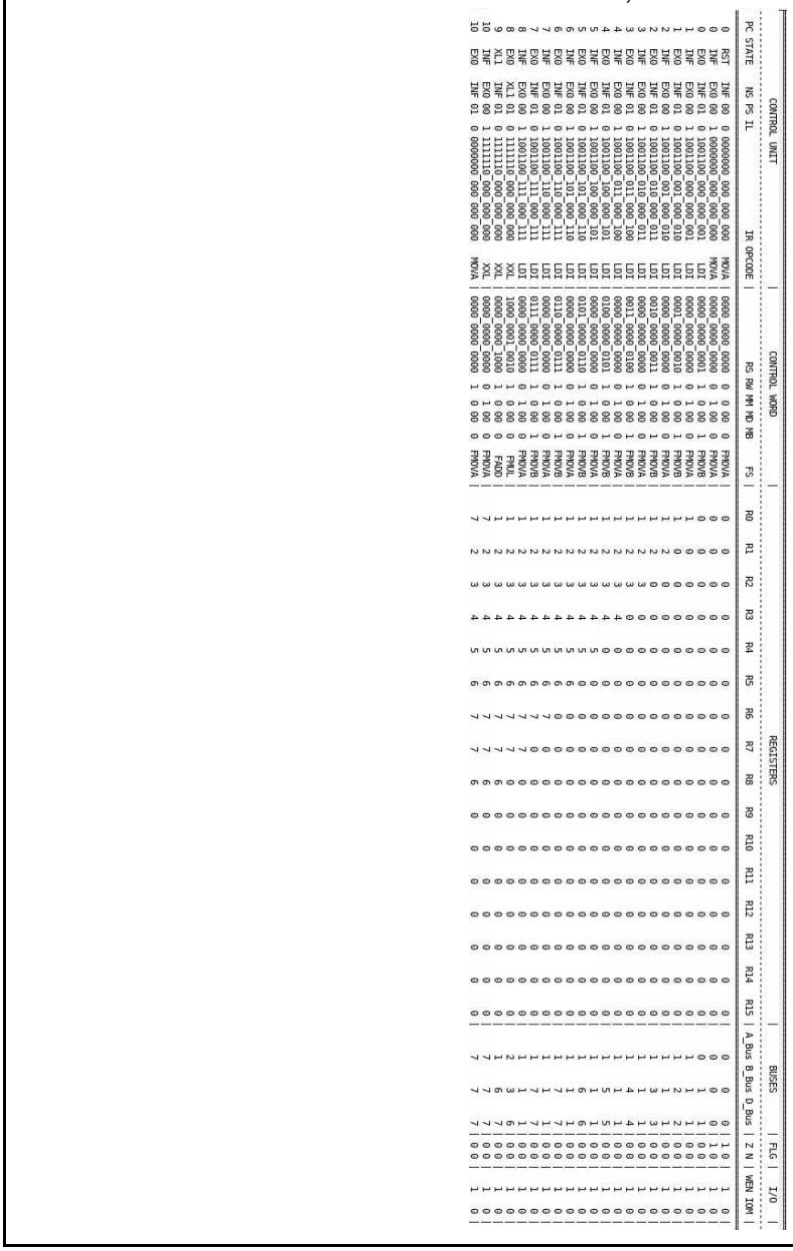
A2. fir.asm simulation results



A3. xxl_test.asm simulation results

(reports/mycpu_simulation.txt as rotated screenshot image)

Paste and select an image in Google Docs and go to Format > Image > Image Options)



A4. Synthesis area report

(reports/mycpu.gatelevel.area.txt)

```
****************************************
Report : area
Design : mycpu
Version: T-2022.03-SP5-1
Date   : Mon Nov  6 16:38:33 2023
****************************************

Library(s) Used:

    saed32hvt_tt1p05v25c (File: /research/cas/public/DT2_2023/lib/logic_lib/saed32hvt_tt1p05v25c.db)

Number of ports:                           68
Number of nets:                          2030
Number of cells:                         1823
Number of combinational cells:           1643
Number of sequential cells:               180
Number of macros/black boxes:               0
Number of buf/inv:                        184
Number of references:                      49

Combinational area:               4139.751591
Buf/Inv area:                      252.110851
Noncombinational area:            1280.885782
Macro/Black Box area:                0.000000
Net Interconnect area:            1530.785773

Total cell area:                  5420.637373
Total area:                       6951.423147

Area of detected synthetic parts
--------------------------------
  No DW parts to report!

Estimated area of ungrouped synthetic parts
-------------------------------------------
                                    Estimated  Perc. of
  Module              Implem.  Count       Area cell area
  ------------------- -------  ----- ---------- ---------
  DP_OP_63J1_123_8560     str      1   319.0368      5.9%
  DP_OP_65J1_122_8819     str      1  1434.6427     26.5%
  DP_OP_72J1_126_3017     str      1   151.0441      2.8%
  ------------------- -------  ----- ---------- ---------
  DP_OP Subtotal:                  3  1904.7236     35.1%
  Total:                           3  1904.7236     35.1%

Subtotal of datapath(DP_OP) cell area:  1904.7236  35.1%  (estimated)
Total synthetic cell area:              1904.7236  35.1%  (estimated)
```

A5. Synthesis Timing Report

(reports/mycpu.gatelevel.timing.txt)

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : mycpu
Version: T-2022.03-SP5-1
Date   : Mon Nov  6 16:38:33 2023
****************************************

Operating Conditions: tt1p05v25c   Library: saed32hvt_tt1p05v25c
Wire Load Model Mode: enclosed

  Startpoint: IR/ir_r_reg[11]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: PC/pc_r_reg[9]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mycpu              8000                  saed32hvt_tt1p05v25c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  IR/ir_r_reg[11]/CLK (DFFARX1_HVT)        0.00       0.00 r
  IR/ir_r_reg[11]/QN (DFFARX1_HVT)         0.14       0.14 r
  U1121/Y (OR2X1_HVT)                      0.09       0.23 r
  U1122/Y (AND3X1_HVT)                     0.08       0.31 r
  U1125/Y (NAND4X0_HVT)                    0.10       0.41 f
  U1126/Y (AND2X1_HVT)                     0.10       0.50 f
  U1127/Y (NAND2X0_HVT)                    0.06       0.57 r
  U1128/Y (INVX0_HVT)                      0.07       0.64 f
  U1130/Y (NAND2X0_HVT)                    0.06       0.70 r
  U949/Y (INVX0_HVT)                       0.05       0.75 f
  U1136/Y (NAND3X0_HVT)                    0.05       0.80 r
  U1137/Y (INVX0_HVT)                      0.04       0.85 f
  U1140/Y (NAND2X0_HVT)                    0.04       0.89 r
  U1141/Y (AND2X1_HVT)                     0.10       0.99 r
  U1252/Y (NAND2X0_HVT)                    0.10       1.09 f
  U771/Y (AND4X2_HVT)                      0.18       1.27 f
  U1415/Y (NAND2X0_HVT)                    0.07       1.35 r
  U903/Y (NAND3X0_HVT)                     0.08       1.43 f
  U774/Y (OR2X2_HVT)                       0.11       1.54 f
  U832/Y (INVX0_HVT)                       0.08       1.62 r
  U1515/Y (AO22X1_HVT)                     0.13       1.75 r
  U780/Y (NAND2X1_HVT)                     0.15       1.90 f
  U870/Y (OAI22X1_HVT)                     0.13       2.03 r
  U1516/Y (AO221X1_HVT)                    0.09       2.12 r
  U1517/Y (NAND2X0_HVT)                    0.10       2.23 f
  U763/Y (OAI21X2_HVT)                     0.14       2.36 r
  U1523/Y (NAND2X0_HVT)                    0.06       2.42 f
  U1526/Y (NAND3X0_HVT)                    0.06       2.48 r
  U1542/Y (NAND2X0_HVT)                    0.06       2.54 f
  U1543/Y (NAND3X0_HVT)                    0.06       2.60 r
  U1828/Y (AO22X1_HVT)                     0.09       2.69 r
  intadd_0/U25/CO (FADDX1_HVT)             0.14       2.83 r
  U1603/Y (AO22X1_HVT)                     0.10       2.93 r
  U1620/Y (AO22X1_HVT)                     0.09       3.03 r
  U1622/Y (AO22X1_HVT)                     0.10       3.13 r
  U1657/Y (NAND2X0_HVT)                    0.06       3.19 f
  U1658/Y (NAND3X0_HVT)                    0.06       3.25 r
```

```
U1835/Y (NAND2X0_HVT)                    0.06       3.31 f
U1838/Y (NAND3X0_HVT)                    0.06       3.37 r
intadd_0/U19/CO (FADDX1_HVT)             0.14       3.51 r
U1826/Y (AO22X1_HVT)                     0.10       3.61 r
intadd_0/U17/CO (FADDX1_HVT)             0.13       3.74 r
intadd_0/U16/CO (FADDX1_HVT)             0.14       3.88 r
intadd_0/U15/CO (FADDX1_HVT)             0.14       4.02 r
intadd_0/U14/CO (FADDX1_HVT)             0.14       4.16 r
intadd_0/U13/CO (FADDX1_HVT)             0.14       4.30 r
U881/Y (INVX0_HVT)                       0.05       4.35 f
U1113/Y (OA22X1_HVT)                     0.08       4.43 f
U921/Y (INVX0_HVT)                       0.04       4.47 r
U1115/Y (AO22X1_HVT)                     0.08       4.55 r
intadd_0/U10/CO (FADDX1_HVT)             0.13       4.69 r
intadd_0/U9/CO (FADDX1_HVT)              0.14       4.83 r
intadd_0/U8/CO (FADDX1_HVT)              0.14       4.97 r
U1834/Y (AO22X1_HVT)                     0.10       5.07 r
intadd_0/U6/CO (FADDX1_HVT)              0.14       5.21 r
U1832/Y (AO22X1_HVT)                     0.10       5.30 r
intadd_0/U4/CO (FADDX1_HVT)              0.14       5.44 r
U1830/Y (AO22X1_HVT)                     0.10       5.54 r
intadd_0/U2/S (FADDX1_HVT)               0.13       5.67 r
U1498/Y (NAND4X0_HVT)                    0.11       5.78 f
U1500/Y (NOR4X0_HVT)                     0.14       5.92 r
U1502/Y (AOI21X1_HVT)                    0.11       6.03 f
U806/Y (NAND2X2_HVT)                     0.10       6.12 r
U1628/Y (NAND4X0_HVT)                    0.12       6.25 f
U1629/Y (OR2X1_HVT)                      0.08       6.33 f
U1665/Y (NOR4X0_HVT)                     0.12       6.45 r
U1666/Y (NAND4X0_HVT)                    0.10       6.55 f
U1713/Y (NOR3X0_HVT)                     0.12       6.67 r
U1721/Y (AND2X1_HVT)                     0.07       6.74 r
U1722/Y (INVX0_HVT)                      0.04       6.77 f
U1724/Y (AO21X1_HVT)                     0.07       6.84 f
U1725/Y (AO21X1_HVT)                     0.08       6.92 f
U1729/Y (NOR2X0_HVT)                     0.11       7.04 r
U762/Y (AND2X1_HVT)                      0.10       7.14 r
U1731/Y (NOR2X0_HVT)                     0.12       7.26 f
U1732/Y (NOR2X0_HVT)                     0.09       7.35 r
U1760/Y (AOI21X1_HVT)                    0.11       7.46 f
U760/Y (OAI21X2_HVT)                     0.10       7.57 r
U1809/Y (AOI21X1_HVT)                    0.13       7.70 f
U1011/Y (XOR2X1_HVT)                     0.12       7.82 r
U1812/Y (AO21X1_HVT)                     0.10       7.91 r
PC/pc_r_reg[9]/D (DFFARX1_HVT)           0.01       7.93 r
data arrival time                                   7.93

clock clk (rise edge)                    8.00       8.00
clock network delay (ideal)              0.00       8.00
PC/pc_r_reg[9]/CLK (DFFARX1_HVT)         0.00       8.00 r
library setup time                      -0.07       7.93
data required time                                  7.93
------------------------------------------------------------
data required time                                  7.93
data arrival time                                  -7.93
------------------------------------------------------------
slack (MET)                                         0.00
```

A6. Power consumption report

(reports/mycpu.gatelevel.power.txt)

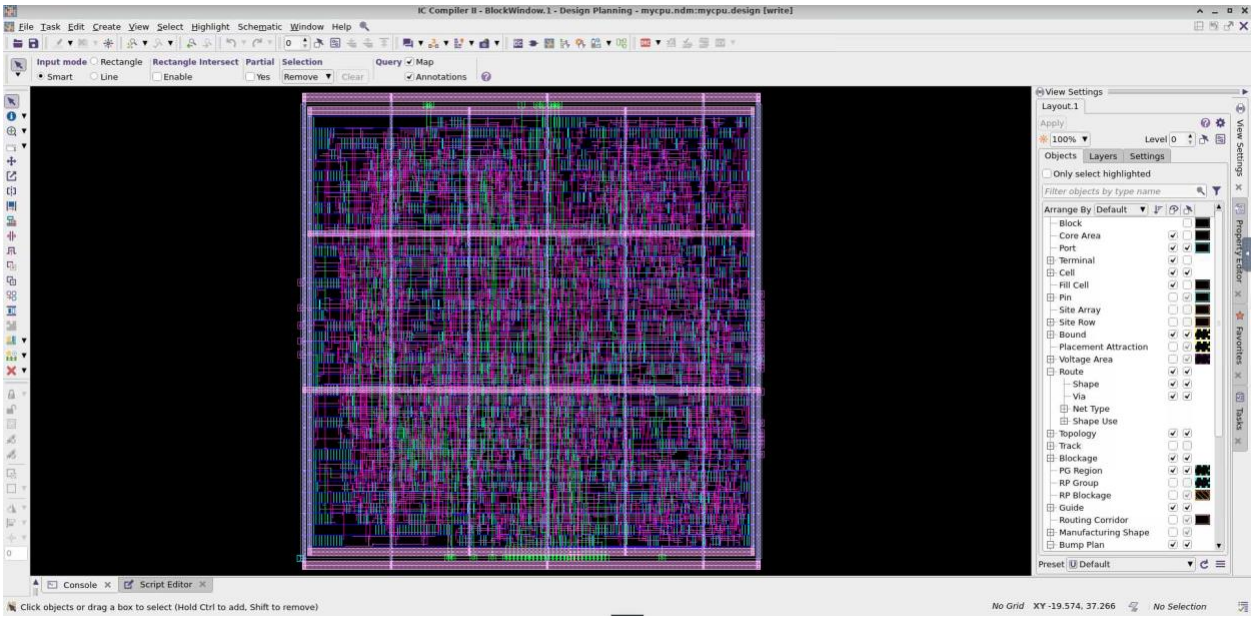
```
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: The derived toggle rate value (0.250000) for the clock net 'clk' conflicts with the annotated value (0.099987). Using the annotated value. (PWR-12)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

****************************************
Report : power
        -analysis_effort low
Design : mycpu
Version: T-2022.03-SP5-1
Date   : Mon Nov  6 16:38:33 2023
****************************************


Library(s) Used:

    saed32hvt_tt1p05v25c (File: /research/cas/public/DT2_2023/lib/logic_lib/saed32hvt_tt1p05v25c.db)


Operating Conditions: tt1p05v25c   Library: saed32hvt_tt1p05v25c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
mycpu                 8000              saed32hvt_tt1p05v25c


Global Operating Voltage = 1.05
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =  66.3790 uW   (95%)
  Net Switching Power  =   3.6812 uW    (5%)
                         ---------
Total Dynamic Power    =  70.0602 uW  (100%)

Cell Leakage Power     =  16.3985 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network     60.8950           0.0000            0.0000            60.8950  (  70.43%)  i
register           1.6178           0.6344        6.4716e+06             8.7239  (  10.09%)
sequential         0.0000           0.0000            0.0000             0.0000  (   0.00%)
combinational      3.8662           3.0468        9.9269e+06            16.8399  (  19.48%)
--------------------------------------------------------------------------------------------------
Total             66.3790 uW        3.6812 uW     1.6399e+07 pW        86.4587 uW
-
```

A7. Logic equivalence check report

(reports/mycpu.gatelevel.lec_status.txt)

```
Report         : status

Reference      : r:/WORK/mycpu
Implementation : i:/WORK/mycpu
Version        : U-2022.12
Date           : Sun Nov  5 16:51:09 2023
*************************************************

***************************** Synopsys Auto Setup Summary ****************************

!!! Synopsys Auto Setup Mode was enabled. !!!
!!! Verification results are valid assuming the following setup constraints: !!!

### RTL Interpretation Setup
   set hdlin_ignore_parallel_case false
   set hdlin_ignore_full_case false
   set hdlin_error_on_mismatch_message false
   set hdlin_ignore_embedded_configuration true

### Undriven Signal Handling Setup
   set verification_set_undriven_signals synthesis

### Test Logic Setup
   set verification_verify_directly_undriven_output false
   For details see report_dont_verify_points and report_constants

For further details on Synopsys Auto Setup Mode: Type man synopsys_auto_setup
**************************************************************************************


******************************** Verification Results ********************************
Verification SUCCEEDED
   ATTENTION: synopsys_auto_setup mode was enabled.
              See Synopsys Auto Setup Summary for details.
---------------------------------------------------------
 Reference design: r:/WORK/mycpu
 Implementation design: i:/WORK/mycpu
 182 Passing compare points
--------------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT   TOTAL
--------------------------------------------------------------------------------------
Passing (equivalent)           0       0       0       0      34     148       0     182
Failing (not equivalent)       0       0       0       0       0       0       0       0
**************************************************************************************
```

IC Layout


IC Compiler II - BlockWindow.1 - Design Planning - mycpu.ndm:mycpu.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Input mode Smart Rectangle Line
Rectangle Intersect Enable
Partial Yes
Selection Remove Clear
Query Map Annotations
View Settings
Layout.1
Apply
100%
Level 0
Objects Layers Settings
Only select highlighted
Filter objects by type name
Arrange By Default
Block
Core Area
Port
Terminal
Cell
Fill Cell
Pin
Site Array
Site Row
Bound
Placement Attraction
Voltage Area
Route
Shape
Via
Net Type
Shape Use
Topology
Track
Blockage
PG Region
RP Group
RP Blockage
Guide
Routing Corridor
Manufacturing Shape
Bump Plan
Preset Default
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid
XY -19.574, 37.266
No Selection