

UNIT - IV

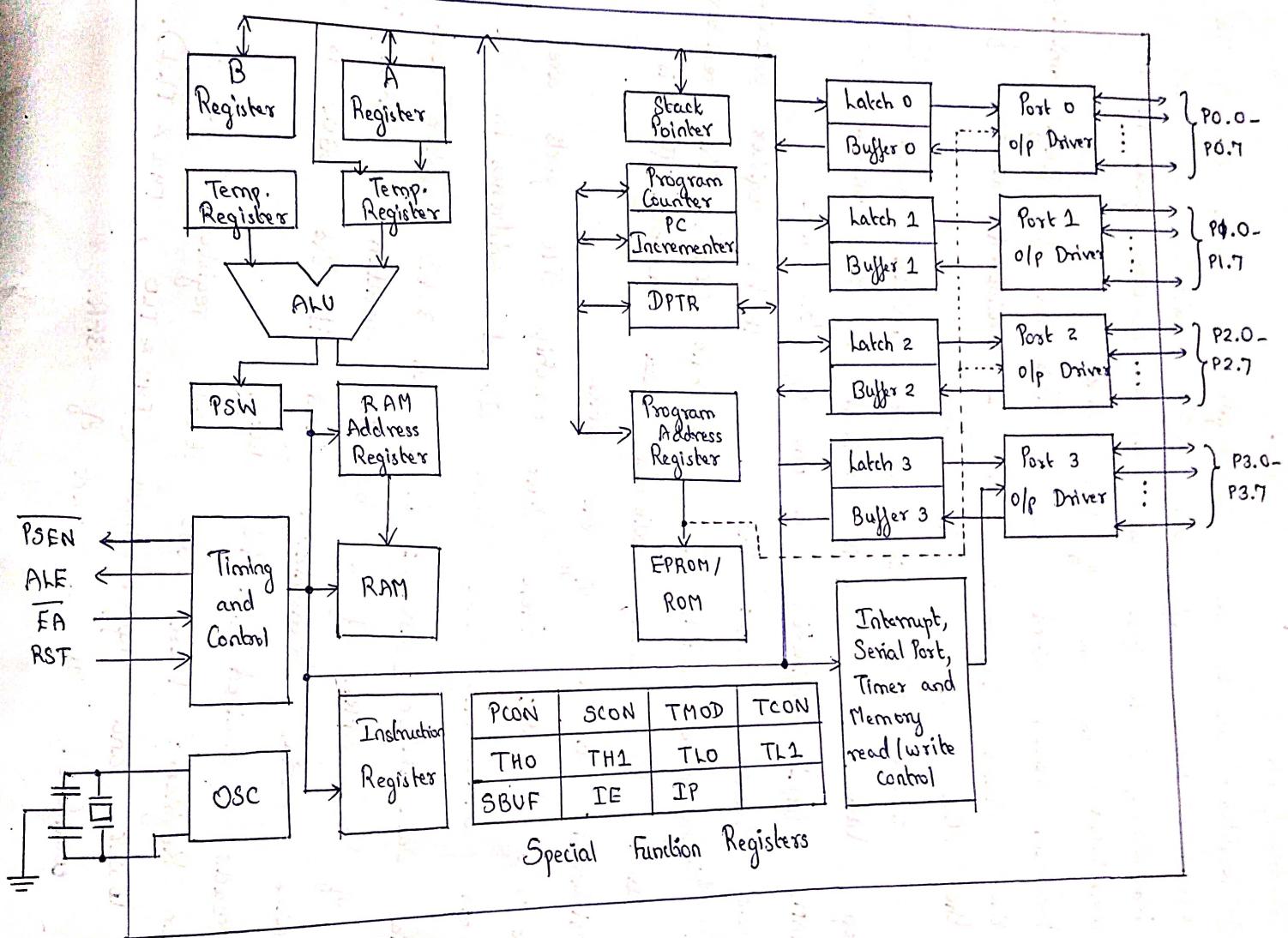
MICROCONTROLLER

ARCHITECTURE OF 8051 - SPECIAL FUNCTION REGISTERS (SFRs) -

I/O PINS . PORTS AND CIRCUITS - INSTRUCTION SET -

ADDRESSING MODES - ASSEMBLY LANGUAGE PROGRAMMING.

Block Diagram of 8051



Accumulator (Acc): The accumulator register (Acc or register A) is an 8-bit register. It acts as an operand register in case of some instructions. It is considered as a special function Register (SFR).

B Register: It is an 8-bit register. It stores one of the operands for multiply and divide instructions. In other instructions, it is just used as a scratch pad. It is considered as one of the SFRs.

Program Status Word (PSW): This set of flags contains the status information and is considered as one of the SFRs. It is an 8-bit register.

Stack Pointer (SP): This register contains 8-bit stack top address. The stack is defined in the on-chip 128 byte RAM. It (SP) is considered as one of the SFRs.

Data Pointer (DPTR): This is a 16-bit register containing a higher-byte (DPH) and lower-byte (DPL). This register is used to access external data memory. This is considered as one of the SFRs.

Port 0 to Port 3: These four on-chip I/O ports are 8-bits wide. They have been allotted addresses in the SFR.

Serial Data Buffer (SBUF): It is an 8-bit register and is one of the SFRs. If a byte is written to SBUF, it initiates serial transmission and if the SBUF is read, it reads received serial data.

Timer Registers: These two 16-bit registers can be accessed as lower and upper bytes (TH0 & TL0, TH1 & TL1). Also considered as a part of SFR.

Control Registers: The special function registers IP, IE, TMOD, TCON, SCON and PCON contain control and status information for interrupts, timer/counters and serial port.

Timing and Control Unit: This unit derives all the necessary timing and control signals required for the internal operation of the circuit.

Oscillator: This circuit generates the basic timing clock signal for the operation of the crystal oscillator.

Instruction Register: This register decodes the instruction to be executed and gives information to the timing and control unit to generate necessary signals for the execution of the instruction.

ROM: The on-chip ROM capacity of 8051 is 4KB.

RAM: The on-chip RAM capacity of 8051 is 128 bytes.

ALU: The arithmetic and logic unit performs 8-bit arithmetic and logical operations.

SFR: All the special function Registers can be accessed by their names or the respective address which lie in the range of 80H to FFH.

PIN CONFIGURATION OF 8051:

P1.0	1	40	Vcc
P1.1	2	39	P0.0 (AD0)
P1.2	3	38	P0.1 (AD1)
P1.3	4	37	P0.2 (AD2)
P1.4	5	36	P0.3 (AD3)
P1.5	6	35	P0.4 (AD4)
P1.6	7	34	P0.5 (AD5)
P1.7	8	33	P0.6 (AD6)
RST	9	32	P0.7 (AD7)
(RXD)	10	31	EA / Vpp
(TXD)	11	30	ALE / PROG
(INT0)	12	29	PSEN
(INT1)	13	28	P2.7 (A15)
(TO)	14	27	P2.6 (A14)
(T1)	15	26	P2.5 (A13)
(WR)	16	25	P2.4 (A12)
(RD)	17	24	P2.3 (A11)
XTAL2	18	23	P2.2 (A10)
XTAL1	19	22	P2.1 (A9)
GND	20	21	P2.0 (A8)

Pin details:

Vcc : +5V supply

Vss: Ground

RESET: The reset input pin resets the 8051.

ALE/ PROG: The Address Latch Enable (ALE) output pulse indicates that the valid address bits are available on the multiplexed bus. This pin also acts as input during on-chip EEPROM programming.

EA/V_{pp}: External Access pin, if tied low, indicates that the 8051 can access external program memory. This pin also receives 21 volts for programming the on-chip EPROM.

PSEN: Program Store Enable is an active-low output signal that acts as a strobe to read the external program memory.

Port 0 (P0.0-P0.7): Port 0 is an 8-bit bidirectional bit-addressable I/O port. Port 0 also acts as multiplexed address / data lines during external memory access. (A_0-A_7).

Port 1 (P1.0-P1.7): Port 1 acts as an 8-bit bidirectional bit-addressable I/O port.

Port 2 (P2.0-P2.7): Port 2 acts as an 8-bit bidirectional bit-addressable I/O port. During external memory access, port 2 acts as higher-order address bus (A_8-A_{15}). Port 3 (P3.0-P3.7): Port 3 acts as an 8-bit bidirectional bit-addressable I/O port. The port 3 pins also serve the alternative functions listed below:

Port 3 Pin

P3.0

P3.1

P3.2

P3.3

P3.4

P3.5

P3.6

P3.7

Alternative Function

RxD - Receives serial data

TxD - Transmits serial data

INT₀ - External interrupt pin 0

INT₁ - External interrupt pin 1

TO - External input to Timer 0

TI - External input to Timer 1.

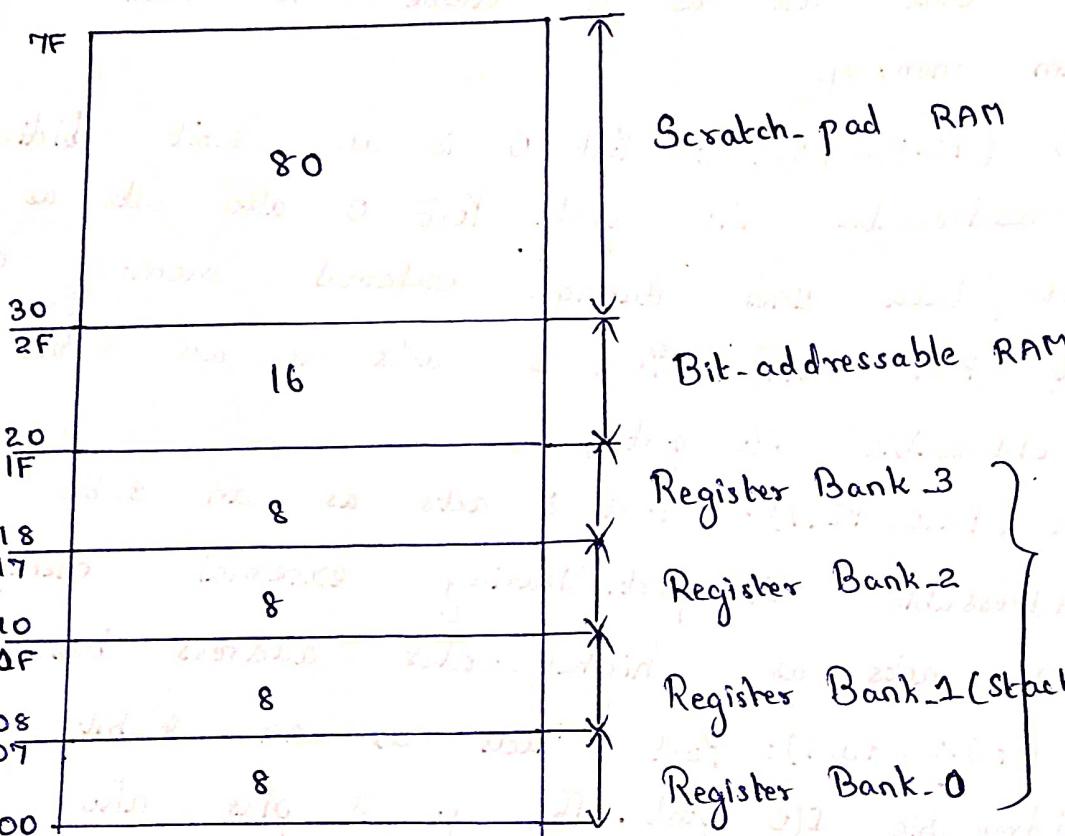
WR - Write control signal

RD - Read control signal

XTA₁, and XTA₂: For connecting crystal oscillator which derives the necessary clock frequency for the operation of 8051.

RAM MEMORY SPACE ALLOCATION IN 8051

* The 128 bytes of on-chip RAM is divided into three groups, and are assigned addresses from 00_H to $7F_H$.



1. 32 bytes (00_H to $1FH$) : Registers Banks and Stack.
2. 16 bytes (20_H to $2FH$) : Bit-addressable RAM
3. 80 bytes (30_H to $7FH$) : Scratch-pad RAM (Read Write Storage)

Register Banks:

* There are 4 Registers Banks.

* Each Bank has 8 registers. ($R_0 - R_7$)

Bank 0	Bank 1	Bank 2	Bank 3
07 _H R7	0F _H R7	17 _H R7	1F _H R7
:	:	:	:
01 _H RI	09 _H RI	11 _H RI	19 _H RI
00 _H RO	08 _H RO	10 _H RO	18 _H RO

The default register bank that would be selected on power-up is Bank 0.

How to switch register banks?

PSW (Program Status Word):

7	6	5	4	3	2	1	0
C4	AC	-	RS1	RS0	OV	-	P

RS1	RS0	Reg. Bank
0	0	0
0	1	1
1	0	2
1	1	3

Register banks can be selected using PSW.3 and PSW.4

Eg: To select Reg. Bank 2 → SETB PSW.4
CLR PSW.3

Stack in 8051:

- * The stack pointer (SP) register is 8-bit wide.
- * When powered-up, SP is initialized with 07_H, indicating that 08_H is the first location being used for stack.
- * Stack can grow from 08_H to 1F_H. (24 bytes)
- * If more than 24 bytes is needed, stack can grow from 30_H to 7F_H. (Not Bit-addressable RAM cannot be used).

SPECIAL FUNCTION REGISTERS (SFRs)

The following are the special function registers in 8051:

Special function Register		Byte address (in hexa)
Symbol	Name	
A or Acc.	A-register or Accumulator	FO
B	B register	F0
DPH	DPTR - higher order register	83
DPL	DPTP - lower order register	82
IE	Interrupt Enable register	A8
IP	Interrupt Priority Register	B8
P0	Port-0	80
P1	Port-1	90
P2	Port-2	A0
P3	Port-3	B0
PCON	Power Control Registers	87
PSW	Program Status Word	DO
SCON	Serial Port Control Register	98
SBUF	Serial Port Data Buffer	99
SP	Stack Pointer	81
TMOD	Timer Mode Register	89
TCON	Timer / Counter Control Registers	88
TLO	Timer-0 lower order register	8A
TH0	Timer-0 higher order register	8C
TL1	Timer-1 lower order register	8B
TH1	Timer-1 higher order register	8D

Bit-addressable Registers :-

The following are the bit-addressable registers in SFRs : P0, P1, P2, P3, A, B, PSW, IP, IE, SCON & TCON.

Bit-address

E7	E6	E5	E4	E3	E2	E1	E0	A Register.
F7	F0	B
D7	D0	PSW
---	---	BC	---	---	---	---	B8	IP
B7	B0	P3
A F	A8	IE
A7	A0	P2
9F	98	SCON
97	90	P1
8F	88	TCON
89	80	P0

Eg: To access the 6th bit of P0, either
SETB P0.6 or SETB 86H can be used.

ADDRESSING MODES IN 8051:

The various ways of specifying the operands are called addressing modes.

The following are the addressing modes of 8051:

1. Immediate Addressing Mode
2. Direct Addressing Mode
3. Register Addressing Mode
4. Register Indirect Addressing Mode
5. Indexed Addressing Mode.
6. Implied Addressing Mode.

1. Immediate Addressing Mode:

An 8-bit / 16-bit immediate data is specified as part of the instruction.

Eg: $\text{MOV A, } \#25H$
 $\text{MOV DPTR, } \#4521H$

2. Direct Addressing Mode:

The address of the data is directly specified in the instruction.

Eg: $\text{MOV A, } 07H$

3. Register Addressing Mode:

The instruction will specify the name of the register in which the data is available.

Eg: MOV A, R0.

4. Register Indirect Addressing Mode:

The instruction specifies the name of the register in which the address of the data is available.

Eg: $\text{MOV A, } @R0$

5. Indexed Addressing Mode:

Only program memory can be accessed using this addressing mode. The contents of register A is added with that of PC or DPTR to form the address.

Eg: $\text{Movc } A, @A + \text{DPTR}$

b. Implied Addressing Mode:

The operand is implicitly specified.

Eg: RLA

INSTRUCTION SET OF 8051:

The instructions are classified into five groups.

1. Data Transfer Instructions
2. Arithmetic Instructions
3. Logical Instructions
4. Branch Instructions
- 5.

1. Data Transfer Instructions:

The instructions that transfer data between source and destination.

Eg: $\text{Mov } A, \# \text{data}$

$\text{Mov } A, Rn$

$\text{Mov } A, 8\text{-bit address}$

$\text{Mov } A, @Ri$

$\text{Mov } Rn, A$

$\text{Mov } Rn, \text{direct}$

$\text{Mov } Rn, \# \text{data}$

$\text{Mov } @Ri, A$

Mov DPTR, # 16-bit data

Movc A, @ A + DPTR

Movx A, @ DPTR

Movx @DPTR, A

Push 8-bit address

Pop 8-bit address

2. Arithmetic Instructions:

This group includes instructions for performing

addition, subtraction, multiplication, division, increment and decrement operations. The results are stored in accumulator except for increment and decrement operations.

Eg:

ADD A, #data

ADD A, Rn

ADD A, 8-bit address

ADD A, @Ri

ADDC A, #data

ADDC A, Rn

ADDC A, 8-bit address

ADDC A, @Ri

SUBB A, #data

SUBB A, Rn

SUBB A, 8-bit address

SUBB A, @Ri

MUL AB

DIV AB

INC A

INC Rn

INC 8-bit address

INC @Ri

DEC A
 DEC Rn
 DEC 8-bit address
 DEC @ Ri

DAA

3. Logical Instructions:

This group includes instructions for performing logical operations such as AND, OR, EX-OR, complement and rotate.

Eg: ANL A, #data

ANL A, Rn

ANL A, 8-bit address

ANL A, @Ri

ORL A, #data

ORL A, Rn

ORL A, 8-bit address

ORL A, @Ri

XRL A, #data

XRL A, Rn

XRL A, 8-bit address

XRL A, @Ri

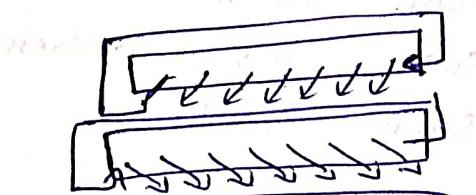
CPL A

RLA

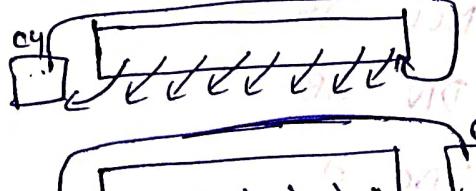
RLCA

RRCA

SWAP A



(Rotate left)



(Rotate Right)

(Rotate left with carry)

(Rotate Right with carry)

A. Branch instructions:

Branch instructions are used to alter the sequence of execution of program. The branch instructions will modify the contents of the PC so that, the program control branches to a new address. It includes conditional and unconditional branching instructions.

JZ	displacement (8-bit)	01111	00000000
JNZ	displacement (8-bit)	01110	00000000
JC	displacement (8-bit)	01111	00000000
JNC	displacement (8-bit)	10110	00000000
DJNZ	reg, label	11110	00000000
CJNE	destination, source, label.	01111	00000000
SJMP	displacement	01111	00000000
LJMP	16-bit address	01111	00000000
LCALL	address (11-bit)	01111	00000000
ACALL	address(16bit)	01111	00000000
RET		10110	00000000

5. SINGLE-BIT INSTRUCTIONS:

The single-bit instructions operate on a particular bit of a data.

SETB	bit	00101	00000000 : target
CLR	(bit)	00100	00000000 : target
CPL	(bit)	00100	00000000 : target
JB	bit, target	00100	00000000 : target
JNB	bit, target	00100	00000000 : target
JBC	bit, target	00100	00000000 : target

<u>ASSEMBLY</u>	<u>LANGUAGE</u>	<u>PROGRAMMING</u>
8051 ALP for 8-bit addition:		
MOV DPTR, #2400H		
MOVX A, @DPTR		
MOV R1, A		
INC DPTR		
MOVX A, @DPTR		
MOV R2, #00H		
ADD A, R1		
JNC L1		
INC R2		
L1: INC DPTR		
MOVX @DPTR, A		
INC DPTR		
MOV A, R2		
MOVX @DPTR, A		
L2: SJMP L2		

Sample Data:

Input:

$2400_H : 02_H$

$2401_H : 03_H$

Output:

$2402_H : 05_H$ (sum)

$2403_H : 00_H$ (Carry)

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