BOOLEAN_FUNCTION_MINIMIZATION

AIM:

To implement the given logic function verify its operation in Quartus using Verilog programming.

F1= A′B′C′D′+AC′D′+B′CD′+A′BCD+BC′D

F2=xy′z+x′y′z+w′xy+wx′y+wxy

Equipment Required:

Hardware – PCs, Cyclone II , USB flasher

Software – Quartus prime

Theory

Logic Diagram

Procedure

1. Type the program in Quartus software.
2. Compile and run the program.
3. Generate the RTL schematic and save the logic diagram.
4. Create nodes for inputs and outputs to generate the timing diagram.
5. For different input combinations generate the timing diagram.

Program:

```
Program to implement the given logic function and to verify its operations in quartus us
Developed by:P.Sudhishna
RegisterNumber:24007608
```

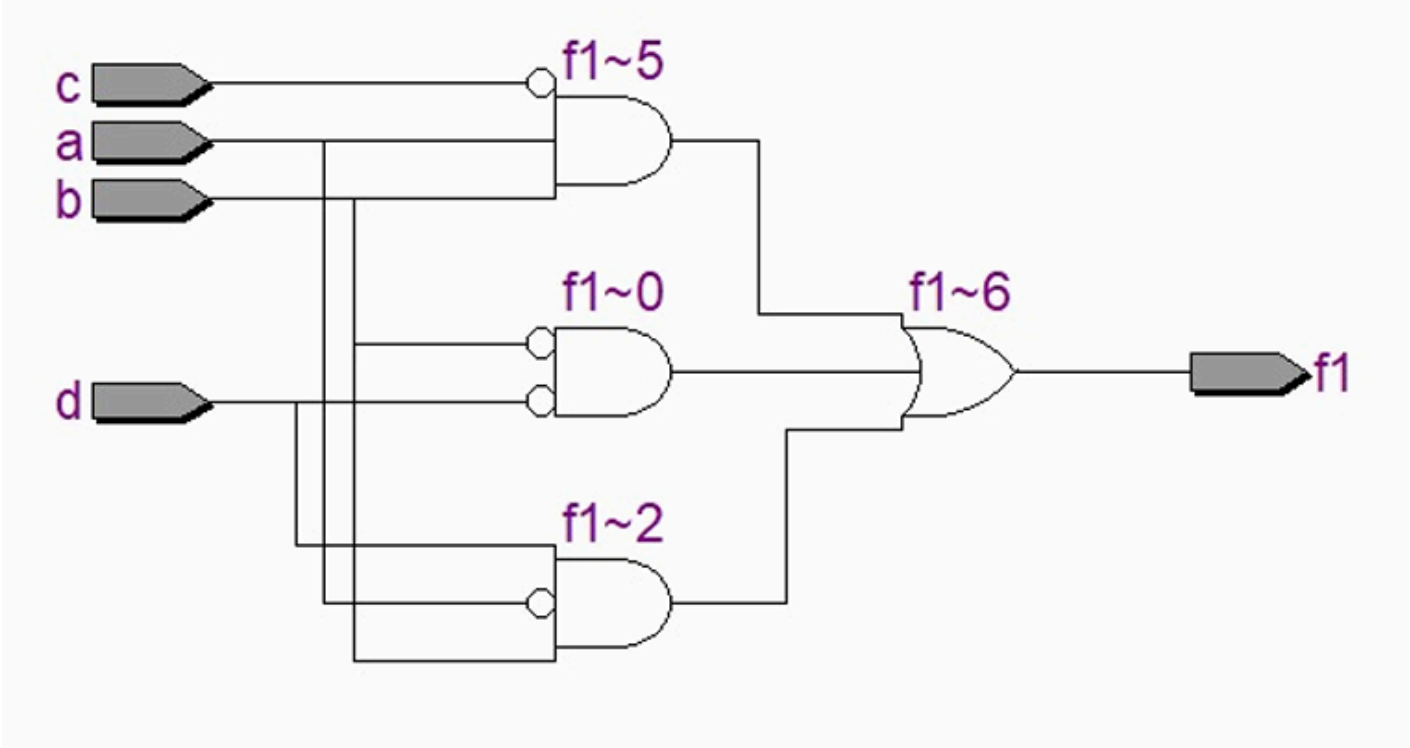
```
module funct1(a,b,c,d,f1);
 input a,b,c,d;
 output f1;
 assign f1=((~b & ~d)|(~a & b & d)|(a & b & ~c));
 endmodule
```

RTL realization

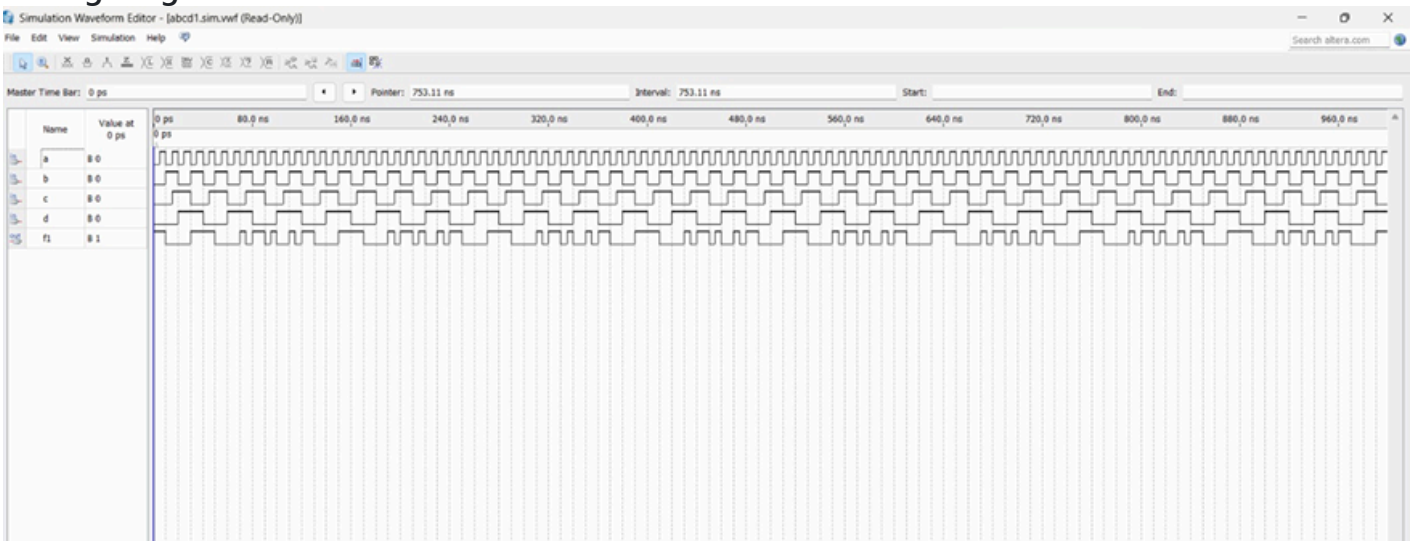
a	b	c	d	a'b'c'd'	ac'd'	b'cd'	a'bcd	bc'd	F1
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	1
0	0	1	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	1	1
0	1	1	0	0	0	0	0	0	0
0	1	1	1	0	0	0	1	0	1
1	0	0	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	1
1	0	1	1	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	1
1	1	0	1	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

w	x	y	z	xy'z	x'y'z	w'xy	wx'y	wxy	F2
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	1
0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	0	1	0	0	1
0	1	1	1	0	0	1	0	0	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	1
1	0	1	0	0	0	0	1	0	1
1	0	1	1	0	0	0	1	0	1
1	1	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	1
1	1	1	0	0	0	0	0	1	1
1	1	1	1	0	0	0	0	1	1

Output:



Timing Diagram



Result:

Thus the given logic functions are implemented using and their operations are verified using Verilog programming.